SRS CS Auto & CSII 5.1 & TruSurround XT Decoder

■ General Description

The NJU26208 is a digital signal processor that provides the function of Circle Surround Automotive / Circle SurroundII5.1 / TruSurroundXT and Mono-to-Stereo. The NJU26208 processes the stereo matrix-encoded signal into spacious sound of 5.1channels by Circle SurroundII5.1. Also non matrix-encoded audio signal can be processed into effective spacious sound.
The decoded 2-channel signal can be converted into spacious 2-channel virtual surround output by the TruSurroundXT technology.
The applications of NJU26208 are suitable for multi-channel products such as DVD Receivers, AV Amplifiers, TV, Car Audio or ordinary audio products such as small speakers system.

■ Package

NJU26208V

■ FEATURES

- Software

- SRS Circle Surround Automotive for Car Audio
- 5.1-Channel signal outputs by Circle Surround II 5.1
- 2-Channel outputs by SRS TruSurround XT
- Speaker sound elevation by Focus
- Rich low frequency reproduction by TruBass
- Generating 5.1-channel outputs from mono signal by Mono-To-Stereo function

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 3 Output ports
- Digital Audio Format : I^2S, Left- justified, Right-justified, 16/18/20/24 bit, BCK : 32/64fs
- Master / Slave Mode : In Master mode, MCK = 256fs, MCK2 = 512fs
- Serial Host Interface : I^2C-Bus (Standard-mode/100kbps, Fast-mode/400kbps)
  : 4-Wire Serial Bus (Clock, Enable, Input data, Output data)
- Power Supply : V_{DD} = V_{DDPLL} = 1.8V
  : V_{DDIO} = 3.3V
- Input terminal : 5.0V Input tolerant
- Package : SSOP44 (Pb-Free)

* The detail hardware specification of the NJU26208 is described in the " NJU26200 Series Hardware Data Sheet".

■ Block Diagram

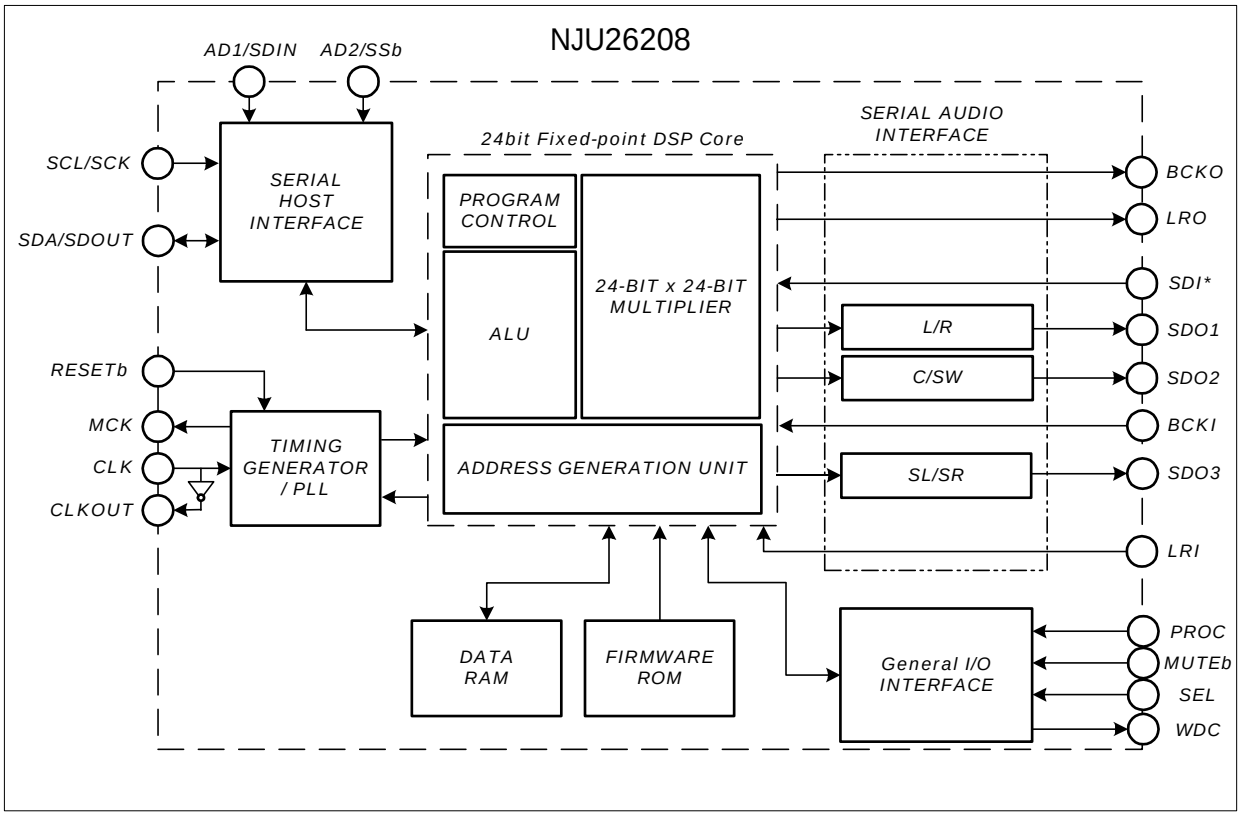


Fig.1 NJU26208 Hardware Block Diagram

■ Function Block Diagram

NJU26208 Block Diagram
(Stereo input mode)

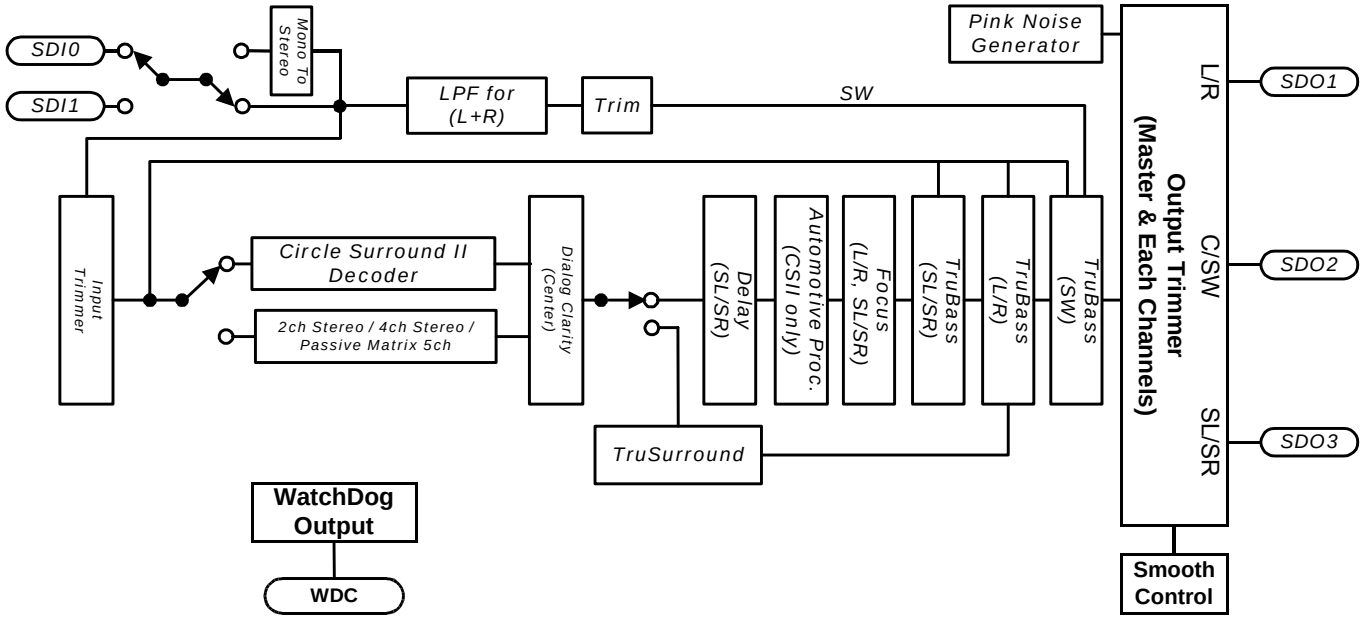


Fig.2 Function Block Diagram (Stereo Input Mode)

NJU26208 Block Diagram
(Multi Input Mode)

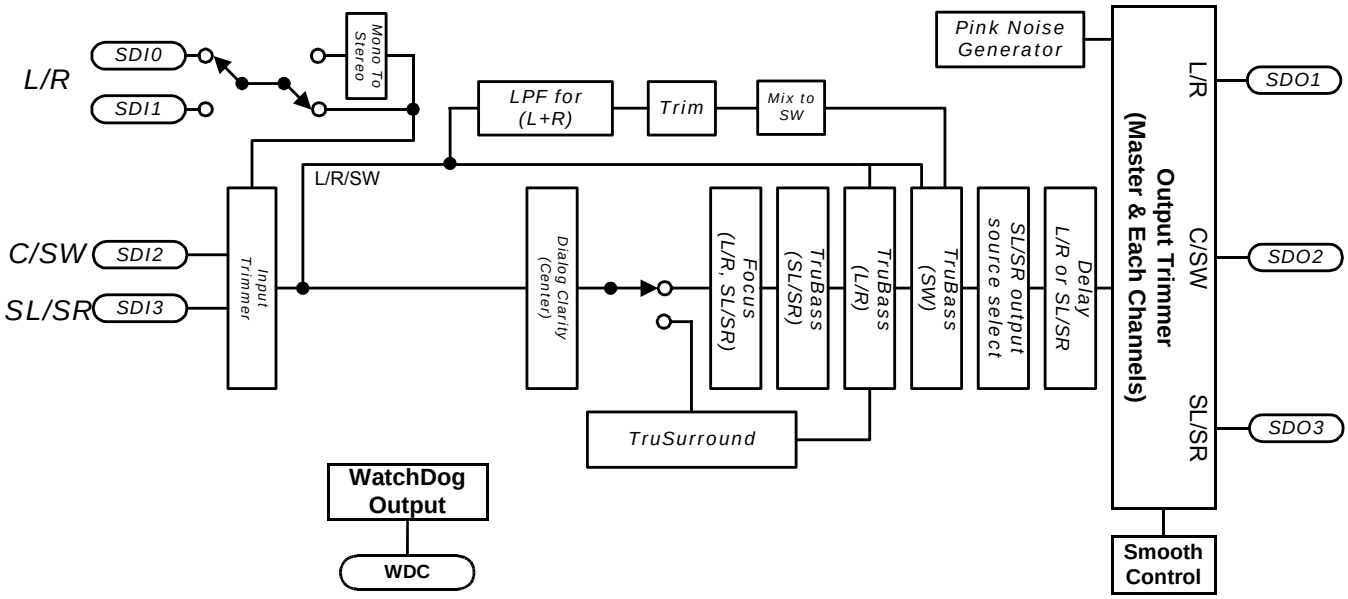


Fig.3 Function Block Diagram (Multi Input Mode)

■ Pin Configuration (SSOP44)

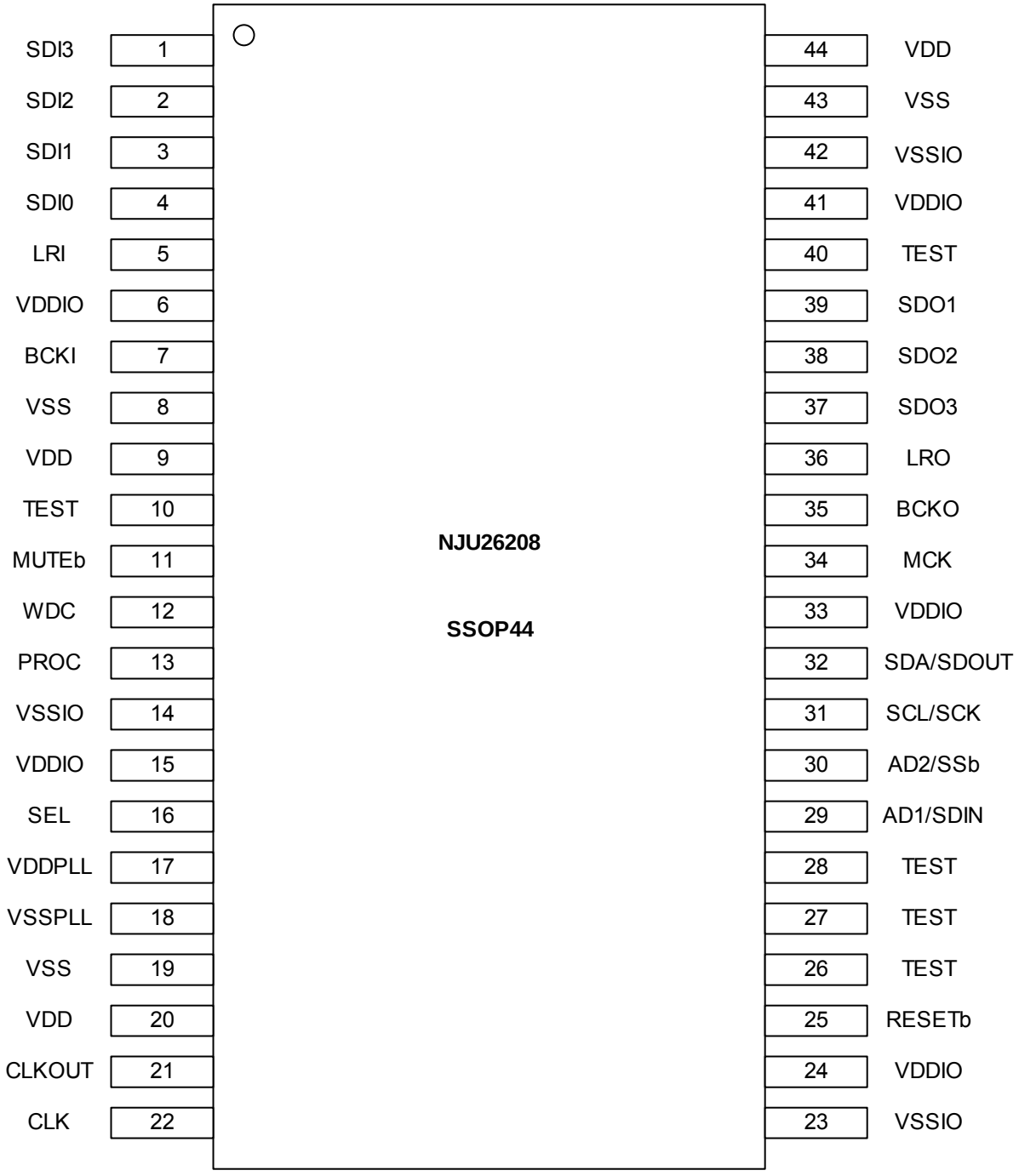


Fig. 4 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No. SSOP44	Symbol	I/O	Description
6, 15, 24, 33, 41	VDDIO	-	I/O Power Supply +3.3V
7	BCKI	I	Bit Clock Input
14, 23, 42	VSSIO	-	I/O GND
8, 19, 43	VSS	-	Core GND
9, 20, 44	VDD	-	Core Power Supply +1.8V
10	TEST	I	for test (connected to VSSIO through 3.3kΩ resistance.)
11	MUTEb *	I	Master Volume level, After Reset DSP (“1” : 0dB , “0” : Mute)
12	WDC *	OD	Clock for Watch Dog Timer (Open Drain Output)
13	PROC *	I	After Reset DSP. (“1” : Normal , “0” : Wait from Command)
16	SEL	I	Select I^2C or Serial bus (‘1’ : Serial , ‘0’ : I^2C-Bus)
17	VDDPLL	-	PLL Analog Power Supply +1.8V
18	VSSPLL	-	PLL Analog GND
21	CLKOUT	O	OSC Output
22	CLK	I	X’tal Clock Input (12.288MHz)
25	RESETb	I	Reset (RESETb=’0’ : DSP Reset)
26	TEST	I	for Test (Connect to VDDIO)
27, 28	TEST	I	for Test (Connect to VSSIO)
29	AD1/SDIN	I	I^2C Address / Serial Input
30	AD2/SSb	I	I^2C Address / Serial Enable
31	SCL/SCK	I	I^2C Clock / Serial Clock
32	SDA/SDOUT	I/O	I^2C I/O (Open Drain output) / Serial Output (CMOS output) I^2C Bus mode : SDA pin requires a pull-up resistance. 4-wire Serial mode : SDOUT does not require a pull-up resistance.
34	MCK	O	Master Clock Output (buffer output of a CLK pin)
35	BCKO	O	Bit Clock Output
36	LRO	O	LR Clock Output
37	SDO3	O	Audio Data Output 3 (Rear Lch / Rch)
38	SDO2	O	Audio Data Output 2 (Center / Subwoofer)
39	SDO1	O	Audio Data Output 1 (Front Lch / Rch)
40	SDO0	O	for Test (Not connected : OPEN)
1	SDI3	I	Audio Data Input 3 (SL / SR)
2	SDI2	I	Audio Data Input 2 (Center / Subwoofer)
3	SDI1	I	Audio Data Input 1 (Front Lch / Rch)
4	SDI0	I	Audio Data Input 0 (Front Lch / Rch)
5	LRI	I	LR Clock Input

I : Input
O : Output
OD : Open Drain Output
I/O : Bi-directional

Note : Pins symbol with * : Connect with VDDIO or VSSIO through 3.3kΩ resistance

■ Audio Interface

The serial audio interface carries audio data to and from the NJU26208. Industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified are supported.
The NJU26208 serial audio interface includes 4 data input lines: SDI0/SDI1/SDI2/SDI3 and 3 data output lines: SDO1/SDO2/SDO3. (Table 2. 3.)

Table 2 Serial Audio Input Pin Description

Pin No.	Symbol	Description	
SSOP44		Stereo Input Mode	Multi channel Input Mode
4	SDI0	Stereo L/R	Stereo L/R
3	SDI1	(SDI0 / SDI1 Pin select)	(SDI0 / SDI1 Pin select)
2	SDI2	No use	Audio Data Input 2 Center / Sub Woofer
1	SDI3	No use	Audio Data Input 3 SL / SR (Surround channel)

Table 3 Serial Audio Output Pin Description

Pin No.	Symbol	Description	
SSOP44			
39	SDO1	Audio Data Output 1	Front Lch / Rch
38	SDO2	Audio Data Output 2	Center / Sub Woofer
37	SDO3	Audio Data Output 3	Rear Lch / Rch

■ Host Interface

The NJU26208 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or I^2C-Bus. Data transfers are in 8 bit packets (1 byte) when using either format.
The SEL pin controls the serial bus mode. When the SEL is "Low" level during the NJU26208 initialization, I^2C-Bus is available. When the SEL is "High" level during the NJU26208 initialization, 4-Wire serial bus is available.(Table 4) Serial Host Interface Pin Description. (Table 5)

Table 4 Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
SSOP44			
16	SEL	"Low"	I^2C-Bus
		"High"	4-Wire serial bus

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C /Serial)	I^2C-Bus Format	4-Wire Serial bus Format
SSOP44			
29	AD1 / SDIN	I^2C-Bus address Bit1	Serial Data Input
30	AD2 / SSb	I^2C-Bus address Bit2	SLAVE Select
31	SCL / SCK	Serial Clock	Serial Clock
32	SDA / SDOUT	Serial Data Input/Output (Open Drain output)	Serial Data Output (CMOS output)

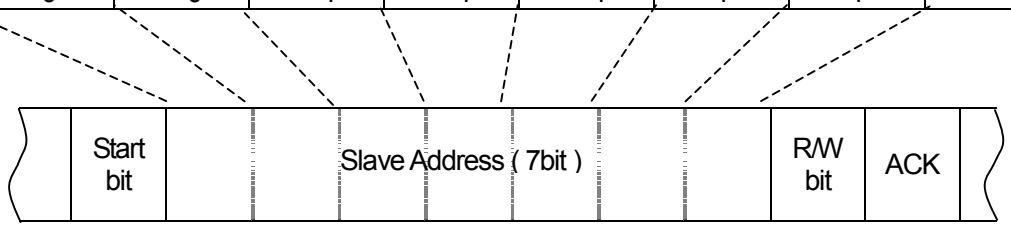
Note: When 4-Wire Serial bus is selected, The SDA/SDOUT pin is CMOS output. The SDOUT pin does not require a pull-up resistance.
When I^2C Bus is selected, this pin is a bi-directional Open Drain output. This pin, which is assigned for I^2C-Bus, requires a pull-up resistance.
The SDA/SDOUT pin isn't +5.0V Input tolerant. Please note the voltage level (Max voltage is VDDIO).

■ I²C-Bus

When the NJU26208 is configured for I²C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6)

Table 6 I²C-Bus Interface Slave address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

Note: The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer. Moreover, after sending S ("START" condition), Sr (repeated "START" condition) is not received but it becomes the waiting for the P ("STOP" condition). Therefore, please be sure to send P ("STOP" condition).

■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) that is latched on the falling transitions of SSb. The SDOUT pin is always CMOS output. This pin does not require a pull-up resistance.

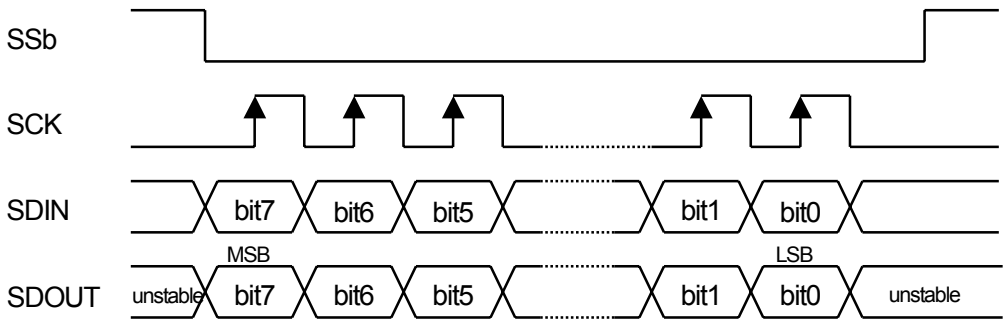


Fig. 5 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High".

When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.

After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High".

■ Pin setting

The NJU26208 operates default command setting after resetting the NJU26208. In addition, the NJU26208 restricts operation at power on by setting PROC pin and MUTEb pin. These pins are input pin. However, these pins operate as bi-directional pins. Connect with V_{DDIO} or V_{SSIO} through 3.3kΩ resistance.

Table 7 Pin setting

Pin No. SSOP44	Symbol	Setting	Function
13	PROC	"High"	The NJU26208 operates default setting after reset.
		"Low"	The NJU26208 does not operate after reset. Sending start command is required for starting operation.
11	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26208 outputs clock pulse through WDC during normal operation. The WDC clock is useful to check the status of the NJU26208 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26208. When the WDC clock pulse is lost or not normal clock cycle, the NJU26208 does not operate correctly. Then reset the NJU26208 and set up the NJU26208 again.
The WDC clock is able to be variable for 32ms to 640ms by command. Default setting of WDC clock is 192ms.

The WDC pin is open drain output. The WDC pin setting (Table 8)

Table 8 WDC pin setting

Pin No. SSOP44	Symbol	Setting	
12	WDC	WDC pin is used.	Connect with V_{DDIO} through 3.3kΩ resistance
		WDC pin is not used.	Connect with V_{SSIO} through 3.3kΩ resistance. Do not open WDC pin.

Note: The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing.
In slave mode, when there is no input of BCKI/LRI, the WDC pin can't output.
It is required to set up a sampling rate correctly.

■ Host command

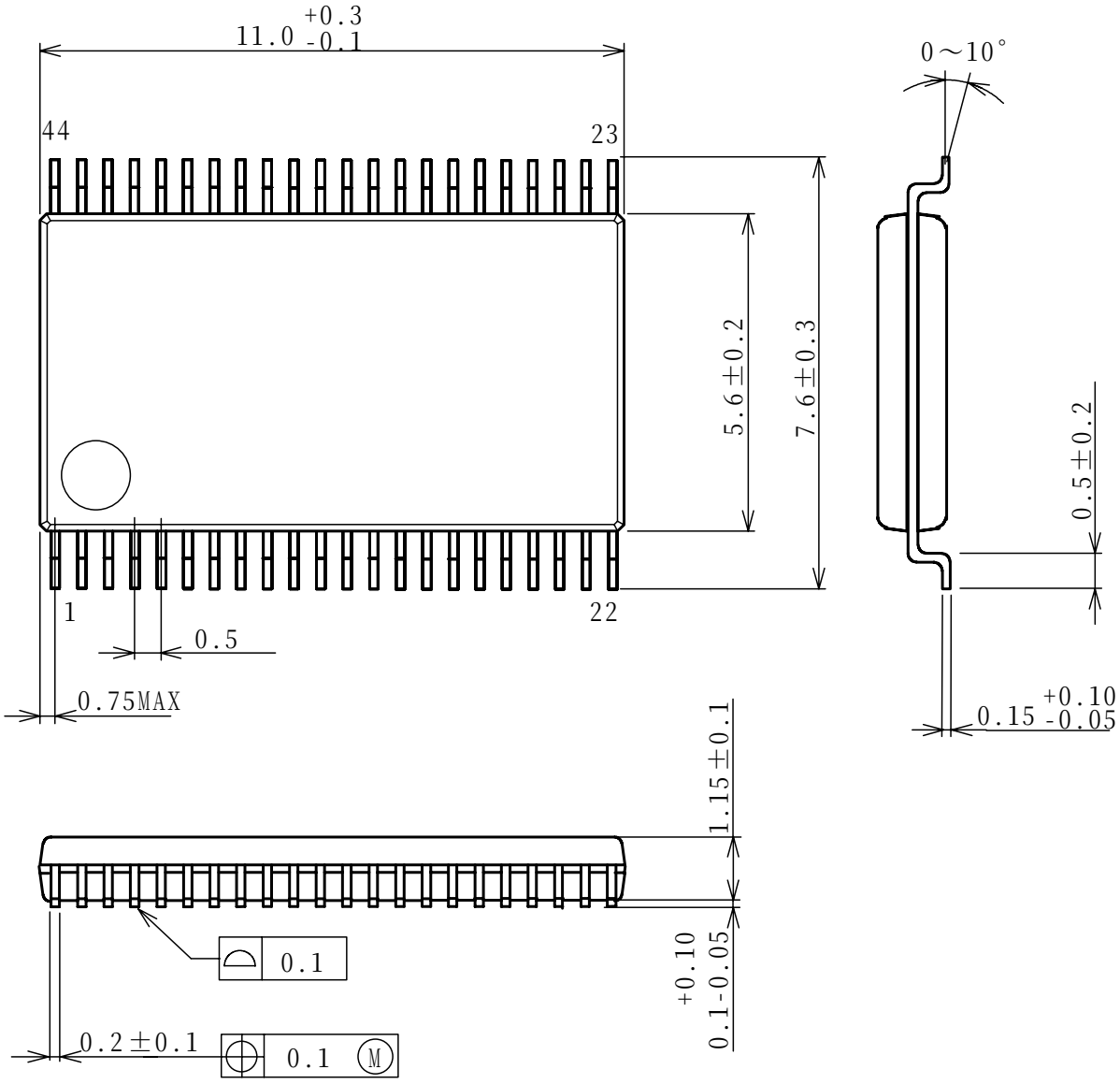
Table 9. NJU26208 command table

No.	Command
1	Set Task
2	CSII mode
3	CS Automotive
4	TruBass config
5	TruBass size select
6	TruBass gain control
7	Focus config
8	Focus gain control
9	Stereo mode select
10	PNG config
11	SW LPF cutoff select
12	TruSurround Config
13	TruSurround Downmix mode select
14	TruSurround gain control
15	Gain control
16	Mono Input Select
17	Sample Rate
18	Delay
19	System Status
20	Watch Dog config
21	Smooth control config.
22	Re initialize
23	Version Number
24	Function enable/disable
25	Reset
26	NOP

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (SRS Labs.) is required.

■ Package Dimensions

SSOP44, Pb Free



■ License Information

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