

Advantech

AQD-SD4L4GN24-HGI Datasheet

Rev. 0.0

2017-05-17

Description

AQD-SD4L4GN24-HGI is a DDR4 2400Mbps SO-DIMM high-speed, memory module that use 8pcs of 512M x 8 bits DDR4 SDRAM in FBGA package and a 4K bits serial EEPROM on a 260-pin printed circuit board.

AQD-SD4L4GN24-HGI is a Dual In-Line Memory Module and is intended for mounting into 260-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
 - JEDEC standard 1.2V(1.14V~1.26V) Power supply
VDDQ= 1.2V(1.14V~1.26V)
 - VPP = 2.5V +0.25V / -0.125V
 - Data transfer rates: PC3-12800
Programmable CAS
- Latency:10,11,12,13,14,15,16,17,18
- 8 bit pre-fetch
 - Burst Length (BL) switch on-the-fly BL8 or BC4
 - Bi-directional Differential Data-Strobe
 - On Die Termination, Nominal, Park, and Dynamic ODT
 - Serial presence detect with EEPROM
Asynchronous reset
 - Anti - sulfur resistor used
 - Industrial Temperature(-40°C ~ 85 °C)

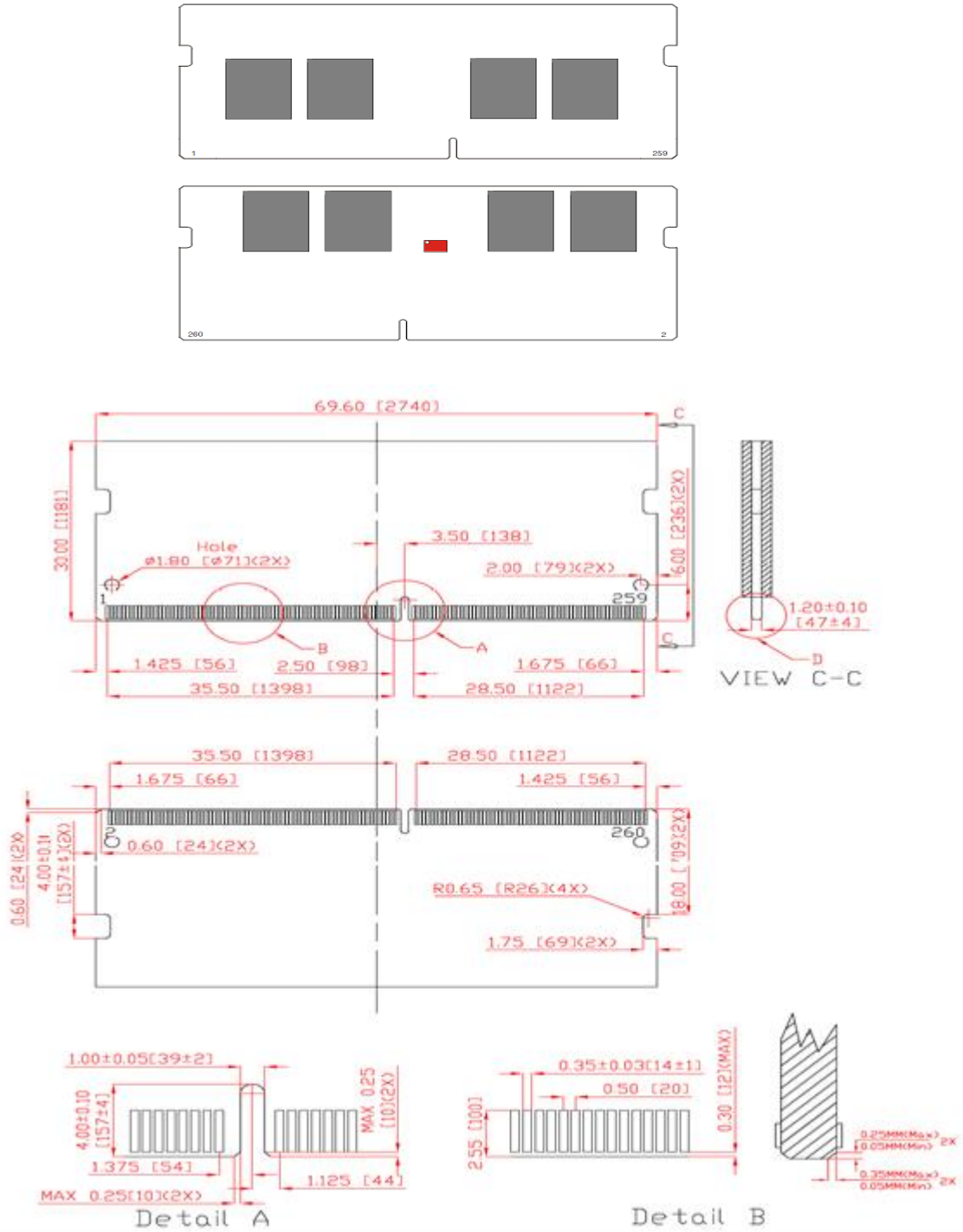
Pin Identification

| Symbol | Function |
|-------------------------------|--------------------|
| A0~A17 ¹ , BA0~BA1 | Address/Bank input |

| | |
|--------------------|--|
| DQ0~DQ63 | Bi-direction data bus. |
| DQS0_t~DQS17_t | Data Buffer data strobes |
| DQS0_c~DQS17_c | Data Buffer data strobes |
| CK0_t, CK1_t | Register clock input |
| CK0_c, CK1_c | Register clocks input |
| ODT0 &ODT1 | On-die termination control line |
| CS0_n~CS3_n | DIMM Rank Select Lines input. |
| RAS_n ² | Row address strobe |
| CAS_n ³ | Column address strobe |
| WE_n ⁴ | Write Enable |
| DM0~DM7 | Data masks/high data strobes |
| VDD | Core power supply |
| VDDQ | I/O driver power supply |
| V _{REFCA} | Command/address reference supply |
| V _{DDSPD} | SPD EEPROM power supply |
| SA0~SA2 | I2C serial bus address select for EEPROM |
| SCL | I2C serial bus clock for EEPROM |
| SDA | I2C serial bus data for EEPROM |
| VSS | Ground |
| RESET_n | Set DRAMs Known State |
| VTT | DRAM I/O termination supply |
| VPP | SDRAM Supply |
| ALERT_n | Register ALERT_n output |
| EVENT_n | SPD signals a thermal event has occurred |
| RFU | Reserved for future use |

1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Dimensions (Unit: millimeter)



Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.



Enabling an Intelligent Planet

260Pin DDR4 2400 1.2V SO-DIMM

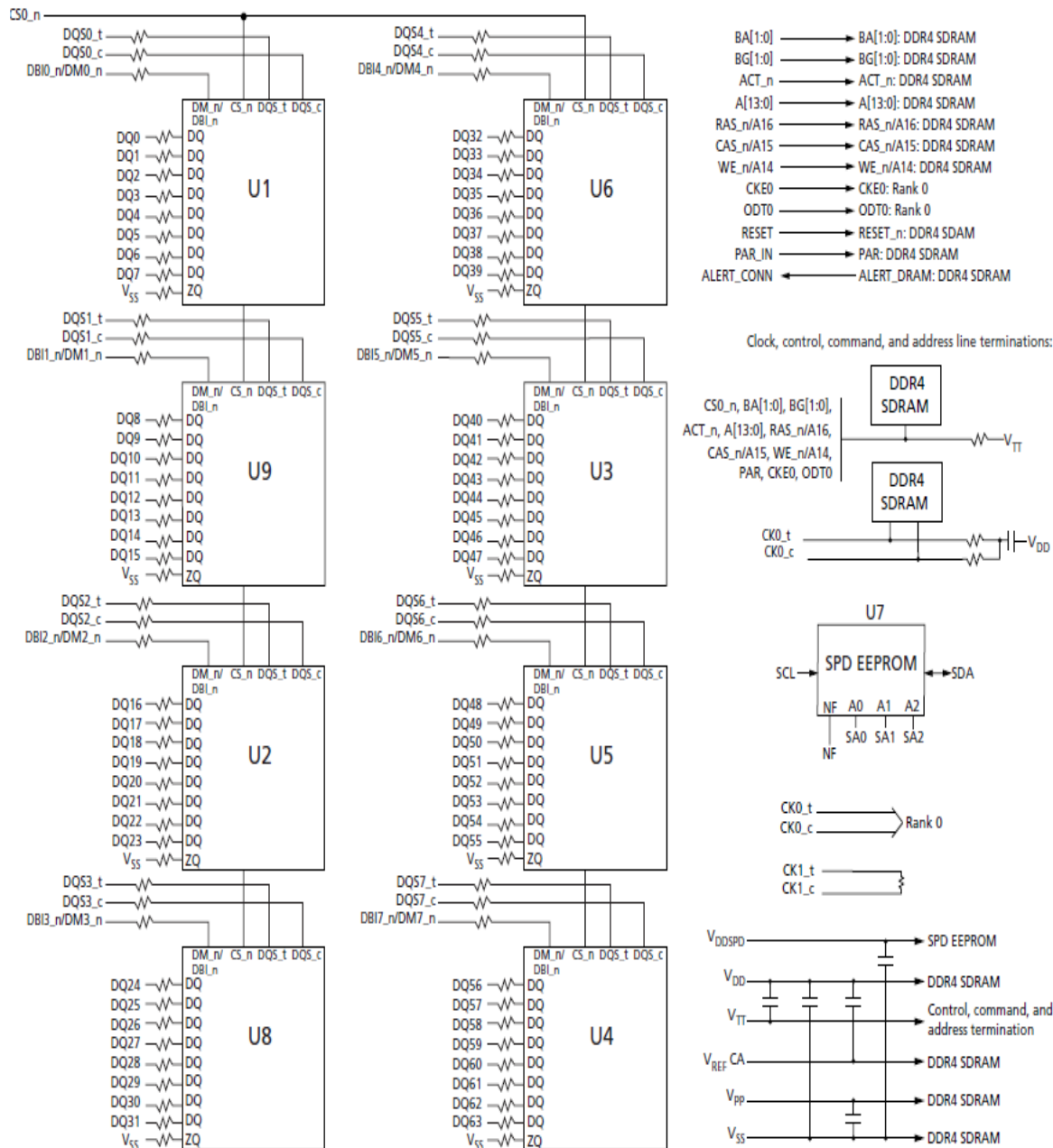
4GB Based on 512Mx8

AQD-SD4L4GN24-HGI

Pin Assignments

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back | Pin | Back |
|-----|--------------------|-----|--------------------|-----|--------------------|-----|-----------|-----|--------------|-----|--------------------|-----|------------|
| 1 | 12V | 41 | DQ10 | 81 | VSS | 121 | A9 | 161 | ODT1 | 201 | VSS | 241 | M7_n/D17_c |
| 2 | VSS | 42 | DQ11 | 82 | VSS | 122 | A7 | 162 | C0_CS2_n,NC | 202 | VSS | 242 | DQS7_t |
| 3 | DQ5 | 43 | VSS | 83 | DQ26 | 123 | VSS | 163 | VDD | 203 | DQ46 | 243 | VSS |
| 4 | DQ4 | 44 | VSS | 84 | DQ27 | 124 | DQ54 | 164 | VREFCA | 204 | DQ47 | 244 | VSS |
| 5 | VSS | 45 | DQ21 | 85 | VSS | 125 | VSS | 165 | C1_CS3_n,NC | 205 | VSS | 245 | DQ62 |
| 6 | VSS | 46 | DQ20 | 86 | VSS | 126 | DQ50 | 166 | SA2 | 206 | VSS | 246 | DQ63 |
| 7 | DQ1 | 47 | VSS | 87 | CB5, NC | 127 | VSS | 167 | VSS | 207 | DQ42 | 247 | VSS |
| 8 | DQ0 | 48 | VSS | 88 | CB4, NC | 128 | DQ60 | 168 | VSS | 208 | DQ43 | 248 | VSS |
| 9 | VSS | 49 | DQ17 | 89 | VSS | 129 | VDD | 169 | DQ37 | 209 | VSS | 249 | DQ58 |
| 10 | VSS | 50 | DQ16 | 90 | VSS | 130 | VDD | 170 | DQ36 | 210 | VSS | 250 | DQ59 |
| 11 | DQ S0_c | 51 | VSS | 91 | CB1, NC | 131 | A3 | 171 | VSS | 211 | DQ52 | 251 | VSS |
| 12 | D M0_n/D B10_n, NC | 52 | VSS | 92 | CB0, NC | 132 | A2 | 172 | VSS | 212 | DQ53 | 252 | VSS |
| 13 | DQS0_t | 53 | DQ S2_c | 93 | VSS | 133 | A1 | 173 | DQ33 | 213 | VSS | 253 | SCL |
| 14 | VSS | 54 | D M2_n/D B12_n, NC | 94 | VSS | 134 | EVENT_n | 174 | DQ32 | 214 | VSS | 254 | SDA |
| 15 | VSS | 55 | DQS2_t | 95 | DQ S8_c | 135 | VDD | 175 | VSS | 215 | DQ49 | 255 | VDDSPD |
| 16 | DQ6 | 56 | VSS | 96 | D M8_n/D B18_n, NC | 136 | VDD | 176 | VSS | 216 | DQ48 | 256 | SA0 |
| 17 | DQ7 | 57 | VSS | 97 | DQ S8_t | 137 | CK0_t | 177 | DQS4_c | 217 | VSS | 257 | VPP |
| 18 | VSS | 58 | DQ22 | 98 | VSS | 138 | CK1_t | 178 | M4_n/D B14_c | 218 | VSS | 258 | VTT |
| 19 | VSS | 59 | DQ23 | 99 | VSS | 139 | CK0_c | 179 | DQS4_t | 219 | DQS6_c | 259 | VPP |
| 20 | DQ2 | 60 | VSS | 100 | CB6, NC | 140 | CK1_c | 180 | VSS | 220 | D M6_n/D B16_n, NC | 260 | SA1 |
| 21 | DQ3 | 61 | VSS | 101 | CB2, NC | 141 | VDD | 181 | VSS | 221 | DQS6_t | | |
| 22 | VSS | 62 | DQ18 | 102 | VSS | 142 | VDD | 182 | DQ39 | 222 | VSS | | |
| 23 | VSS | 63 | DQ19 | 103 | VSS | 143 | PARITY | 183 | DQ38 | 223 | VSS | | |
| 24 | DQ12 | 64 | VSS | 104 | CB7, NC | 144 | A0 | 184 | VSS | 224 | DQ54 | | |
| 25 | DQ13 | 65 | VSS | 105 | CB3, NC | 145 | BA1 | 185 | VSS | 225 | DQ55 | | |
| 26 | VSS | 66 | DQ28 | 106 | VSS | 146 | A10/AP | 186 | DQ35 | 226 | VSS | | |
| 27 | VSS | 67 | DQ29 | 107 | VSS | 147 | VDD | 187 | DQ34 | 227 | VSS | | |
| 28 | DQ8 | 68 | VSS | 108 | RESET_n | 148 | VDD | 188 | VSS | 228 | DQ50 | | |
| 29 | DQ9 | 69 | VSS | 109 | CKE0 | 149 | CS0_n | 189 | VSS | 229 | DQ51 | | |
| 30 | VSS | 70 | DQ24 | 110 | CKE1 | 150 | BA0 | 190 | DQ45 | 230 | VSS | | |
| 31 | VSS | 71 | DQ25 | 111 | VDD | 151 | A14/WE_n | 191 | DQ44 | 231 | VSS | | |
| 32 | DQ S1_c | 72 | VSS | 112 | VDD | 152 | A16/RAS_n | 192 | VSS | 232 | DQ60 | | |
| 33 | D M1_n/D B11_n, NC | 73 | VSS | 113 | BG1 | 153 | VDD | 193 | VSS | 233 | DQ61 | | |
| 34 | DQS1_t | 74 | DQ S3_c | 114 | ACT_n | 154 | VDD | 194 | DQ41 | 234 | VSS | | |
| 35 | VSS | 75 | D M3_n/D B13_n, NC | 115 | BG0 | 155 | ODT0 | 195 | DQ40 | 235 | VSS | | |
| 36 | VSS | 76 | DQ S3_t | 116 | ALERT_n | 156 | A15/CAS_n | 196 | VSS | 236 | DQ57 | | |
| 37 | DQ15 | 77 | VSS | 117 | VDD | 157 | CS1_n | 197 | VSS | 237 | DQ56 | | |
| 38 | DQ14 | 78 | VSS | 118 | VDD | 158 | A13 | 198 | DQS5_c | 238 | VSS | | |
| 39 | VSS | 79 | DQ30 | 119 | A12 | 159 | VDD | 199 | M5_n/D B15_c | 239 | VSS | | |
| 40 | VSS | 80 | DQ31 | 120 | A11 | 160 | VDD | 200 | VSS | 240 | DQS7_c | | |

4GB, 512Mx8 Module (1 Rank x8)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

- This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

| Parameter | Symbol | Rating | Unit | Note |
|-----------------------|--------|-----------|------|------|
| Operating Temperature | TOPER | -40 to 85 | °C | 1,2 |

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

| Parameter | Symbol | Value | Unit | Note |
|-------------------------------------|-----------|------------|------|------|
| Voltage on VDD relative to Vss | VDD | -0.3 ~ 1.5 | V | 1 |
| Voltage on VDDQ pin relative to Vss | VDDQ | -0.3 ~ 1.5 | V | 1 |
| Voltage on any pin relative to Vss | VIN, VOUT | -0.3 ~ 1.5 | V | 1 |
| Storage temperature | TSTG | -55~+100 | °C | 1,2 |

Note:

1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

| Parameter | Symbol | Voltage | Rating | | | Unit | Notes |
|---------------------------------|-------------------------|---------|------------------|----------|------------------|------|-------|
| | | | Min | Typ. | Max | | |
| Supply voltage | VDD | 1.2V | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| Supply voltage for Output | VDDQ | 1.2V | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| I/O Reference Voltage (DQ) | VREF _{DQ} (DC) | 1.2V | 0.49*VDD | 0.50*VDD | 0.51*VDD | V | 4 |
| I/O Reference Voltage (CMD/ADD) | VREF _{CA} (DC) | 1.2V | 0.49*VDD | 0.50*VDD | 0.51*VDD | V | 4 |
| AC Input Logic High | VIH(AC) | 1.2V | VREF+100 | - | VDD ² | mV | |
| AC Input Logic Low | VIL(AC) | 1.2V | VSS ² | - | VREF-100 | mV | |
| DC Input Logic High | VIH(DC) | 1.2V | VREF+75 | - | VDD | mV | |
| DC Input Logic Low | VIL(DC) | 1.2V | VSS | - | VREF-75 | mV | |

Note:

- (1) Under all conditions VDDQ must be less than or equal to VDD.
- (2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- (3) The DC bandwidth is limited to 200MHz.
- (4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

IDD Specification parameters Definition - 4GB (1 Rank x8)

| Parameter | Symbol | DDR4 2400 CL17 | Unit |
|---|---------------------|----------------|------|
| One bank ACTIVATE-PRECHARGE current | IDD0 ¹ | 232 | mA |
| One bank ACTIVATE-PRECHARGE, wordline boost, IPP current | IPP0 ¹ | 14 | mA |
| One Bank Active-Read-Precharge Current | IDD1 ¹ | 282 | mA |
| Precharge Standby Current | IDD2N ² | 117 | mA |
| Precharge standby ODT current | IDD2NT ¹ | 156 | mA |
| Precharge Power-Down Current | IDD2P ² | 79 | mA |
| Precharge Quiet Standby Current | IDD2Q ² | 114 | mA |
| Active standby current | IDD3N ² | 213 | mA |
| Active standby IPP current | IPP3N ² | 7 | mA |
| Active Power-Down Current | IDD3P ² | 156 | mA |
| Burst Read Current | IDD4R ¹ | 742 | mA |
| Burst write current | IDD4W ¹ | 798 | mA |
| Burst refresh current (1x REF) | IDD5B ¹ | 1457 | mA |
| Burst refresh IPP current (1x REF) | IPP5B ¹ | 254 | mA |
| Self refresh current: Normal temperature range (0–85°C) | IDD6N ² | 77 | mA |
| Self refresh current: Extended temperature range (0–95°C) | IDD6E ² | 97 | mA |
| Bank interleave read current | IDD7 ¹ | 991 | mA |
| Bank interleave read IPP current | IPP7 ¹ | 77 | mA |
| Maximum power-down current | IDD8 ² | 30 | mA |

Note: 1. One module rank in the active IDD/PP, the other rank in IDD2P/PP3N.
2. All ranks in this IDD/PP condition.
3. IDD current measure method and detail patterns are described on DDR4 component datasheet. Only for reference.

■ Timing Parameters & Specifications

| Parameter | Symbol | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | Units | NOTE |
|--|----------------|--|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|----------|-----------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Speed | | | | | | | | | |
| Clock Timing | | | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF) | 8 | - | 8 | - | 8 | 20 | ns | 22 |
| Average Clock Period | tCK(avg) | 1.071 | <1.25 | 0.938 | <1.071 | 0.833 | <0.938 | ps | 35,36 |
| Average high pulse width | tCH(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | tCK(avg)min + tJIT(per)min_tot | tCK(avg)max + tJIT(per)max_tot | tCK(avg)min + tJIT(per)min_tot | tCK(avg)max + tJIT(per)max_tot | tCK(avg)min + tJIT(per)min_tot | tCK(avg)max + tJIT(per)max_tot | tCK(avg) | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.45 | - | 0.45 | - | 0.45 | - | tCK(avg) | 23 |
| Absolute clock LOW pulse width | tCL(abs) | 0.45 | - | 0.45 | - | 0.45 | - | tCK(avg) | 24 |
| Clock Period Jitter- total | tJIT(per)_tot | -54 | 54 | -0.1 | 0.1 | -42 | 42 | ps | 23 |
| Clock Period Jitter- deterministic | tJIT(per)_dj | -27 | 27 | TBD | TBD | -21 | 21 | ps | 26 |
| Clock Period Jitter during DLL locking period | tJIT(per)_lck | -43 | 43 | TBD | TBD | -33 | 33 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc)_total | | 107 | | 94 | | 83 | ps | 25 |
| Cycle to Cycle Period Jitter deterministic | tJIT(cc)_dj | | 54 | | 47 | | 42 | ps | 26 |
| Cycle to Cycle Period Jitter during DLL locking period | tJIT(cc)_lck | | 86 | | 75 | | 67 | ps | |
| Duty Cycle Jitter | tJIT(duty) | TBD | TBD | TBD | TBD | TBD | TBD | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -79 | 79 | -69 | 69 | -61 | 61 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -94 | 94 | -82 | 82 | -73 | 73 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -104 | 104 | -91 | 91 | -81 | 81 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -112 | 112 | -98 | 98 | -87 | 87 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -119 | 119 | -104 | 104 | -92 | 92 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -124 | 124 | -109 | 109 | -97 | 97 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -129 | 129 | -113 | 113 | -101 | 101 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -134 | 134 | -117 | 117 | -104 | 104 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -137 | 137 | -120 | 120 | -107 | 107 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -141 | 141 | -123 | 123 | -110 | 110 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -144 | 144 | -126 | 126 | -112 | 112 | ps | |
| Cumulative error across 13 cycles | tERR(13per) | -147 | 147 | -129 | 129 | -114 | 114 | ps | |
| Cumulative error across 14 cycles | tERR(14per) | -150 | 150 | -131 | 131 | -116 | 116 | ps | |
| Cumulative error across 15 cycles | tERR(15per) | -152 | 152 | -133 | 133 | -118 | 118 | ps | |
| Cumulative error across 16 cycles | tERR(16per) | -155 | 155 | -135 | 135 | -120 | 120 | ps | |
| Cumulative error across 17 cycles | tERR(17per) | -157 | 157 | -137 | 137 | -122 | 122 | ps | |
| Cumulative error across 18 cycles | tERR(18per) | -159 | 159 | -139 | 139 | -124 | 124 | ps | |
| Cumulative error across n = 13, 14 ... 49, 50 cycles | tERR(nper) | tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max) | | | | | | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 100 | - | 80 | - | 62 | - | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vref levels | tIS(Vref) | 200 | - | 180 | - | 162 | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 125 | - | 105 | - | 87 | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vref levels | tIH(Vref) | 200 | - | 180 | - | 162 | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 525 | - | 460 | - | 410 | - | ps | |
| Command and Address Timing | | | | | | | | | |
| CAS_n to CAS_n command delay for same bank group | tCCD_L | max(5 nCK, 6.250 ns) | - | max(5 nCK, 6.250 ns) | - | max(5 nCK, 6.250 ns) | - | nCK | 34 |
| CAS_n to CAS_n command delay for different bank group | tCCD_S | 4 | - | 4 | - | 4 | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | tRRD_S(2K) | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size | tRRD_S(1K) | Max(4nCK,4.2ns) | - | Max(4nCK,3.7ns) | - | Max(4nCK,3.3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size | tRRD_S(1/2K) | Max(4nCK,4.2ns) | - | Max(4nCK,3.7ns) | - | Max(4nCK,3.3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size | tRRD_L(2K) | Max(4nCK,6.4ns) | - | Max(4nCK,6.4ns) | - | Max(4nCK,6.4ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size | tRRD_L(1K) | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,4.9ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size | tRRD_L(1/2K) | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,4.9ns) | - | nCK | 34 |
| Four activate window for 2KB page size | tFAW_2K | Max(28nCK,3 0ns) | - | Max(28nCK,3 0ns) | - | Max(28nCK,3 0ns) | - | ns | 34 |
| Four activate window for 1KB page size | tFAW_1K | Max(20nCK,2 3ns) | - | Max(20nCK,2 1ns) | - | Max(20nCK,2 1ns) | - | ns | 34 |
| Four activate window for 1/2KB page size | tFAW_1/2K | Max(16nCK,1 7ns) | - | Max(16nCK,1 5ns) | - | Max(16nCK,1 3ns) | - | ns | 34 |
| Delay from start of internal write transaction to internal read command for different bank group | tWTR_S | max(2nCK,2.5ns) | - | Max(28nCK,30ns) | - | max(2nCK, 2.5ns) | - | | 1,2,e, 34 |
| Delay from start of internal write transaction to internal read command for same bank group | tWTR_L | max(4nCK,7.5ns) | - | Max(20nCK,21ns) | - | max(4nCK,7.5ns) | - | | 1,34 |
| Internal READ Command to PRECHARGE Command delay | tRTP | max(4nCK,7.5ns) | - | Max(16nCK,13ns) | - | max(4nCK,7.5ns) | - | | |
| WRITE recovery time | tWR | 15 | - | 15 | - | 15 | - | ns | 1 |

| Speed | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | Units | NOTE |
|---|------------------|---|--------|------------------------------|--------|------------------------------|--------|------------|----------|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Write recovery time when CRC and DM are enabled | tWR_CRC_DM | tWR+max (5nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | ns | 1,28 |
| delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled | tWTR_S_C RC_DM | tWTR_S+max (5nCK,3.75ns) | - | tWTR_S+max (5nCK,3.75ns) | - | tWTR_S+max (5nCK,3.75ns) | - | ns | 2, 29,34 |
| delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled | tWTR_L_C RC_DM | tWTR_L+max (5nCK,3.75ns) | - | tWTR_L+max (5nCK,3.75ns) | - | tWTR_L+max (5nCK,3.75ns) | - | ns | 3,30,34 |
| DLL locking time | tDLLK | 597 | - | 768 | - | 768 | - | nCK | |
| Mode Register Set command cycle time | tMRD | 8 | - | 8 | - | 8 | - | nCK | |
| Mode Register Set command update delay | tMOD | max(24nCK,15ns) | - | max(24nCK,15ns) | - | max(24nCK,15ns) | - | | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | 1 | - | nCK | 33 |
| Multi Purpose Register Write Recovery Time | tWR_MPR | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | | |
| Auto precharge write recovery + precharge time | tDAL(min) | Programmed WR + roundup (tRP / tCK(avg)) | | | | | | nCK | |
| DQ0 or DQ0 driven to 0 set-up time to first DQS rising edge | tPDA_S | 0.5 | - | 0.5 | - | 0.5 | - | UI | 45,47 |
| DQ0 or DQ0 driven to 0 hold time from last DQS fall-ing edge | tPDA_H | 0.5 | - | 0.5 | - | 0.5 | - | UI | 45,47 |
| CS_n to Command Address Latency | | | | | | | | | |
| CS_n to Command Address Latency | tCAL | 4 | - | 4 | - | 5 | - | nCK | |
| DRAM Data Timing | | | | | | | | | |
| DQS_t,DQS_c to DQ skew, per group, per access | tDQSQ | - | 0.16 | - | 0.16 | - | 0.16 | tCK(avg)/2 | 13,18 |
| DQ output hold time from DQS_t,DQS_c | tQH | 0.76 | - | 0.76 | - | 0.76 | - | tCK(avg)/2 | 13,17,18 |
| Data Valid Window per device: tQH - tDQSQ for a device | tDVWd | 0.63 | - | 0.64 | - | 0.64 | - | UI | 16,17,18 |
| Data Valid Window per device, per pin: tQH - tDQSQ each device' s output | tDVWp | 0.66 | - | 0.69 | - | 0.72 | - | UI | 16,17,18 |
| Data Strobe Timing | | | | | | | | | |
| DQS_t, DQS_c differential READ Preamble | tRPRE | 0.9 | NOTE44 | 0.9 | NOTE44 | 0.9 | NOTE44 | tCK | 40 |
| DQS_t, DQS_c differential READ Postamble | tRPST | 0.33 | TBD | 0.33 | TBD | 0.33 | TBD | tCK | 41 |
| DQS_t,DQS_c differential output high time | tQSH | 0.4 | - | 0.4 | - | 0.4 | - | tCK | |
| DQS_t,DQS_c differential output low time | tQSL | 0.4 | - | 0.4 | - | 0.4 | - | tCK | 21 |
| DQS_t, DQS_c differential WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | tCK | 20 |
| DQS_t, DQS_c differential WRITE Postamble | tWPST | 0.33 | TBD | 0.33 | TBD | 0.33 | TBD | tCK | 42 |
| DQS_t and DQS_c low-impedance time (Referenced from RL-1) | tLZ(DQS) | -390 | 195 | -360 | 180 | -300 | 150 | tCK | 43 |
| DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 195 | - | 180 | - | 150 | tCK | |
| DQS_t, DQS_c differential input low pulse width | tDQSL | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | ps | |
| DQS_t, DQS_c differential input high pulse width | tDQSH | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | ps | |
| DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble) | tDQSS | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | tCK | |
| DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge | tDSS | 0.18 | - | 0.18 | - | 0.18 | - | tCK | |
| DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge | tDSH | 0.18 | - | 0.18 | - | 0.18 | - | tCK | |
| DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode | tDQSCK (DLL On) | -195 | 195 | -180 | 180 | -175 | 175 | ps | 37,38,39 |
| DQS_t, DQS_c rising edge output variance window per DRAM | tDQSCKI (DLL On) | - | 330 | - | 310 | - | 290 | ps | 37,38,39 |
| MPSM Timing | | | | | | | | | |
| Command path disable delay upon MPSM entry | tMPED | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | | |
| Valid clock requirement after MPSM entry | tCKMPE | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | | |
| Valid clock requirement before MPSM exit | tCKMPX | tCKSRX(min) | - | tCKSRX(min) | - | tCKSRX(min) | - | | |
| Exit MPSM to commands not requiring a locked DLL | tXMP | txs(imin) | - | txs(imin) | - | txs(imin) | - | | |
| Exit MPSM to commands requiring a locked DLL | tXMPDLL | tXMP(min) + tXSDDL(min) | - | tXMP(min) + tXSDDL(min) | - | tXMP(min) + tXSDDL(min) | - | | |
| CS setup time to CKE | tMPX_S | tISmin + tIHmin | - | tISmin + tIHmin | - | tISmin + tIHmin | - | | |
| Calibration Timing | | | | | | | | | |
| Power-up and RESET calibration time | tZQinit | 1024 | - | 1024 | - | 1024 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 512 | - | 512 | - | 512 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 128 | - | 128 | - | 128 | - | nCK | |
| Reset/Self Refresh Timing | | | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max (5nCK,tRFC(min)+10ns) | - | max (5nCK,tRFC(min)+10ns) | - | max (5nCK,tRFC(min)+10ns) | - | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tRFC(min)+10ns | - | tRFC(min)+10ns | - | tRFC(min)+10ns | - | | |
| SRX to commands not requiring a locked DLL in Self Refresh ABORT | tXS_ABORT(min) | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | | |
| Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down) | tXS_FAST (min) | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | | |



Enabling an Intelligent Planet

260Pin DDR4 2400 1.2V SO-DIMM

4GB Based on 512Mx8

AQD-SD4L4GN24-HGI

| Speed | Parameter | Symbol | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | Units | NOTE |
|------------------------------|--|----------------|---------------------|---------------|---------------------|---------------|---------------------|---------------|----------|-------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| | Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | | |
| | Minimum CKE low width for Self refresh entry to exit timing | tCKESR | tCKE(min)+1nCK | - | tCKE(min)+1nCK | - | tCKE(min)+1nCK | - | | |
| | Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled | tCKESR_PAR | tCKE(min)+1nCK+PL | - | tCKE(min)+1nCK+PL | - | tCKE(min)+1nCK+PL | - | | |
| | Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | max(5nCK,10ns) | - | max(5nCK,10ns) | - | max(5nCK,10ns) | - | | |
| | Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled | tCKSRE_PAR | max(5nCK,10ns)+PL | - | max(5nCK,10ns)+PL | - | max(5nCK,10ns)+PL | - | | |
| | Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | max(5nCK,10ns) | - | max(5nCK,10ns) | - | max(5nCK,10ns) | - | | |
| Power Down Timing | | | | | | | | | | |
| | Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max(4nCK,6ns) | - | max(4nCK,6ns) | - | max(4nCK,6ns) | - | | |
| | CKE minimum pulse width | tCKE | max(3nCK, 5ns) | - | max(3nCK, 5ns) | - | max(3nCK, 5ns) | - | nCK | 31,32 |
| | Command pass disable delay | tCPDED | 4 | - | 4 | - | 4 | - | | |
| | Power Down Entry to Exit Timing | tPD | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | | 6 |
| | Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | 2 | - | 2 | - | nCK | 7 |
| | Timing of PRE or PREA command to Power Down entry | tPRPDEN | 1 | - | 2 | - | 2 | - | nCK | 7 |
| | Timing of RD/RDA command to Power Down entry | tRDPDEN | RL+4+1 | - | RL+4+1 | - | RL+4+1 | - | nCK | |
| | Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | WL+4+(tWR/tCK)(avg) | - | WL+4+(tWR/tCK)(avg) | - | WL+4+(tWR/tCK)(avg) | - | nCK | 4 |
| | Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | WL+4+WR+1 | - | WL+4+WR+1 | - | WL+4+WR+1 | - | nCK | 5 |
| | Timing of WR command to Power Down entry (BC4MRS) | tWRPBC4DEN | WL+2+(tWR/tCK)(avg) | - | WL+2+(tWR/tCK)(avg) | - | WL+2+(tWR/tCK)(avg) | - | nCK | 4 |
| | Timing of WRA command to Power Down entry (BC4MRS) | tWRAPBC4DEN | WL+2+WR+1 | - | WL+2+WR+1 | - | WL+2+WR+1 | - | nCK | 5 |
| | Timing of REF command to Power Down entry | tREFPDEN | 1 | - | 2 | - | 2 | - | nCK | 7 |
| | Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | | |
| PDA Timing | | | | | | | | | | |
| | Mode Register Set command cycle time in PDA mode | tMRD_PDA | max(16nCK,10ns) | | max(16nCK,10ns) | | max(16nCK,10ns) | | | |
| | Mode Register Set command update delay in PDA mode | tMOD_PDA | | tMOD | | tMOD | | tMOD | | |
| ODT Timing | | | | | | | | | | |
| | Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONAS | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | ns | |
| | Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFAS | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | ns | |
| | RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| Write Leveling Timing | | | | | | | | | | |
| | First DQS _t /DQS _n rising edge after write leveling mode is programmed | tWLMRD | 40 | - | 40 | - | 40 | - | nCK | 12 |
| | DQS _t /DQS _n delay after write leveling mode is programmed | tWLDQSEN | 25 | - | 25 | - | 25 | - | nCK | 12 |
| | Write leveling setup time from rising CK _t , CK _c crossing to rising DQS _t /DQS _n crossing | tWLS | 0.13 | - | 0.13 | - | 0.13 | - | tCK(avg) | |
| | Write leveling hold time from rising DQS _t /DQS _n crossing to rising CK _t , CK _c crossing | tWLH | 0.13 | - | 0.13 | - | 0.13 | - | tCK(avg) | |
| | Write leveling output delay | tWLO | 0 | 9.5 | 0 | 9.5 | 0 | 9.5 | ns | |
| | Write leveling output error | tWLOE | | | | | | | ns | |
| CA Parity Timing | | | | | | | | | | |
| | Commands not guaranteed to be executed during this time | tPAR_UNKNOWN | - | Max(2nCK,3ns) | - | Max(2nCK,3ns) | - | Max(2nCK,3ns) | | |
| | Delay from errant command to ALERT _n assertion | tPAR_ALERT_ON | - | PL+6ns | - | PL+6ns | - | PL+6ns | | |
| | Pulse width of ALERT _n signal when asserted | tPAR_ALERT_PW | 56 | 112 | 64 | 128 | 72 | 144 | nCK | |
| | Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode | tPAR_ALERT_RSP | - | 50 | - | 57 | - | 64 | nCK | |
| | Parity Latency | PL | | 4 | | 4 | | 5 | nCK | |
| CRC Error Reporting | | | | | | | | | | |
| | CRC error to ALERT _n latency | tCRC_ALERT | 3 | 13 | 3 | 13 | 3 | 13 | ns | |
| | CRC ALERT _n pulse width | CRC_ALERT_PW | 6 | 10 | 6 | 10 | 6 | 10 | nCK | |
| tREFI | | | | | | | | | | |
| tRFC1 (min) | 2Gb | 160 | - | 160 | - | 160 | - | 160 | ns | |
| | 4Gb | 260 | - | 260 | - | 260 | - | 260 | ns | |
| | 8Gb | 350 | - | 350 | - | 350 | - | 350 | ns | |
| | 16Gb | TBD | - | TBD | - | TBD | - | TBD | ns | |
| tRFC2 (min) | 2Gb | 110 | - | 110 | - | 110 | - | 110 | ns | |
| | 4Gb | 160 | - | 160 | - | 160 | - | 160 | ns | |
| | 8Gb | 260 | - | 260 | - | 260 | - | 260 | ns | |
| | 16Gb | TBD | - | TBD | - | TBD | - | TBD | ns | |
| tRFC4 (min) | 2Gb | 90 | - | 90 | - | 90 | - | 90 | ns | |
| | 4Gb | 110 | - | 110 | - | 110 | - | 110 | ns | |
| | 8Gb | 160 | - | 160 | - | 160 | - | 160 | ns | |
| | 16Gb | TBD | - | TBD | - | TBD | - | TBD | ns | |



Enabling an Intelligent Planet

260Pin DDR4 2400 1.2V SO-DIMM
 4GB Based on 512Mx8
 AQD-SD4L4GN24-HGI

SERIAL PRESENCE DETECT SPECIFICATION (AQD-SD4L4GN24-HGI Serial Presence Detect)

| Byte | Function Described | Function | HEX Value |
|-------|--|--|-----------|
| 0 | Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage | SPD Total: 512Bytes, SPD Used : 384Bytes | 23 |
| 1 | SPD Revision | Version 1.1 | 11 |
| 2 | Key Byte / DRAM Device Type | DDR4 SDRAM | 0C |
| 3 | Key Byte / Module Type | SO-DIMM | 03 |
| 4 | SDRAM Density and Banks | 4 bank group / 4 bank 4Gb | 84 |
| 5 | SDRAM Addressing | Row : 15 Column : 10 | 19 |
| 6 | SDRAM Package Type | Mono / Not specified | 00 |
| 7 | SDRAM Optional Features | Unlimited MAC | 08 |
| 8 | SDRAM Thermal and Refresh Options | - | 00 |
| 9 | Other SDRAM Optional Features | Post package repair supported | 40 |
| 10 | Reserved | - | 00 |
| 11 | Module Nominal Voltage, VDD | 1.2v | 03 |
| 12 | Module Organization | 1Rank x8 | 01 |
| 13 | Module Memory Bus Width | Non ECC 64bits | 03 |
| 14 | Module Thermal Sensor | Thermal Sensor on Module | 80 |
| 15-16 | Reserved | - | 00 |
| 17 | Timebases | MTB: 125ps FTB: 1ps | 00 |
| 18 | SDRAM Minimum Cycle Time (tCKAVGmin) | 0.893 ns | 07 |
| 19 | SDRAM Maximum Cycle Time (tCKAVGmax) | 1.5 ns | 0C |
| 20 | CAS Latencies Supported, First Byte | CL 10,11,12,13,14 | F8 |
| 21 | CAS Latencies Supported, Second Byte | CL 15,16,17,18 | 0F |
| 22 | CAS Latencies Supported, Third Byte | - | 00 |
| 23 | CAS Latencies Supported, Fourth Byte | - | 00 |
| 24 | Minimum CAS Latency Time(tAmin) | 13.75 ns | 6E |
| 25 | Minimum RAS to CAS Delay Time (tRCDmin) | 13.75 ns | 6E |
| 26 | Minimum Row Precharge Delay Time (tRPmin) | 13.75 ns | 6E |
| 27 | Upper Nibbles for tRASmin and tRCmin | - | 11 |
| 28 | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte | 32 ns | 00 |
| 29 | Minimum Active to Active Refresh Delay Time (tRCmin), Least Significant Byte | 45.75 ns | 6E |
| 30 | Minimum Refresh Recovery Delay Time (tRFC1min), Least Significant Byte | - | 20 |
| 31 | Minimum Refresh Recovery Delay Time (tRFC1min), Most Significant Byte | 260 ns | 08 |
| 32 | Minimum Refresh Recovery Delay Time (tRFC2min), Least Significant Byte | - | 00 |
| 33 | Minimum Refresh Recovery Delay Time (tRFC2min), Most Significant Byte | 160 ns | 05 |
| 34 | Minimum Refresh Recovery Delay Time (tRFC4min), Least Significant Byte | - | 70 |
| 35 | Minimum Refresh Recovery Delay Time (tRFC4min), Most Significant Byte | 110 ns | 03 |
| 36 | Minimum Four Activate Window Time (tFAWmin), Most Significant Nibble | - | 00 |
| 37 | Minimum Four Activate Window Time (tFAWmin), Least Significant Byte | 21 ns | A8 |
| 38 | Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group | 3.3 ns | 1B |
| 39 | Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group | 4.9 ns | 28 |
| 40 | Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group | 5 ns | 28 |
| 41 | Upper Nibble for tWRmin | 15 ns | 00 |
| 42 | Minimum Write Recovery Time(tWRmin) | 15 ns | 78 |
| 43 | Upper Nibbles for tWRmin | 257.5 ns | 00 |
| 44 | Minimum Write to Read Time(tWTR_Smin) , different bank group | 2.5 ns | 14 |
| 45 | Minimum Write to Read Time(tWTR_Lmin) , same bank group | 7.5 ns | 3C |
| 46-59 | Reserved, Base Configuration Section | - | 00 |
| 60 | Connector to SDRAM Bit Mapping | DQ0, DQ1, DQ2, DQ3 | 0E |
| 61 | Connector to SDRAM Bit Mapping | DQ4, DQ5, DQ6, DQ7 | 2E |
| 62 | Connector to SDRAM Bit Mapping | DQ8, DQ9, DQ10, DQ11 | 2E |
| 63 | Connector to SDRAM Bit Mapping | DQ12, DQ13, DQ14, DQ15 | 04 |
| 64 | Connector to SDRAM Bit Mapping | DQ16, DQ17, DQ18, DQ19 | 03 |
| 65 | Connector to SDRAM Bit Mapping | DQ20, DQ21, DQ22, DQ23 | 23 |
| 66 | Connector to SDRAM Bit Mapping | DQ24, DQ25, DQ26, DQ27 | 24 |
| 67 | Connector to SDRAM Bit Mapping | DQ28, DQ29, DQ30, DQ31 | 04 |
| 68 | Connector to SDRAM Bit Mapping | CB0-3 | 00 |
| 69 | Connector to SDRAM Bit Mapping | CB4-7 | 00 |
| 70 | Connector to SDRAM Bit Mapping | DQ32, DQ33, DQ34, DQ35 | 24 |
| 71 | Connector to SDRAM Bit Mapping | DQ36, DQ37, DQ38, DQ39 | 04 |
| 72 | Connector to SDRAM Bit Mapping | DQ40, DQ41, DQ42, DQ43 | 04 |
| 73 | Connector to SDRAM Bit Mapping | DQ44, DQ45, DQ46, DQ47 | 24 |
| 74 | Connector to SDRAM Bit Mapping | DQ48, DQ49, DQ50, DQ51 | 24 |
| 75 | Connector to SDRAM Bit Mapping | DQ52, DQ53, DQ54, DQ55 | 04 |
| 76 | Connector to SDRAM Bit Mapping | DQ56, DQ57, DQ58, DQ59 | 04 |

| Byte | Function Described | Function | HEX Value |
|---------|--|----------------------------|-----------|
| 77 | Connector to SDRAM Bit Mapping | DQ60, DQ61, DQ62, DQ63 | 2E |
| 78-116 | Reserved, Base Configuration Section | - | 00 |
| 117 | Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group | 0ns | 00 |
| 118 | Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Lmin), different bank group | -0.1ns | 9C |
| 119 | Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Smin), same bank group | -0.075ns | B5 |
| 120 | Fine Offset for Minimum Activate to Activate/Refresh Delay Time(tRCmin) | 0ns | 00 |
| 121 | Fine Offset for Minimum Row Precharge Delay Time(tRPmin) | 0ns | 00 |
| 122 | Fine Offset for Minimum RAS to CAS Delay Time(tRCDmin) | 0ns | 00 |
| 123 | Fine Offset for Minimum CAS Latency Time(tAmin) | 0ns | 00 |
| 124 | Fine Offset for SDRAM Maximum Cycle Time(tCKAVGmax) | 0ns | 00 |
| 125 | Fine Offset for SDRAM Minimum Cycle Time(tCKAVGmin) | -0.042ns | D6 |
| 126 | Cyclical Redundancy Code for Base Configuration Section, LSB | CRC-CCITT(LOW) | FD |
| 127 | Cyclical Redundancy Code for Base Configuration Section, MSB | CRC-CCITT(HIGH) | 68 |
| 128 | (Unbuffered): Raw Card Extension, Module Nominal Height | Revision 0 30.00 mm | 0F |
| 129 | (Unbuffered): Module Maximum Thickness | - | 11 |
| 130 | (Unbuffered): Reference Raw Card Used | Raw Card A Revision 0 | 00 |
| 131 | (Unbuffered): Address Mapping from Edge Connector to DRAM | Standard | 00 |
| 132-253 | (Unbuffered): Reserved | - | 00 |
| 254 | (Unbuffered): CRC for Module Specific Section, Least Significant Byte | CRC-CCITT(LOW) | 45 |
| 255 | (Unbuffered): CRC for Module Specific Section, Most Significant Byte | CRC-CCITT(HIGH) | AD |
| 256-319 | Hybrid Memory Architecture Specific Parameters | | 00 |
| 320 | Module Manufacturer ID Code, LSB | ADATA | 04 |
| 321 | Module Manufacturer ID Code, MSB | | CB |
| 322 | Module ID: Module Manufacturing Location | *Note: 1 | - |
| 323 | Module ID: Module Manufacturing Date(Year) | *Note: 2 | - |
| 324 | Module ID: Module Manufacturing Date(Week) | *Note: 3 | - |
| 325-328 | Module ID : Module Serial Number | *Note: 4 | - |
| 329-348 | Module Part Number | *Note: 5 | - |
| 349 | Module Revision Code | - | 00 |
| 350 | SDRAM Manufacturer's JEDEC ID Code, LSB | | 80 |
| 351 | SDRAM Manufacturer's JEDEC ID Code, MSB | Hynix | AD |
| 352 | DRAM Stepping | | FF |
| 353-381 | Manufacturer's Specific Data | *Note: 6 | - |
| 382 | Reserved | | 00 |
| 383 | Reserved | | 00 |
| 384-511 | End User Programmable | *Note: 7 | - |

- Note : 1. Byte 322 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
2. Byte 323 -- Module manufacturing date by year (YY).
3. Byte 324 -- Module manufacturing date by week (WW).
4. Bytes 325~328 -- Module Serial Number.
5. Bytes 329~348 -- Manufacturer Part Number by module part number , (Unused digits are coded as ASCII blanks (20h)).
6. Bytes 353~381 -- These bytes are undefined and can be used for ADATA's own purpose. Digits are coded as 00h except the following:
- 6-1. Bytes 353~367 -- Manufacturer's Specific Data by working order number.
 - 6-2. Bytes 368~381 -- Manufacturer's Specific Data by SPD naming number.
7. Bytes 384~511 -- These bytes are undefined and can be used for ADATA's own purpose. Digits are coded as 00h except the following:
- 7-1. Bytes 384 -- The byte is coded as ADh.