HEF4043B

Quad R/S latch with 3-state outputs

Rev. 12 — 30 January 2020

Product

1. General description

The HEF4043B is a quad R/S latch with 3-state outputs with a common output enable input (OE). Each latch has an active HIGH set input (1S to 4S), an active HIGH reset input (1R to 4R) and an active HIGH 3-state output (1Q to 4Q).

When OE is HIGH, the latch output (nQ) is determined by the nR and nS inputs (see <u>Table 3</u>). When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. The high impedance off-state feature allows common bussing of the outputs.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- · Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- · Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

· Four-bit storage with output enable

4. Ordering information

Table 1. Ordering information

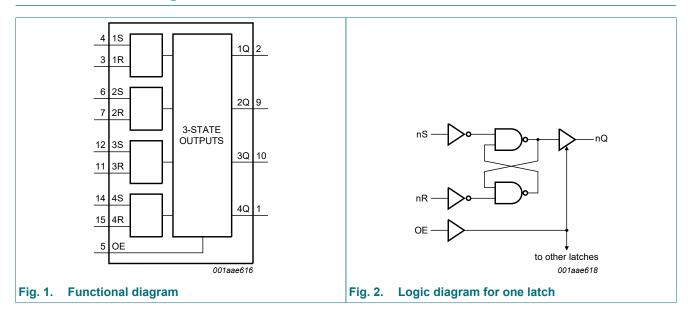
All types operate from -40 °C to +85 °C.

Type number			
	Name	Description	Version
HEF4043BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



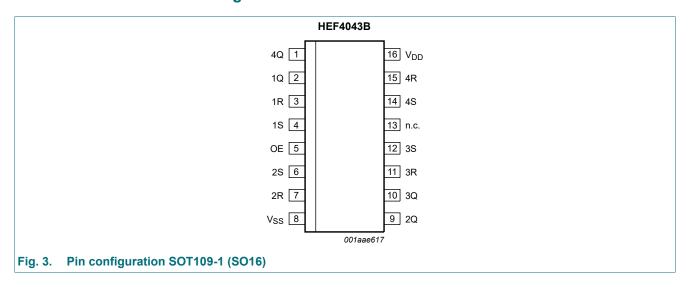
Quad R/S latch with 3-state outputs

5. Functional diagram



6. Pinning information

6.1. Pinning



Quad R/S latch with 3-state outputs

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q to 4Q	2, 9, 10, 1	3-state buffered latch output
1R to 4R	3, 7, 11, 15	reset input (active HIGH)
1S to 4S	4, 6, 12, 14	set input (active HIGH)
OE	5	common output enable input
V _{SS}	8	ground supply voltage
n.c.	13	not connected
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance state.

Inputs	nputs							
OE	nS	nR	nQ					
L	X	X	Z					
Н	L	Н	L					
Н	Н	X	Н					
Н	L	L	latched					

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V_{O} < -0.5 V or V_{O} > V_{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} -40 °C to +85 °C			
		SO16 package	-	500	mW
Р	power dissipation	per output	-	100	mW

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9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 \ V$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} =	-40 °C	T _{amb} =	25 °C	T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μΑ	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	10 V 9.95 - 9.95 - 9.95 - 15 V 14.95 - 14.95 - 14.95 - 5 V - 0.05 - 0.05 - 0.05 15 V - 0.05 - 0.05 - 0.05 15 V - 1.7 - 1.4 - 1.1 5 V0.520.440.36 10 V1.31.10.9 15 V3.63.02.4 5 V 0.52 - 0.44 - 0.36 - 10 V 1.3 - 1.1 - 0.9 - 15 V 3.6 - 3.0 - 2.4 - 15 V 3.6 - 3.0 - 2.4 - 15 V - ±0.3 - ±0.3 - ±1.0 IGH; VDD	mA						
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μΑ
l _{OZ}	OFF-state output current	nQ output HIGH; returned to V _{DD}	15 V	-	1.6	-	1.6	-	12.0	μΑ
		nQ output LOW; returned to V _{SS}	15 V	-	1.6	-	1.6	-	12.0	μΑ
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
Cı	input capacitance			-	-	-	7.5	-	-	pF

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11. Dynamic characteristics

Table 7. Dynamic characteristics

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ °C}$; For waveforms and test circuit see Section 11.1; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	$nR \rightarrow nQ$;	5 V [1]	63 ns + (0.55 ns/pF)C _L	-	90	180	ns
	propagation delay	see Fig. 4	10 V	24 ns + (0.23 ns/pF)C _L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF)C _L	-	25	50	ns
t _{PLH}	LOW to HIGH	$nS \rightarrow nQ$;	5 V [1]	38 ns + (0.55 ns/pF)C _L	-	65	135	ns
	propagation delay	see Fig. 4	10 V	14 ns + (0.23 ns/pF)C _L	-	25	50	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	35	ns
t _t	transition time	nQ output;	5 V [1] [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
		see Fig. 4	10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{PHZ}	HIGH to OFF-state	$OE \rightarrow nQ;$	5 V		-	45	90	ns
	propagation delay	see Fig. 5	10 V		-	20	35	ns
			15 V		-	10	25	ns
t _{PLZ}	LOW to OFF-state	$OE \rightarrow nQ;$	5 V		-	50	100	ns
	propagation delay	see Fig. 5	10 V		-	20	40	ns
			15 V		-	10	25	ns
t _{PZH}	OFF-state to HIGH	$OE \rightarrow nQ;$	5 V		-	25	50	ns
	propagation delay	see Fig. 5	10 V		-	15	30	ns
			15 V		-	10	25	ns
t _{PZL}	OFF-state to LOW	$OE \rightarrow nQ;$	5 V		-	40	80	ns
	propagation delay	see Fig. 5	10 V		-	20	45	ns
			15 V		-	15	35	ns
t _W	pulse width	nS input HIGH;	5 V		30	15	-	ns
		minimum width;	10 V		20	10	-	ns
		see Fig. 4	15 V		16	8	-	ns
		nR input HIGH;	5 V		30	15	-	ns
		minimum width;	10 V		20	10	-	ns
		see Fig. 4	15 V		16	8	-	ns

^[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_{D}

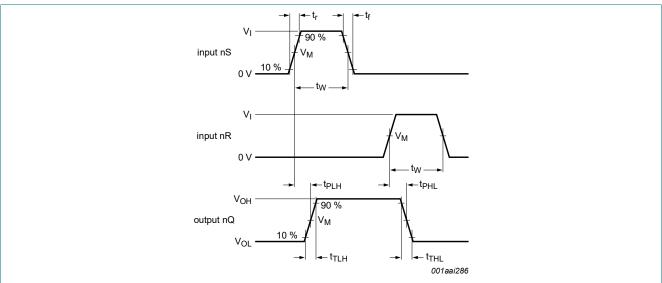
 P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	where:
P_D	dynamic power	5 V	0 1 (0 1) 00	f _i = input frequency in MHz;
dissipation		10 V		f _o = output frequency in MHz; C _L = output load capacitance in pF;
		15 V	D 44400 (. E/(O))/ /	V_{DD} = supply voltage in V; $\Sigma(f_0 \times G_L)$ = sum of the outputs.

^[2] t_t is the same as t_{THL} and t_{TLH} .

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11.1. Waveforms



 t_r and t_f are the input rise and fall times.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Transition times: transition time (t_t) = HIGH LOW (t_{THL}) or LOW HIGH (t_{TLH}) transition times.

Measurement points are given in Table 9 and test data is given in Table 10.

Fig. 4. Input minimum set (nS) and reset (nR) pulse widths, inputs nS or nR to latch output (nQ) propagation delay and nQ transition time

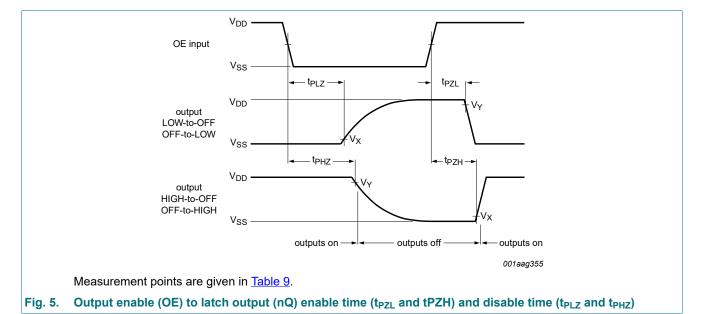
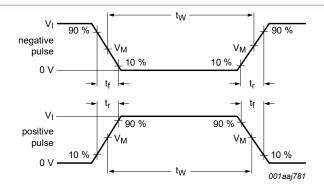


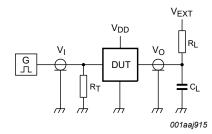
Table 9. Measurement points

Supply voltage	Input		Output		
V_{DD}	V _I V _M		V _M	V _X	V _Y
5 V to 15 V	V _{DD} or 0 V	0.5V _{DD}	0.5V _{DD}	0.1V _{DD}	0.9V _{DD}

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a. Input waveform



b. Test circuit

Test and measurement data is given in <u>Table 10</u>.

Definitions test circuit:

DUT = Device Under Test.

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

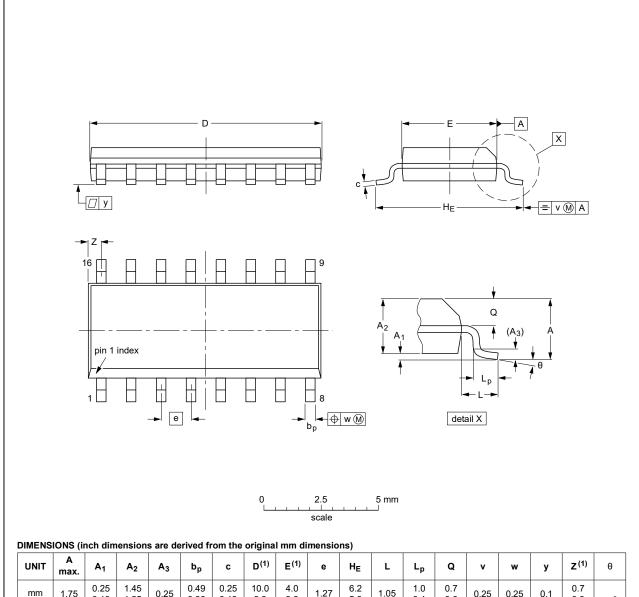
Supply voltage	Input				V _{EXT}			
V_{DD}	$V_l \qquad t_r, t_f$		CL	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}	
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 kΩ	open	V_{DD}	GND	

Quad R/S latch with 3-state outputs

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UN	IT ma		A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mr	n 1.1	75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inch	es 0.0	069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 7. Package outline SOT109-1 (SO16)

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13. Revision history

Table 11. Revision history

Parament ID Parame						
Document ID	Release date	Data sheet status	Change notice	Supersedes		
HEF4043B v.12	20200130	Product data sheet	-	HEF4043B v.11		
Modifications:	Nexperia. • Legal texts h					
HEF4043B v.11	20160324	Product data sheet	-	HEF4043B v.10		
Modifications:	Type numbe	Type number HEF4043BP (SOT38-4) removed.				
HEF4043B v.10	20111118	Product data sheet	-	HEF4043B v.9		
Modifications:	• <u>Table 6</u> : I _{OH}	<u>Table 6</u> : I _{OH} minimum values changed to maximum				
HEF4043B v.9	20091216	Product data sheet	-	HEF4043B v.8		
HEF4043B v.8	20091127	Product data sheet	-	HEF4043B v.7		
HEF4043B v.7	20090710	Product data sheet	-	HEF4043B v.6		
HEF4043B v.6	20081111	Product data sheet	-	HEF4043B v.5		
HEF4043B v.5	20080729	Product data sheet	-	HEF4043B v.4		
HEF4043B v.4	20080710	Product data sheet	-	HEF4043B_CNV v.3		
HEF4043B_CNV v.3	19950101	Product specification	-	HEF4043B_CNV v.2		
HEF4043B_CNV v.2	19950101	Product specification	-	-		

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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