User's Guide

SLVU330–September 2009

TPS54318EVM-512 3-A, SWIFT™ Regulator Evaluation Module

Contents

List of Figures

List of Tables

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1 Introduction

This user's guide contains background information for the TPS54318 as well as support documentation for the TPS54318EVM-512 evaluation module (HPA375). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54318EVM-512.

1.1 Background

The TPS54318 dc/dc converter is designed to provide up to a 3 A output from an input voltage source of 2.95 V to 6 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54318 regulator. The switching frequency is externally set at a nominal 1000 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54318 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allow the TPS54318 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54318 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 7 V for the TPS54318EVM-512.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54318EVM-512	VIN = 3 V to 6 V (VIN start = 3.1 V)	0 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS54318EVM-512 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 3.3 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54318EVM-512 is designed and tested for V_{IN} = 3 V to 6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54318EVM-512 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} operating voltage range			3	3.3	6	V
V_{IN} start voltage				3.1		V
V_{IN} stop voltage				2.8		V
Output voltage set point				1.8		V
Output current range	V_{IN} = 3 V to 6 V		0		3	A
Line regulation	I_O = 2 A, V_{IN} = 3 V to 6 V			±0.04%		
Load regulation	V_{IN} = 3.3 V, I_O = 0 A to 3 A			±0.06%		
Load transient response	I_O = 0.75 A to 2.25 A	Voltage change		–40		mV
		Recovery time		400		µs
	I_O = 2.25 A to 0.75 A	Voltage change		40		mV
		Recovery time		400		µs
Loop bandwidth	V_{IN} = 3.3 V, I_O = 3 A			35		kHz
Phase margin	V_{IN} = 3.3 V , I_O = 3 A			74		°
Input ripple voltage	I_O = 3 A			100		mV_{PP}
Output ripple voltage	I_O = 3 A			5		mV_{PP}
Output rise time				4		ms
Operating frequency				1000		kHz
Maximum efficiency	TPS54318EVM-512, V_{IN} = 3.3 V, I_O = 0.6 A			94%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54318. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The voltage divider R6 and R7 is used to set the output voltage. To change the output voltage of the EVM, it is necessary to change the value of resistor R7. Changing the value of R7 can change the output voltage above 0.8 V. The value of R7 for a specific output voltage can be calculated using Equation 1.

$$R7 = 100\ k\Omega \times \frac{0.8\ V}{V_{OUT} - 0.8\ V} \quad (1)$$

Table 3 lists the R7 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 80 ns, and the maximum duty cycle is less than 92%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R7 Value (kΩ)
1.0	402
1.2	200
1.5	115
1.8	80.6
2.5	47.5

1.3.2 Slow Start Time

The slow start time can be adjusted by changing the value of C7. Use Equation 2 to calculate the required value of C7 for a desired slow start time

$$C7(nF) = \frac{Tss(mS) \times Iss(\mu A)}{Vref(V)} \quad (2)$$

C7 is set to 0.01 µF on the EVM for a default slowstart time of 4 msec.

1.3.3 Adjustable UVLO

The undervoltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 3.1 V and a stop voltage of 2.8 V using R1 = 48.8 kΩ and R2 = 32.4 kΩ. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{0.944 \cdot V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad (3)$$

$$R2 = \frac{1.18 \cdot R1}{V_{STOP} - 1.18 + R1 \cdot 3.2 \times 10^{-6}} \quad (4)$$

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54318EVM-512 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54318EVM-512 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be at least 3 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP7 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range).
J2	2-pin header for enable. Connect EN to ground to disable, open to enable.
J3	2-pin header for to allow pull up of PWRGD to V_{IN}.
J4	V_{OUT}, 1.8 V at 4 A maximum.
TP1	V_{IN} test point at V_{IN} connector.
TP2	GND test point at V_{IN}.
TP3	PH test point
TP4	Slow start monitor test point.
TP5	Test point between voltage divider network and output. Used for loop response measurements.
TP6	Output voltage test point at OUT connector.
TP7	GND test point at OUT connector.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54318EVM-512 at an ambient temperature of 25°C.

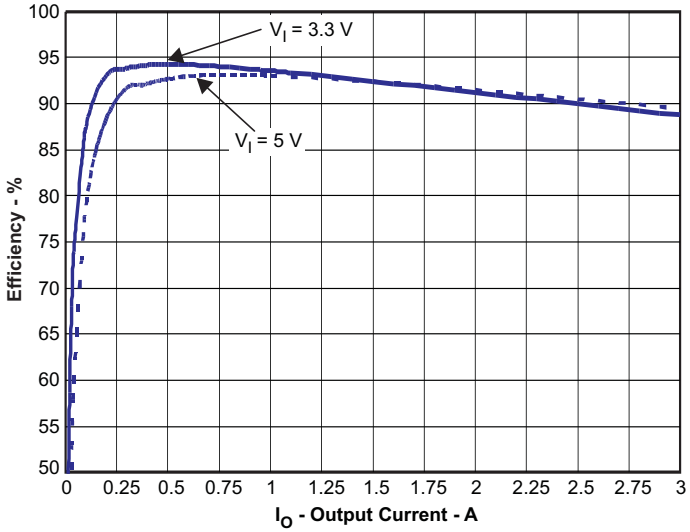

Figure 1. TPS54318EVM-512 Efficiency

Figure 2 shows the efficiency for the TPS54318EVM-512 at lower output currents between using a semi log scale at an ambient temperature of 25°C.

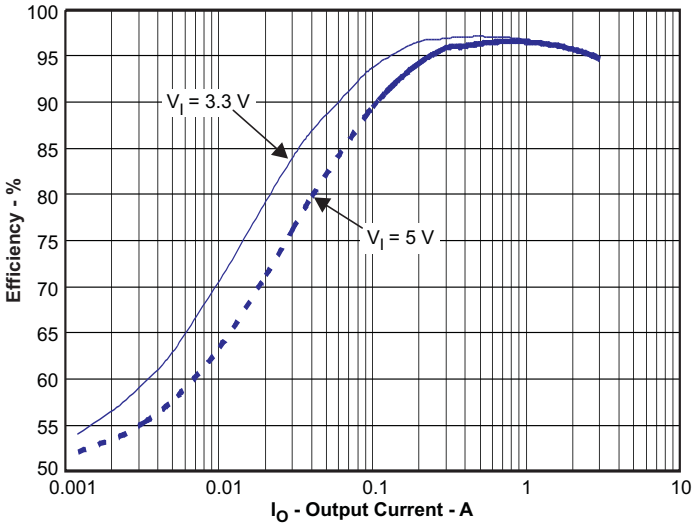

Figure 2. TPS54318EVM-512 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 3 shows the load regulation for the TPS54318EVM-512.

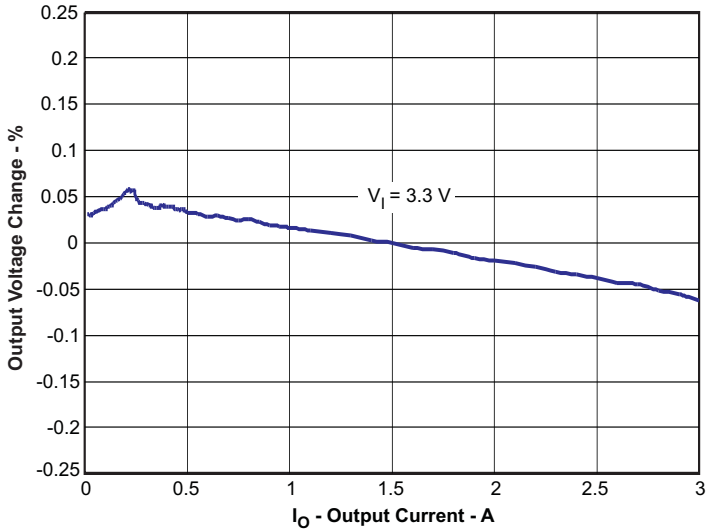

Figure 3. TPS54318EVM-512 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 4 shows the line regulation for the TPS54318EVM-512.

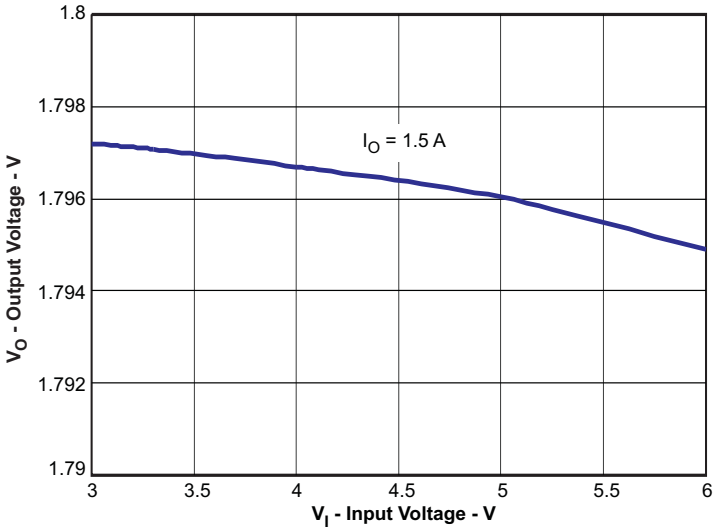

Figure 4. TPS54318EVM-512 Line Regulation

2.5 Load Transients

Figure 5 shows the TPS54318EVM-375 response to load transients. The current step is from 25% to 75% of maximum rated load at 3.3 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

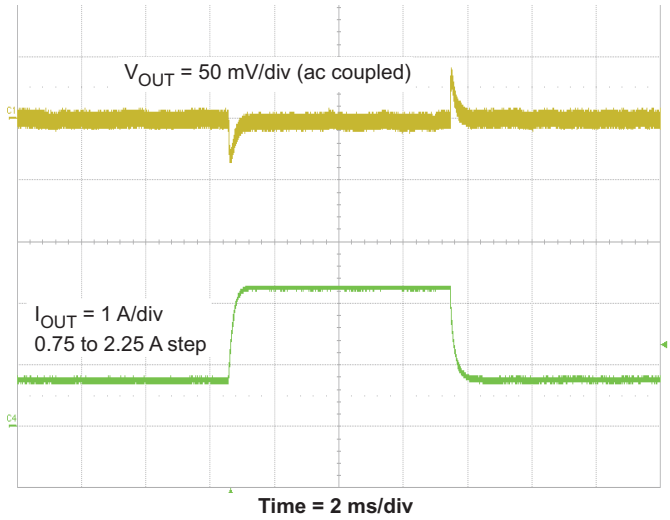

Figure 5. TPS54318EVM-512 Transient Response

2.6 Loop Characteristics

Figure 6 shows the TPS54318EVM-512 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 3.3 V. Load current for the measurement is 4 A.

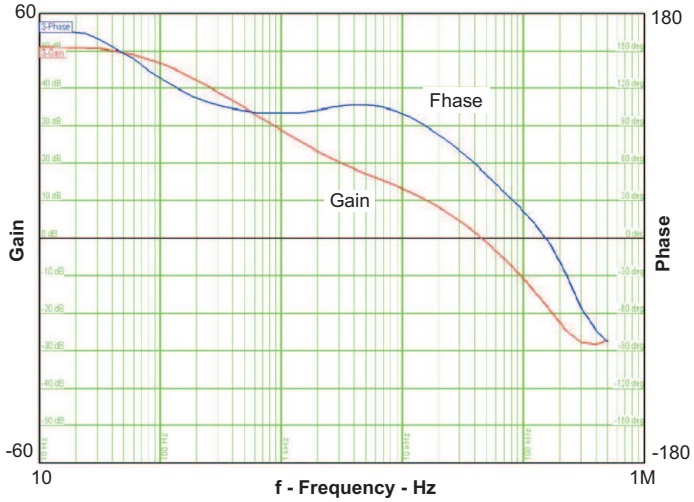

Figure 6. TPS54318EVM-512 Loop Response

2.7 Output Voltage Ripple

Figure 7 shows the TPS54318EVM-512 output voltage ripple. The output current is the rated full load of 3 A and V_{IN} = 3.3 V. The ripple voltage is measured directly across the output capacitors.

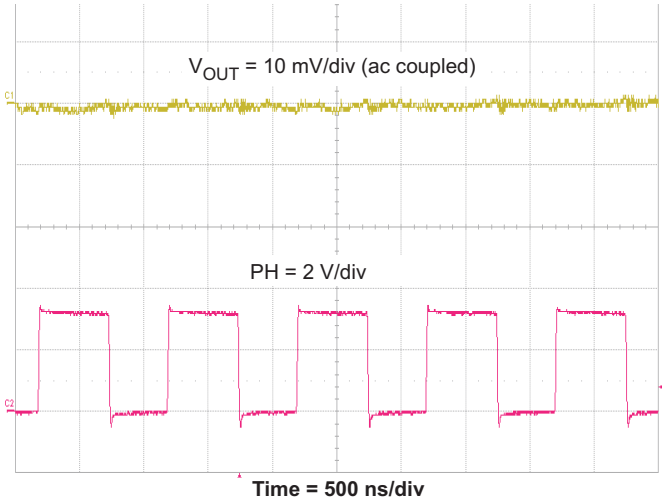

Figure 7. TPS54318EVM-512 Output Ripple

2.8 Input Voltage Ripple

Figure 8 shows the TPS54318EVM-512 input voltage ripple. The output current is the rated full load of 3 A and V_{IN} = 3.3 V. The ripple voltage is measured directly across the input capacitors.

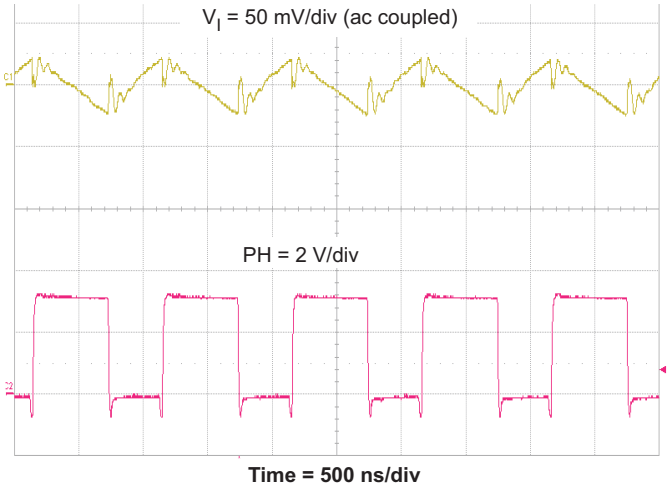

Figure 8. TPS54318EVM-512 Input Ripple

2.9 Powering Up

Figure 9 and Figure 10 show the start-up waveforms for the TPS54318EVM-512. In Figure 9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R_1 and R_2 resistor divider network. In Figure 10, the input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.8 V. The input voltage for these plots is 5 V and the load is 1 Ω.

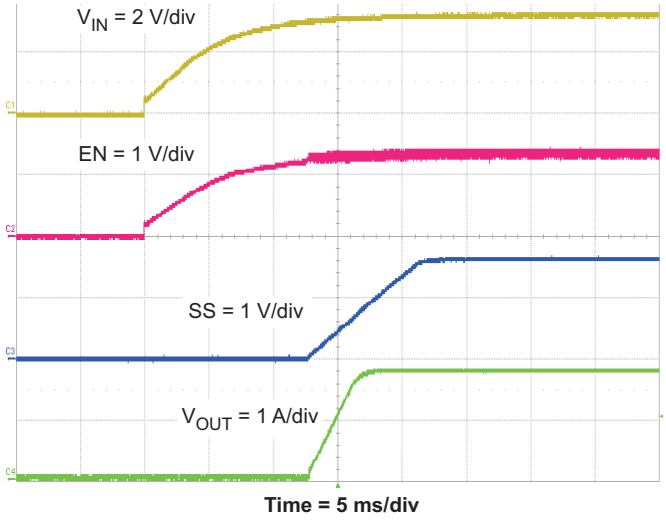

Figure 9. TPS54318EVM-512 Start-Up Relative to V_{IN}

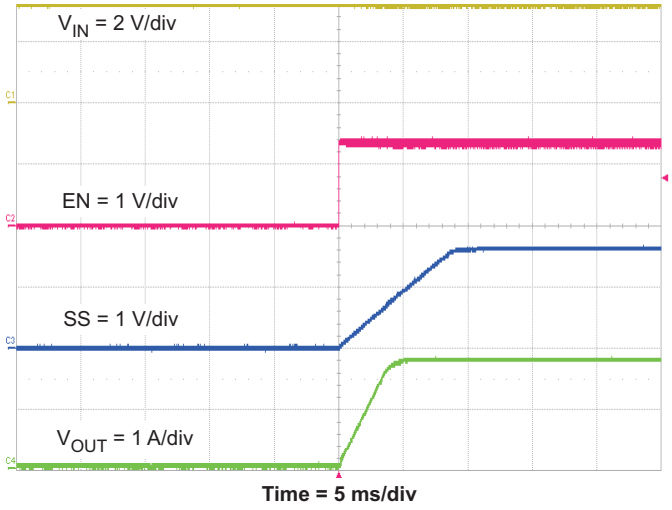

Figure 10. TPS54318EVM-512 Start-up Relative to Enable

3 Board Layout

This section provides a description of the TPS54318EVM-512, board layout, and layer illustrations.

3.1 Layout

Figure 11 through Figure 15 shows the board layout for the TPS54318EVM-512. The topside layer of the EVM is laid out in a manner typical of a user application. The top, bottom and internal layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54318 and a large area filled with ground. The bottom and internal layers contain ground planes only. The top-side ground areas are connected to the bottom and internal ground planes with multiple vias placed around the board including four vias directly under the TPS54318 device to provide a thermal path from the top-side ground area to the bottom-side and internal ground planes.

The input decoupling capacitors (C2, and C3) and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace near the output connector J4. For the TPS54318, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

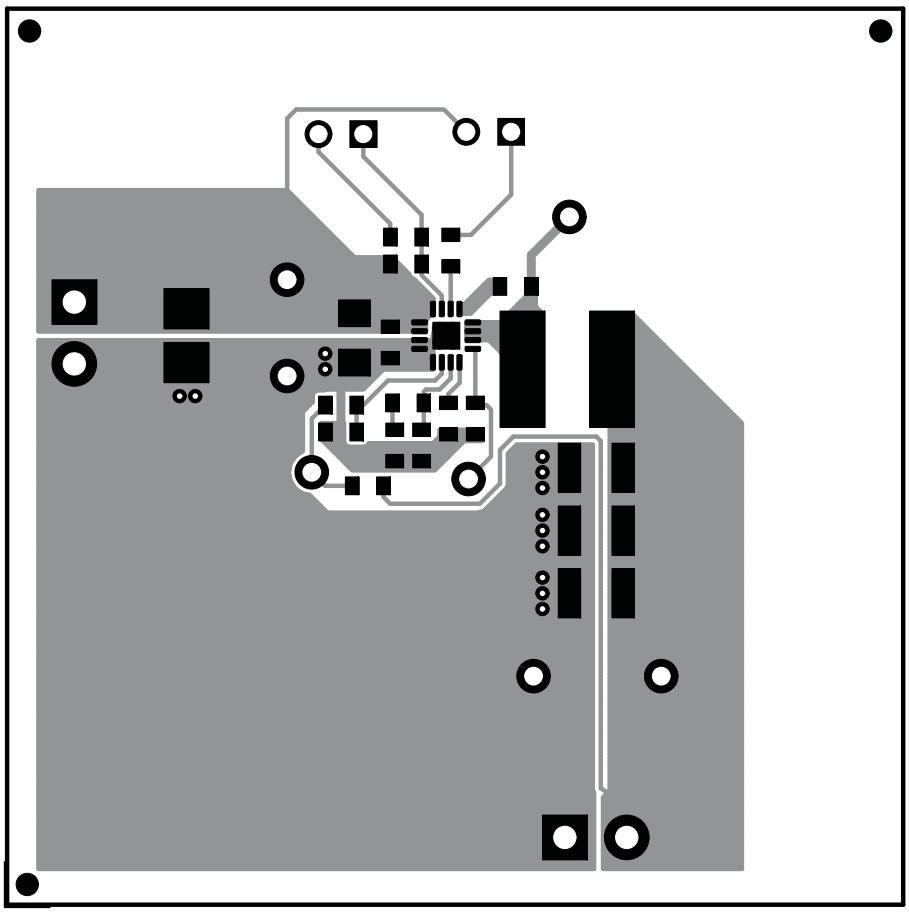

Figure 11. TPS54318EVM-512 Top-Side Layout

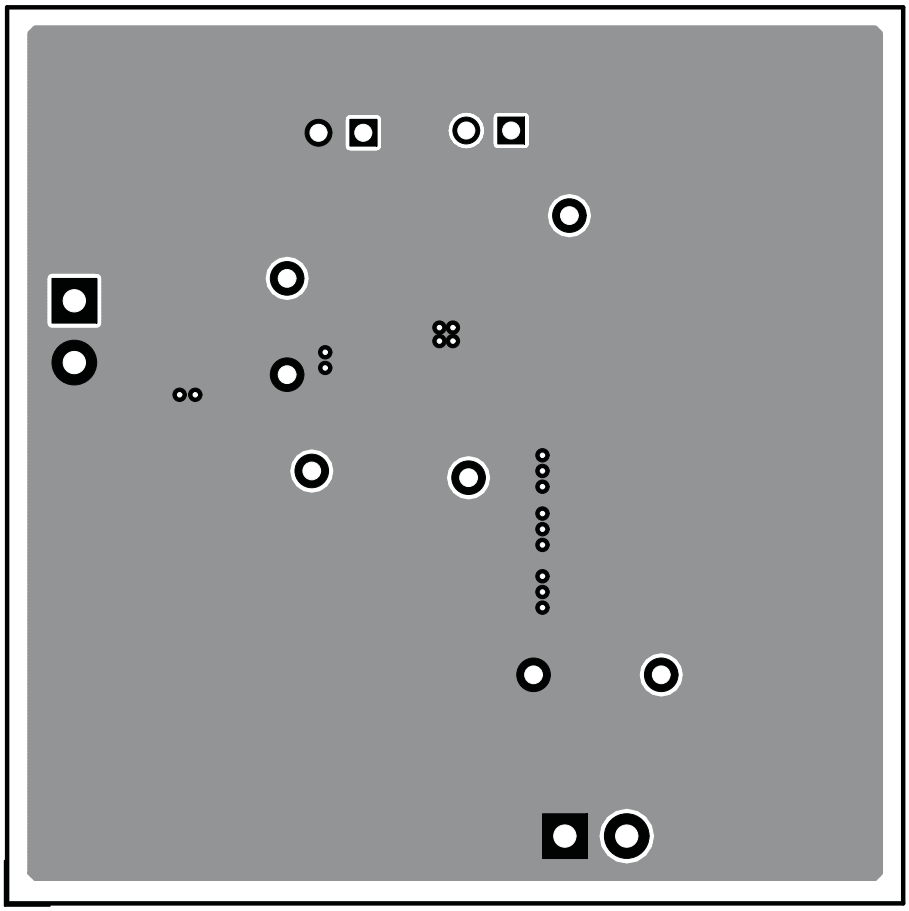

Figure 12. TPS54318EVM-512 Bottom-Side Layout

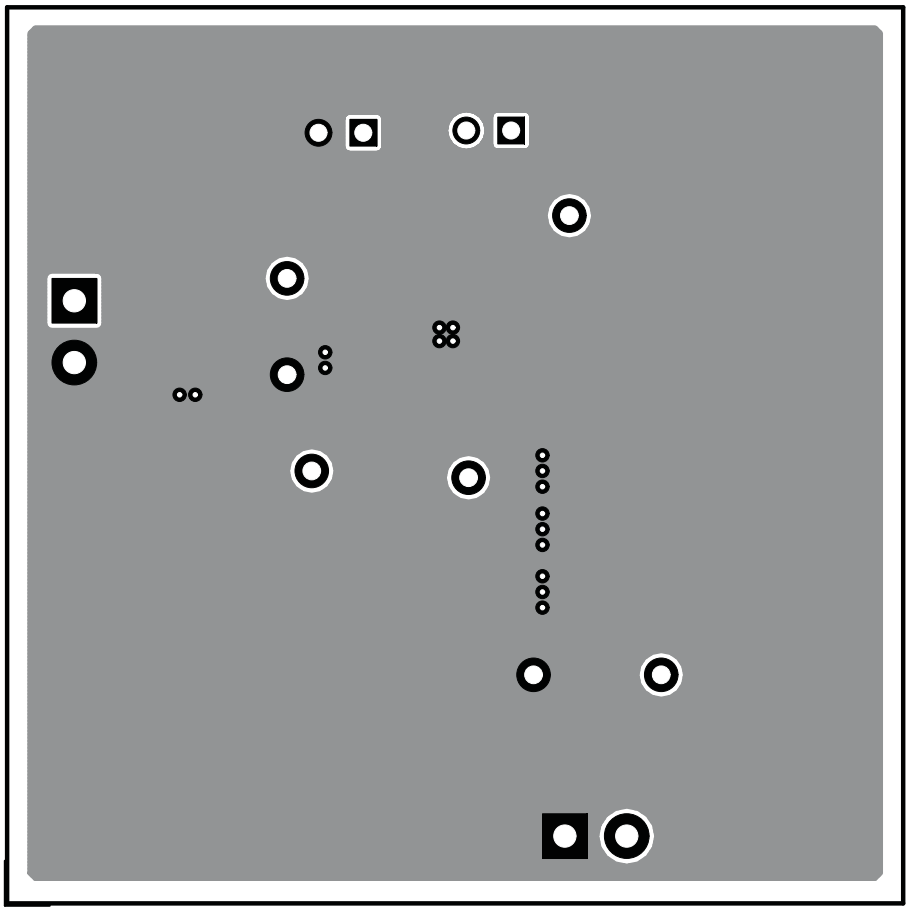

Figure 13. TPS54318EVM-512 Layout 2

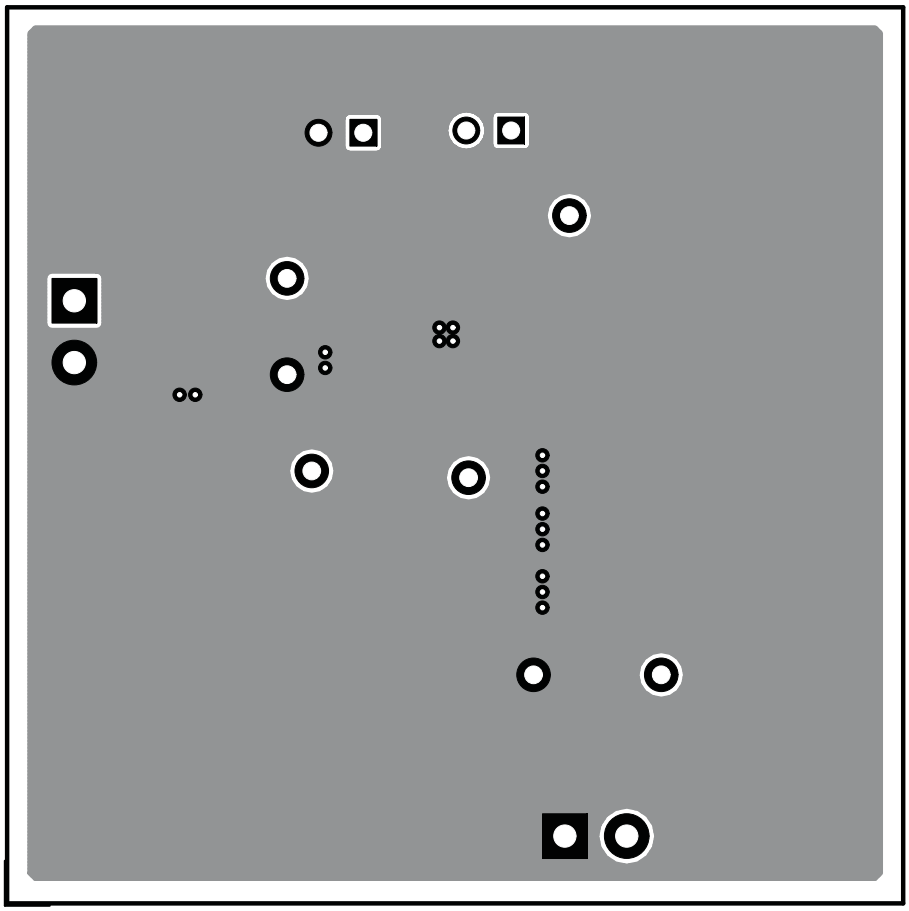

Figure 14. TPS54318EVM-512 Layout 3

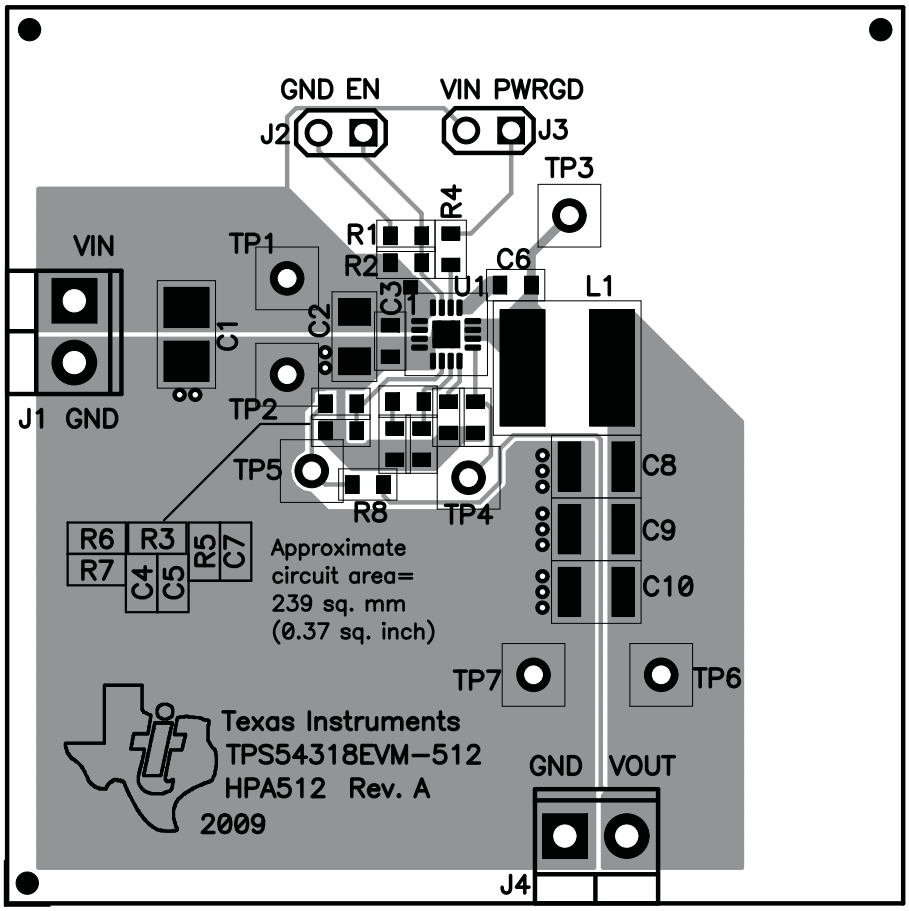

Figure 15. TPS54318EVM-512 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.37 in^2 (239 mm^2). This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54318EVM-512 schematic and bill of materials.

4.1 Schematic

Figure 16 is the schematic for the TPS54318EVM-512.

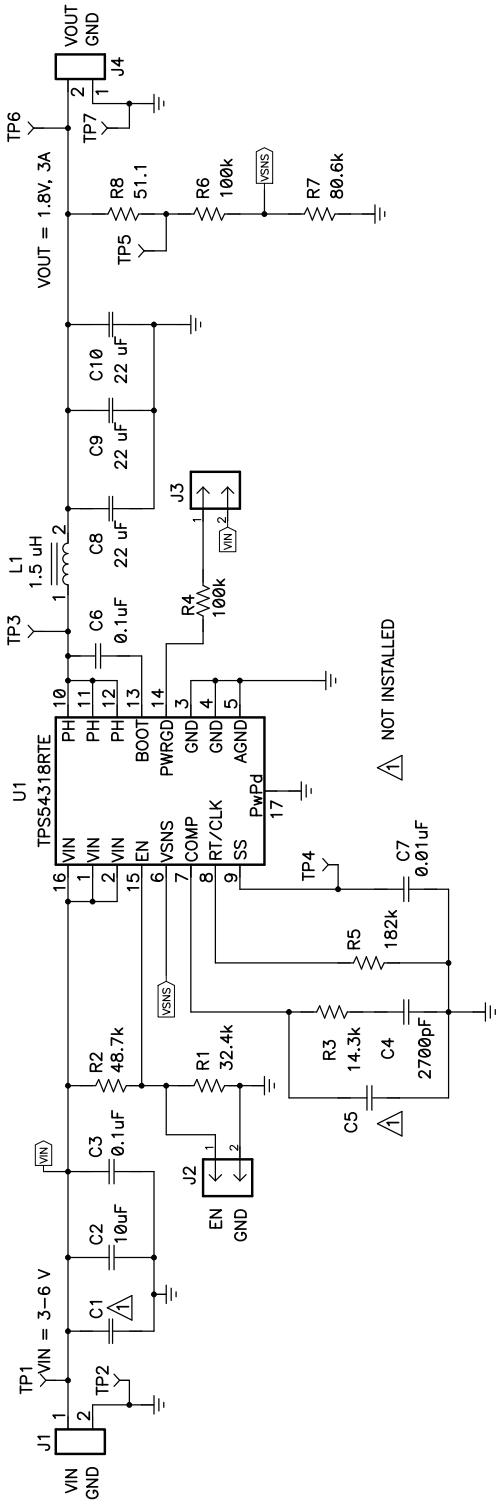

Figure 16. TPS54318EVM-512 Schematic

4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54318EVM-512.

Table 5. TPS54318EVM-512 Bill of Materials

COUNT	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, Ceramic	Multi sizes	Engineering Only	Std
1	C2	10uF	Capacitor, Ceramic, 10V, X5R, 20%	1206	Std	Std
2	C3, C6	0.1uF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
1	C4	2700pF	Capacitor, Ceramic, 50V, X5R, 10%	0603	Std	Std
0	C5	Open	Capacitor, Ceramic	0603	Std	Std
1	C7	0.01uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
3	C8, C9, C10	22 uF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std
2	J1, J4	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
2	J2, J3	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	1.5 uH	INDUCTOR, Power, TYP DCR 12.1mohms, Irms 9.2A	0.276 x 0.276 inch	XPL7030-152ML	Coilcraft
1	R1	32.4k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	48.7k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	14.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R4, R6	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	182k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	80.6k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
5	TP1, TP3 - TP6	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
2	TP2, TP7	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54318RTE	IC, DC-DC Converter, 3-6 V, 3A	QFN-16	TPS54318RTE	TI
2	--		Shunt, 100-mil, Black	0.100	929950-00	
1	--		PCB, 2.0" x 2.0" x 0.062"		HPA511	

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent 's components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output current range specified in Table 1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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