

NBSG16MMNEVB

NBSG16M Evaluation Board User's Manual



ON Semiconductor®

<http://onsemi.com>

EVAl BOARD USER'S MANUAL

Description

This document describes the NBSG16M evaluation board and the appropriate lab test setups. It should be used in conjunction with the NBSG16M data sheets which contain full technical details on the device specifications and operation. The same PCB is used to evaluate the NBSG16MN and NB4L16M devices.

The evaluation board is designed to facilitate a quick evaluation of the NBSG16M GigaComm™ Differential Receiver/Driver/Translator. The NBSG16M is designed to function as a high speed receiver/driver/translator device with CML output for use in high speed signal amplification and backplane interface applications.

The board is implemented in two layers and provides a high bandwidth 50 Ω controlled impedance environment for higher performance. The first layer or primary trace layer is 5 mils thick Rogers RO6002 material, which is engineered to have equal electrical length on all signal traces from the NBSG16M device to the sense output. The second layer is 32 mils thick copper ground plane.

What measurements can you expect to make?

With this evaluation board, the following measurements could be performed in differential modes of operation:

- Jitter
- Output Skew
- Gain/Return Loss
- Eye Pattern Generation
- Frequency Performance
- Output Rise and Fall Time
- V_{CMR} (Input High Common Mode Range)

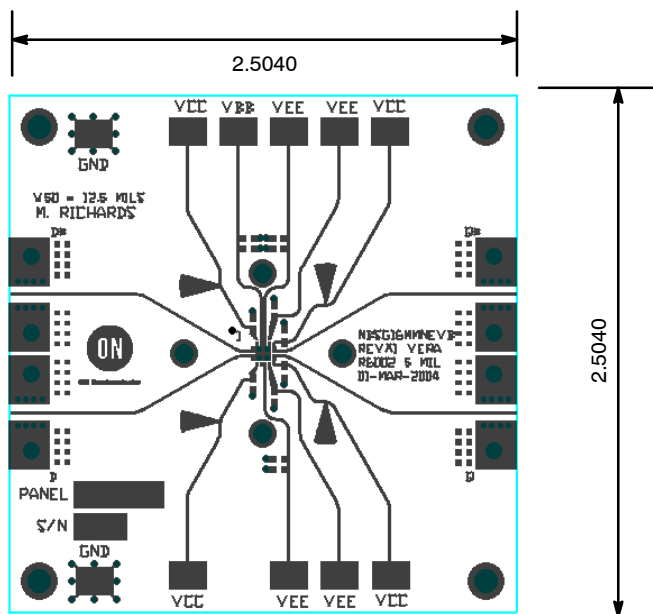


Figure 1. NBSG16MMN Evaluation PCB with Pin Label/Connection Change

NBSG16MMNEVB

SETUP FOR TIME DOMAIN MEASUREMENTS

Table 1. BASIC EQUIPMENT

Description	Example Equipment (Note 1)	Qty.
Power Supply with 4 Outputs	HP6624A	1
Oscilloscope	TDS8000 with 80E01 Sampling Head (Note 2)	1
Differential Signal Generator	HP 8133A, Advantest D3186	1
Matched High Speed Cables with SMA Connectors	Storm, Semflex	4
Power Supply Cables with Clips		8

1. Equipment used to generate example measurements within this document.
2. 50 GHz sampling head used (for effective rise, fall and jitter performance measurement)

Setup

Step 1: Connect Power

1a: Two power levels must be provided to the board for V_{CC} and V_{EE} via the surface mount clips.

Step 2: Connect Inputs

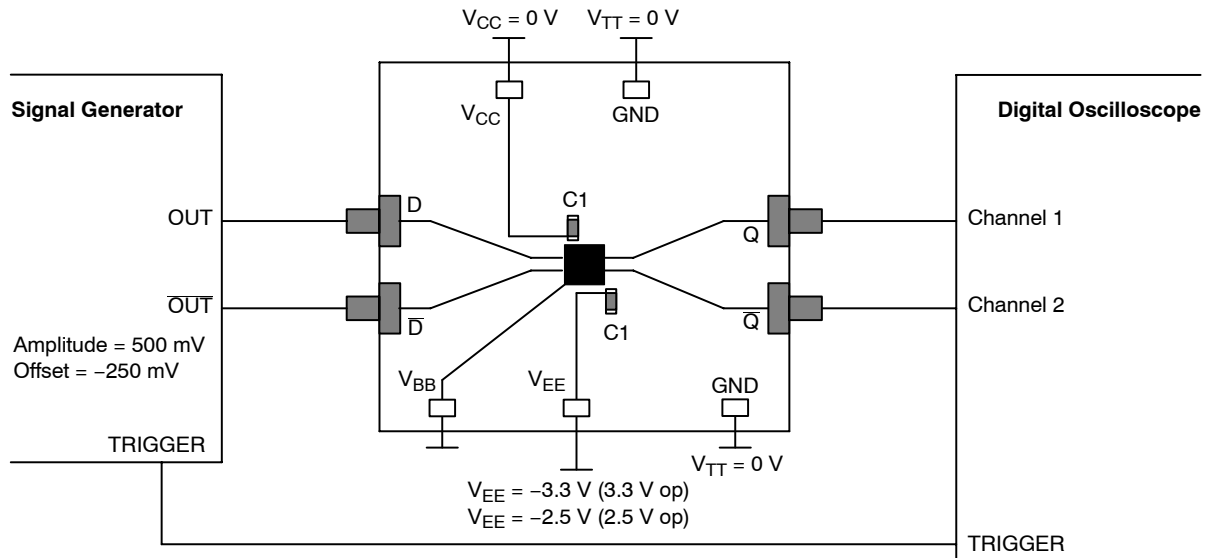
For Differential Mode (3.3 V and 2.5 V operation)

2a: Connect the differential output of the generator to the differential input of the device (D and \bar{D}).

NOTE: Device may oscillate when the input is not driven.

Table 2. NBSG16M POWER SUPPLY CONNECTIONS

3.3 V Setup	2.5 V Setup
$V_{CC} = 0 \text{ V} = \text{GND}$	$V_{CC} = 0 \text{ V} = \text{GND}$
$V_{TT} = V_{CC} = 0 \text{ V} = \text{GND}$	$V_{TT} = V_{CC} = 0 \text{ V} = \text{GND}$
$V_{EE} = -3.3 \text{ V}$	$V_{EE} = -2.5 \text{ V}$



NOTE: All differential cable pairs **must be** matched.

Figure 2. NBSG16M Board Setup – Time Domain (Differential Mode)

NBSG16MMNEVB

Setup (Continued)

Step 3: Setup Input Signals

3a: Set the signal generator amplitude to 500 mV

NOTE: The signal generator amplitude can vary from 75 mV to 900 mV to produce a 400 mV DUT output.

3b: Set the signal generator offset to -250 mV

NOTE: The V_{IHCMR} (Input High Voltage Common Mode Range) allows the signal generator offset to vary as long as V_{IH} is within the V_{IHCMR} range. Refer to the device data sheet for further information.

3c: Set the generator output for a PRBS data signal, or for a square wave clock signal with a 50% duty cycle.

Step 4: Connect Output Signals

4a: Connect the outputs of the device (Q , \bar{Q}) to the oscilloscope. The oscilloscope sampling head must have internal 50 Ω termination to ground.

NOTE: Where a single output is being used, the unconnected output for the pair **must be** terminated to V_{TT} through a 50 Ω resistor for best operation. Unused pairs may be left unconnected. Since $V_{TT} = 0$ V, a standard 50 Ω SMA termination is recommended.

SETUP FOR FREQUENCY DOMAIN MEASUREMENTS

Table 3. BASIC EQUIPMENT

Description	Example Equipment (Note 1)	Qty.
Power Supply with 4 Outputs	HP 6624A	1
Vector Network Analyzer (VNA)	R&S ZVK (10 MHz to 40 GHz)	1
180° Hybrid Coupler	Krytar Model #4010180	1
Bias Tee with 50 Ω Resistor Termination	Picosecond Model #5542-219	1
Matched High Speed Cables with SMA Connectors	Storm, Semflex	3
Power Supply Cables with Clips		8

1. Equipment used to generate example measurements within this document.

Setup

Step 1: Connect Power

1a: Two power levels must be provided to the board for V_{CC} and V_{EE} via the surface mount clips.

Table 4. NBSG16M POWER SUPPLY CONNECTIONS

3.3 V Setup
$V_{CC} = 0$ V = GND
$V_{TT} = V_{CC} =$ GND
$V_{EE} = -3.3$ V

Setup Test Configurations for Differential Operation

A) Small Signal Setup

Step 2: Input Setup

2a: Calibrate VNA from 1.0 GHz to 12 GHz.

2b: Set input level to -35 dBm at the output of the 180° Hybrid coupler (input of the DUT).

Step 3: Output Setup

3a: Set display to measure S21 and record data.

B) Large Signal Setup

Step 2: Input Setup

2a: Calibrate VNA from 1.0 GHz to 12 GHz.

2b: Set input levels to -2.0 dBm (500 mV) at the input of DUT.

Step 3: Output Setup

3a: Set display to measure S21 and record data.

NBSG16MMNEVB

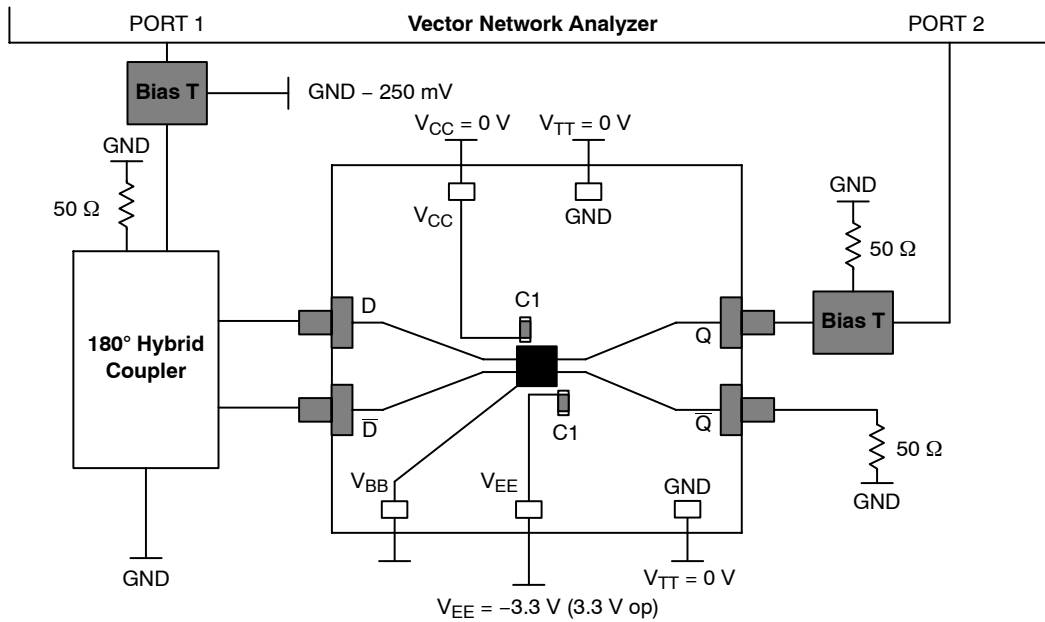


Figure 3. NBSG16M Board Setup – Frequency Domain (Differential Mode)

MORE INFORMATION ABOUT EVALUATION BOARD

Design Considerations for >10 GHz operation

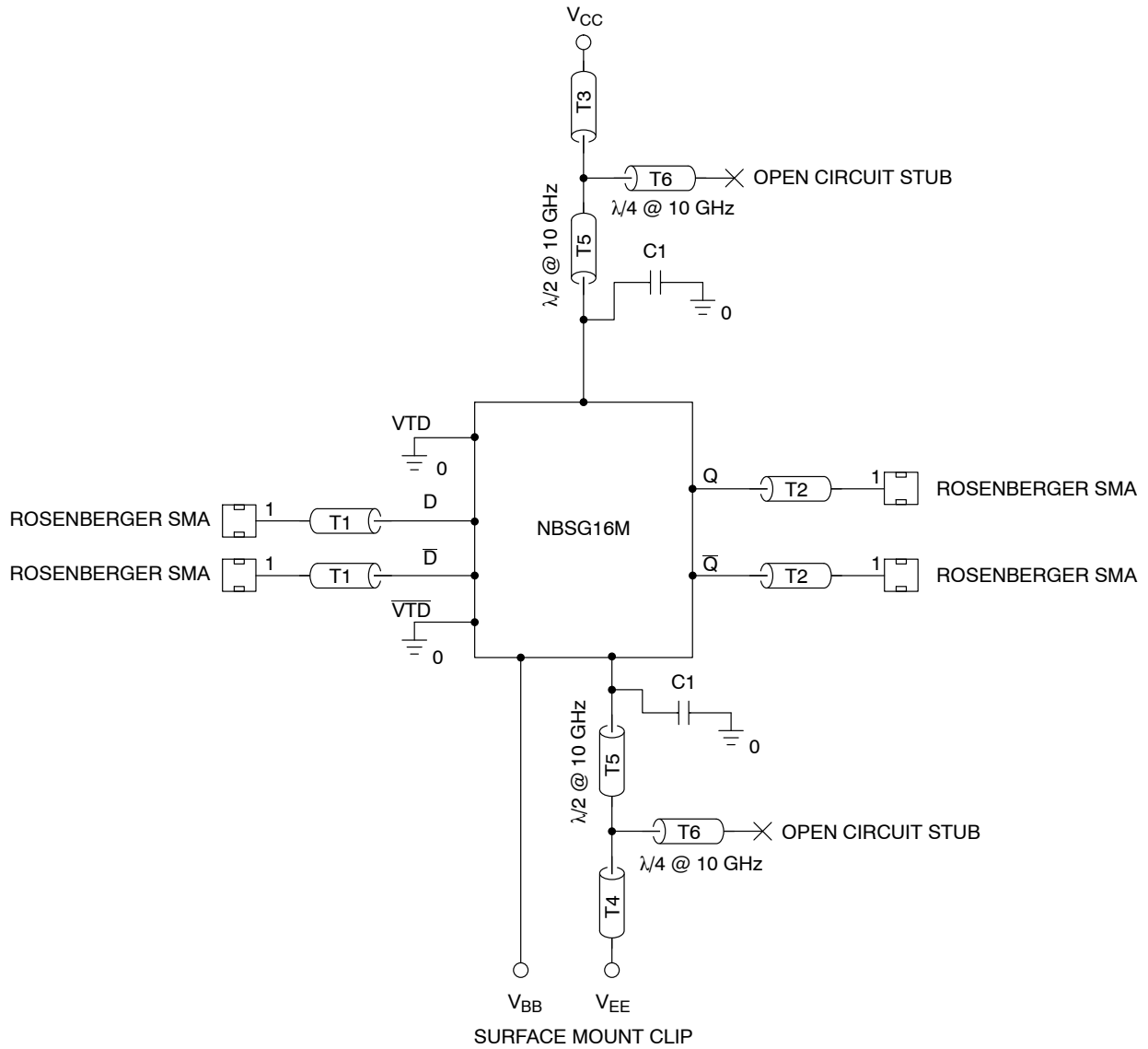
While the NBSG16M is specified to operate at 12 GHz, this evaluation board is designed to support operating frequencies up to 20 GHz.

The following considerations played a key role to ensure this evaluation board achieves high-end microwave performance:

- Optimal SMA Connector Launch
- Minimal Insertion Loss and Signal Dispersion
- Accurate Transmission Line Matching (50 Ω)
- Distributed Effects while Bypassing and Noise Filtering

NBSG16MMNEVB

SURFACE MOUNT CLIP



NOTE: C1, C2* = Decoupling cap
Tx = 50 Ω Transmission line

Figure 4. Evaluation Board Schematic

NBSG16MMNEVB

Table 5. PARTS LIST

Part No	Qty.	Description	Manufacturer	Web Address
NBSG16MMN	1	2.5 V/3.3 V SiGe Differential Receiver/Driver with CML Outputs	ON Semiconductor	http://www.onsemi.com/NBSG16M
32K243-40ME3	4	Gold Plated Connector	Rosenberger	http://www.rosenberger.de
CO6BLBB2X5CO6 03CL04K6RAC	9	2 MHz – 30 GHz Capacitor 0603 0.1 μ F \pm 10%	Dielectric Laboratories Kemet	http://www.dilabs.com http://www.newark.com
SO16	9	Test Point-Anvil	Keystone	http://www.newark.com http://www.digikey.com

Table 6. BOARD MATERIAL

Material	Thickness
Rogers 6002	5 mil
Copper Plating	32 mil

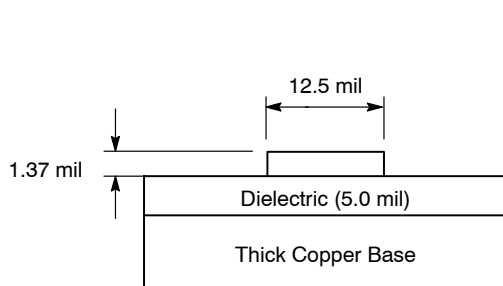


Figure 5. Board Stack-up

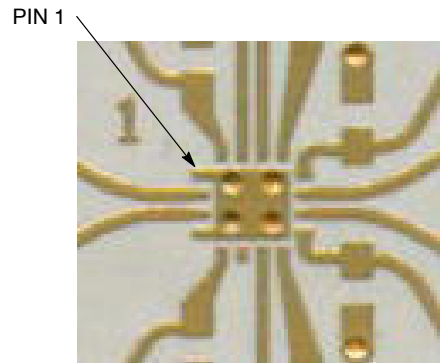
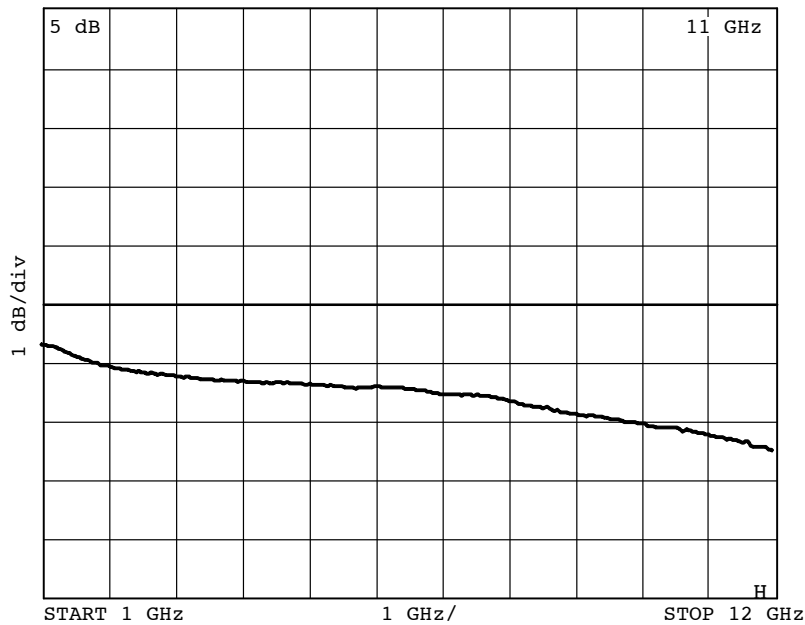


Figure 6. Layout Mask for NBSG16M



NOTE: The insertion loss curve can be used to calibrate out board loss if testing under small signal conditions.

Figure 7. Insertion Loss

NBSG16MMNEVB

ADDITIONAL EVALUATION BOARD INFORMATION

www.onsemi.com

In all cases, the most up-to-date information can be found on our website.

- Sample Orders for Devices and Boards
- New Product Updates
- Literature Download/Order
- IBIS and Spice Models

References

NBSG16M/D, Data Sheet, *NBSG16M, 2.5V/3.3V SiGe Differential Receiver/Driver with CML Outputs*

AND8077/D, Application Note, *GigaComm™ (SiGe) SPICE Modeling Kit*.

AND8075/D, Application Note, *Board Mounting Considerations for the FCBGA Packages*.

Table 7. ORDERING INFORMATION

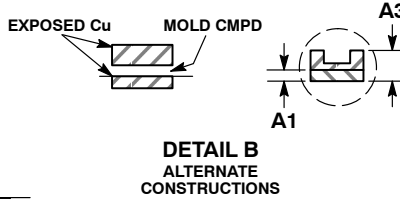
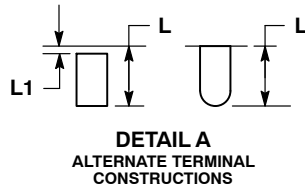
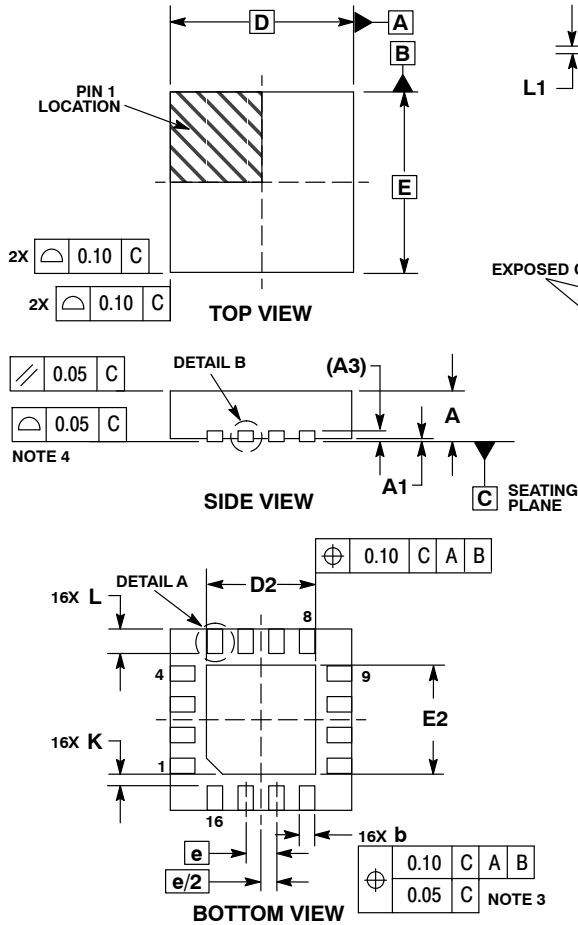
Part No	Description	Package	Shipping†
NBSG16MMN	2.5 V/3.3 V SiGe Differential Receiver/Driver with CML Outputs	3×3 mm QFN-16	123 Units/Tray
NBSG16MMNG	2.5 V/3.3 V SiGe Differential Receiver/Driver with CML Outputs	3×3 mm QFN-16 (Pb-Free)	123 Units/Tray
NBSG16MMNR2	2.5 V/3.3 V SiGe Differential Receiver/Driver with CML Outputs	3×3 mm QFN-16	3,000/Tape & Reel
NBSG16MMNEVB	NBSG16MN Evaluation Board		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NBSG16MMNEVB

PACKAGE DIMENSIONS

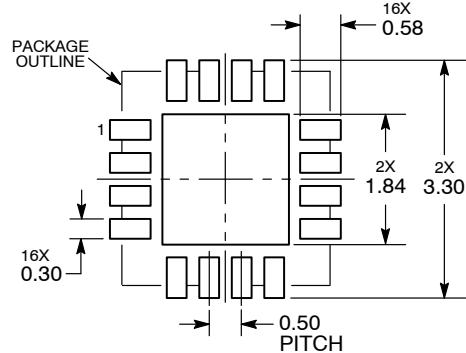
QFN16 3x3, 0.5P
CASE 485G-01
ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GigaComm is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative