GaAs pHEMT MMIC 0.25 WATT POWER AMPLIFIER DC - 40 GHz

Typical Applications

The HMC5805ALS6 is ideal for:

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Features

High P1dB Output Power: 24.5 dBm

High Psat Output Power: 27 dBm

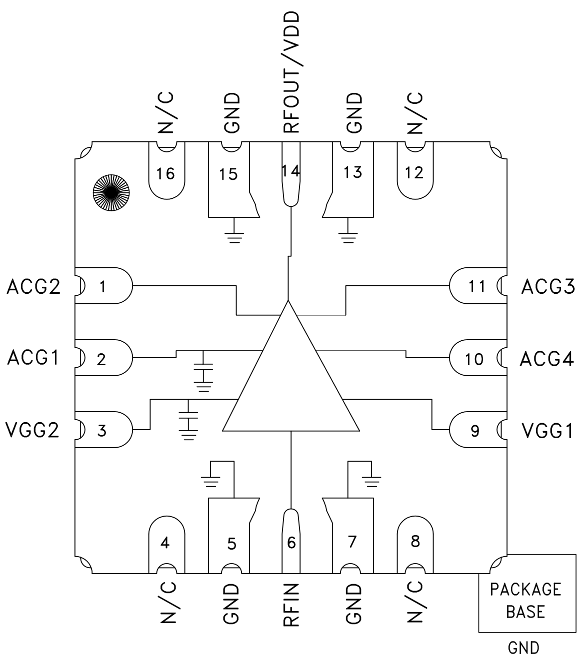
Gain: 11.5 dB

Output IP3: 29 dBm

Supply Voltage: +10 V @ 175 mA

16 Lead Ceramic 6x6 mm SMT Package: 36 mm^2

Functional Diagram



General Description

The HMC5805ALS6 is a GaAs pHEMT MMIC Distributed Power Amplifier which operates between DC and 40 GHz. The amplifier provides 11.5 dB of gain, 29 dBm output IP3 and +24 dBm of output power at 1 dB gain compression while requiring 175 mA from a +10 V supply. The HMC5805ALS6 is ideal for EW, ECM, Radar and test equipment applications. The HMC5805ALS6 amplifier I/Os are internally matched to 50 Ohms and the 6x6 mm SMT package is well suited for automated assembly techniques.

Electrical Specifications, T_A = +25° C, Vdd = +10 V, Vgg2 = +3.5 V, Idd = 175 mA*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		DC - 5			5 - 30			30 - 40		GHz
Gain	9	12.5		9	11.5			11.5		dB
Gain Flatness		±1.0			±0.75			±0.75		dB
Gain Variation Over Temperature		0.01			0.02			0.025		dB/ °C
Input Return Loss		17			11			11		dB
Output Return Loss		18			13			9		dB
Output Power for 1 dB Compression (P1dB)	19	25		18	24.5			23		dBm
Saturated Output Power (Psat)		27			27			26		dBm
Output Third Order Intercept (IP3)		34			29			26		dBm
Noise Figure		4.5			4			7		dB
Supply Current (Idd) (Vdd= 10V, Vgg1= -0.8V Typ.)		175			175			175		mA

* *Adjust Vgg1 between -2 to 0 V to achieve Idd = 175 mA typical.*

*For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D*

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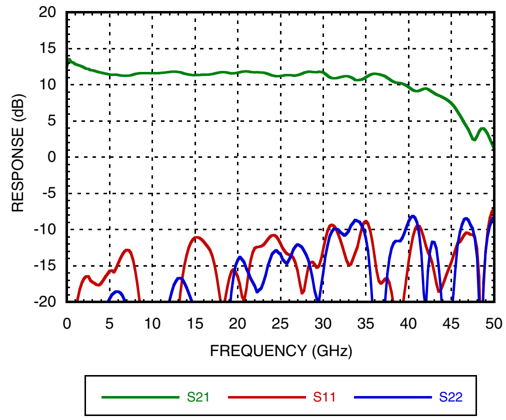
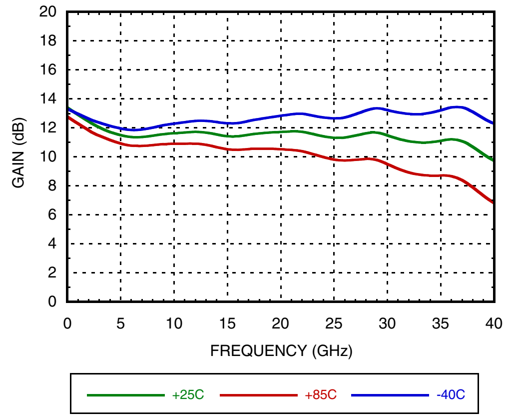
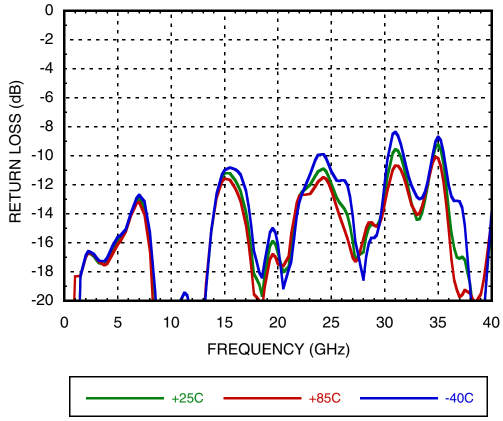
Gain & Return Loss



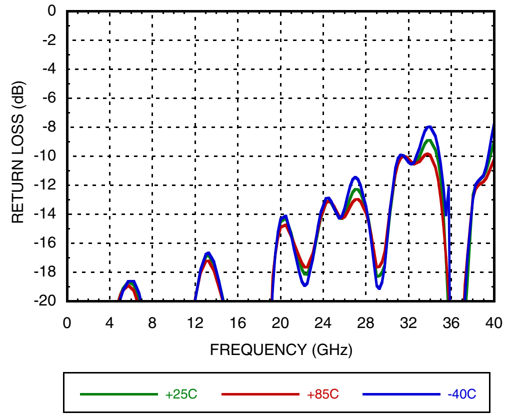
Gain vs. Temperature



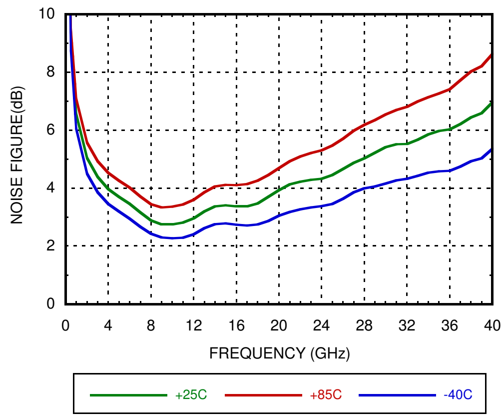
Input Return Loss vs. Temperature



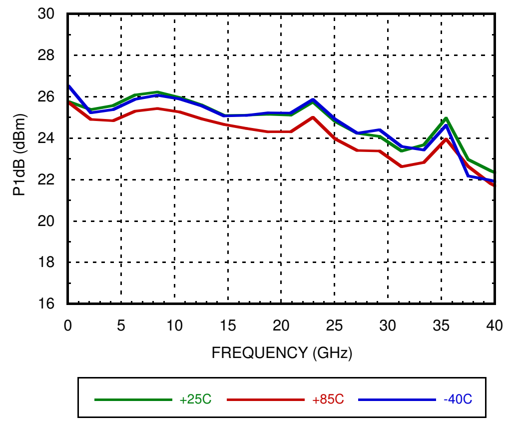
Output Return Loss vs. Temperature



Noise Figure vs. Temperature



P1dB vs. Temperature



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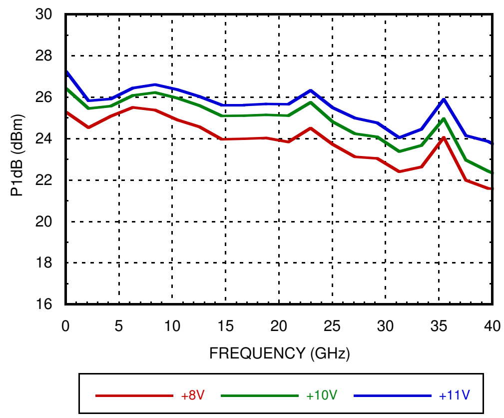
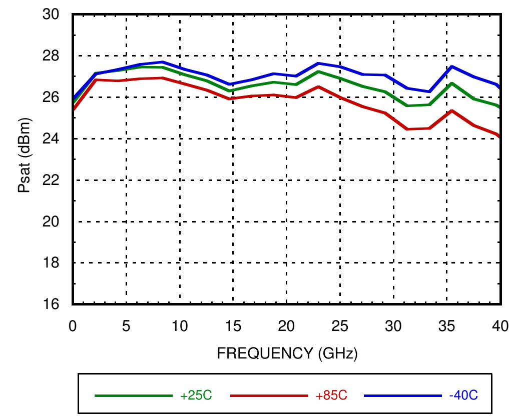
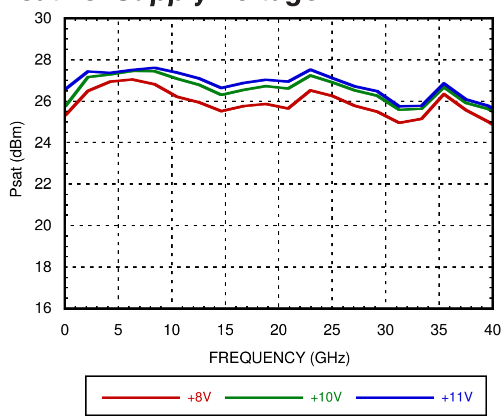
P1dB vs. Supply Voltage



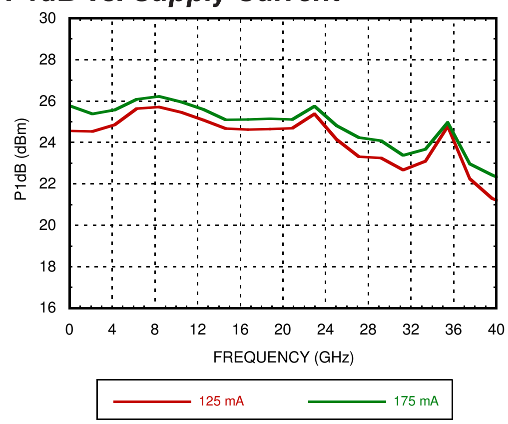
Psat vs. Temperature



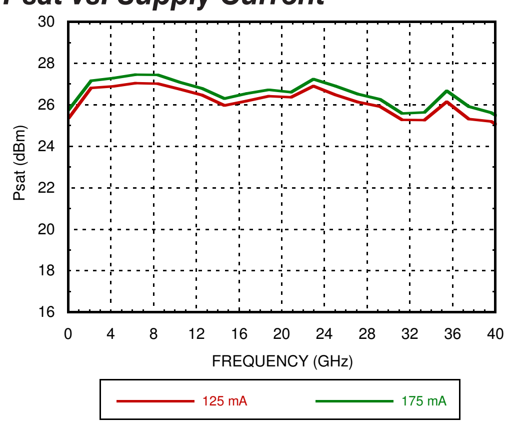
Psat vs. Supply Voltage



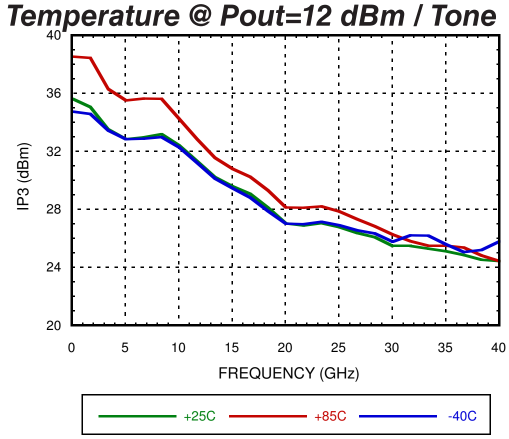
P1dB vs. Supply Current



Psat vs. Supply Current



Output IP3 vs. Temperature @ Pout=12 dBm / Tone



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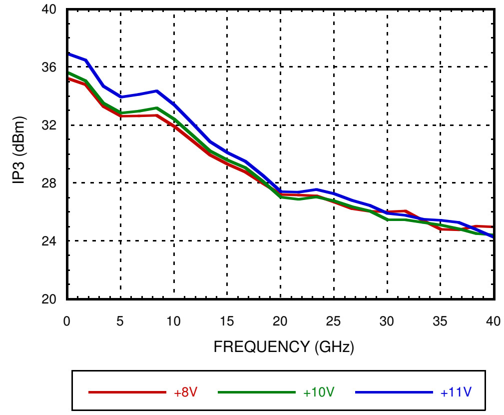
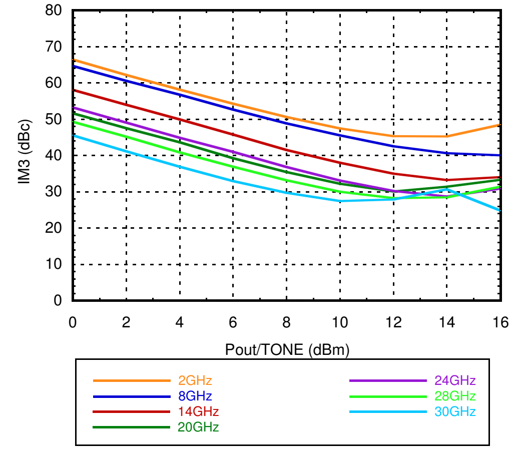
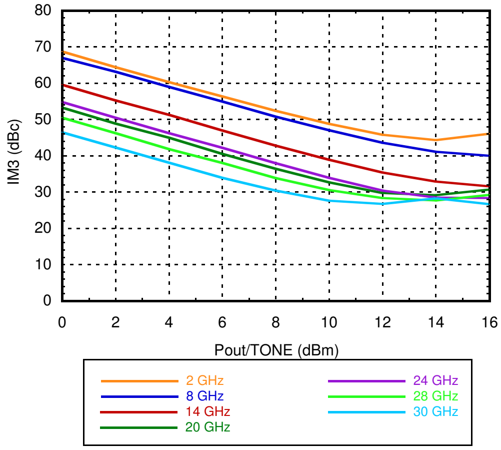
Output IP3 vs. Supply Voltage @ Pout=12 dBm / Tone



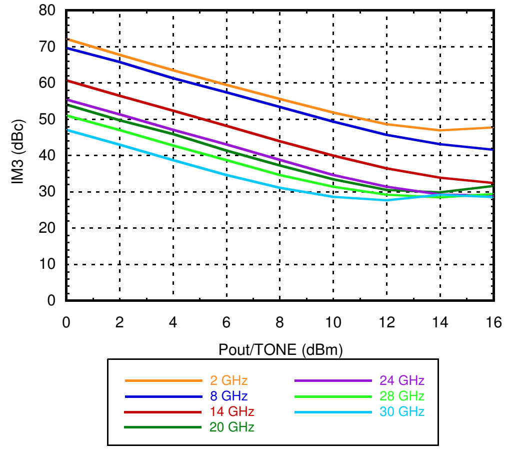
Output IM3 @ Vdd=+8V



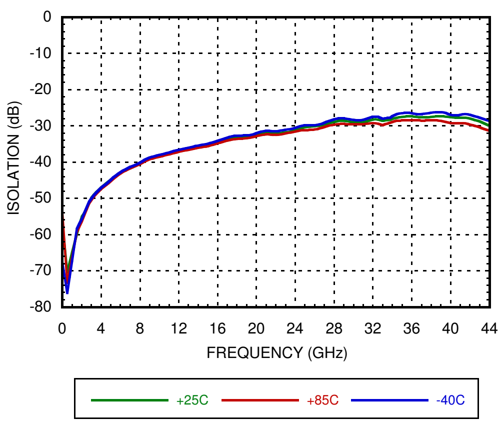
Output IM3 @ Vdd=+10V



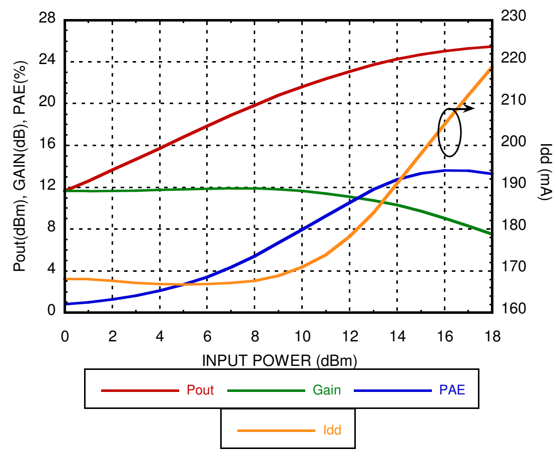
Output IM3 @ Vdd=+11V



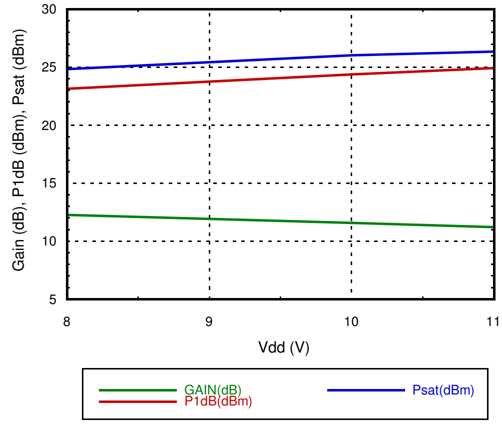
Reverse Isolation vs. Temperature



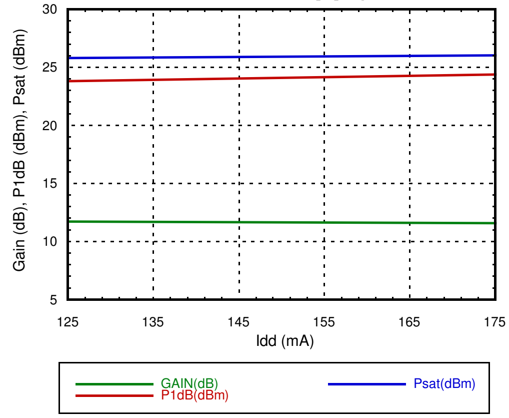
Power Compression @ 20GHz



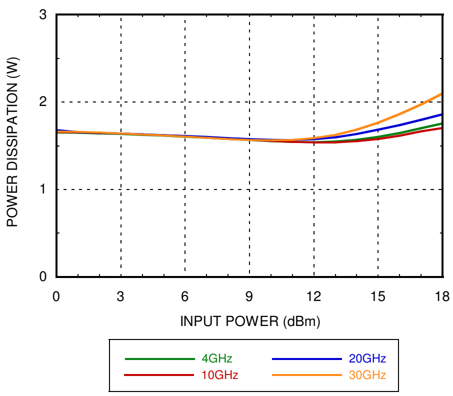
Gain and Power vs. Supply Voltage



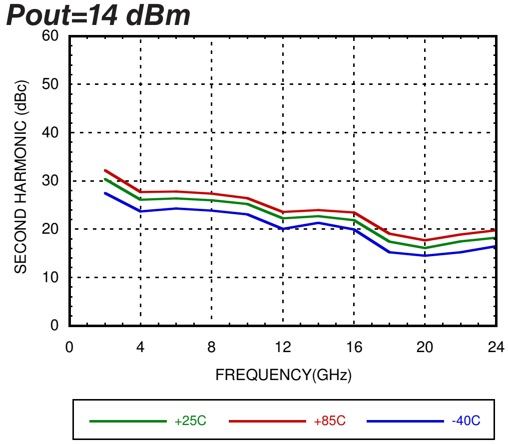
Gain and Power vs. Supply Current



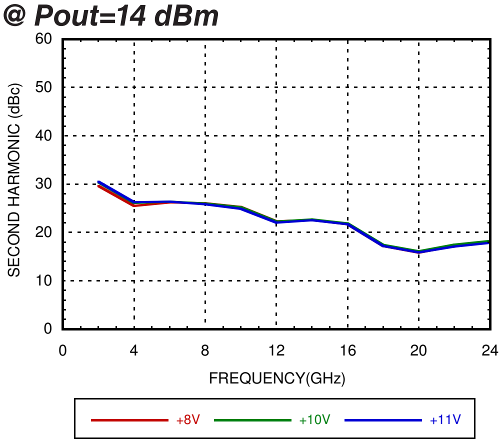
Power Dissipation @ 85C



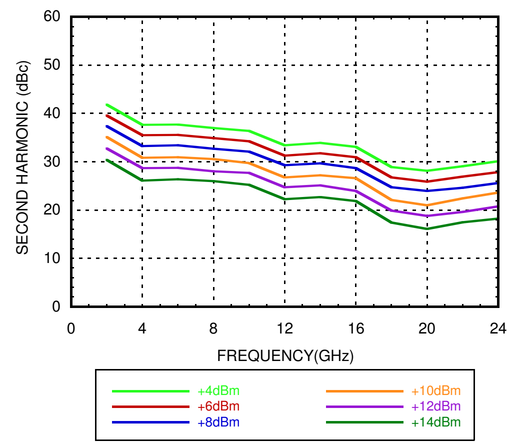
Second Harmonics vs. Temperature @ Pout=14 dBm



Second Harmonics vs. Vdd @ Pout=14 dBm



Second Harmonics vs. Pout



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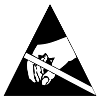
Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	12V
Gate Bias Voltage (Vgg1)	-3 to 0 Vdc
Gate Bias Voltage (Vgg2)	For Vdd = 12V, Vgg2 = 5.5V Idd >145mA For Vdd between 8.5V to 11V, Vgg2 = (Vdd - 6.5V) up to 4.5V For Vdd < 8.5V, Vgg2 must remain > 2V
RF Input Power (RFIN)	22 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 32.2 mW/°C above 85 °C)	2.89 W
Thermal Resistance (channel to ground paddle)	31.1 °C/W
Storage Temperature	-65 to 150 °C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class1B Passed 500V

Typical Supply Current vs. Vdd

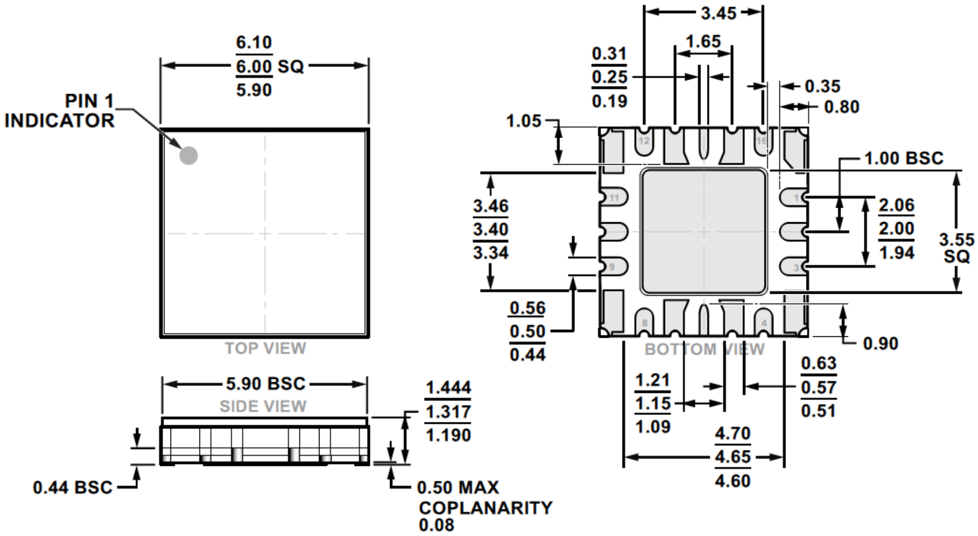
Vdd (V)	Idd (mA)
+8	175
+10	175
+11	175

Note: Amplifier will operate over full voltage ranges shown above. Vgg adjusted to achieve Idd = 175 mA.



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS] Dimensions shown in millimeters.

Table 1. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Option	Package Marking [1]
HMC5805ALS6	ALUMINA, WHITE	Gold over Nickel	MSL3	EP-16-2	H5805A XXXX
HMC5805ALS6TR	ALUMINA, WHITE	Gold over Nickel	MSL3	EP-16-2	H5805A XXXX

[1] 4-Digit lot number XXXX

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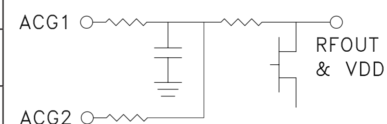
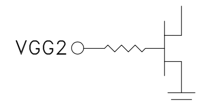
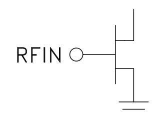
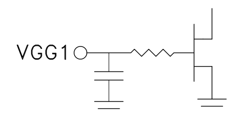
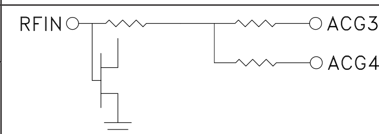
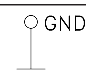
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 14	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
	ACG1	Low frequency termination. Attach bypass capacitor per application circuit herein.	
	RFOUT & VDD	RF output for amplifier. Connect DC bias (VDD) network to provide drain current (Idd). See application circuit herein.	
3	VGG2	Gate control 2 for amplifier. Attach bypass capacitors per application circuit herein. For normal operation +3.5V should be applied to Vgg2.	
6	RFIN	This pin is DC coupled and matched to 50 Ohms. Blocking capacitor is required.	
9	VGG1	Gate control 1 for amplifier. Attach bypass capacitors per application circuit herein. Please follow “MMIC Amplifier Biasing Procedure” application note.	
10	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
11	ACG3	Low frequency termination. Attach bypass capacitor per application circuit herein.	
5, 7, 13, 15	GND	These pins and exposed ground paddle must be connected to RF/DC ground.	
4, 8, 12, 16	N/C	These pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	

Application Information

BIASING PROCEDURES:

DC bias must be applied to the drain via an RF choke/inductor connection to the RFOUT/VDD pin. Gate bias must be applied to VGG1 and VGG2. Capacitive bypassing is recommended for all of the DC bias pins and AC terminations to ground are recommended for ACG1-ACG4, as shown in the Application Circuit.

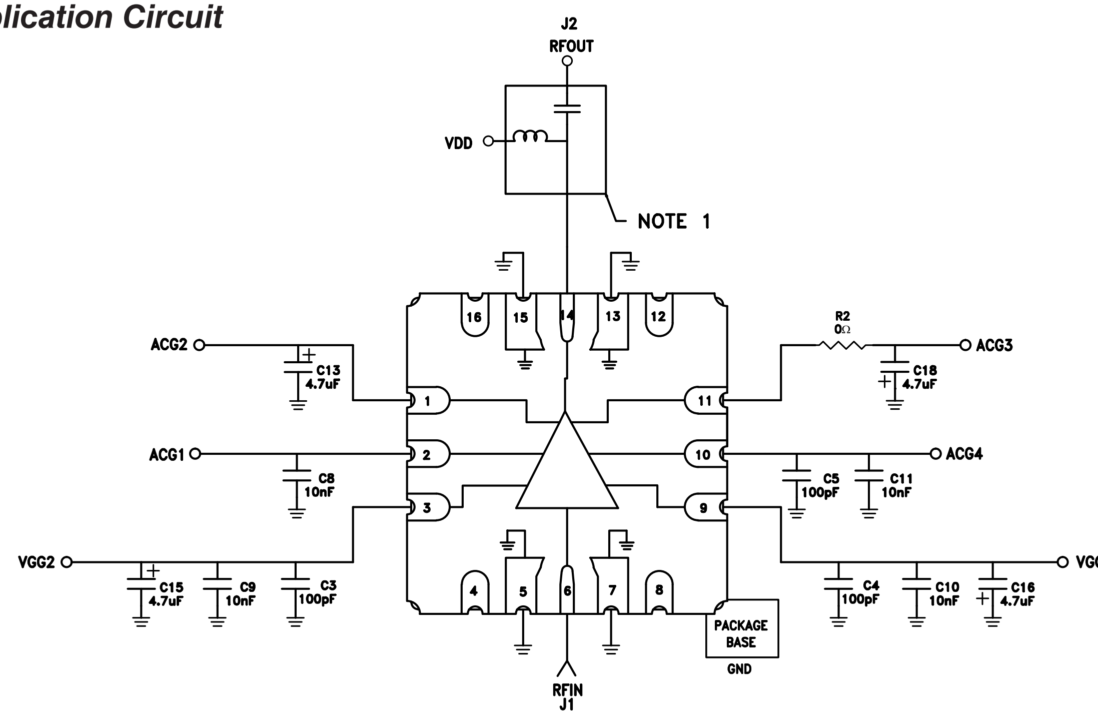
The recommended bias sequence during power-up is as follows:
1. Set VGG1 to −2.0 V to pinch off the channels of the lower FETs.
2. Set VDD to 10.0 V. Because the lower FETs are pinched off, IDQ remains very low upon application of VDD.
3. Set VGG2 to 3.5 V.
3. Adjust VGG1 to be more positive until a quiescent drain current of 175 mA has been obtained.
4. Apply the RF input signal.

The recommended bias sequence during power-down is as follows:
1. Turn off the RF input signal.
2. Set VGG1 to −2.0 V to pinch off the channels of the lower FETs.
3. Set VGG2 to 0 V.
4. Set VDD to 0 V.
5. Set VGG1 to 0 V.

Power-up and power-down sequences may differ from the ones described, though care must always be taken to ensure adherence to the values shown in the Absolute Maximum Ratings.

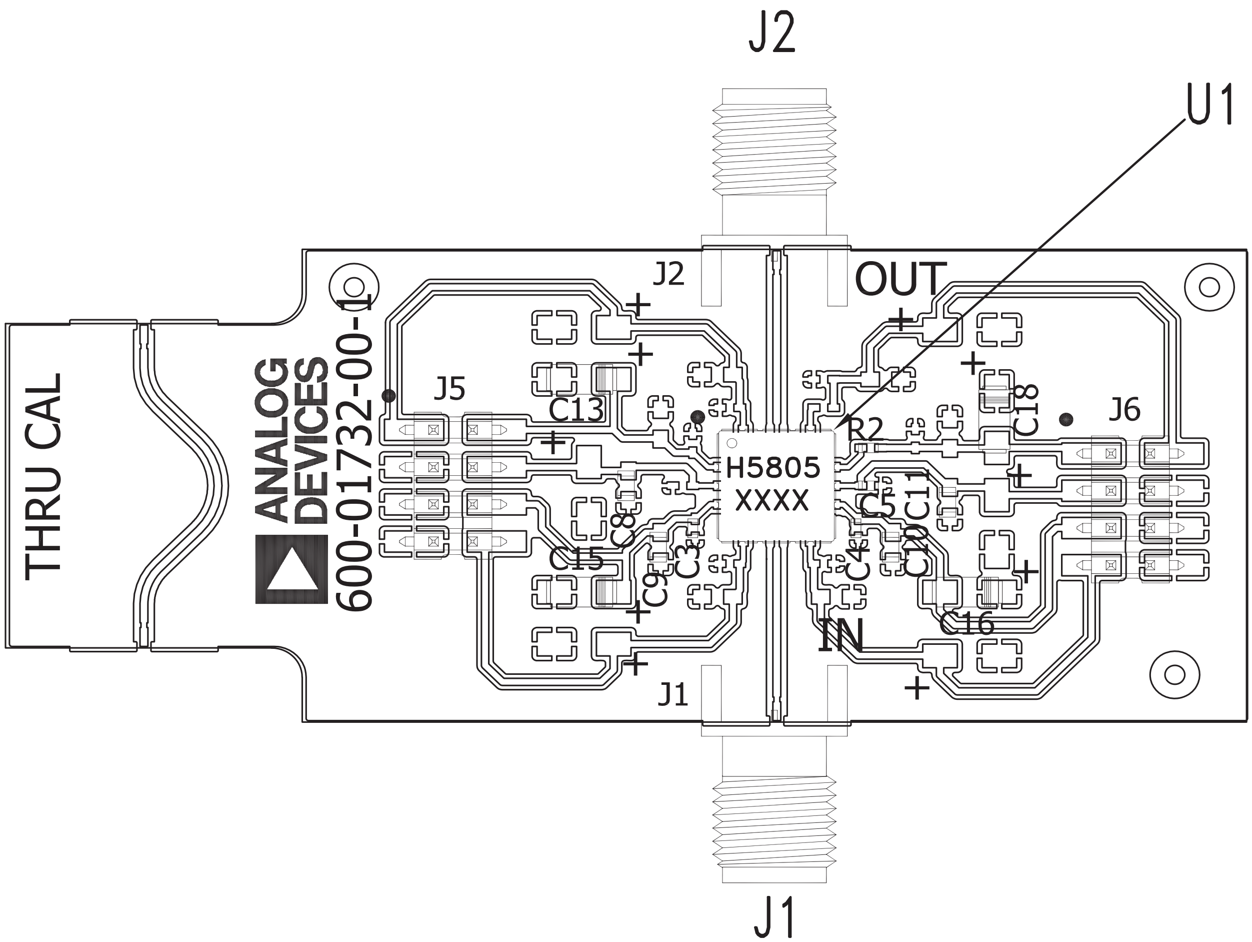
Unless otherwise noted, all measurements and data shown were taken using the typical application circuit as configured on our evaluation board. The bias conditions shown in the specifications section are the operating points recommended to optimize the overall performance. Operation using other bias conditions may provide performance that differs from what is shown in this data sheet.

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee with low series resistance and capable of providing 250 mA

Evaluation PCB



List of Materials for Evaluation EV1HMC5805ALS6 [1]

Item	Description
J1, J2	PCB Mount K Connectors, SRI
J5, J6	DC Pins
C3 - C5	100 pF Capacitors, 0402 Pkg.
C8 - C11	0.01 µF Capacitors, 0603 Pkg.
C13, C15, C16 , C18	4.7 µF Capacitors, Case A Pkg.
R2	Zero Ohm Resistor, 0402 Pkg.
U1	HMC5805ALS6 Amplifier
PCB [2]	128996 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices upon request.

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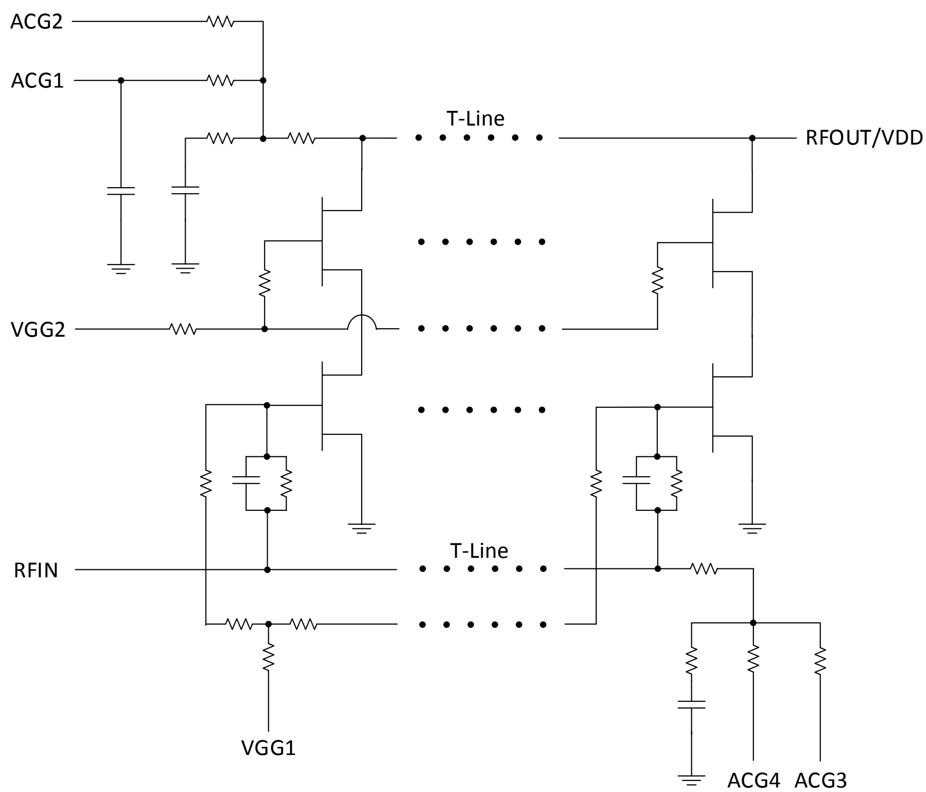
Theory of Operation

The HMC5805ALS6 is a GaAs, pHEMT, MMIC power amplifier. Its basic architecture is that of a cascode distributed amplifier which allows for control of DC bias for a drain and two gates. The cascode distributed architecture uses a fundamental cell consisting of a stack of two field effect transistors (FETs) with the source of the upper FET connected to the drain of the lower FET. The fundamental cell is then duplicated several times, with a transmission line feeding the RFIN signal to the gates of the lower FETs and a separate transmission line interconnecting the drains of the upper FETs and routing the amplified signal to the RFOUT/VDD pin. Additional circuit design techniques are used around each cell to optimize the overall performance for broadband operation. The major benefit of this architecture is that high performance is maintained across a bandwidth far greater than what a single instance of the fundamental cell would provide. Additionally, ACG1-ACG4 provide access to internal nodes which, when provided with the recommended AC terminations to ground, ensure that the overall response remains flat across the widest possible frequency range. A simplified Schematic of Architecture is shown in below.

Schematic of Architecture



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