

## FEATURES

- Outstanding gain linearity**
- Ultrahigh gain, 5000 V/mV min**
- Low  $V_{OS}$  over temperature, 55  $\mu\text{V}$  max**
- $\text{TCV}_{OS}$ , 0.3  $\mu\text{V}/^\circ\text{C}$  max**
- High PSRR, 3  $\mu\text{V}/\text{V}$  max**
- Low power consumption, 60 mW max**
- Available in die form**

## PIN CONNECTIONS

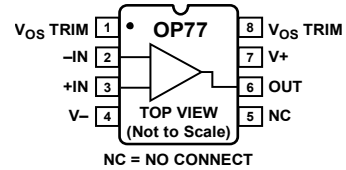


Figure 1. 8-Pin Hermetic CERDIP\_Q-8 (Z Suffix)

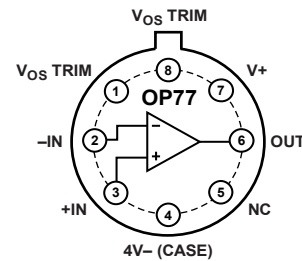


Figure 2. TO-99 (J Suffix)

## GENERAL DESCRIPTION

The **OP77** has outstanding gain of 10,000,000 or more that is maintained over the full 10 V output range. This gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps and provides superior performance in high closed-loop gain applications. Low initial  $V_{OS}$  drift and rapid stabilization time, combined with only 50 mW of power consumption, are significant improvements over previous designs. These characteristics, plus the  $\text{TCV}_{OS}$  of 0.3  $\mu\text{V}/^\circ\text{C}$  maximum and the low  $V_{OS}$  of 25  $\mu\text{V}$  maximum, eliminates

the need for  $V_{OS}$  adjustment and increases system accuracy over temperature.

A PSRR of 3  $\mu\text{V}/\text{V}$  (110 dB) and CMRR of 1.0  $\mu\text{V}/\text{V}$  maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the **OP77** ideally suited for high resolution instrumentation and other tight error budget systems.

**TABLE OF CONTENTS**

Features .....	1	Thermal Resistance .....	6
Pin Connections .....	1	ESD Caution.....	6
General Description .....	1	Typical Performance Characteristics .....	7
Revision History .....	2	Test Circuits.....	10
Specifications.....	3	Applications.....	11
Electrical Specifications.....	3	Precision Current Sinks.....	12
Wafer Test Limits.....	4	Outline Dimensions .....	15
Typical Electrical Characteristics .....	5	Ordering Guide .....	16
Absolute Maximum Ratings.....	6		

**REVISION HISTORY**

**10/15—Rev. F to Rev. G**

Changes to Features Section and General Description Section.....	1
Changes to Note 1, Ordering Guide.....	16

**3/15—Rev. E to Rev. F**

Updated Outline Dimensions .....	15
Changes to Ordering Guide .....	16

**4/10—Rev. D to Rev. E**

Removed Figure 33 and Two Subsequent Paragraphs.....	12
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**6/09—Rev. C to Rev. D**

Changes to Figure 1 and Figure 2.....	1
Changes to Table 1.....	3
Removed Endnote 1 and Endnote 2 in Table 3 .....	4
Changes to Figure 16.....	9
Changes to Figure 31 and Figure 32.....	12
Changes to Figure 38.....	14
Moved Figure 39 .....	14

**10/02—Rev. B to Rev. C**

Edits to Specifications .....	2
Figure 2 Caption Changed .....	10
Figure 3 Caption Changed .....	10
Edits to Figure 10.....	11
Updated Outline Dimensions.....	15

**2/02—Rev. A to Rev. B**

Remove 8-Lead SO PIN Connection Diagrams.....	1
Changes to Absolute Maximum Rating.....	2
Remove OP77B column from Specifications.....	2
Remove OP77B column from Electrical Characteristics .....	3, 5
Remove OP77G column from Wafer Test Limits.....	6
Remove OP77G column from Typical Electrical Characteristics .....	6

## SPECIFICATIONS

### ELECTRICAL SPECIFICATIONS

@  $V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP77E			OP77F			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	$V_{OS}$		10	25		20	60		$\mu\text{V}$
LONG-TERM STABILITY <sup>1</sup>	$V_{OS}/\text{time}$		0.3			0.4			$\mu\text{V}/\text{Mo}$
INPUT OFFSET CURRENT	$I_{OS}$		0.3	1.5		0.3	2.8		nA
INPUT BIAS CURRENT	$I_B$		-0.2	+1.2	+2.0	-0.2	+1.2	+2.8	nA
INPUT NOISE VOLTAGE <sup>2</sup>	$e_{n\text{-p-p}}$	0.1 Hz to 10 Hz	0.35	0.6		0.38	0.65		$\mu\text{V}_{\text{p-p}}$
INPUT NOISE VOLTAGE DENSITY	$e_n$	$f_0 = 10\text{ Hz}$ $f_0 = 100\text{ Hz}^2$ $f_0 = 1000\text{ Hz}$	10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5		$\text{nV}/\sqrt{\text{Hz}}$
INPUT NOISE CURRENT <sup>2</sup>	$i_{n\text{-p-p}}$	0.1 Hz to 10 Hz	14	30		15	35		$\text{pA}_{\text{p-p}}$
INPUT NOISE CURRENT DENSITY	$i_n$	$f_0 = 10\text{ Hz}$ $f_0 = 100\text{ Hz}^2$ $f_0 = 1000\text{ Hz}$	0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18		$\text{pA}/\sqrt{\text{Hz}}$
INPUT RESISTANCE Differential Mode <sup>3</sup> Common Mode	$R_{IN}$ $R_{INCM}$		26	45 200		18.5	45 200		$\text{M}\Omega$ $\text{G}\Omega$
INPUT VOLTAGE RANGE	IVR		$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$	0.1	1.0		0.1	1.6		$\mu\text{V}/\text{V}$
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	0.7	3.0		0.7	3.0		$\mu\text{V}/\text{V}$
LARGE-SIGNAL VOLTAGE GAIN	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	5000	12,000		2000	6000		V/mV
OUTPUT VOLTAGE SWING	$V_O$	$R_L \geq 10\text{ k}\Omega$ $R_L \geq 2\text{ k}\Omega$ $R_L \geq 1\text{ k}\Omega$	$\pm 13.5$ $\pm 12.5$ $\pm 12.0$	$\pm 14.0$ $\pm 13.0$ $\pm 12.5$		$\pm 13.5$ $\pm 12.5$ $\pm 12.0$	$\pm 14.0$ $\pm 13.0$ $\pm 12.5$		V
SLEW RATE <sup>2</sup>	SR	$R_L \geq 2\text{ k}\Omega$	0.1	0.3		0.1	0.3		$\text{V}/\mu\text{s}$
CLOSED-LOOP BANDWIDTH <sup>2</sup>	BW	$A_{VCL} + 1$	0.4	0.6		0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	$R_O$		60			60			$\Omega$
POWER CONSUMPTION	$P_d$	$V_S = \pm 15\text{ V}$ , no load $V_S = \pm 3\text{ V}$ , no load	50 3.5	60 4.5		50 3.5	60 4.5		mW
OFFSET ADJUSTMENT RANGE		$R_p = 20\text{ kn}$	$\pm 3$			$\pm 3$			mV

<sup>1</sup> Long-term input offset voltage stability refers to the averaged trend line of  $V_{OS}$  vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\ \mu\text{V}$ .

<sup>2</sup> Sample tested.

<sup>3</sup> Guaranteed by design.

@  $V_S = \pm 15\text{ V}$ ,  $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for OP77FJ and OP77E/OP77F, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	OP77E			OP77F			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	$V_{OS}$			10	45		20	100	$\mu\text{V}$
AVERAGE INPUT OFFSET VOLTAGE DRIFT <sup>1</sup>	$TCV_{OS}$			0.1	0.3		0.2	0.6	$\mu\text{V}/^\circ\text{C}$
INPUT OFFSET CURRENT	$I_{OS}$			0.5	2.2		0.5	4.5	nA
AVERAGE INPUT OFFSET CURRENT DRIFT <sup>2</sup>	$TCI_{OS}$			1.5	4.0		1.5	85	$\text{pA}/^\circ\text{C}$
INPUT BIAS CURRENT	$I_B$		-0.2	+2.4	+4.0	-0.2	+2.4	+6.0	nA
AVERAGE INPUT BIAS CURRENT DRIFT <sup>2</sup>	$TCI_B$			8	40		15	60	$\text{pA}/^\circ\text{C}$
INPUT VOLTAGE RANGE	IVR		$\pm 13.0$	$\pm 13.5$		$\pm 13.0$	$\pm 13.5$		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$		0.1	1.0		0.1	3.0	$\text{pV}/\text{V}$
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$		1.0	3.0		1.0	5.0	$\mu\text{V}/\text{V}$
LARGE-SIGNAL VOLTAGE GAIN	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	2000	6000		1000	4000		$\text{V}/\text{mV}$
OUTPUT VOLTAGE SWING	$V_O$	$R_L \geq 2\text{ k}\Omega$	$\pm 12$	$\pm 13.0$		$\pm 12$	$\pm 13.0$		V
POWER CONSUMPTION	$P_d$	$V_S = \pm 15\text{ V}$ , no load		60	75		60	75	mW

<sup>1</sup> OP77E:  $TCV_{OS}$  is 100% tested on J and Z packages.

<sup>2</sup> Guaranteed by end-point limits.

**WAFER TEST LIMITS**

@  $V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , for OP77NBC devices, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	OP77NBC Limit	Unit
INPUT OFFSET VOLTAGE	$V_{OS}$		40	$\mu\text{V max}$
INPUT OFFSET CURRENT	$I_{OS}$		2.0	nA max
INPUT BIAS CURRENT	$I_B$		$\pm 2$	nA max
INPUT RESISTANCE Differential Mode	$R_{IN}$		26	$\text{M}\Omega\text{ min}$
INPUT VOLTAGE RANGE	IVR		$\pm 13$	V min
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$	1	$\mu\text{V}/\text{V max}$
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	3	$\mu\text{V}/\text{V max}$
OUTPUT VOLTAGE SWING	$V_O$	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$ $R_L = 1\text{ k}\Omega$	$\pm 13.5$ $\pm 12.5$ $\pm 12.0$	V min
LARGE-SIGNAL VOLTAGE GAIN	$A_{VO}$	$R_L = 2\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	2000	$\text{V}/\text{mV min}$
DIFFERENTIAL INPUT VOLTAGE			$\pm 30$	V max
POWER CONSUMPTION	$P_d$	$V_O = 0\text{ V}$	60	mW max

**TYPICAL ELECTRICAL CHARACTERISTICS**

@  $V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Symbol	Conditions	OP77NBC Limit	Unit
AVERAGE INPUT OFFSET VOLTAGE DRIFT	$TCV_{OS}$	$R_S = 50\ \Omega$	0.1	$\mu\text{V}/^\circ\text{C}$
NULLED INPUT OFFSET VOLTAGE DRIFT	$TCV_{OSn}$	$R_S = 50\ \Omega$ , $R_P = 20\ \text{k}\Omega$	0.1	$\mu\text{V}/^\circ\text{C}$
AVERAGE INPUT OFFSET CURRENT DRIFT	$TCI_{OS}$		0.5	$\text{pA}/^\circ\text{C}$
SLEW RATE	SR	$R_L \geq 2\ \text{k}\Omega$	0.3	$\text{V}/\mu\text{s}$
BANDWIDTH	BW	$A_{VCL} + 1$	0.6	MHz

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter <sup>1</sup>	Rating
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage <sup>2</sup>	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–25°C to +85°C
Junction Temperature (T <sub>J</sub> )	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

<sup>1</sup> Absolute Maximum Ratings apply to both dice and packaged parts, unless otherwise noted.

<sup>2</sup> For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Table 6.

Package Type	$\theta_{JA}$ <sup>1</sup>	$\theta_{JC}$	Unit
8-Pin TO-99 H-08 (J Suffix)	150	18	°C/W
8-Lead Hermetic CERDIP Q-8 (Z Suffix)	148	16	°C/W

<sup>1</sup>  $\theta_{JA}$  is specified for worst-case mounting conditions, i.e.,  $\theta_{JA}$  is specified for a device in socket for the TO-99 and CERDIP packages.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

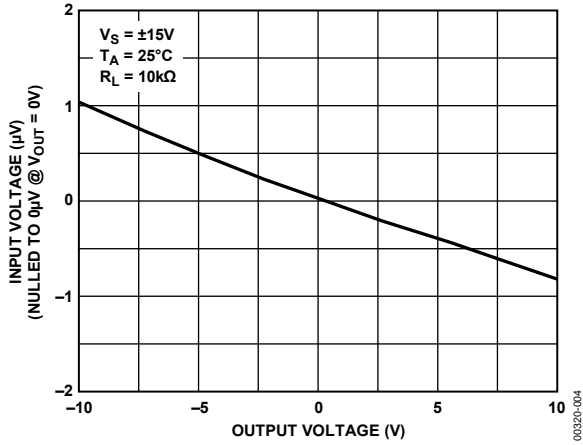


Figure 3. Gain Linearity (Input Voltage vs. Output Voltage)

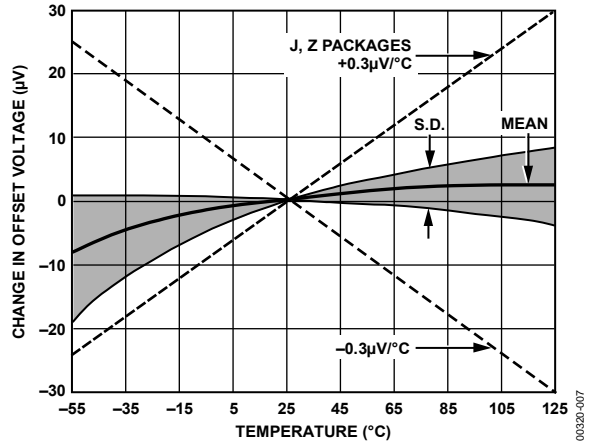


Figure 6. Untrimmed Offset Voltage vs. Temperature

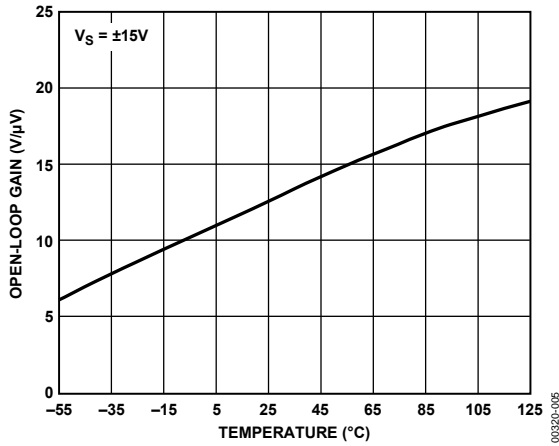


Figure 4. Open-Loop Gain vs. Temperature

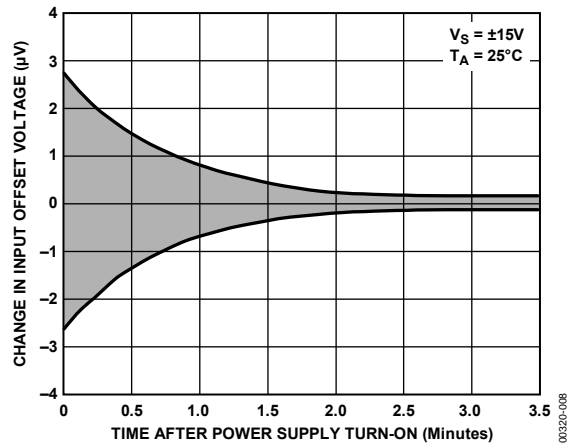


Figure 7. Warm-Up Drift

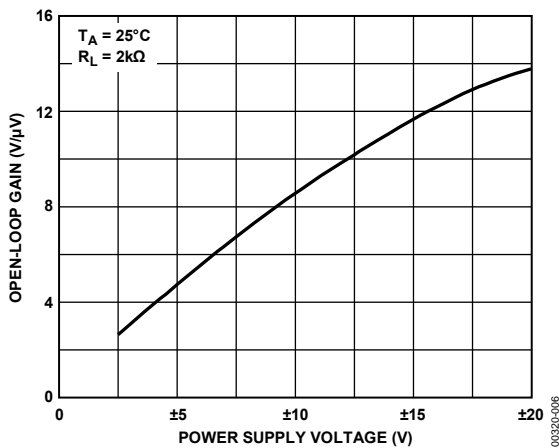


Figure 5. Open-Loop Gain vs. Power Supply Voltage

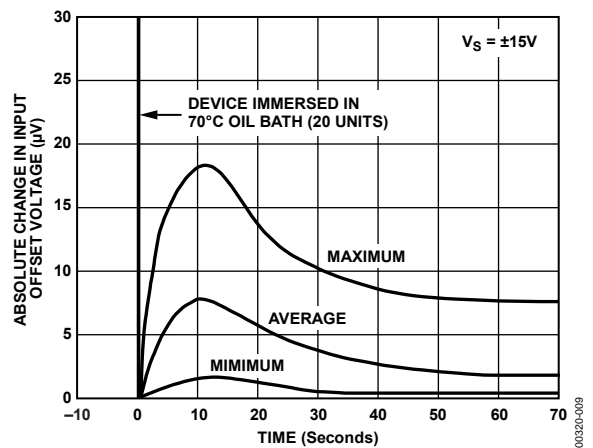


Figure 8. Offset Voltage Change Due to Thermal Shock

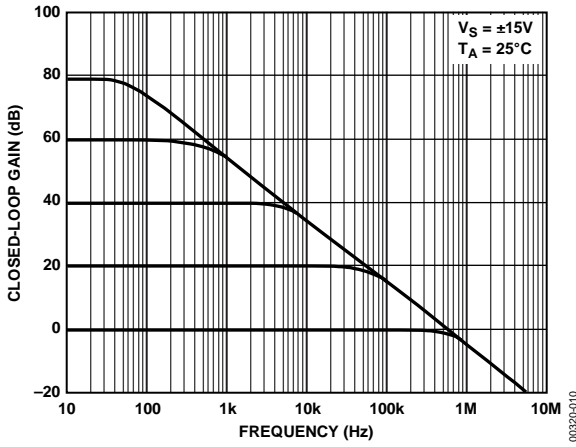


Figure 9. Closed-Loop Response for Various Gain Configurations

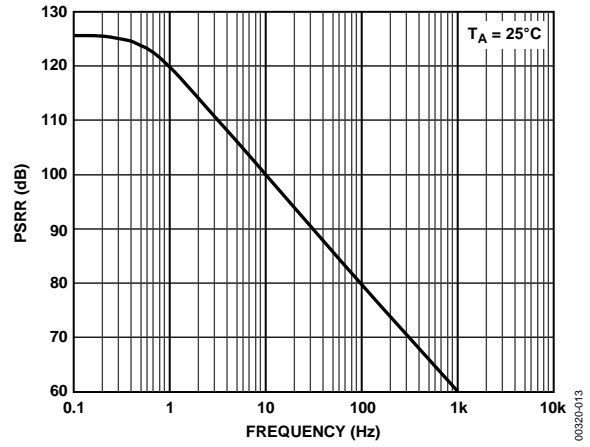


Figure 12. PSRR vs. Frequency

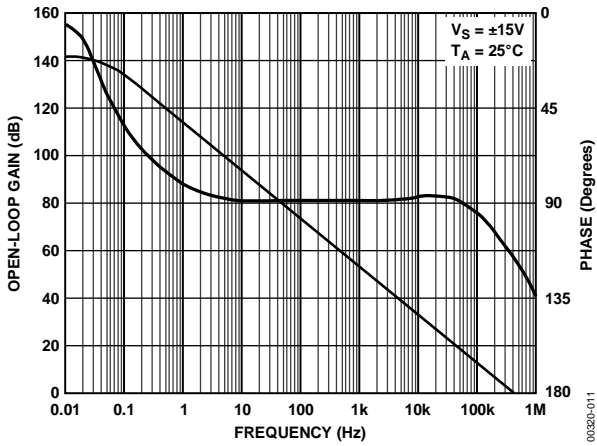


Figure 10. Open-Loop Gain/Phase Response

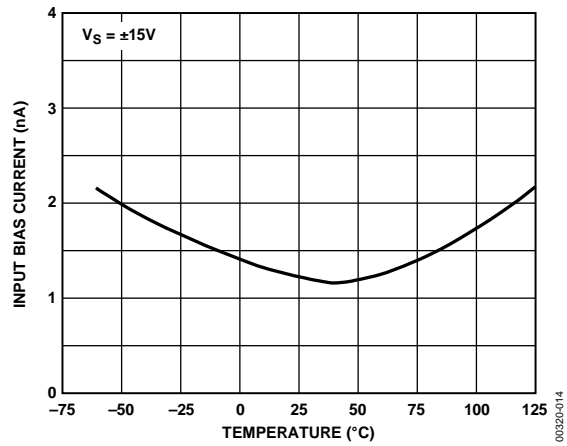


Figure 13. Input Bias Current vs. Temperature

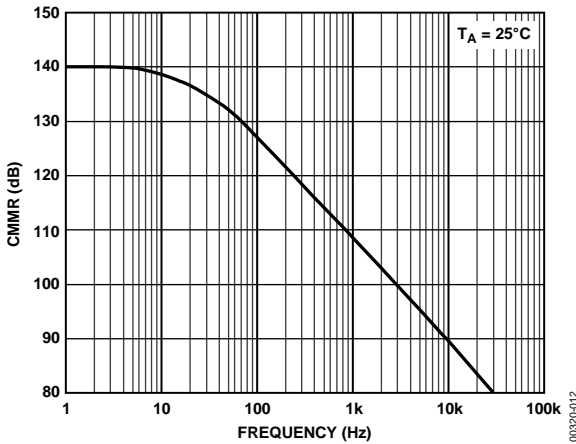


Figure 11. CMRR vs. Frequency

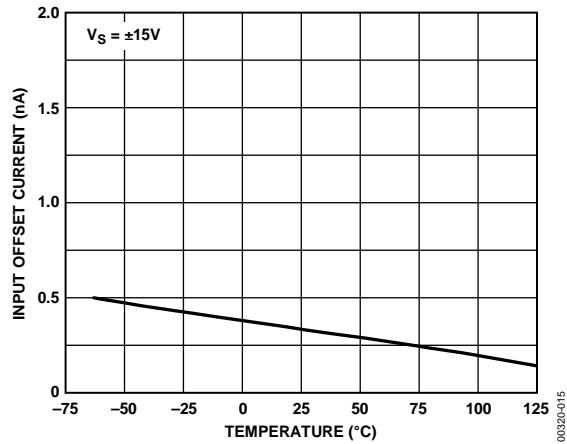


Figure 14. Input Offset Current vs. Temperature



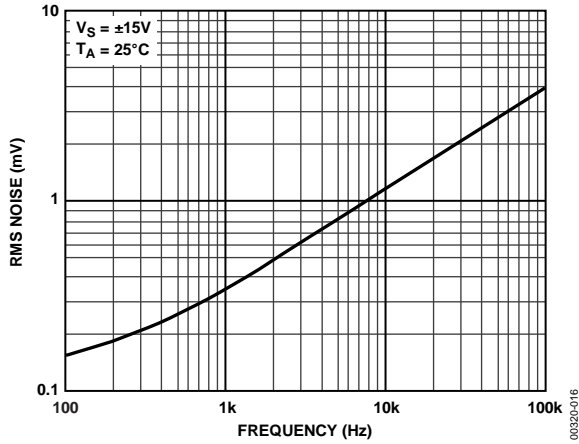


Figure 15. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

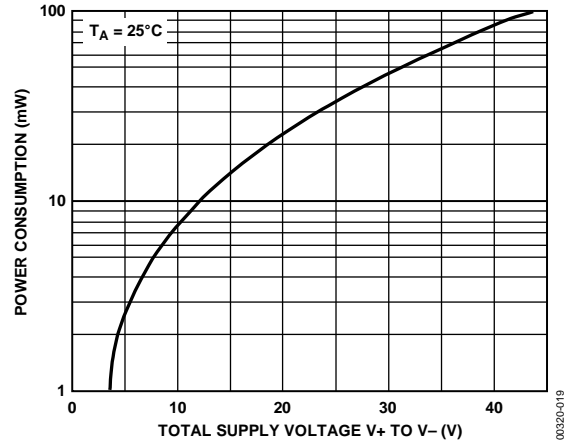


Figure 18. Power Consumption vs. Power Supply

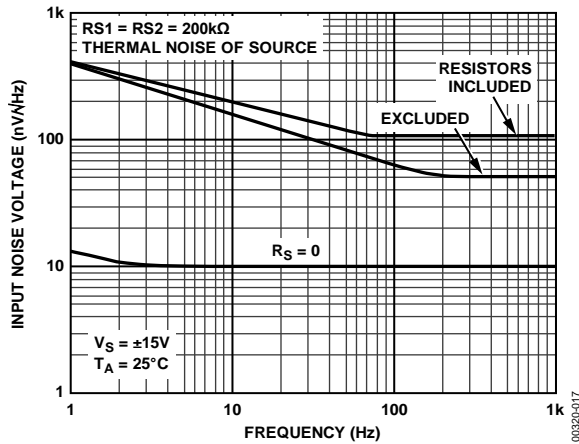


Figure 16. Total Input Noise Voltage vs. Frequency

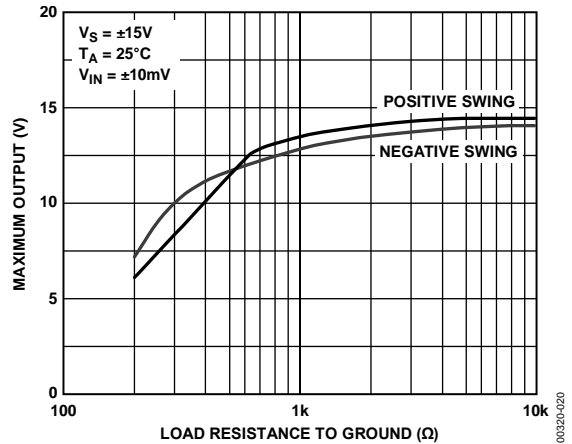


Figure 19. Maximum Output Voltage vs. Load Resistance

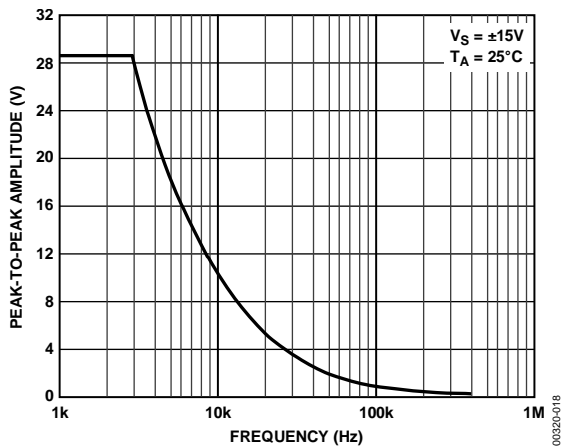


Figure 17. Maximum Output Swing vs. Frequency

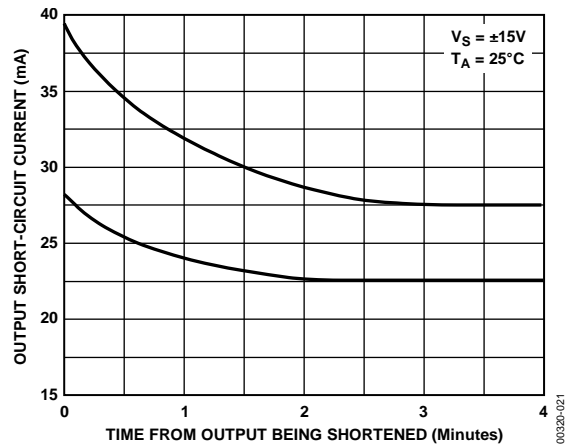


Figure 20. Output Short-Circuit Current vs. Time

TEST CIRCUITS

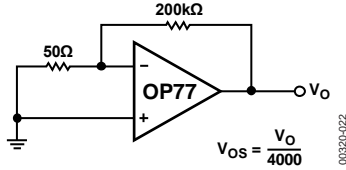


Figure 21. Typical Offset Voltage Test Circuit

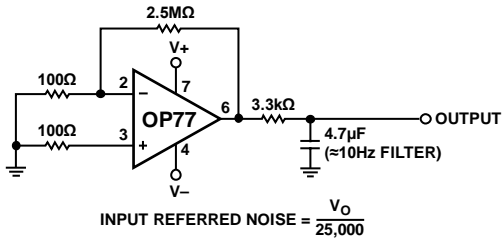


Figure 22. Typical Low-Frequency Noise Test Circuit

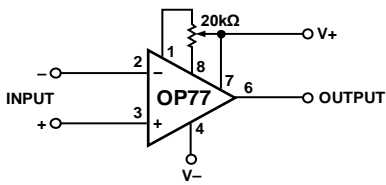
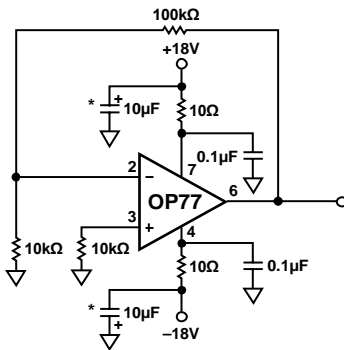
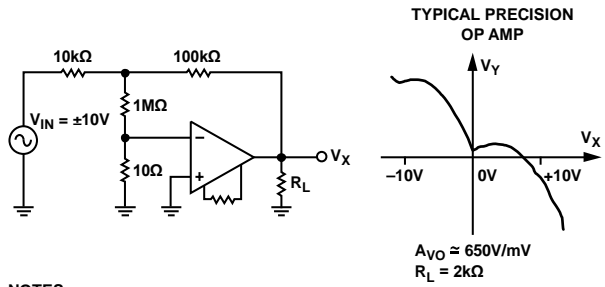


Figure 23. Optional Offset Nulling Circuit



NOTES  
\*1 PER BOARD

Figure 24. Burn-In Circuit



NOTES  
1. GAIN NOT CONSISTANT. CAUSES NONLINEAR ERRORS.  
2. A<sub>VO</sub> SPEC IS ONLY PART OF THE SOLUTION.  
3. CHECK SPECIFICATION TABLE 1 AND TABLE 2 FOR PERFORMANCE.

Figure 25. Open-Loop Gain Linearity

Actual open-loop voltage gain can vary greatly at various output voltages. All automated testers use endpoint testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Because this is difficult for manufacturers to test, users should make their own evaluations. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

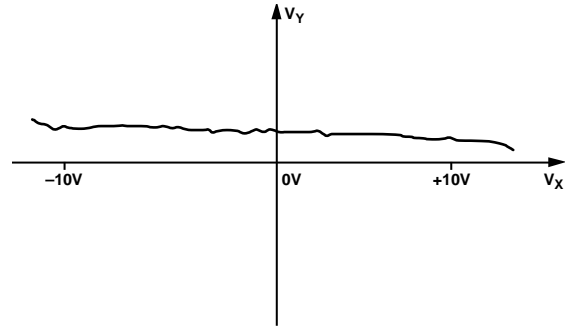


Figure 26. Output Gain Linearity Trace

This is the output gain linearity trace for the new OP77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive—approximately 10,000,000.

# APPLICATIONS

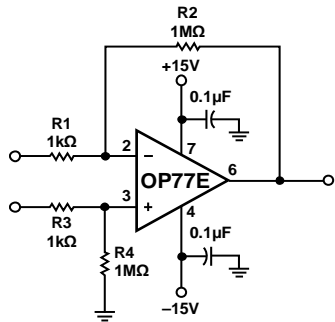


Figure 27. Precision High-Gain Differential Amplifier

The high gain, gain linearity, CMRR, and low TC<sub>VOs</sub> of the OP77 make it possible to obtain performance not previously available in single-stage, very high-gain amplifier applications.

For best CMR,  $\frac{R1}{R2}$  must equal  $\frac{R3}{R4}$ . In this example, with a 10 mV differential signal, the maximum errors are as listed in Table 7.

Table 7. Maximum Errors

Type	Amount
Common-Mode Voltage	0.01%/V
Gain Linearity, Worst Case	0.02%
TC <sub>VOs</sub>	0.003%/°C
TC <sub>Ios</sub>	0.008%/°C

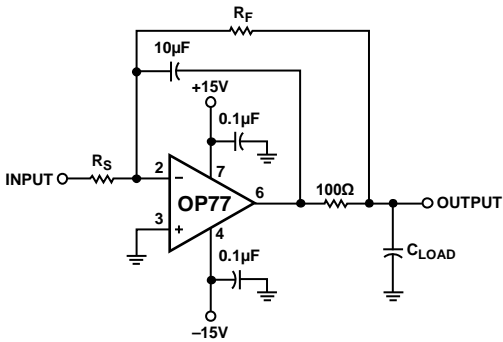


Figure 28. Isolating Large Capacitive Loads

This circuit reduces maximum slew rate but allows driving capacitive loads of any size without instability. Because the boom resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP77.

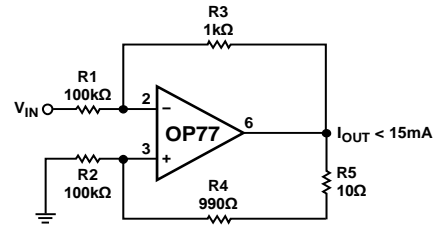
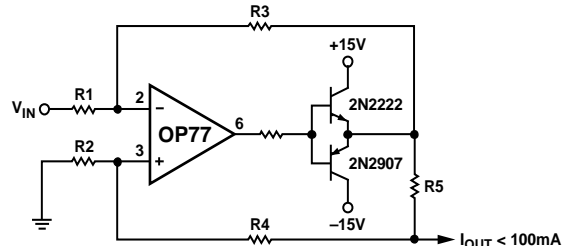


Figure 29. Basic Current Source



$$I_{OUT} = V_{IN} \left( \frac{R3}{R1 - R5} \right)$$

$$\text{GIVEN } R3 = R4 + R5, R1 = R2$$

Figure 30. 100 mA Current Source

These current sources can supply both positive and negative current into a grounded load.

Note that

$$Z_O = \frac{R5 \left( \frac{R4}{R2} + 1 \right)}{\frac{R5 + R4}{R2} \frac{R3}{R1}}$$

And that for  $Z_O$  to be infinite  $\frac{R5 + R4}{R2}$  must =  $\frac{R3}{R1}$

PRECISION CURRENT SINKS

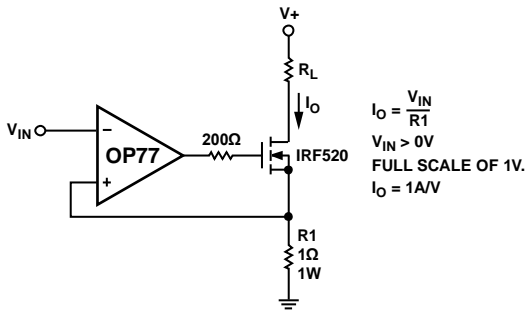


Figure 31. Positive Current Sink

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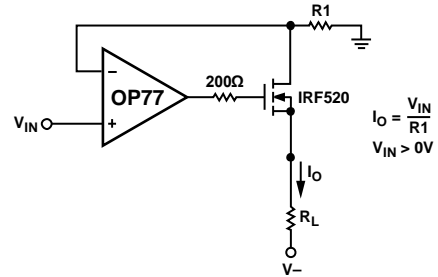


Figure 32. Positive Current Source

00320-033

The simple high-current sinks, shown Figure 31 and Figure 32, require the load to float between the power supply and the sink. In these circuits, the high gain, high CMRR, and low TCV<sub>OS</sub> of the OP77 ensure high accuracy.

The high gain and low TCV<sub>OS</sub> ensure accurate operation with inputs from microvolts to volts. In Figure 33, the signal always appears as a common-mode signal to the op amps. The OP77EZ CMRR of 1 μV/V ensures errors of less than 2 ppm.

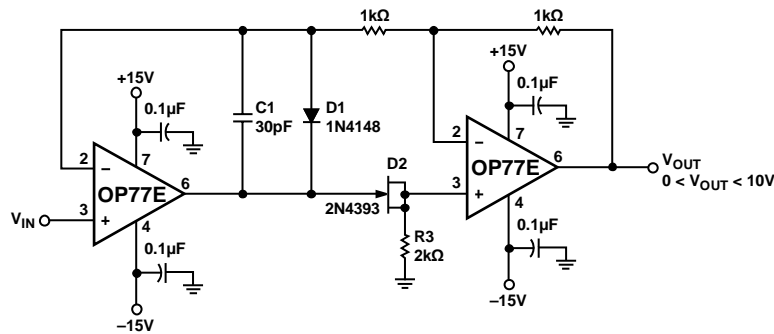


Figure 33. Precision Absolute Value Amplifier

00320-035

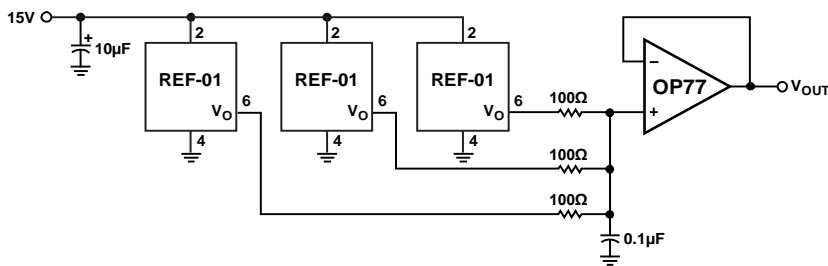


Figure 34. Low Noise Precision Reference

00320-036

Figure 34 relies upon low  $TCV_{OS}$  of the OP77 and noise combined with very high CMRR to provide precision buffering of the averaged REF-01 voltage outputs.

In Figure 35,  $C_H$  must be of polystyrene, Teflon\*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of  $C_H$  and the bias current of the AD820.

\*Teflon is a registered trademark of the Dupont Company

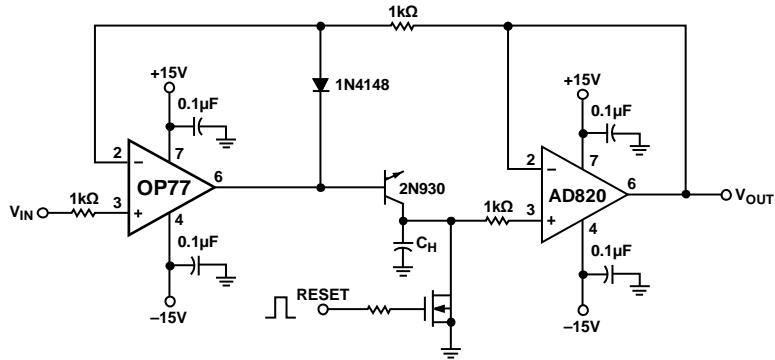


Figure 35. Precision Positive Peak Detector

00320-037

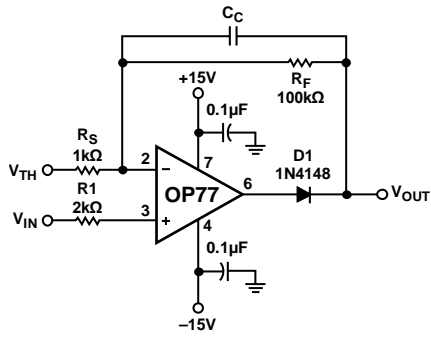


Figure 36. Precision Threshold Detector/Amplifier

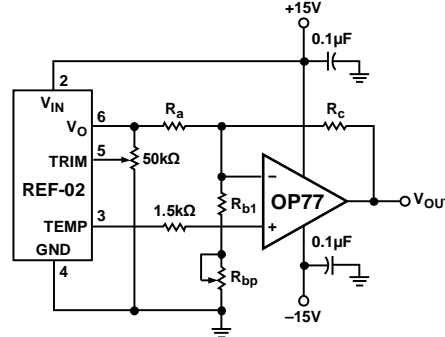


Figure 37. Precision Temperature Sensor

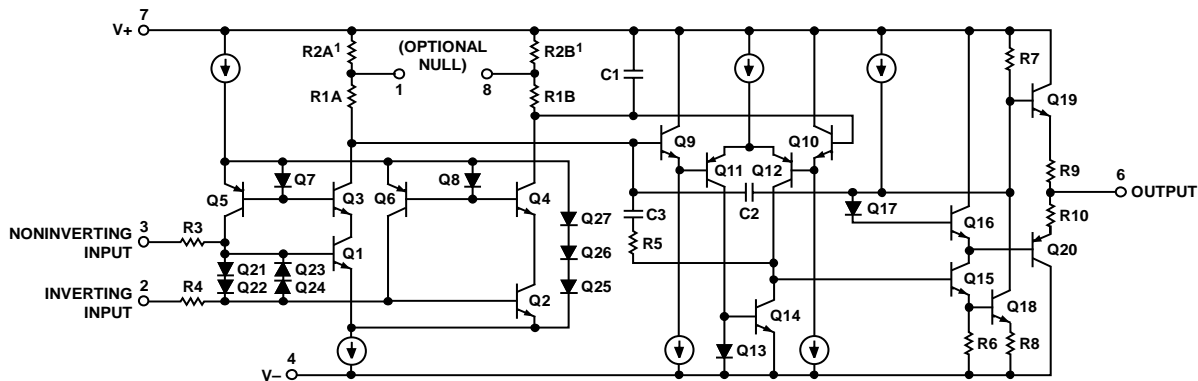
When  $V_{IN} < V_{TH}$ , amplifier output swings negative, reversing the biasing diode D1.  $V_O = V_{TH}$  if  $R_L = \infty$  when  $V_{IN} > V_{TH}$ , the loop closes,

$$V_O = V_{TH} + (V_{IN} - V_{TH}) \left( 1 + \frac{R_F}{R_S} \right)$$

$C_C$  is selected to smooth the response of the loop.

Table 8. Resistor Values

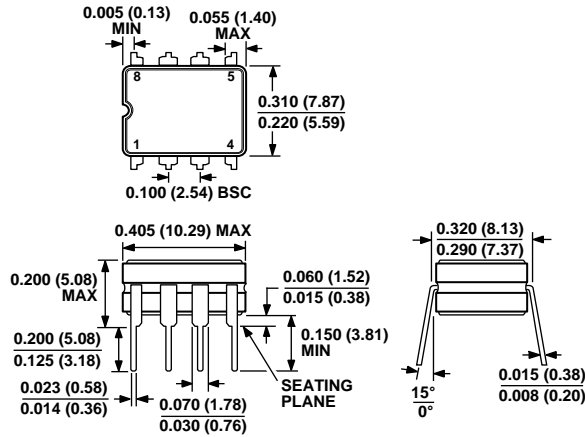
TCV <sub>OUT</sub> Slope (S)	10 mV/°C	100 mV/°C	10 mV/°F
Temperature Range	-55°C to +125°C	-55°C to +125°C	-67°F to +257°C
Output Voltage Range	-0.55 V to +1.25 V	-5.5 V to +12.5V	-0.67 V to +2.57V
Zero-Scale	0 V @ 0°C	0 V @ 0°C	0 V @ 0°F
R <sub>a</sub> (±1% Resistor)	9.09 kΩ	15 kΩ	7.5 kΩ
R <sub>b1</sub> (±1% Resistor)	1.5 kΩ	1.82 kΩ	1.21 kΩ
R <sub>bp</sub> (Potentiometer)	200 Ω	500 Ω	200 Ω
R <sub>c</sub> (±1% Resistor)	5.11 kΩ	84.5 kΩ	8.25 kΩ



<sup>1</sup>R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY.

Figure 38. Simplified Schematic

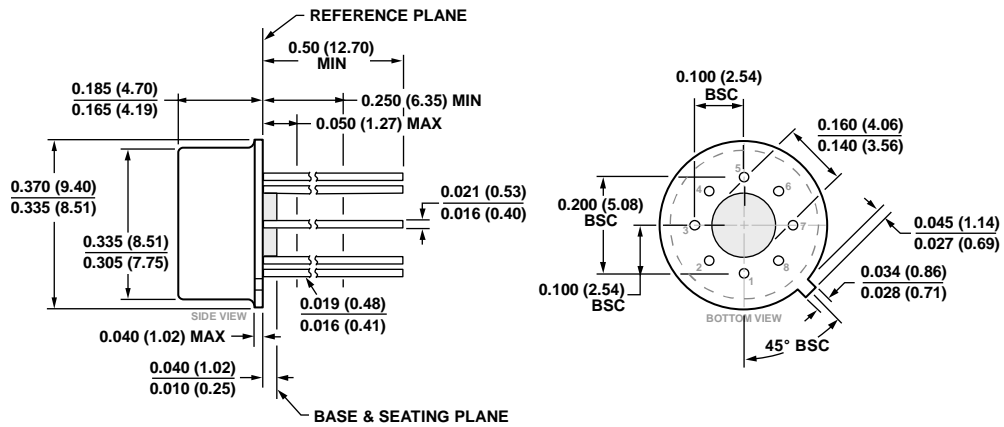
# OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-002-AK  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 40. 8-Pin Metal Header [TO-99] (H-08)

Dimensions shown in inches and (millimeters)

01-15-2015-B

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
OP77FJZ	-25°C to +85°C	8-Pin Metal Header [TO-99]	H-08 (J Suffix)
OP77EZ	-25°C to +85°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8 (Z Suffix)
OP77FZ	-25°C to +85°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8 (Z Suffix)
OP77NBC		Die	

<sup>1</sup> The OP77FJZ is a RoHS compliant part.