

74HC390; 74HCT390

Dual decade ripple counter

Rev. 3 — 16 August 2016

Product data sheet

1. General description

The 74HC390; 74HCT390 is a dual 4-bit decade ripple counter divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections share an asynchronous master reset input (nMR) and can be used in a BCD decade or bi-quinary configuration. If master reset inputs 1MR and 2MR are used to clear all 8 bits of the counter simultaneously, numerous counting configurations are possible within one package. Section clocks $\overline{\text{nCP0}}$ and $\overline{\text{nCP1}}$, allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100. The HIGH-to-LOW transition of the clock inputs $\overline{\text{nCP0}}$ and $\overline{\text{nCP1}}$ trigger each section. For BCD decade operation, the nQ0 output is connected to the $\overline{\text{nCP1}}$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ3 output is connected to the $\overline{\text{nCP0}}$ input and nQ0 becomes the decade output. A HIGH on the nMR input overrides the clocks and sets the four outputs LOW. Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Input levels:
 - ◆ For 74HC390: CMOS level
 - ◆ For 74HCT390: TTL level
- Two BCD decade or bi-quinary counters
- One device can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC390D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT390D				
74HC390DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT390DB				
74HCT390PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

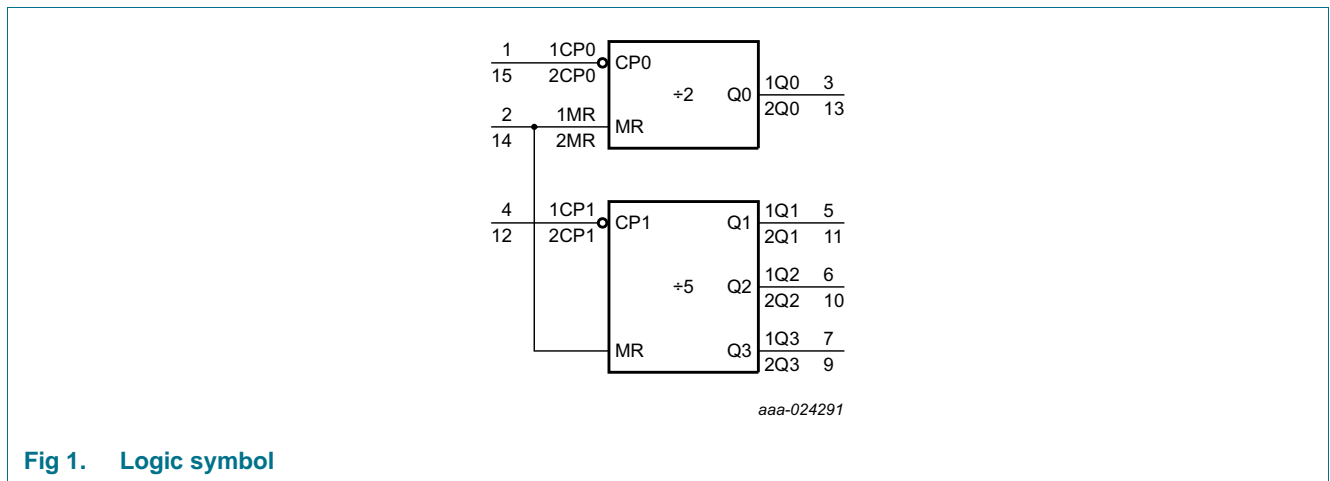


Fig 1. Logic symbol

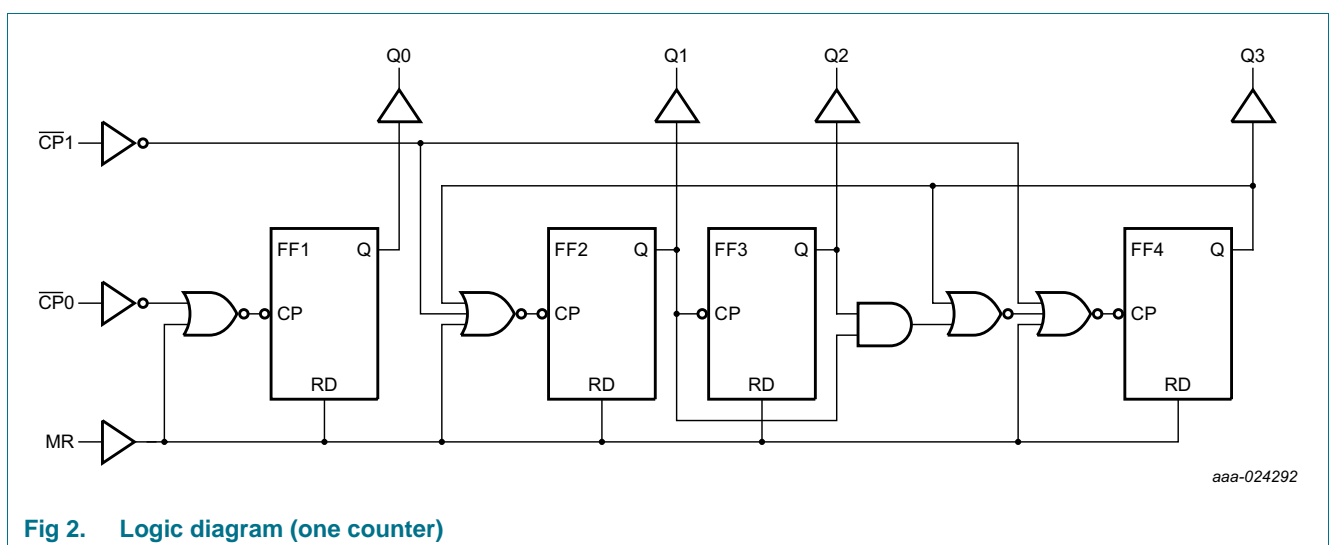


Fig 2. Logic diagram (one counter)

5. Pinning information

5.1 Pinning

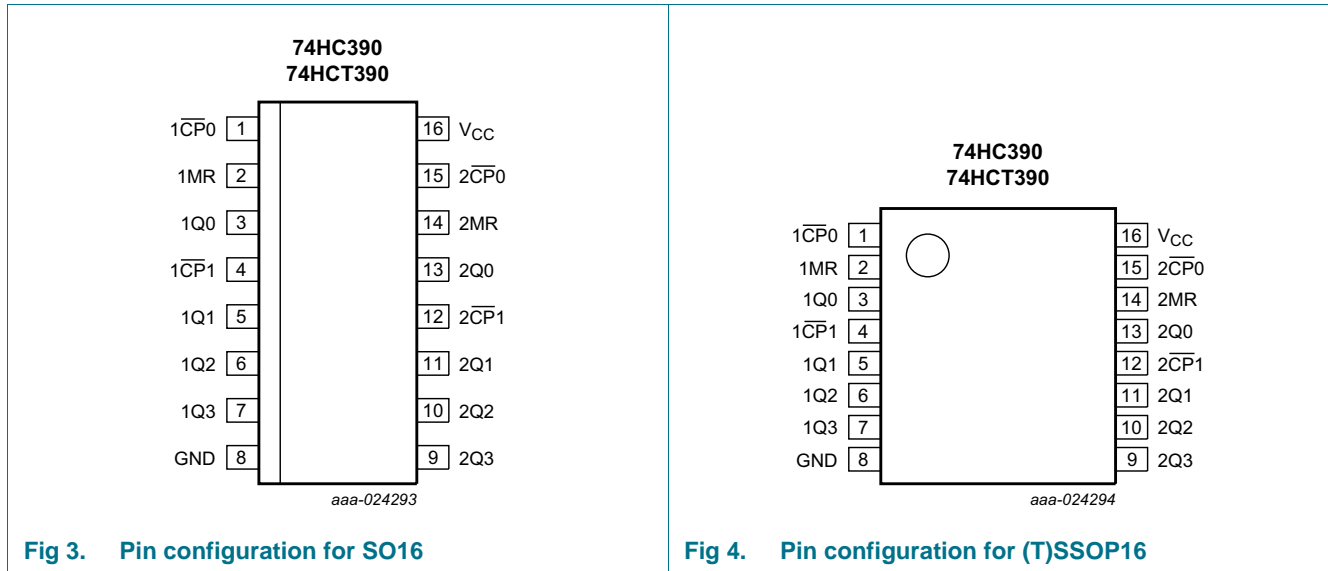


Fig 3. Pin configuration for SO16

Fig 4. Pin configuration for (T)SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1CP0}$, $\overline{2CP0}$	1, 15	clock input divide-by-2 section (HIGH-to-LOW; edge-triggered)
1MR, 2MR	2, 14	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 5, 6, 7	flip-flop outputs
$\overline{1CP1}$, $\overline{2CP1}$	4, 12	clock input divide-by-5 section (HIGH-to-LOW; edge-triggered)
GND	8	ground (0 V)
2Q0, 2Q1, 2Q2, 2Q3	13, 11, 10, 9	flip-flop outputs
V _{CC}	16	supply voltage

6. Functional description

Table 3. BCD count sequence^[1]

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

- [1] Output nQ0 connected to $\overline{\text{nCP1}}$; counter input on $\overline{\text{nCP0}}$.
 H = HIGH voltage level
 L = LOW voltage level

Table 4. Bi-quinary count sequence^[1]

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

- [1] Output nQ3 connected to $\overline{\text{nCP0}}$; counter input on $\overline{\text{nCP1}}$.
 H = HIGH voltage level
 L = LOW voltage level

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO16 and (T)SSOP16 packages [1]	-	500	mW

- [1] For SO16 packages: above 70 °C, the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC390			74HCT390			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC390										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT390										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} − 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		nCP0 inputs	-	45	162	-	202.5	-	220.5	μA
		nCP1, nMR inputs	-	60	216	-	270	-	294	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74HC390										
t_{pd}	propagation delay	$\overline{nCP0}$ to nQ0; see Figure 5 ^[2]								
		$V_{CC} = 2.0$ V	-	47	145	-	180	-	220	ns
		$V_{CC} = 4.5$ V	-	17	29	-	36	-	44	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	25	-	31	-	38	ns
		$\overline{nCP1}$ to nQ1; see Figure 5								
		$V_{CC} = 2.0$ V	-	50	155	-	195	-	235	ns
		$V_{CC} = 4.5$ V	-	18	31	-	39	-	47	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	40	ns
		$\overline{nCP1}$ to nQ2; see Figure 5								
		$V_{CC} = 2.0$ V	-	74	210	-	265	-	315	ns
		$V_{CC} = 4.5$ V	-	27	42	-	53	-	63	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	23	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	22	36	-	45	-	54	ns
		$\overline{nCP1}$ to nQ3; see Figure 5								
$V_{CC} = 2.0$ V	-	50	155	-	195	-	235	ns		
$V_{CC} = 4.5$ V	-	18	31	-	39	-	47	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	14	26	-	33	-	40	ns		
t_{PHL}	HIGH to LOW propagation delay	nMR to nQn; see Figure 6								
		$V_{CC} = 2.0$ V	-	52	165	-	205	-	250	ns
		$V_{CC} = 4.5$ V	-	19	33	-	41	-	50	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	15	28	-	35	-	43	ns
t_t	transition time	nQn; see Figure 5 ^[3]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t_w	pulse width	$\overline{nCP0}$, $\overline{nCP1}$; HIGH or LOW; see Figure 5								
		$V_{CC} = 2.0$ V	80	19	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
		\overline{nMR} HIGH; see Figure 6								
		$V_{CC} = 2.0$ V	80	28	-	105	-	130	-	ns
		$V_{CC} = 4.5$ V	17	10	-	21	-	26	-	ns
t_{rec}	recovery time	\overline{nMR} to \overline{nCPn} ; see Figure 6								
		$V_{CC} = 2.0$ V	75	22	-	95	-	110	-	ns
		$V_{CC} = 4.5$ V	15	8	-	19	-	22	-	ns
		$V_{CC} = 6.0$ V	13	6	-	16	-	19	-	ns
f_{max}	maximum frequency	\overline{nCPn} ; see Figure 5								
		$V_{CC} = 2.0$ V	6.0	20	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5$ V	30	60	-	24	-	20	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	66	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	71	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ ^[4]	-	20	-	-	-	-	-	pF
74HCT390										
t_{pd}	propagation delay	$\overline{nCP0}$ to $\overline{nQ0}$; see Figure 5 ^[2]								
		$V_{CC} = 4.5$ V	-	21	34	-	43	-	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
		$\overline{nCP1}$ to $\overline{nQ1}$; see Figure 5								
		$V_{CC} = 4.5$ V	-	22	38	-	48	-	57	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$\overline{nCP1}$ to $\overline{nQ2}$; see Figure 5								
		$V_{CC} = 4.5$ V	-	30	51	-	64	-	77	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	26	-	-	-	-	-	ns
		$\overline{nCP1}$ to $\overline{nQ3}$; see Figure 5								
t_{PHL}	HIGH to LOW propagation delay	\overline{nMR} to \overline{nQn} ; see Figure 6								
		$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
t_t	transition time	\overline{nQn} ; see Figure 5 ^[3]								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns

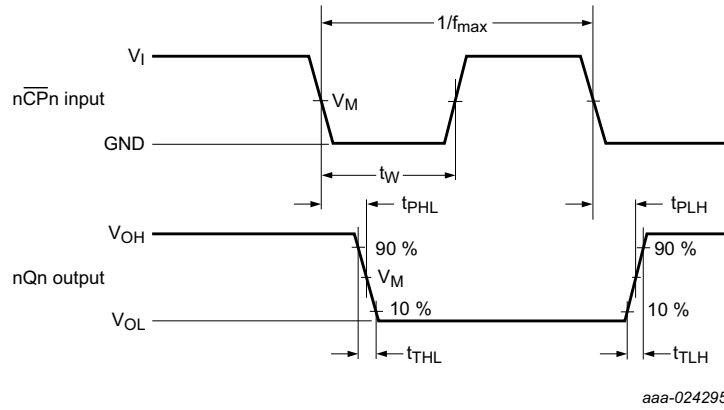
Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t_W	pulse width	$\overline{nCP0}$, $\overline{nCP1}$; HIGH or LOW; see Figure 5								
		$V_{CC} = 4.5$ V	18	8	-	23	-	27	-	ns
		nMR HIGH; see Figure 6								
		$V_{CC} = 4.5$ V	17	10	-	21	-	26	-	ns
t_{rec}	recovery time	nMR to \overline{nCPn} ; see Figure 6								
		$V_{CC} = 4.5$ V	15	8	-	19	-	22	-	ns
f_{max}	maximum frequency	\overline{nCPn} ; see Figure 5								
		$V_{CC} = 4.5$ V	27	55	-	22	-	18	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	61	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC} - 1.5$ V ^[4]	-	21	-	-	-	-	-	pF

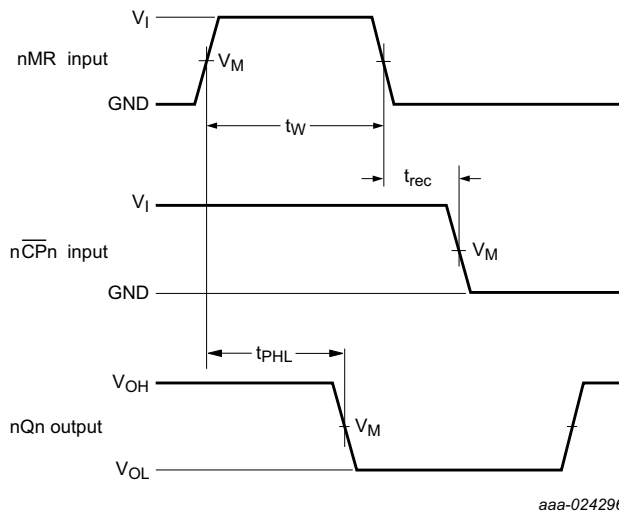
- [1] All typical values are measured at $T_{amb} = 25$ °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_t is the same as t_{THL} and t_{TLH} .
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. The clock input (nCPn) to output (nQn) propagation delays, output transition time, clock pulse width and maximum clock frequency

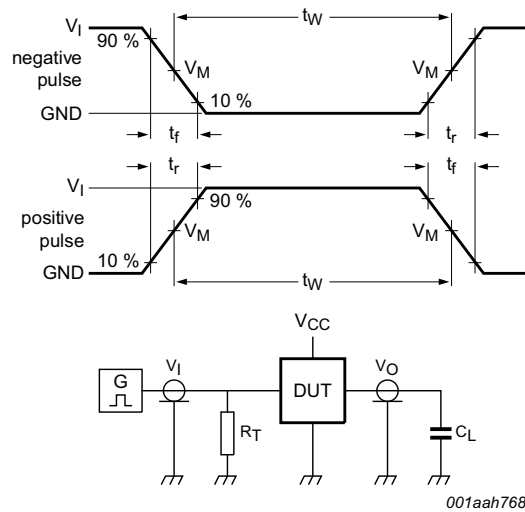


Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The master reset (nMR) pulse width, master reset to output (nQn) propagation delays and master reset to clock (nCPn) recovery time

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC390	$0.5V_{CC}$	$0.5V_{CC}$
74HCT390	1.3 V	1.3 V



001aah768

Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC390	V_{CC}	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT390	3 V	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

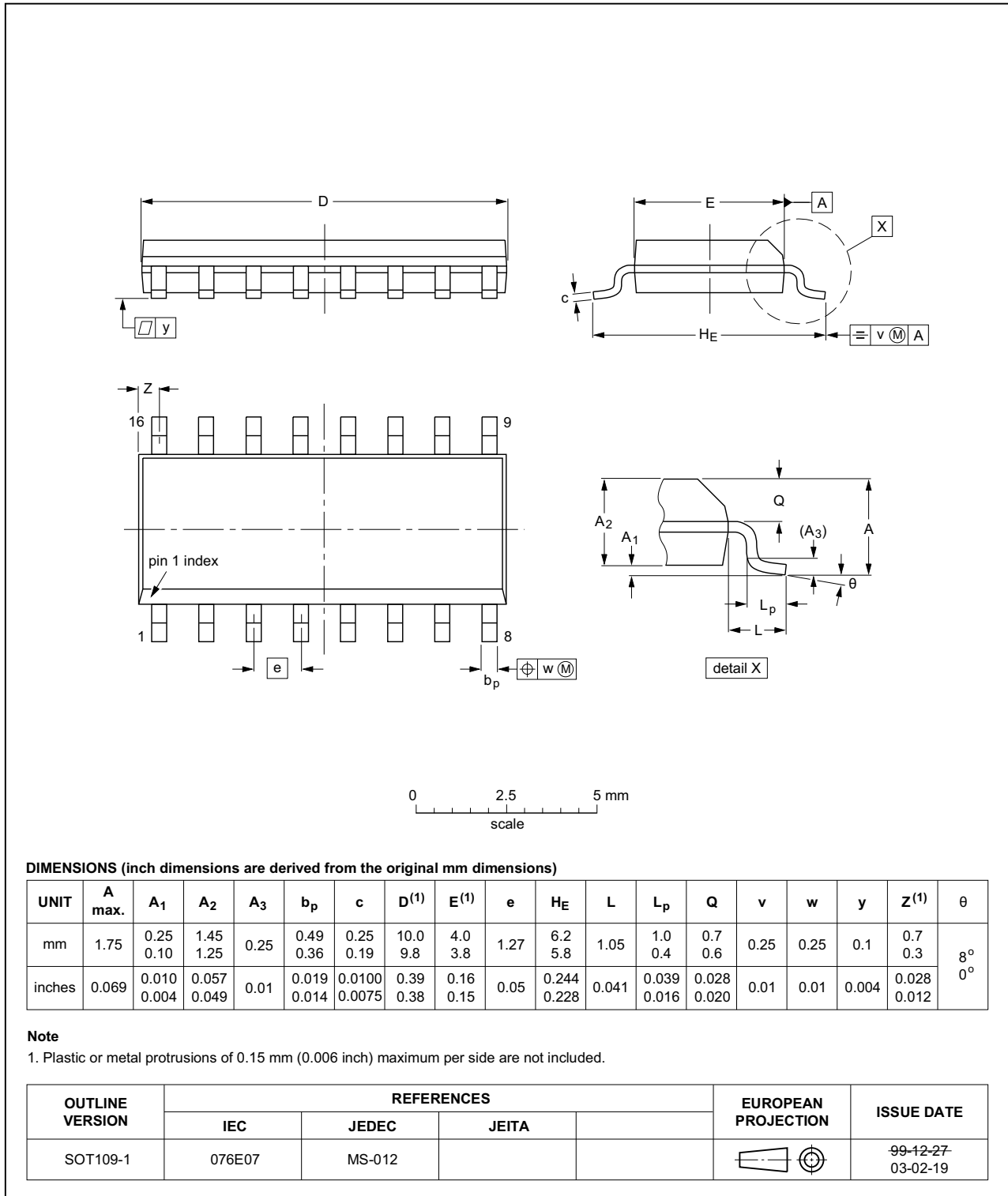


Fig 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

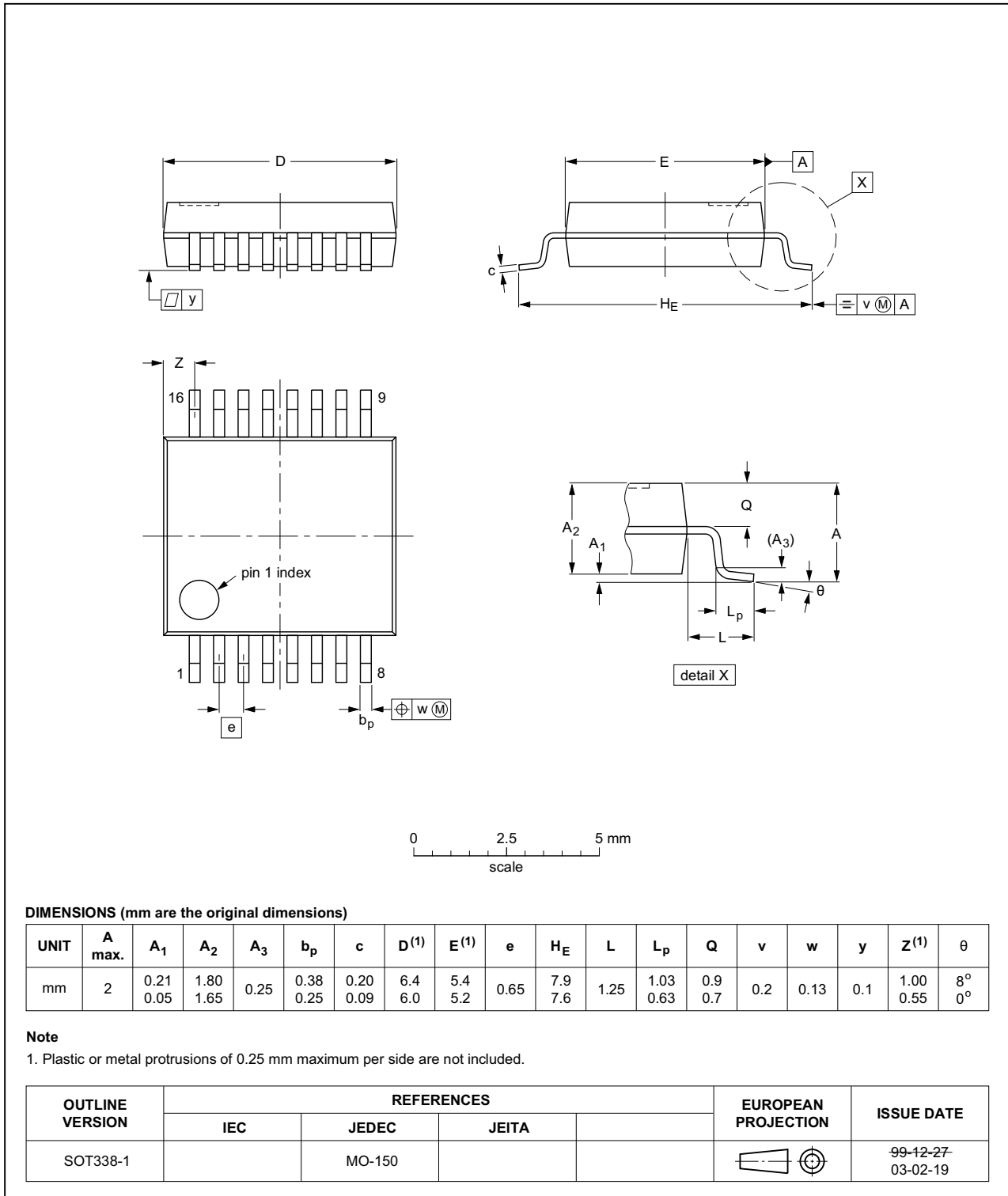


Fig 9. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

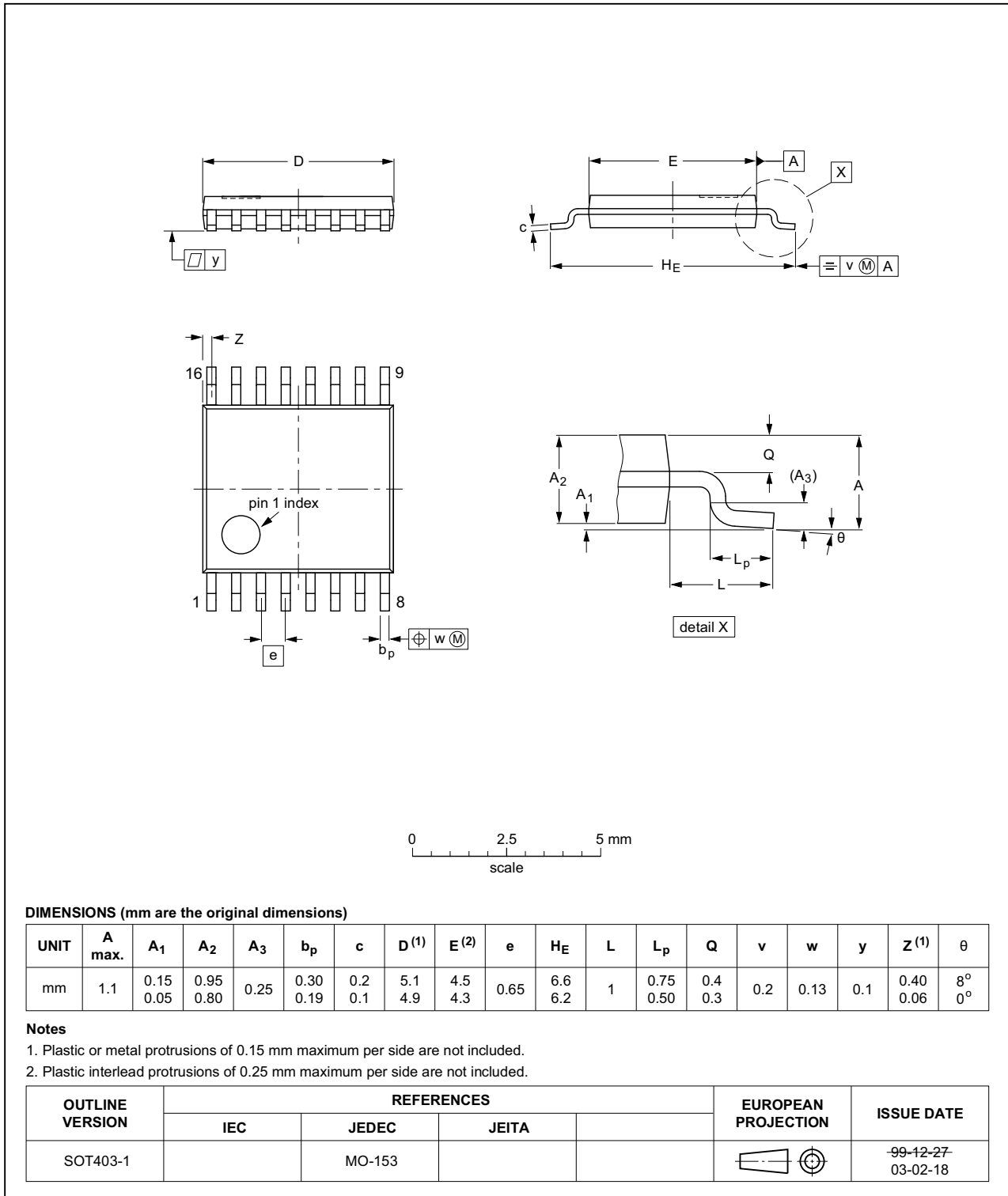


Fig 10. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT390 v.3	20160816	Product data sheet	-	74HC_HCT390_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC390N and 74HCT390N removed. 			
74HC_HCT390_CNV v.2	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	5
8	Recommended operating conditions	5
9	Static characteristics	5
10	Dynamic characteristics	7
11	Waveforms	10
12	Package outline	12
13	Abbreviations	15
14	Revision history	15
15	Legal information	16
15.1	Data sheet status	16
15.2	Definitions	16
15.3	Disclaimers	16
15.4	Trademarks	17
16	Contact information	17
17	Contents	18