

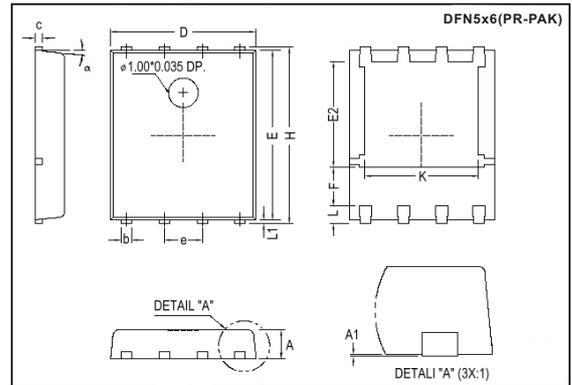
CMS70N04H8-HF

Description

The CMS70N04H8-HF is using trench DOMS technology. This advanced technology has been especially tailored to minimize minimize $R_{DS(ON)}$, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devicesw are well suited for high efficiency fast switching applications.

The CMS70N04H8-HF meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Package Dimensions

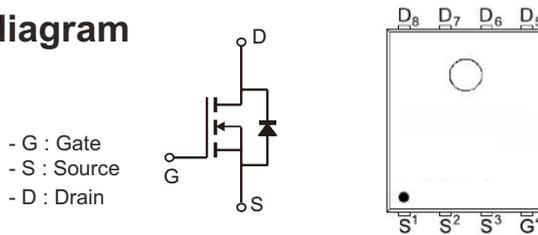


REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.85	1.00	1.15	E	5.70	-	5.90
A1	0.00	-	0.10	e	-	1.27	-
b	0.30	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	L	-	0.60	-
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.10REF.			α	0°	-	12°
E2	3.50REF.			K	3.70	3.90	4.10

Features

- Advanced DMOS trench technology
- Improve dv/dt capability
- Green device available
- Fast switching
- 100% EAS guaranteed

Circuit diagram



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	$I_D @ T_C=25^\circ C$	70	A
	$I_D @ T_C=100^\circ C$	44	A
Pulsed Drain Current ^{1,2}	I_{DM}	280	A
Total Power Dissipation	$P_D @ T_C=25^\circ C$	72.3	W
	$P_D @ T_A=25^\circ C$	2	W
Single Pulse Avalanche Energy, $L=0.1mH^3$	E_{AS}	61	mJ
Single Pulse Avalanche Current, $L=0.1mH^3$	I_{AS}	35	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	°C

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient ²	$R_{\theta JA}$	Steady State	62.5	°C/W
Thermal Resistance Junction-case ²	$R_{\theta JC}$	Steady State	1.73	°C/W

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REV: A

Electrical Characteristics (T_J=25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	40	-	-	V	V _{GS} =0, I _D =250uA
Gate Threshold Voltage	V _{GS(th)}	1.2	1.6	2.5	V	V _{DS} =V _{GS} , I _D =250uA
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} =±20V
Drain-Source Leakage Current(T _J =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =40V, V _{GS} =0
Drain-Source Leakage Current(T _J =85°C)		-	-	10	uA	V _{DS} =32V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{Ds(on)}	-	6.9	8.5	mΩ	V _{GS} =10V, I _D =20A
		-	9.1	12		V _{GS} =4.5V, I _D =10A
Total Gate Charge ²	Q _g	-	19.7	-	nC	I _D =10A
Gate-Source Charge	Q _{gs}	-	2.8	-		V _{DS} =20V
Gate-Drain (“Miller”) Change	Q _{gd}	-	5.1	-		V _{GS} =10V
Turn-on Delay Time ²	T _{d(on)}	-	13.2	-	ns	V _{DD} =15V
Rise Time	T _r	-	2.2	-		I _D =1A
Turn-off Delay Time	T _{d(off)}	-	72	-		V _{GS} =10V
Fall Time	T _f	-	4.5	-		R _G =3.3Ω
Input Capacitance	C _{iss}	-	1278	-	pF	V _{GS} =0V
Output Capacitance	C _{oss}	-	135	-		V _{DS} =25V
Reverse Transfer Capacitance	C _{rss}	-	87	-		f=1.0MHz
Gate Resistance	R _g	-	2.2	-	Ω	f=1.0MHz

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy ⁵	EAS	16	-	-	mJ	V _{DD} =25V, L=0.1mH, I _{AS} =18A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage ²	V _{DS}	-	-	1.2	V	I _S =20A, V _{GS} =0V, T _J =25 °C
Continuous Source Current ^{1,6}	I _S	-	-	70	A	V _G =V _D =0V, Force Current
Pulsed Source Current ^{2,6}	I _{SM}	-	-	140	A	

Notes: 1.The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper.

2.The data tested by pulsed,pulse width ≤ 300us,duty cycle ≤ 2%.

3.The EAS data shows Max. rating. The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=35A.

4.The power dissipation is limited by 150 °C junction temperature.

5. The Min. value is 100% EAS tested guarantee.

6.The data is theoretically the same as I_D and I_{DM},in real applications,should be limited by total power dissipation.

Typical Characteristics

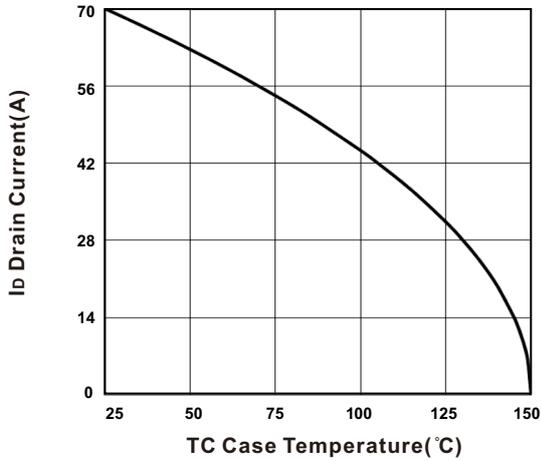


Fig. 1 Drain Current vs. Tc

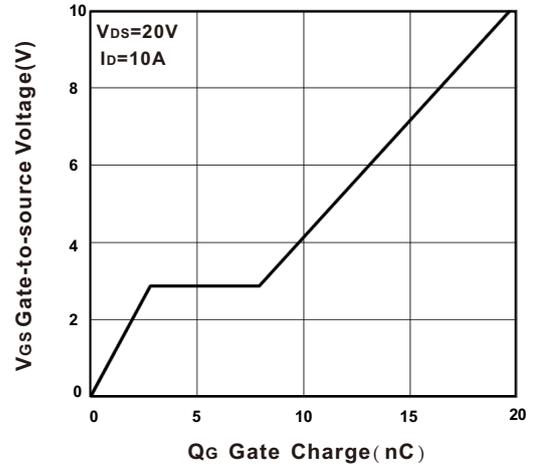


Fig. 2 Gate Charge Characteristics

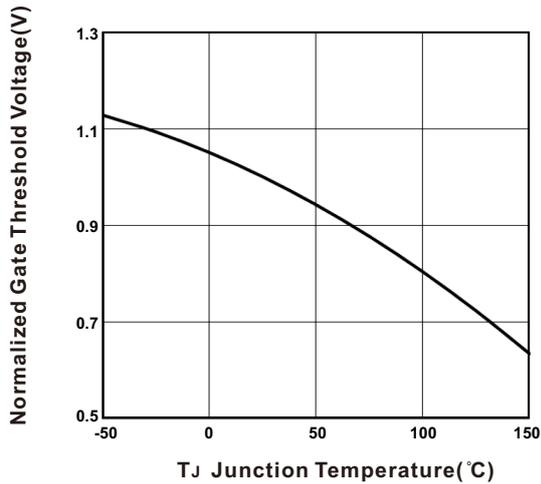


Fig. 3 Normalized $V_{GS(th)}$ VS. T_J

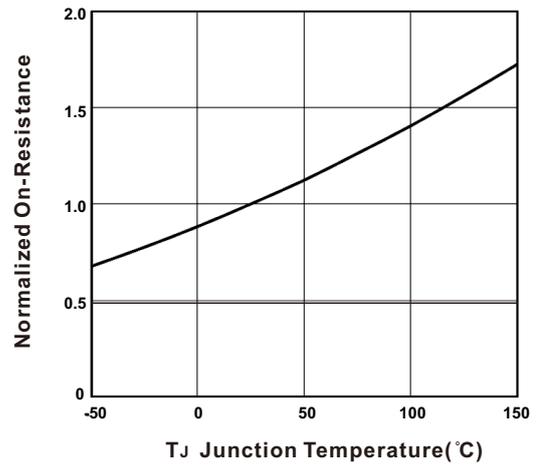


Fig. 4 Normalized $R_{DS(on)}$ VS. T_J

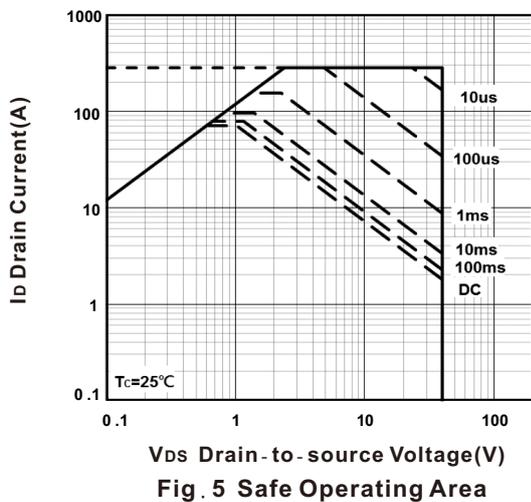


Fig. 5 Safe Operating Area

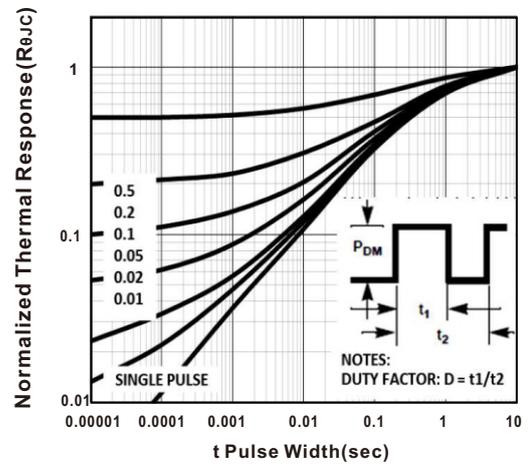


Fig. 6 Transient Thermal Impedance

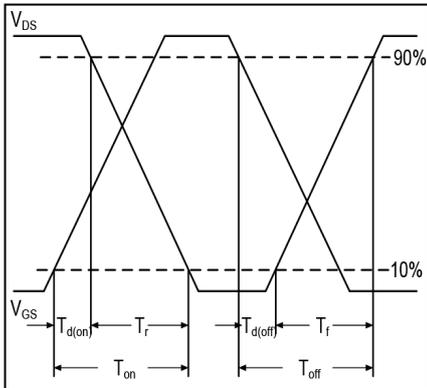


Fig. 7 Switching Time Waveform

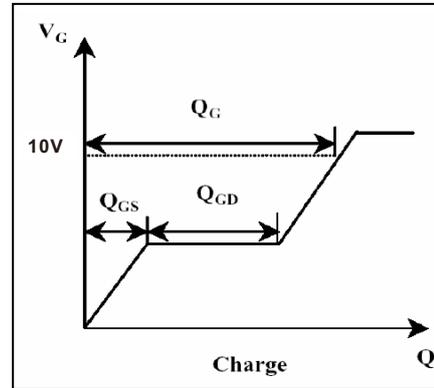
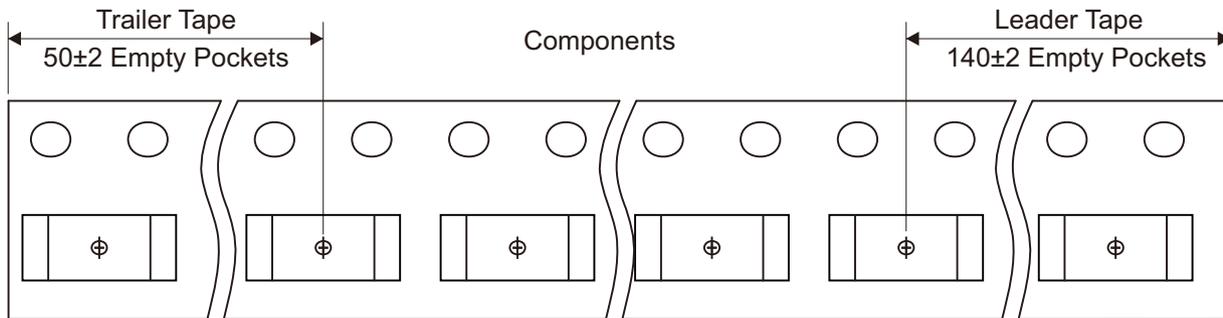
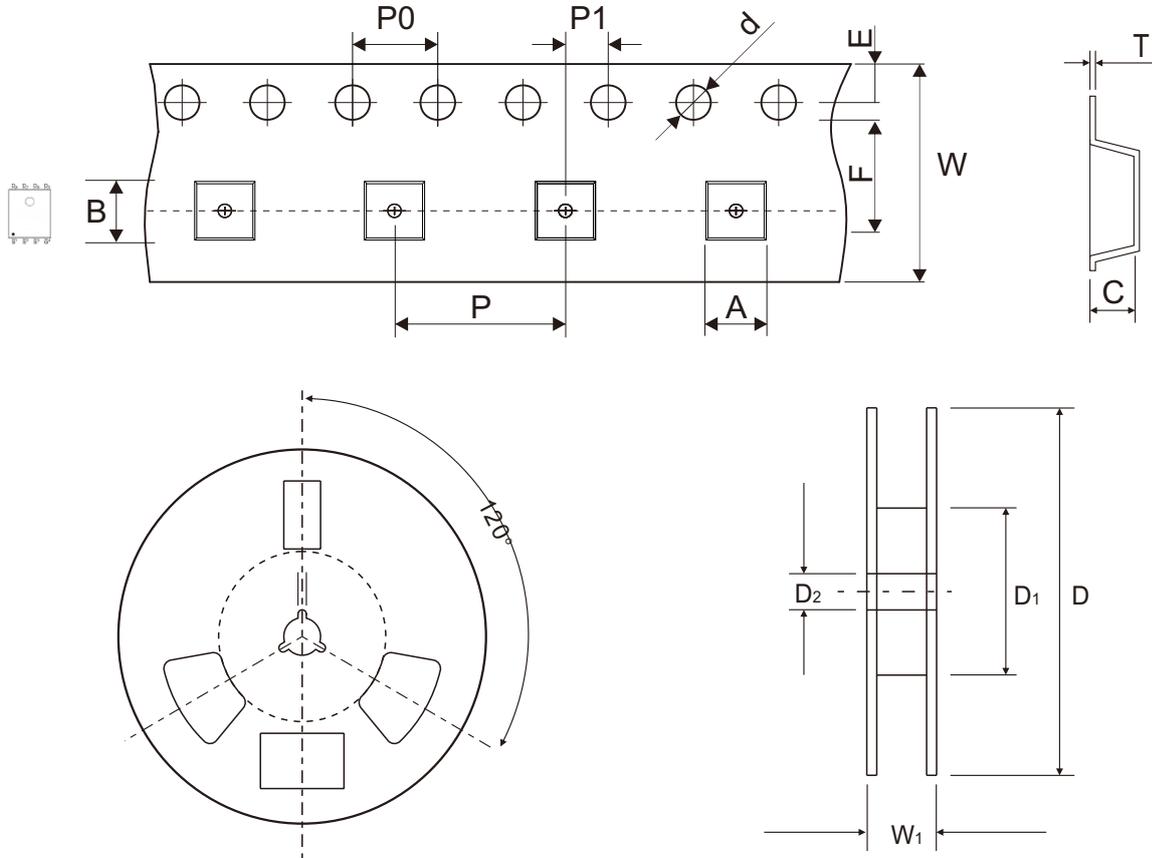


Fig. 8 Gate Charge Waveform

Reel Taping Specification



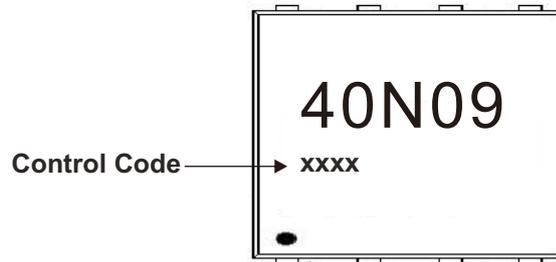
DFN5x6 (PR-PAK)	Symbol	A	B	C	d	D	D1	D2
	(mm)	6.50 ± 0.10	5.30 ± 0.10	1.40 ± 0.10	1.50 ± 0.05	330.00 ± 2.00	178.00 ± 2.00	13.00 ± 1.00
	(inch)	0.256 ± 0.004	0.209 ± 0.004	0.055 ± 0.004	0.059 ± 0.002	12.992 ± 0.079	7.008 ± 0.079	0.512 ± 0.039

DFN5x6 (PR-PAK)	Symbol	E	F	P	P0	P1	T	W	W1
	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 ± 0.30	18.40 ± 1.00
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 ± 0.012	0.724 ± 0.039

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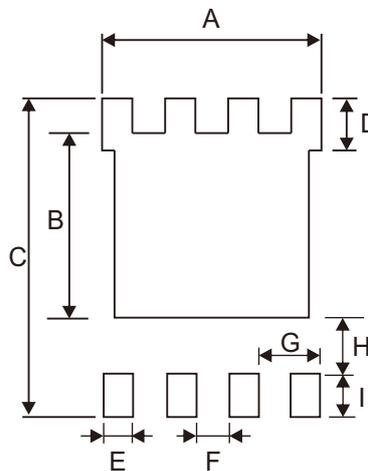
Marking Code

Part Number	Marking Code
CMS70N04H8	40N09



Suggested PAD Layout

Dimensions	Value (in mm)
A	4.420
B	3.810
C	6.610
D	1.020
E	0.610
F	0.660
G	1.270
H	0.820
I	1.270



Note:

1. The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
DFN5x6 (PR-PAK)	3,000	13