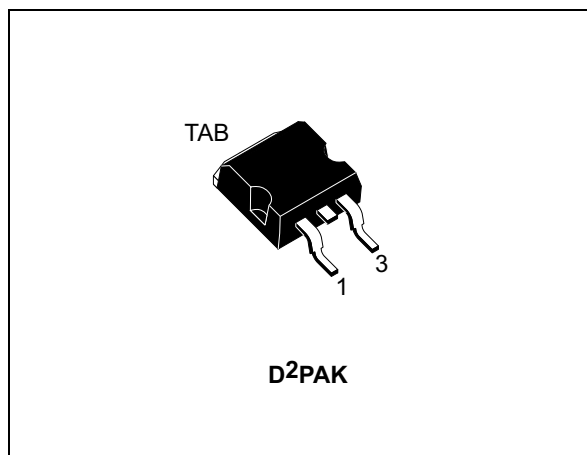


N-channel 60 V, 4.7 mΩ typ., 100 A STripFET™ F7 Power MOSFET in a D²PAK package

Datasheet - production data



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB100N6F7	60 V	5.6 mΩ	100A	125 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Figure 1. Internal schematic diagram

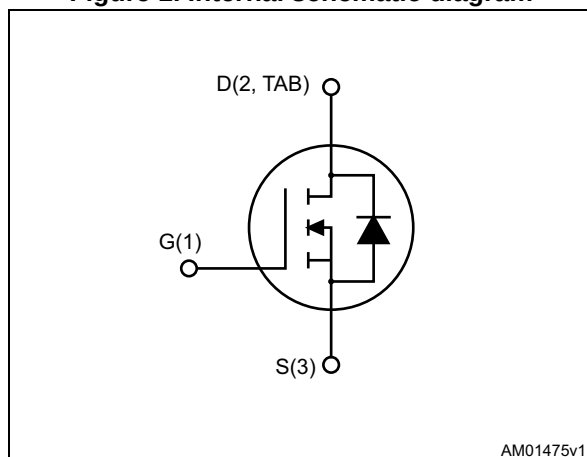


Table 1. Device summary

Order code	Marking	Package	Packaging
STB100N6F7	100N6F7	D ² PAK	Tape and Reel

Contents

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3 **Test circuits** 8

4 **Package information** 9

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	100	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	75	A
$I_{DM}^{(1)}$	Drain current (pulsed)	400	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	125	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	200	mJ
T_j	Operating junction temperature	- 55 to 175	°C
T_{stg}	Storage temperature		

1. Pulse width is limited by safe operating area

2. Starting $T_j = 25\text{ °C}$, $I_D = 20\text{ A}$, $V_{DD} = 30\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.2	°C/W
$R_{thj-pcb}^{(1)}$	thermal resistance junction-pcb	35	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	60			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$			100	μA
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 50\text{ A}$		4.7	5.6	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$	-	1980	-	pF
C_{oss}	Output capacitance		-	970	-	pF
C_{rss}	Reverse transfer capacitance		-	86	-	pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 100\text{ A}$, $V_{GS} = 10\text{ V}$	-	30	-	nC
Q_{gs}	Gate-source charge		-	12.6	-	nC
Q_{gd}	Gate-drain charge		-	5.9	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 50\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	21.6	-	ns
t_r	Rise time		-	55.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	28.6	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 100\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 100\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 48\text{ V}$	-	48.4		ns
Q_{rr}	Reverse recovery charge		-	47		nC
I_{RRM}	Reverse recovery current		-	2.0		A

1. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

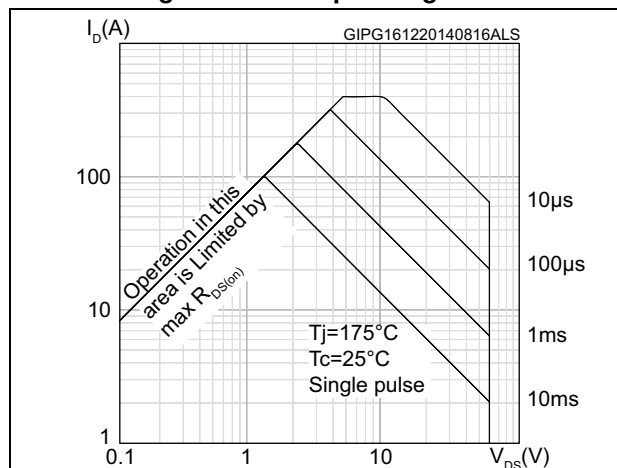


Figure 3. Thermal impedance

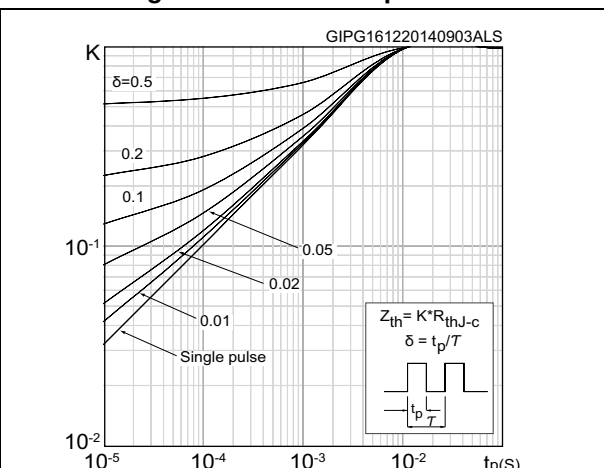


Figure 4. Output characteristics

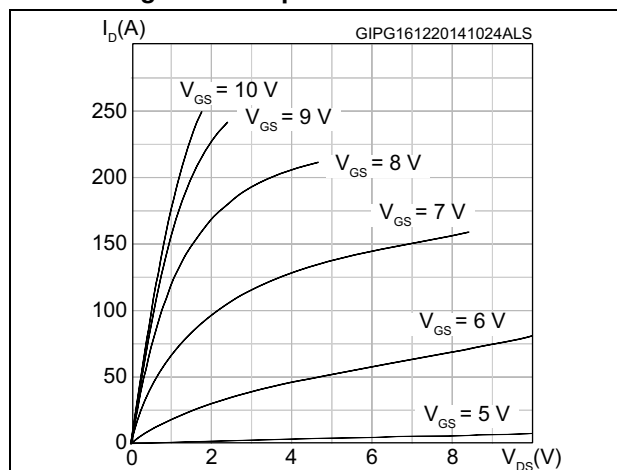


Figure 5. Transfer characteristics

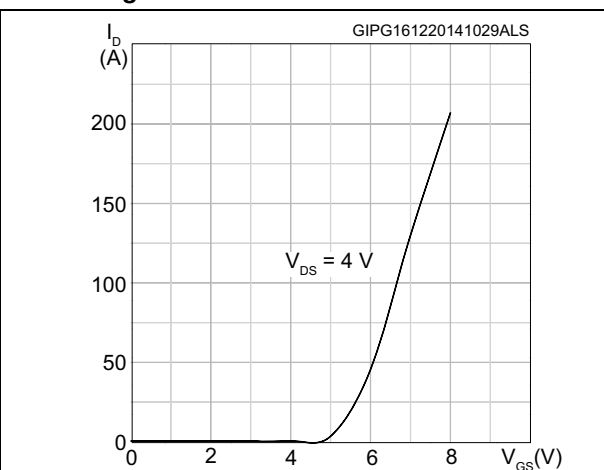


Figure 6. Gate charge vs gate-source voltage

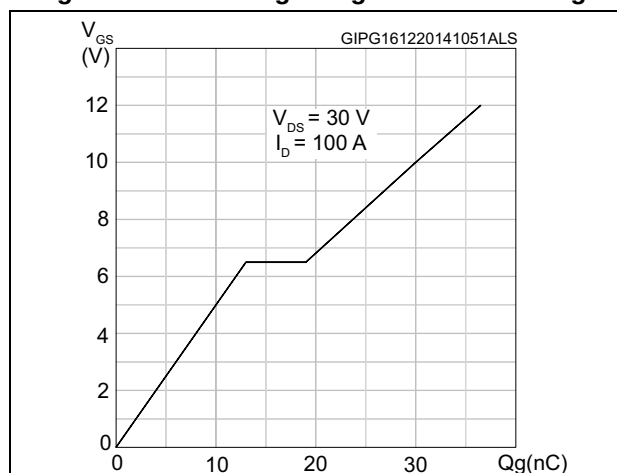


Figure 7. Static drain-source on-resistance

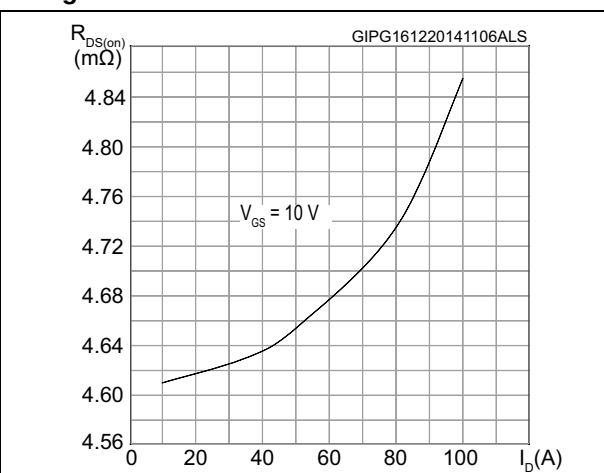


Figure 8. Capacitance variations

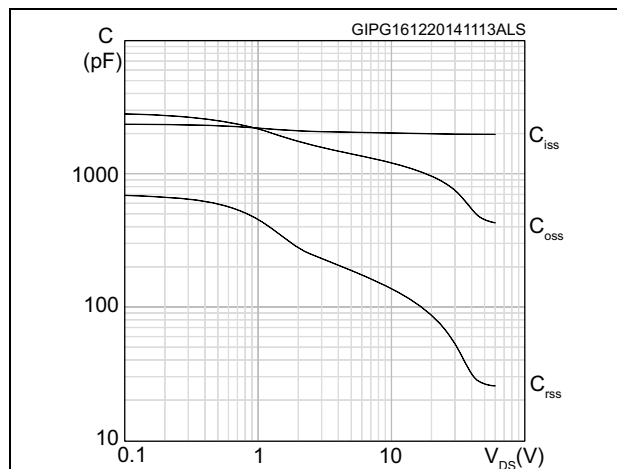


Figure 9. Normalized gate threshold voltage vs temperature

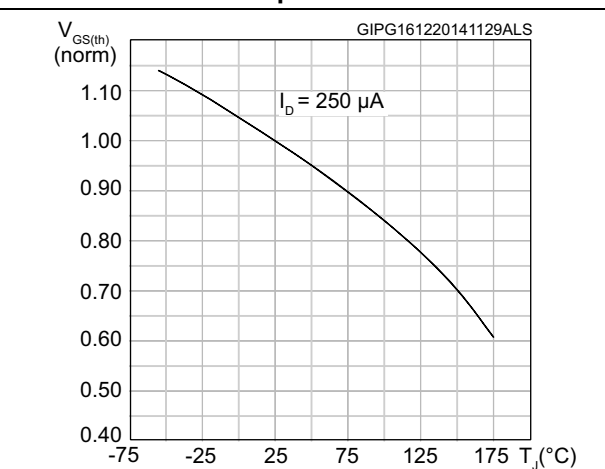


Figure 10. Normalized on-resistance vs temperature

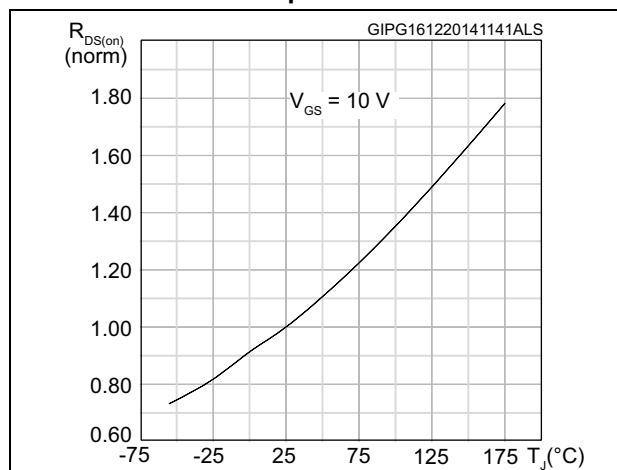
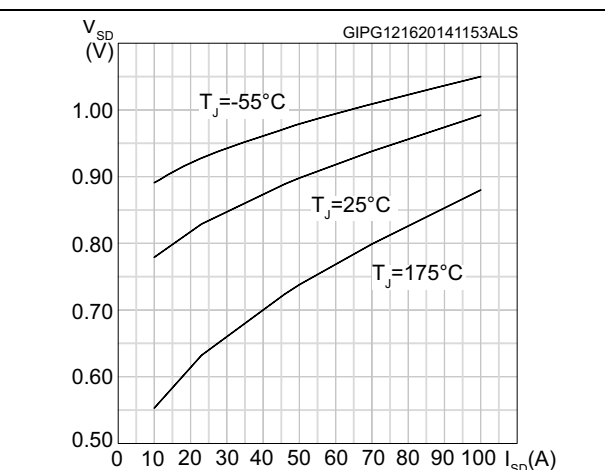
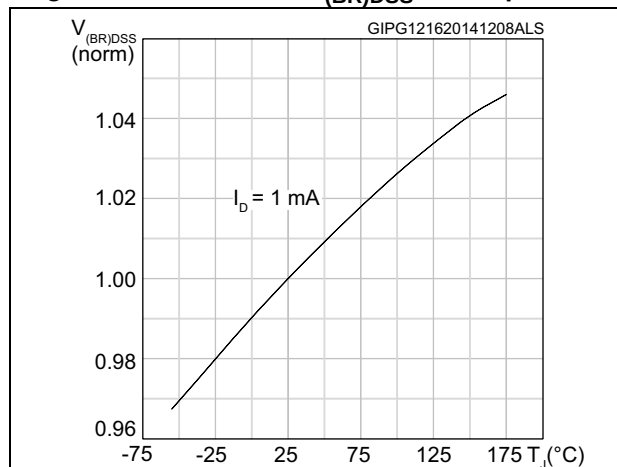


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

3 Test circuits

Figure 13. Switching times test circuit for resistive load

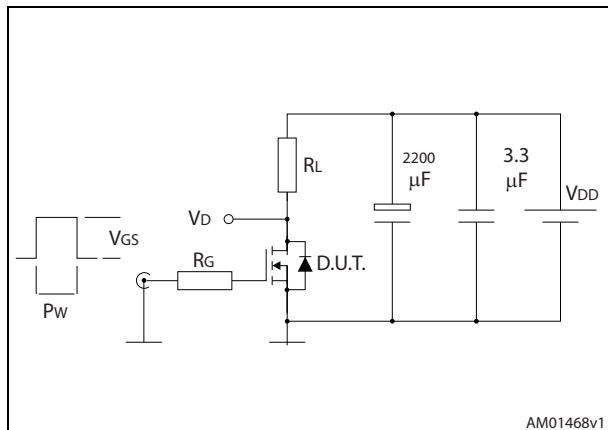


Figure 14. Gate charge test circuit

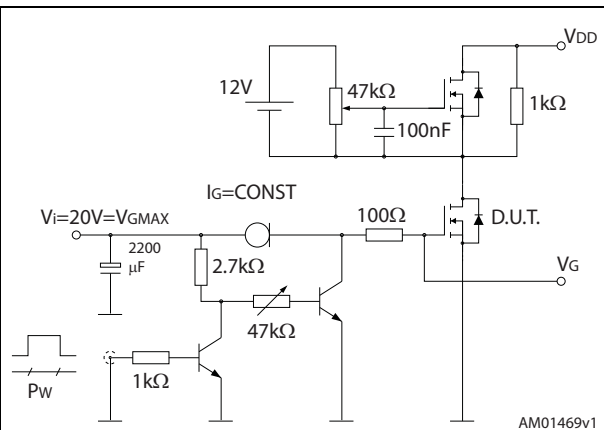


Figure 15. Test circuit for inductive load switching and diode recovery times

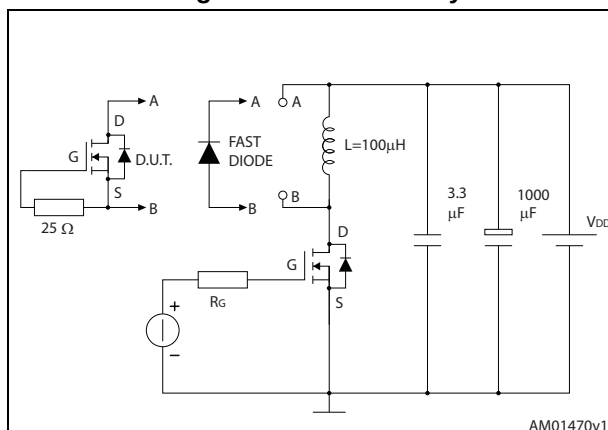


Figure 16. Unclamped inductive load test circuit

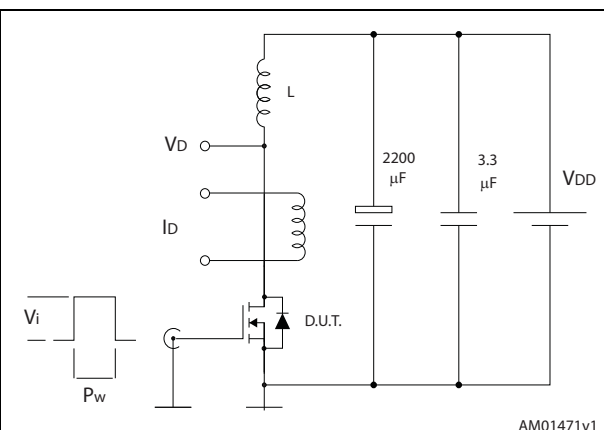


Figure 17. Unclamped inductive waveform

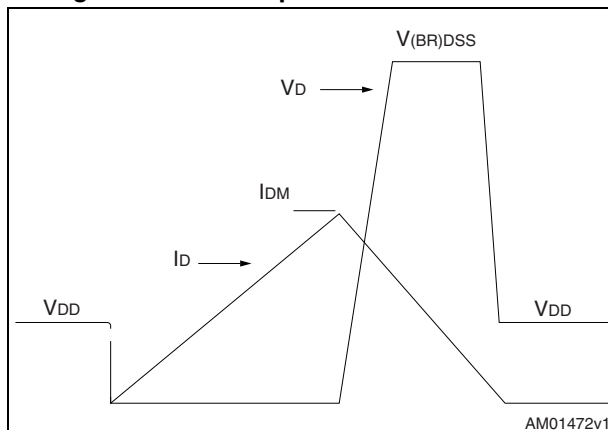
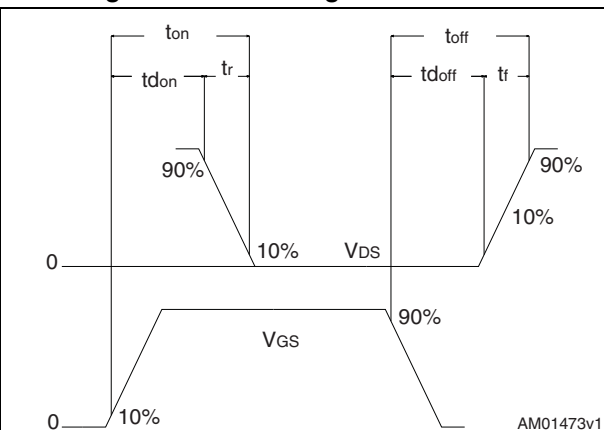


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 19. D²PAK (TO-263) package outline

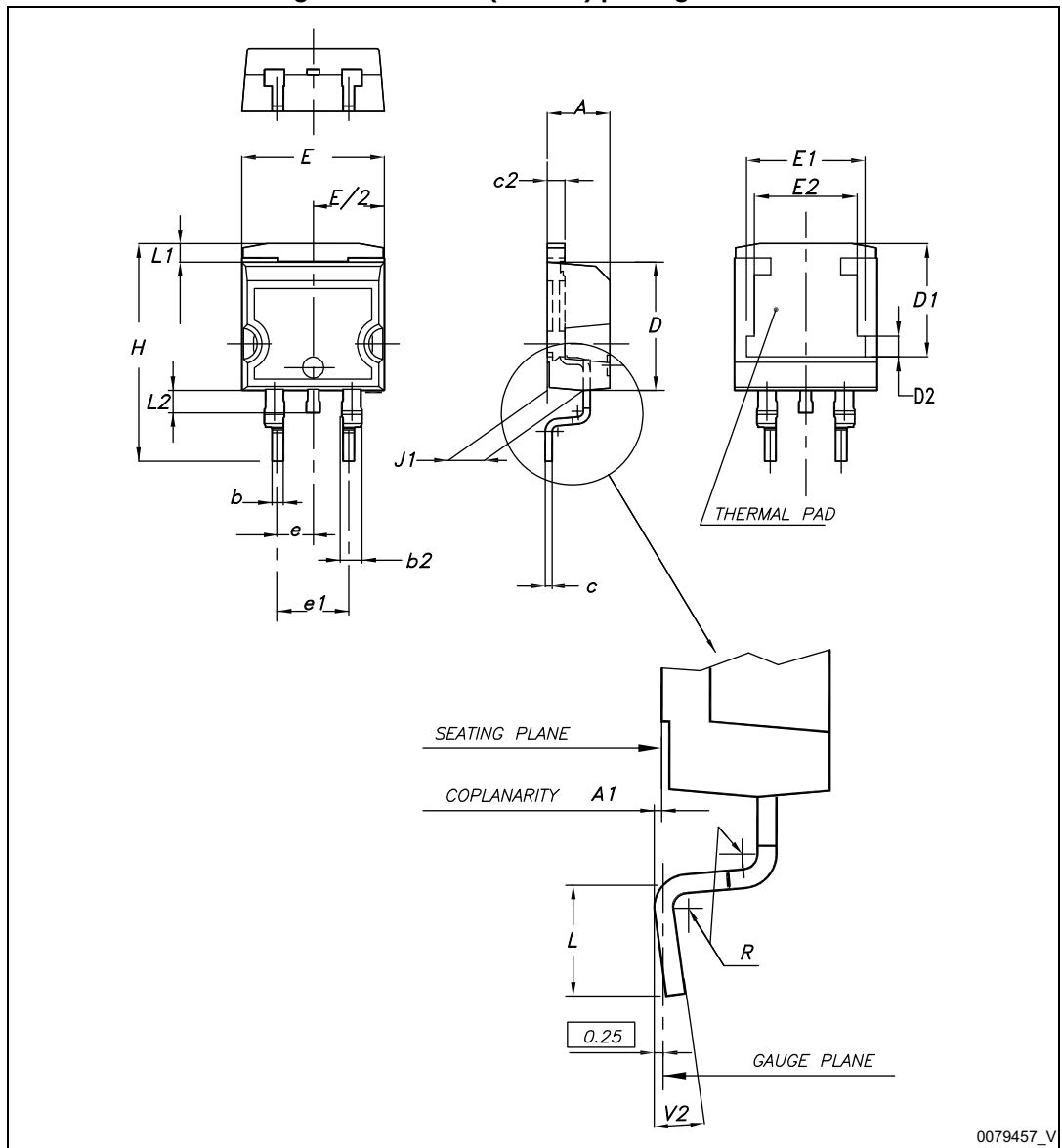
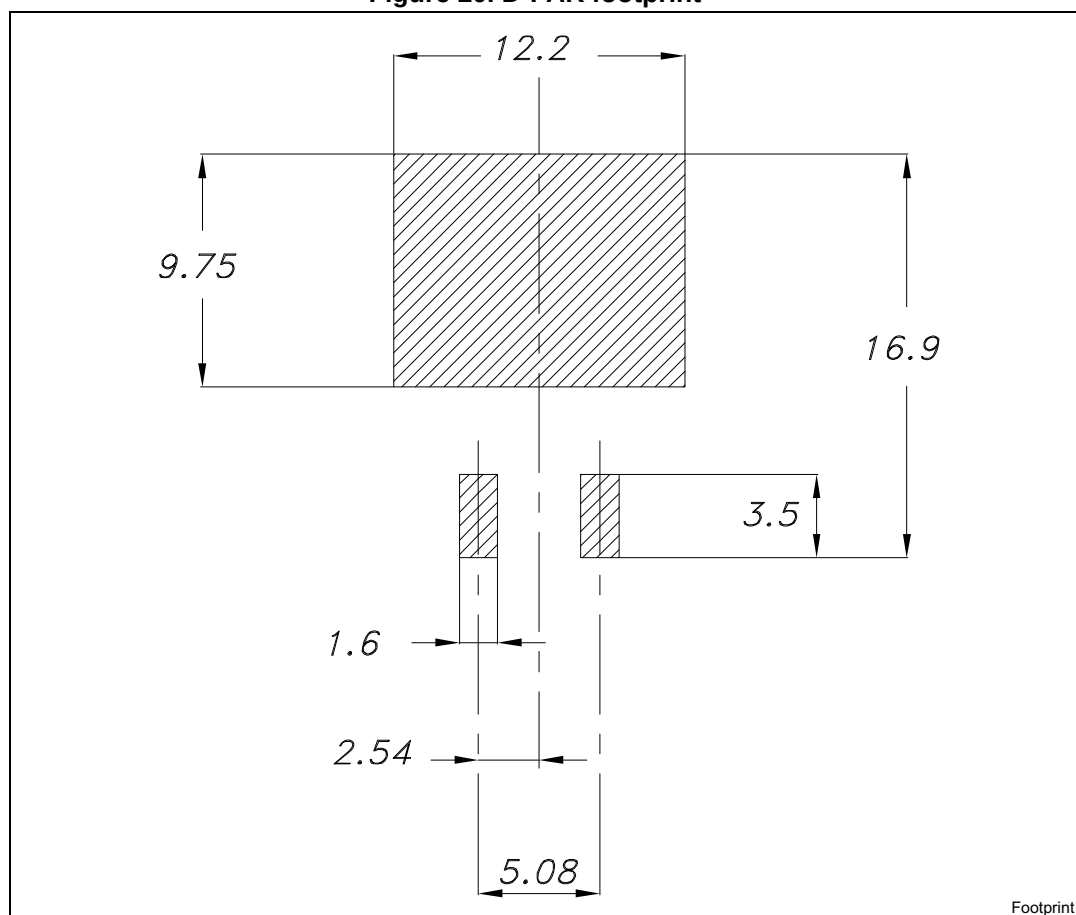


Table 8. D²PAK (TO-263) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D²PAK footprint^(a)

a. All dimension are in millimeters

5 Packing information

Figure 21. Tape

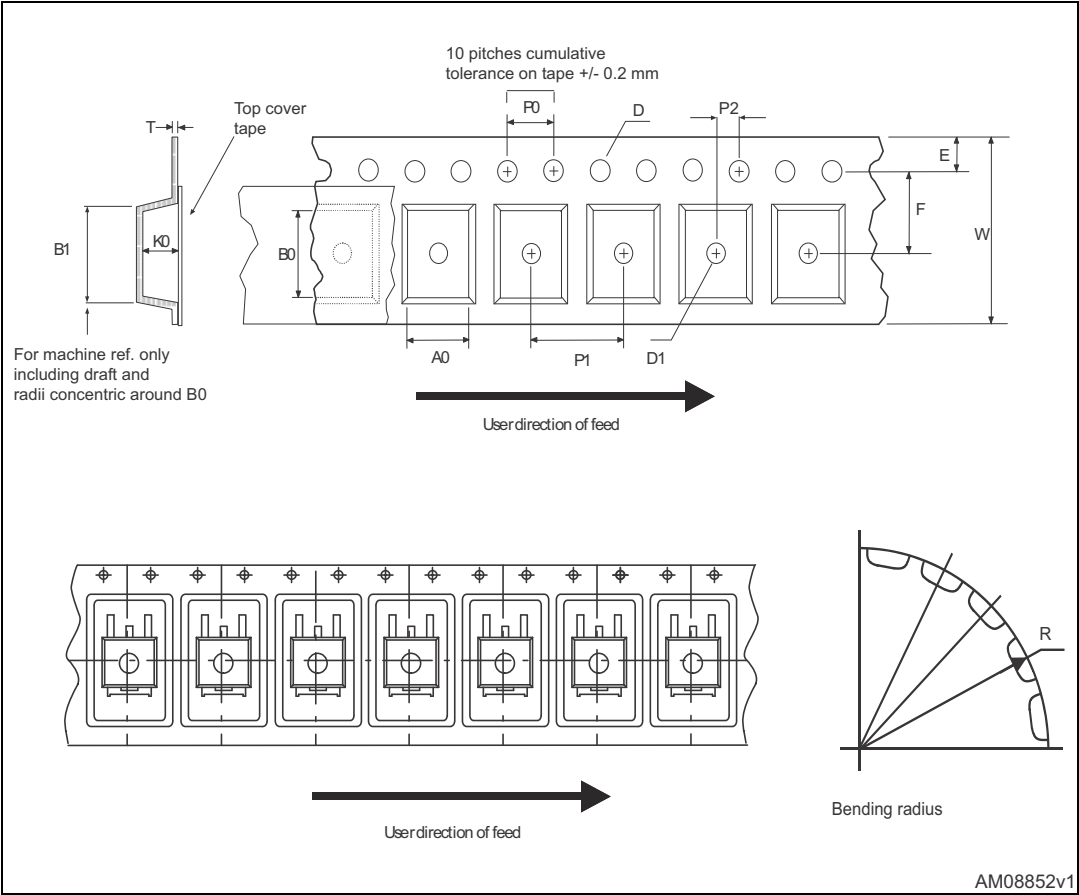
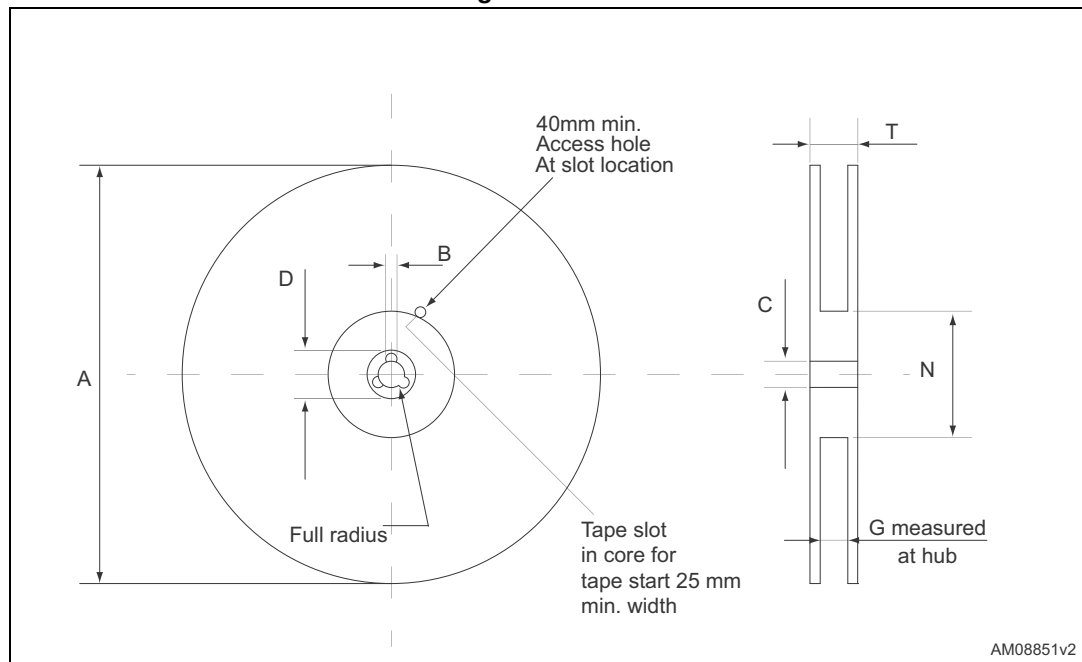


Figure 22. Reel

Table 9. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Nov-2014	1	First release.
14-Jan-2015	2	Text amendments throughout document On cover page: Changed title description Changed features and descriptions Updated Table 2: Absolute maximum ratings Updated Table 4: On/off states Updated Table 5: Dynamic Updated Table 6: Switching times Updated Table 7: Source drain diode Added Section 2.1: Electrical characteristics (curves) Updated Section 4: Package mechanical data
15-Dec-2015	3	Updated Table 3: Thermal data . Minor text changes.

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