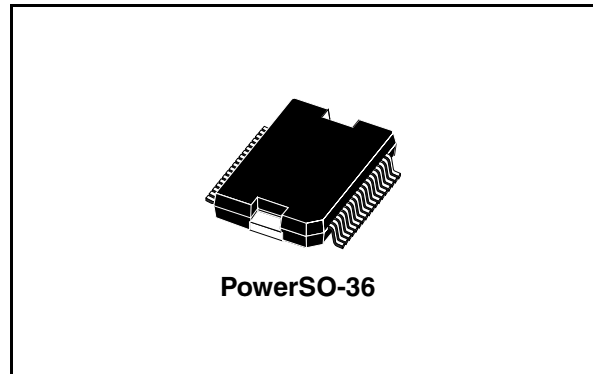


Intelligent quad (2 x 5A / 2 x 2.5A) low-side switch

Features

- Quad low-side switch
- 2 x 5 A designed as conventional switch
- 2 x 2.5 A designed as switched current-regulator
- Low ON-resistance 4 x 0.2 Ω (typ.)
- PowerSO-36 - package with integrated cooling area
- Integrated free-wheeling and clamping Z-diodes
- Output slope control
- Short circuit protection
- Selective overtemperature shutdown
- Open load detection
- Ground and supply loss detection
- External clock control
- Recirculation control
- Regulator drift detection
- Regulator error control
- Status monitoring



- status push-pull stages
- Electrostatic discharge (ESD) protection

Description

The L9352B is an integrated quad low-side power switch to drive inductive loads like valves used in ABS systems. Two of the four channels are current regulators with current range from 0 mA to 2.25 A.

All channels are protected against fail functions. They are monitored by a status output.

Table 1. Device summary

| Order code | Package ⁽¹⁾ | Packing |
|--------------|------------------------|---------------|
| L9352B-LF | PowerSO-36 | Tray |
| L9352B-TR-LF | PowerSO-36 | Tape and reel |

1. ECOPACK® package (see [Section 6: Package information](#)).

Contents

- 1 Block diagram 5**
- 2 Pins description 6**
- 3 Electrical specifications 8**
 - 3.1 Absolute maximum ratings 8
 - 3.2 Thermal data 9
 - 3.3 Operating range 9
 - 3.4 Electrical characteristics 10
- 4 Functional description 13**
 - 4.1 Overview 13
 - 4.2 Input circuits 13
 - 4.3 Output stages (not regulated) channel 1 and 2 13
 - 4.4 Current-regulator-stages channel 3 and 4 13
 - 4.5 Protective circuits 15
 - 4.6 Error detection 15
 - 4.7 Drift detection (regulated channels only) 17
 - 4.8 Other test modes 17
 - 4.9 Diagnostic 18
- 5 Timing diagrams 19**
 - 5.1 Non regulated channels 19
 - 5.2 Regulated channels (timing diagrams of diagnostic with 2kHz PWM input signal) 22
- 6 Package information 25**
- 7 Revision history 26**

List of tables

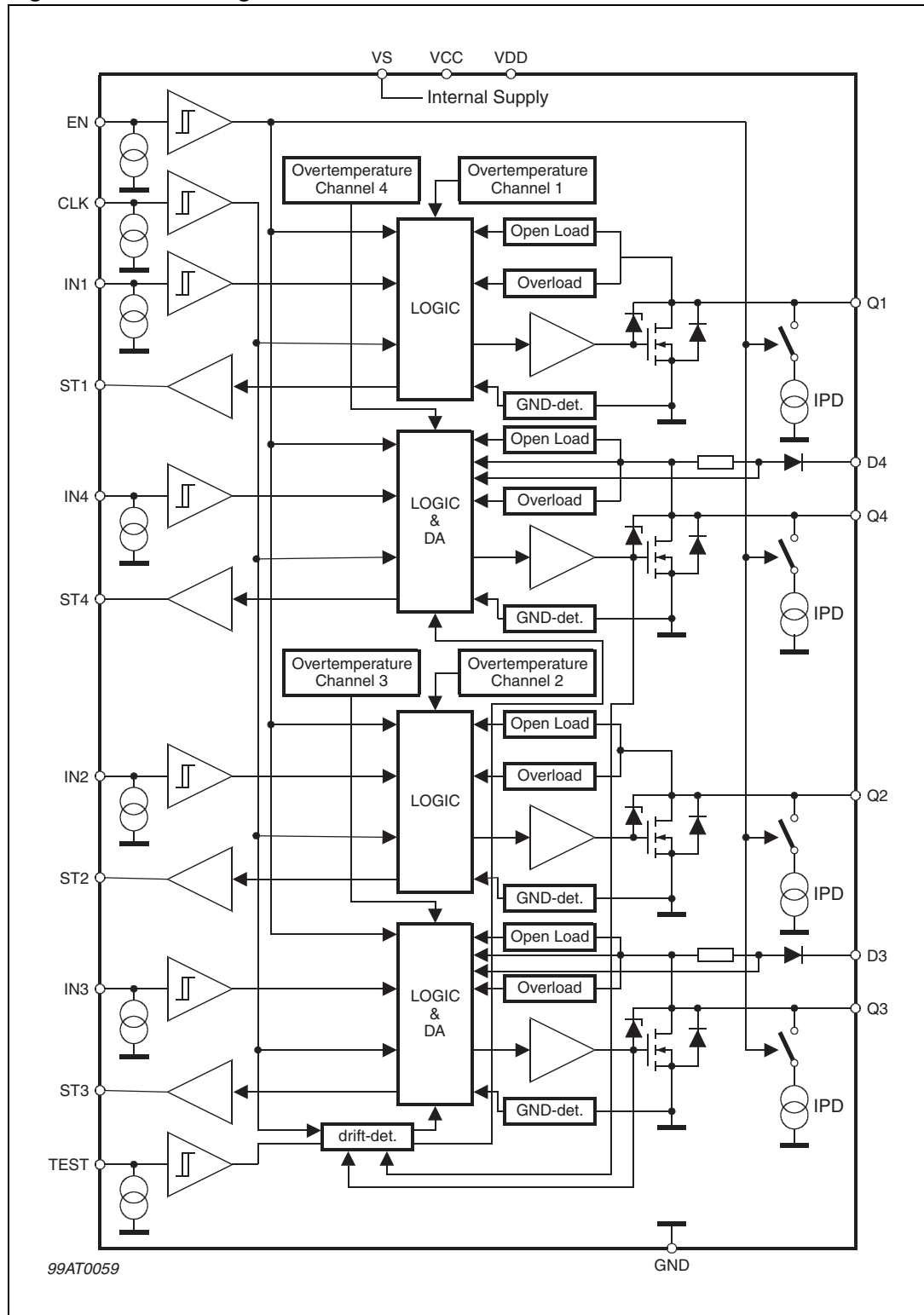
| | | |
|-----------|---|----|
| Table 1. | Device summary | 1 |
| Table 2. | Pins description | 6 |
| Table 3. | Absolute maximum ratings | 8 |
| Table 4. | Thermal data | 9 |
| Table 5. | Operating range | 9 |
| Table 6. | Electrical characteristics | 10 |
| Table 7. | Error detection | 15 |
| Table 8. | Special test mode functionality | 17 |
| Table 9. | Diagnostic | 18 |
| Table 10. | Document revision history | 26 |

List of figures

| | | |
|------------|--|----|
| Figure 1. | Block diagram | 5 |
| Figure 2. | Pins connection (top view) | 6 |
| Figure 3. | Input PWM to output current range. | 14 |
| Figure 4. | Current accuracy according to the input and clock frequency ratio | 14 |
| Figure 5. | Output slope, resistive load | 19 |
| Figure 6. | Overload switch-off delay | 19 |
| Figure 7. | Normal condition, resistive load, pulsed input signal | 20 |
| Figure 8. | Current overload | 20 |
| Figure 9. | Diagnostic status output at different open load current conditions | 21 |
| Figure 10. | Pulsed open load conditions (regulated and non-regulated channels). | 22 |
| Figure 11. | Normal condition, inductive load | 22 |
| Figure 12. | Current overload | 23 |
| Figure 13. | Recirculation error | 23 |
| Figure 14. | Current regulation error (e.g. as a result of voltage reduction) | 24 |
| Figure 15. | Over temperature | 24 |
| Figure 16. | Test mode 4 | 24 |
| Figure 17. | PowerSO-36 mechanical data and package dimensions | 25 |

1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

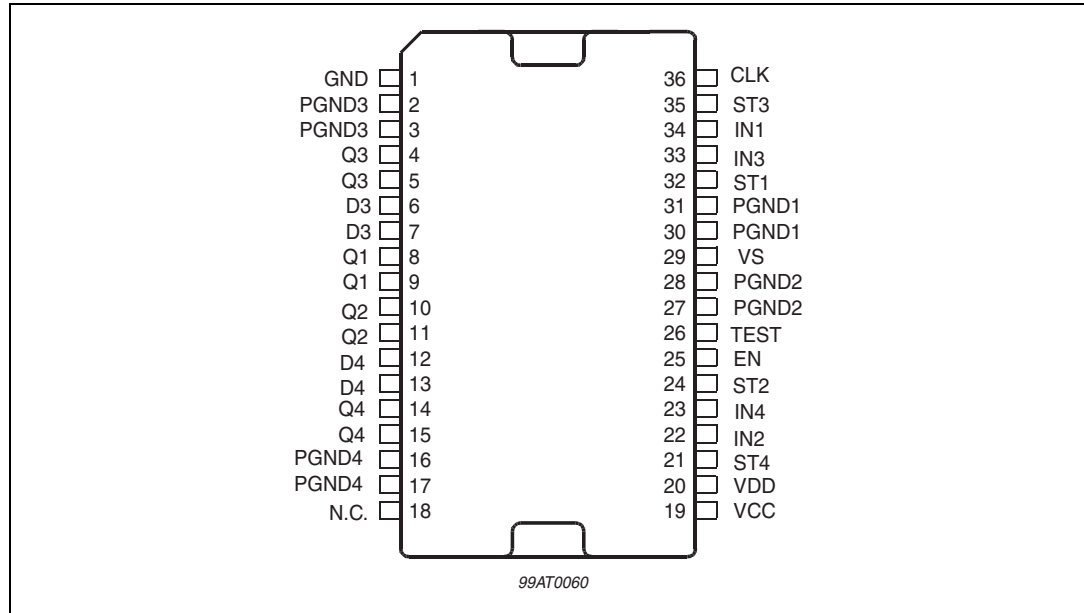


Table 2. Pins description

| N° | Pin | Description |
|--------|-------|------------------------------------|
| 1 | GND | Logic ground |
| 2, 3 | PGND3 | Power ground - Channel 3 |
| 4, 5 | Q3 | Power output - Channel 3 |
| 6, 7 | D3 | Free-wheeling diode - Channel 3 |
| 8, 9 | Q1 | Power output - Channel 1 |
| 10, 11 | Q2 | Power output - Channel 2 |
| 12, 13 | D4 | Free-wheeling diode - Channel 4 |
| 14, 15 | Q4 | Power output - Channel 4 |
| 16, 17 | PGND4 | Power ground - Channel 4 |
| 18 | NC | Not Connected |
| 19 | VCC | 5 V supply |
| 20 | VDD | 5 V supply |
| 21 | ST4 | Status output - Channel 4 |
| 22 | IN2 | Control input - Channel 2 |
| 23 | IN4 | Control input - Channel 4 |
| 24 | ST2 | Status output - Channel 2 |
| 25 | EN | Enable input for all four channels |

Table 2. Pins description (continued)

| N° | Pin | Description |
|-----------|------------|----------------------------------|
| 26 | TEST | Enable input for drift detection |
| 27, 28 | PGND2 | Power ground - Channel 2 |
| 29 | VS | Supply voltage |
| 30, 31 | PGND1 | Power ground - Channel 1 |
| 32 | ST1 | Status output - Channel 1 |
| 33 | IN3 | Control input - Channel 3 |
| 34 | IN1 | Control input - Channel 1 |
| 35 | ST3 | Status output - Channel 3 |
| 36 | CLK | Clock input |

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings are the limiting values for this device.

Warning: Damage may occur if this device is subjected to conditions which are beyond these values.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-------------------------|--|----------------------|---------|-----|------------------|------|
| E_Q | Switch off energy for inductive loads | | | | 50 | mJ |
| Voltages | | | | | | |
| V_S | Supply voltage | | -0.3 | | 40 | V |
| V_{CC}, V_{DD} | Supply voltage | | -0.3 | | 6 | V |
| V_Q | Output voltage static | | | | 40 | V |
| V_Q | Output voltage during clamping | $t < 1\text{ms}$ | | | 60 | V |
| V_{IN}, V_{EN} | Input voltage IN1 to IN4, EN | $I_I < 110\text{mA}$ | -1.5 | | 6 | V |
| V_{CLK} | Input voltage CLK | | -1.5 | | 6 | V |
| V_{ST} | Output voltage status | | -0.3 | | 6 | V |
| V_D | Recirculation circuits D3, D4 | | | | 40 | V |
| V_{DRmax} | Max. reverse breakdown voltage of free wheeling diodes D3, D4 | | | | 55 | V |
| Currents | | | | | | |
| $I_{Q1/2}$ | Output current for Q1 and Q2 | | >5 | | internal limited | A |
| $I_{Q3/4}$ | Output current for Q3 and Q4 | | >3 | | internal limited | A |
| $I_{Q1/2}, I_{PGND1/2}$ | Output current at reversal supply for Q1 and Q2 | | -4 | | | A |
| $I_{Q3/4}, I_{PGND3/4}$ | Output current at reversal supply for Q3 and Q4 | | -2 | | | A |
| I_{ST} | Output current status pin | | -5 | | 5 | mA |
| ESD protection | | | | | | |
| ESD | Electrostatical discharging GND, PGND, Qx, Dx, CLK, ST, IN, TEST, EN | MIL883C | ± 2 | | | kV |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|--|----------------------|-----------------------------------|-----|-----|-----|------|
| V _S , V _{CC} ,V _{DD} | Supply pins | vs. GND and PGND | ±1 | | | kV |
| ESD | Output pins (Qx, Dx) | vs. Common GND (PGND1-4 + GND) | ±4 | | | kV |

3.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|------------------------|---|--------------------------|-----|-----|------------|------|
| T _j | Junction temperature | T _j | -40 | | 150 | °C |
| T _{jc} | Junction temperature during clamping (life time) | ∑t = 30min ∑t = 15min | | | 175 190 | °C |
| T _{stg} | Storage temperature | T _{stg} | -55 | | 150 | °C |
| T _{th} | Over temperature shutdown threshold | (1) | 175 | | 200 | °C |
| T _{hy} | Over temperature shutdown hysteresis | (1) | | 10 | | °C |
| R _{th j-case} | Thermal resistance junction to case | | | | 2 | K/W |

1. This parameter will not be tested but assured by design.

3.3 Operating range

Table 5. Operating range

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|------|------|------------|------|
| V _S | Supply voltage | | 4.8 | | 18 | V |
| V _{CC} , V _{DD} | Supply voltage | | 4.5 | | 5.5 | V |
| dV _S /dt | Supply voltage transient time | | -1 | | 1 | V/μs |
| V _Q | Output voltage static | | -0.3 | | 40 | V |
| V _Q | Output voltage induced by inductive switching | Voltage will be limited by internal Z-diode clamping | | | 60 | V |
| V _{ST} | Output voltage status | | -0.3 | | 6 | V |
| I _{ST} | Output current status | | -1 | | 1 | mA |
| T _j | Junction temperature | | -40 | | 150 | °C |
| T _{jc} | Junction temperature during clamping | ∑ = 30min ∑ = 15min | | | 175 190 | °C |

3.4 Electrical characteristics

Table 6. Electrical characteristics
($V_S = 4.8$ to $18V$; $T_j = -40$ to $150^\circ C$ unless otherwise specified)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|--|-------|------|-------|--------------|
| Power supply | | | | | | |
| I_{SON} | Supply current | $V_S \leq 18V$ (outputs ON) | | | 5 | mA |
| I_{SOFF} | Quiescent current | $V_S \leq 18V$ (outputs OFF) | | | 5 | mA |
| I_{CC} | Supply current VCC (analog supply) | $V_{CC} = 5V$ | | | 5 | mA |
| I_{DD} | Supply current VDD (digital supply) | $V_{DD} = 5V$ $f_{CLK}=0Hz$ | | | 5 | μA |
| I_{DD} | Supply current VDD (digital supply) | $V_{DD} = 5V$ $f_{CLK}=250kHz$ | | | 5 | mA |
| General diagnostic functions | | | | | | |
| V_{QU} | Open load voltage | $V_S \geq 6.5V$ (outputs OFF) | 0.3 | 0.33 | 0.36 | $\times V_Q$ |
| V_{thGND} | Signal-GND-loss threshold | $V_{CC} = 5V$ | 0.1 | | 1 | V |
| V_{thPGL} | Power-GND-loss threshold | $V_{CC} = 5V$ | 1.5 | 2.5 | 3.5 | V |
| $f_{CLK,min}$ | Clock frequency error | | 10 | | 100 | kHz |
| DC_{CLKe_low} | Clock duty cycle error detection low | $f_{CLK} = 250$ kHz | | 33,3 | 45 | % |
| DC_{CLKe_high} | Clock duty cycle error detection high | $f_{CLK} = 250$ kHz | 55 | 66,6 | | % |
| V_{Sloss} | Supply detection | $V_{CC} = V_{DD} = 5V$ | 2 | | 4.5 | V |
| Additional diagnostic functions channel 1 and channel 2 (non regulated channels) | | | | | | |
| $I_{QU1,2}$ | Open-load current channel 1, 2 | $V_S \geq 6.5V$ | 50 | | 300 | mA |
| $I_{QO1,2}$ | Over-load current channel 1, 2 | $V_S \geq 6.5V$ | 5 | 7.5 | 9 | A |
| Additional diagnostic functions channel 3 and channel 4 (regulated channels) | | | | | | |
| DC_{OUT} | Output duty cycle error | filtered with 10ms | 90 | | 100 | % |
| $I_{QO3,4}$ | Overload current channel 3,4 | $V_S \geq 6.5V$ | 2.5 | 5 | 8 | A |
| V_{rerr} | Recirculation error shutdown threshold (open D3/D4) | $I_{out} > 50mA$ | 45 | 50 | 60 | V |
| PWM_{dOUT} | Output PWM ratio during drift comparison | $V_{IN3} = V_{IN4} = PWM_{IN}$ $V_{TEST} = H$ | -14.3 | | +14.3 | % |
| Digital inputs (IN1 to IN4, ENA, CLK, TEST). The valid PWM-Ratio for IN3/IN4 is 10% to 90% | | | | | | |
| V_{IL} | Input low voltage | | -0.3 | | 1 | V |
| V_{IH} | Input high voltage | | 2 | | 6 | V |
| V_{IHy} | Input voltage hysteresis ⁽¹⁾ | | 20 | | 500 | mV |

Table 6. Electrical characteristics (continued)

(V_S = 4.8 to 18V; T_j = -40 to 150°C unless otherwise specified)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|--|---|------|------|------|------|
| I _I | Input pull down current | V _{IN} = 5V, V _S ≥ 6.5V | 8 | 20 | 40 | μA |
| Digital outputs (ST1 to ST4) | | | | | | |
| V _{STL} | Status output voltage in low state ⁽²⁾ | I _{ST} ≤ 40μA | 0 | | 0.4 | V |
| V _{STH} | Status output voltage in high state ⁽²⁾ | I _{ST} ≥ -40μA | 2.5 | | 3.45 | V |
| | | I _{ST} ≥ -120μA | 2 | | 3.45 | V |
| R _{DIAGL} | R _{OUT} + R _{DSON} in low state | | 0.3 | 0.64 | 1.5 | kΩ |
| R _{DIAGH} | R _{OUT} + R _{DSON} in high state | | 1.5 | 3.2 | 7.0 | kΩ |
| Power outputs (Q1 to Q4) | | | | | | |
| R _{DSON} | Static drain-source ON-resistance | I _Q = 1A; V _S ≥ 9.5V | | 0.2 | 0.4 | W |
| V _{F_250mA} | Forward voltage of free wheeling path D3, D4 @250mA | I _{D3/4} = -250mA | 0.5 | | 1.5 | V |
| V _{F_2.25A} | Forward voltage of free wheeling path D3, D4 @2.25A | I _{D3/4} = -2.25A | 2.0 | | 4.5 | V |
| R _{sens} | Sense resistor = (V _{F_2.25A} - V _{F_250mA})/2A | | | 1 | | W |
| V _Z | Z-diode clamping voltage | I _Q ≥ 100mA | 45 | | 60 | V |
| I _{PD} | Output pull down current | V _{EN} = H, V _{IN} = L | 10 | | 150 | μA |
| I _{Qlk} | Output leakage current | V _{EN} = L; V _Q = 20V | | | 5 | μA |
| Timing | | | | | | |
| t _{ON} | Output ON delay time | I _Q = 1A | 0 | 5 | 20 | μs |
| t _{OFF} | Output OFF delay time channel | I _Q = 1A | 0 | 10 | 30 | μs |
| t _{IN3/4min} | Minimum Input Register ON time | ⁽³⁾ | | 2 | | μs |
| t _{OFFREG} | Output OFF delay time regulator | | | 528 | | μs |
| t _r | Output rise time | I _Q = 1A | 0.5 | 1.5 | 8 | μs |
| t _f | Output fall time | I _Q = 1A | 0.5 | 1.5 | 8 | μs |
| t _{sf} | Short error detection filter time | f _{CLK} = 250kHz DC = 50% ⁽³⁾ | 4 | | 8 | μs |
| t _{lf} | Long error detection filter time | f _{CLK} = 250kHz DC = 50% ⁽³⁾ | 16 | | 32 | μs |
| t _{SCP} | Short circuit switch-OFF delay time | ⁽³⁾ | 4 | | 30 | μs |
| t _D | Status delay time | ⁽³⁾ | 896 | | 1024 | μs |
| t _{RE} | Regulation error status delay time | ⁽³⁾ (reg. channels only) | | 10 | | ms |
| t _{Dreg} | Output off status delay time | ⁽³⁾ (reg. channels only) | | 528 | | μs |
| Reg. current accuracy (reg. channels only) | | | | | | |
| I _{Q3/Q4} | Maximum current | DC = 90% | 2 | 2.25 | 2.5 | A |

Table 6. Electrical characteristics (continued) $(V_S = 4.8 \text{ to } 18\text{V}; T_j = -40 \text{ to } 150^\circ\text{C} \text{ unless otherwise specified})$

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------------------|---|---|------|------|------|------|
| $I_{Q3/Q4}$ | Current Resolution Input Duty Cycle 0.4% - 99% $f_{clk} = 2\text{KHz}$ @ | $0.00\text{A} \leq I_{Q3/Q4} \leq 0.25\text{A}$ | | | 25 | mA |
| | | $0.25\text{A} \leq I_{Q3/Q4} \leq 0.40\text{A}$ | | | 10 | % |
| | | $0.40\text{A} \leq I_{Q3/Q4} \leq 0.80\text{A}$ | | | 6 | % |
| | | $0.80\text{A} \leq I_{Q3/Q4} \leq 2.25\text{A}$ | -8 | | 6 | % |
| $\Delta I_{Q3/Q4}$ | Min. quant. step | | | 5 | | mA |
| Frequencies | | | | | | |
| | CLK frequency | crystal-controlled | | 250 | | kHz |
| | Input PWM frequency | (reg. channels only) | | 2 | | kHz |

1. This parameter will not be tested but assured by design.
2. Short circuit between two digital outputs (one in high the other in low state) will lead to the defined result "LOW".
3. Digital filtered with external clock, only functional test.

4 Functional description

4.1 Overview

The L9352B is designed to drive inductive loads (relays, electromagnetic valves) in low side configuration. Integrated active Zener-clamp (for channel1 and 2) or free wheeling diodes (for channel 3 and 4) allow the recirculation of the inductive loads. All four channels are monitored with a status output. All wiring to the loads and supply pins of the device are controlled. The device is self-protected against short circuit at the outputs and over temperature. For each channel one independent push-pull status output is used for a parallel diagnostic function.

Channel 3 and 4 work as current regulator. A PWM signal on the input defines the target output current. The output current is controlled through the output PWM of the power stage. The regulator limit of 90% is detected and monitored with the status signal. The current is measured during recirculation phase of the load.

A test mode compares the differences between the two regulators. This “drift” test compares the output PWM of the regulators. By this feature a drift of the load during lifetime can be detected.

4.2 Input circuits

The INput, CLK, TEST and ENable inputs, are active high, consist of Schmidt triggers with hysteresis. All inputs are connected to pull-down current sources.

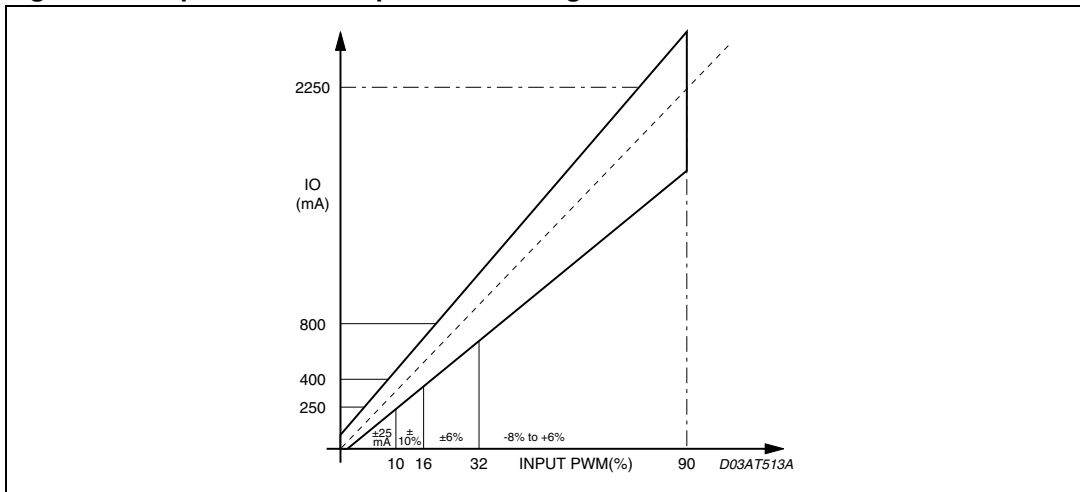
4.3 Output stages (not regulated) channel 1 and 2

The two power outputs (5A) consist of DMOS-power transistors with open drain output. The output stages are protected against short circuit. Via integrated Zener-clamp-diodes the overvoltage of the inductive loads due to recirculation are clamped to typ. 52V for fast shut off of the valves. Parallel to the DMOS transistors there are internal pull-down current sources. They are provided to assure an open load condition in the OFF-state. With EN=low this current source is switched off, but the open load comparator is still active.

4.4 Current-regulator-stages channel 3 and 4

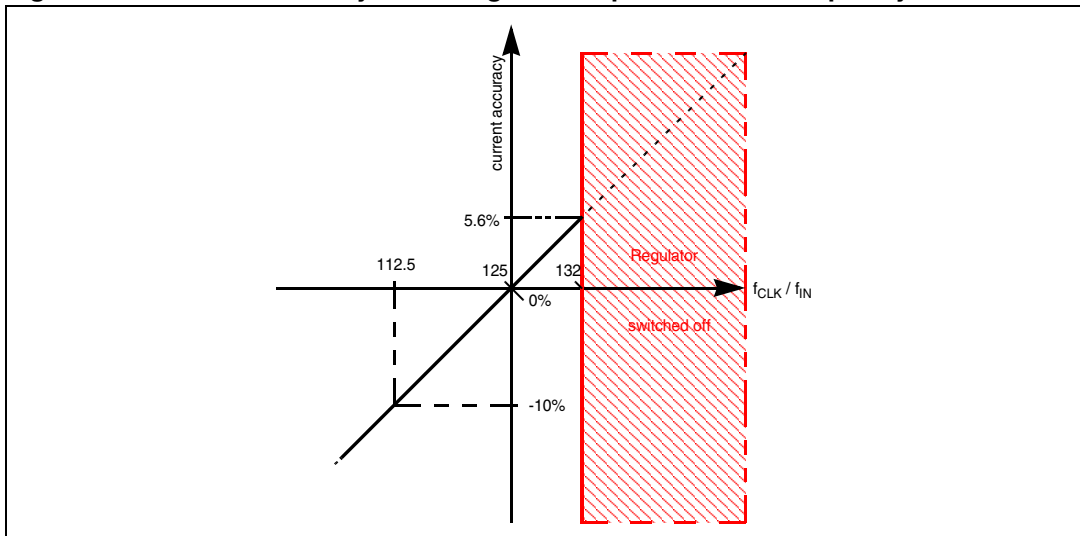
The current-regulator channels are designed to drive inductive loads. The target value of the current is given by the duty cycle (DC) of the 2 kHz PWM input signal. The following figure shows the relation between the input PWM and the output current and the specified accuracy.

Figure 3. Input PWM to output current range



The ON period of the input signal is measured with a 1MHz clock, synchronized with the external 250kHz clock. For requested precision of the output current the ratio between the frequencies of the input signal and the external 250kHz clock has to be fixed according to the graph shown in [Figure 4](#).

Figure 4. Current accuracy according to the input and clock frequency ratio



The theoretical error is zero for $f_{CLK} / f_{IN} = 125$.

If the period of the input signal is longer than 132 times the period of the clock the regulator is switched off. For a clock frequency lower than 100kHz the clock control will also disable the regulator. For high precision applications the clock frequency and the input frequency have to be correlated.

The output current is measured during the recirculation of the load. The current sense resistor is in series to the free wheeling diode. If this recirculation path is interrupted the regulator stops immediately and the status output remains low for the rest of the input cycle.

The output period is 64 times the clock period. With a clock frequency of 250kHz the output PWM frequency is 3.9kHz. The output PWM is synchronized with the first negative edge of the input signal. After that the output and the input are asynchronous. The first period is

used to measure the current. This means the first turn-on of the power is 256 μ s after the first negative edge of the input signal.

As regulator a digital PI-regulator with the Transfer function for:

$$KI: \frac{0.126}{z-1} \quad \text{and KP: } 0.96$$

for a sampling time of 256 μ s is realized.

To speed up the current settling time the regulator output is locked to 90% output PWM until the target current value is reached. This happens also when the target current value changes and the output PWM reaches 90% during the regulation. The status output gets low if the target current value is not reached within the regulation error delay time of $t_{RE}=10$ ms.

4.5 Protective circuits

The outputs are protected against current overload, over temperature, and power-GND-loss. The external clock is monitored by a clock watchdog. This clock watchdog detects a minimal frequency $f_{CLK,min}$ and wrong clock duty cycles. The allowed clock duty cycle range is 45% to 55%. The current-regulator stages are protected against recirculation errors, when D3 or D4 is not connected. All these error conditions shut off the power stage and invert the status output information.

4.6 Error detection

The status outputs indicate the switching state under normal conditions (status LOW = OFF; status HIGH = ON). If an error occurs, the logic level of the status output is inverted, as listed in the diagnostic table below. All external errors, for example open load, are filtered internally. The following table shows the detected errors, the filter times and the detection mode (on/off).

Table 7. Error detection

| | ON State EN & IN = HIGH | OFF State EN & IN = LOW | Filter time | Reset done by |
|--|----------------------------|----------------------------|-------------|--|
| Short circuit of the load | X | | t_{sf} | EN & IN = "LOW" for T_D or T_{Dreg} |
| Open load (under voltage detection) | | X | t_{if} | timer T_D |
| Open load (under current detection) | X | | t_{sf} | timer T_D |
| Overtemperature | X | | t_{sf} | EN & IN = "LOW" for T_D or T_{Dreg} |
| Power-GND-loss | X | X | t_{if} | in on: EN & IN = "LOW" for T_D or T_{Dreg} in off: timer T_D |
| Signal-GND-loss | X | X | t_{if} | timer T_D |

Table 7. Error detection (continued)

| | ON State EN & IN = HIGH | OFF State EN & IN = LOW | Filter time | Reset done by |
|-----------------------------|----------------------------|----------------------------|-------------|--|
| Supply-VS-loss | X | X | t_{if} | timer T_D |
| Clock control | X | X | no | in on: EN & IN = "LOW" for T_D or T_{Dreg} in off: timer T_D |
| Output voltage clamp active | X (regulated channels) | | no | in on: EN & IN = "LOW" for T_D or T_{Dreg} in off: timer T_D |

EN&IN = low means that at least one between enable and input is low. For the inputs IN=low means also no input PWM. For the regulator input period longer than T_{Dreg} and for the standard channel input period longer than T_D .

A detected error is stored in an error register. The reset of this register is made with a timer T_D . With this approach all errors are present at the status output at least for the time T_D .

All protection functions like short circuit of the output, over temperature, clock failure or power-GND-loss in ON condition are stored into an internal "fail" register. The output is then shut off. The register must be reset with a low signal at the input. A "low signal" means that the input is low for a time longer than T_D or T_{Dreg} for the related channel, otherwise it is interpreted as a PWM input signal and the register is left in set mode.

Signal-GND-loss and VS-loss are detected in the active on mode, but they do not set the fail register. This type of error is only delayed with the standard timer t_{if} function.

Open load is detected for all four channels in on- and off-state.

Open load in off condition detects the voltage on the output pin. If this voltage is below $0.33 * VS$ the error register is set and delayed with T_D . A sink current stage pull the output down to ground, with EN high. With EN low the output is floating in case of openload and the detection is not assured. In the ON state the load current is monitored by the non-regulated channels. If it drops below the specified threshold value I_{QU} an open load is detected and the error register is set and delayed with T_D . A regulated channel detects the open load in the on state with the current regulator error detection. If the output PWM reaches 90% for a time longer than t_{RE} than an error occurs. This could happen when no load is connected, the resistivity of the load is too high or the supply voltage too low.

A clock failure (clock loss) is detected when the frequency becomes lower than $f_{CLK,min}$. All status outputs are set on error and all power outputs are shut off. The status signals remain in their state until the clock signal is present again. A clock failure during power on of V_{CC} is detected only on the regulated channels. The status outputs of the channel 1 and 2 are low in this case.

4.7 Drift detection (regulated channels only)

The drift detection is used to compare the two regulated channels during regulation. This "Drift" test compares the output PWM of the regulators. The resistivity of the load influences the output PWM. The approximated formula for the output current below shows the dependency of the load resistor to the output PWM. In this formula the energy reduction during the recirculation is not taken into account. The real output PWM is higher. The testmode is enabled with IN, EN and TEST high. With an identical 2kHz PWM-Signal connected to the IN-inputs the output PWM must be in a range of $\pm 14.3\%$. If the difference between the two on-times is more than $\pm 14.3\%$ of the expected value an error is detected and monitored by the status outputs, in the same way as described above, but a drift error will not be registered and also not delayed with T_D as other errors.

$$I_{OUT} = \frac{V_{BAT}}{R_L + R_{ON}} \cdot PWM$$

Drift Definition:

$$\text{Drift} = PWM(1+E) - PWM(1-E) = 2PWM E$$

$$\text{Drift} * 4 < PWM(1+E)$$

with $E > 14.3\%$ a drift is detected

E.. not correlated Error of the channels






%PWM ... Corresponding ideal output PWM to a given input PWM

A 7bit output-PWM-register is used for the comparison. The register with the lower value is subtracted from the higher one. This result is multiplied by four and compared with the higher value.

4.8 Other test modes

The test pin is also used to test the regulated channels in the production. With a special sequence on this pin the power stages of the regulated channels can be controlled direct from the input. No status feedback of the regulated channels is given. The status output is clocked by the regulator logic. The output sequence is a indication of a proper logic functionality. The following table shows the functionality of this special test mode.

Table 8. Special test mode functionality

| EN | IN | TEST | OUT | STATUS | Note |
|----|----|---|-----|--------------|----------------------|
| 1 | X | X | X | X | disable test mode |
| 1 | 1 | 1 | on | 1 | Drift mode |
| 0 | X |  | off | test pattern | test condition one |
| 0 | X |  | off | test pattern | test condition two |
| 0 | X |  | off | test pattern | test condition three |
| 0 | 0 |  | off | test pattern | test condition four |
| 0 | 1 |  | on | test pattern | test condition four |

For more details about the test condition four see timing diagram.

4.9 Diagnostic

The status follows the input signal in normal operating conditions.
If any error is detected the status is inverted.

Table 9. Diagnostic

| Operating condition | Test input TEST | Enable input ENA | Control input non-reg./reg. IN | Power output/current reg. Q | Status output ST |
|---|--------------------|---------------------|-----------------------------------|--------------------------------|---------------------|
| Normal function | L | L | L | OFF | L |
| | L | L | H/PWM | OFF | L |
| | L | H | L | OFF | L |
| | L | H | H/PWM | ON | H |
| Open load or short to ground | L | L | L | OFF | X |
| | L | L | H/PWM | OFF | X |
| | L | H | L | OFF | H |
| | L | H | H/PWM | ON | L |
| Overload or short to supply Latched overload Reset latch Reset latch | L | H | H/PWM | OFF | L |
| | L | H | H/PWM | OFF | L |
| | L | H → L | X | OFF | L |
| | L | H | H/PWM → L | OFF | L |
| Overtemperature Latched overtemperature Reset latch Reset latch | L | H | H/PWM | OFF | L |
| | L | H | H/PWM | OFF | L |
| | L | H → L | X | OFF | L |
| | L | H | H/PWM → L | OFF | L |
| Recirculation error (reg.chn.) Latched error Reset latch Reset latch | L | H | PWM | OFF | L |
| | L | H | PWM | OFF | L |
| | L | H → L | X | OFF | L |
| | L | H | PWM → L | OFF | L |
| Clock failure (clock loss) ⁽¹⁾ | L | L | L | OFF | H |
| | L | L | H/PWM | OFF | H |
| | L | H | L | OFF | H |
| | L | H | H/PWM | OFF | L |
| Drift ⁽²⁾ Failure No failure | H | L | L | OFF | X |
| | H | L | H/PWM | OFF | X |
| | H | H | H/PWM | ON | L |
| | H | H | H/PWM | ON | H |

1. during power on sequence only detected on channel 3 and 4 (see description).

2. This input combination is also used for an internal chip-test and must not be used.

5 Timing diagrams

5.1 Non regulated channels

Figure 5. Output slope, resistive load

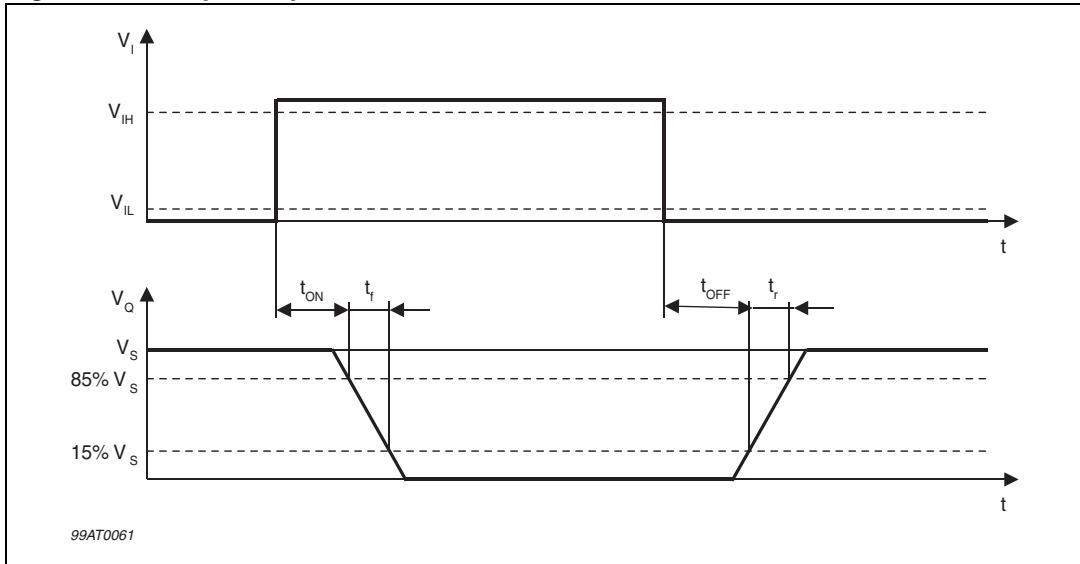


Figure 6. Overload switch-off delay

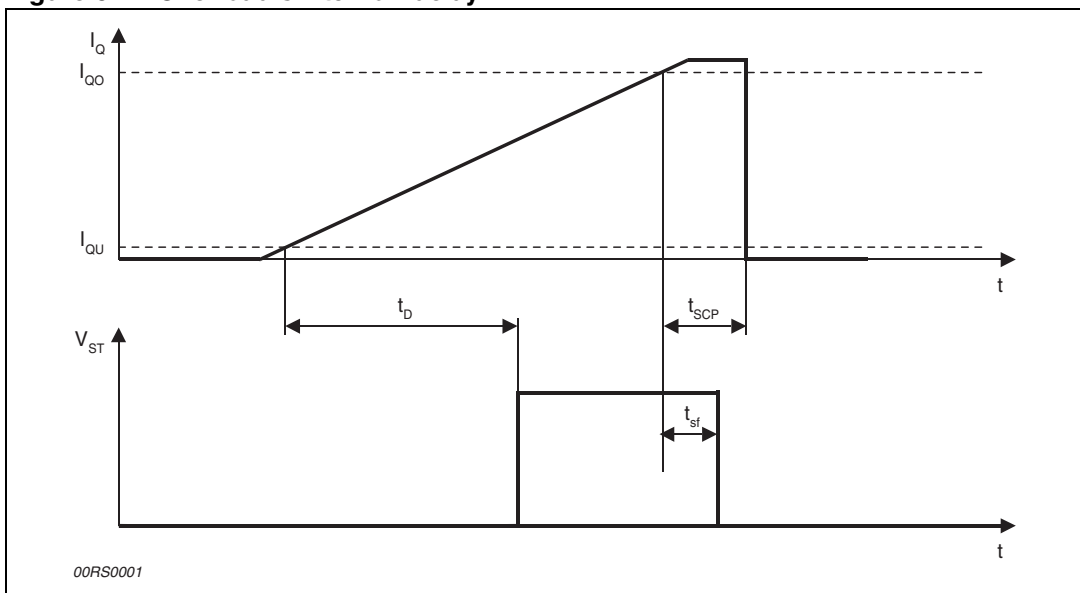


Figure 7. Normal condition, resistive load, pulsed input signal

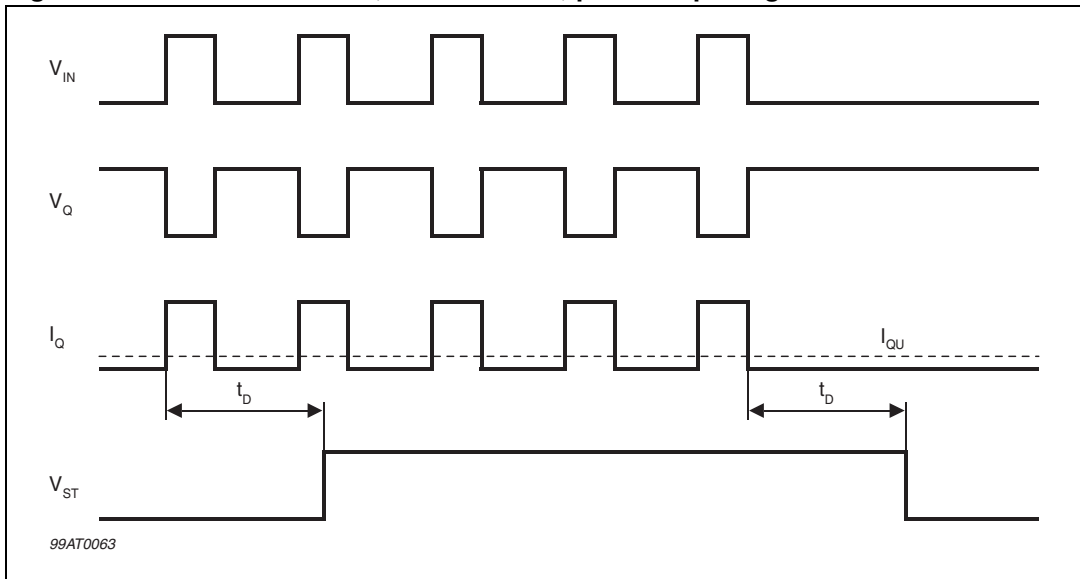


Figure 8. Current overload

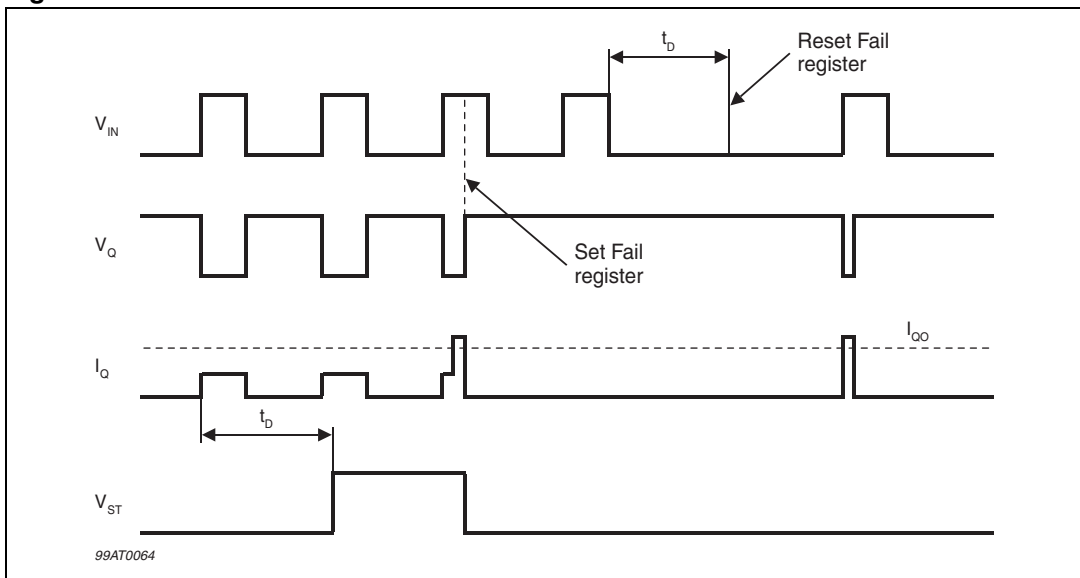


Figure 9. Diagnostic status output at different open load current conditions

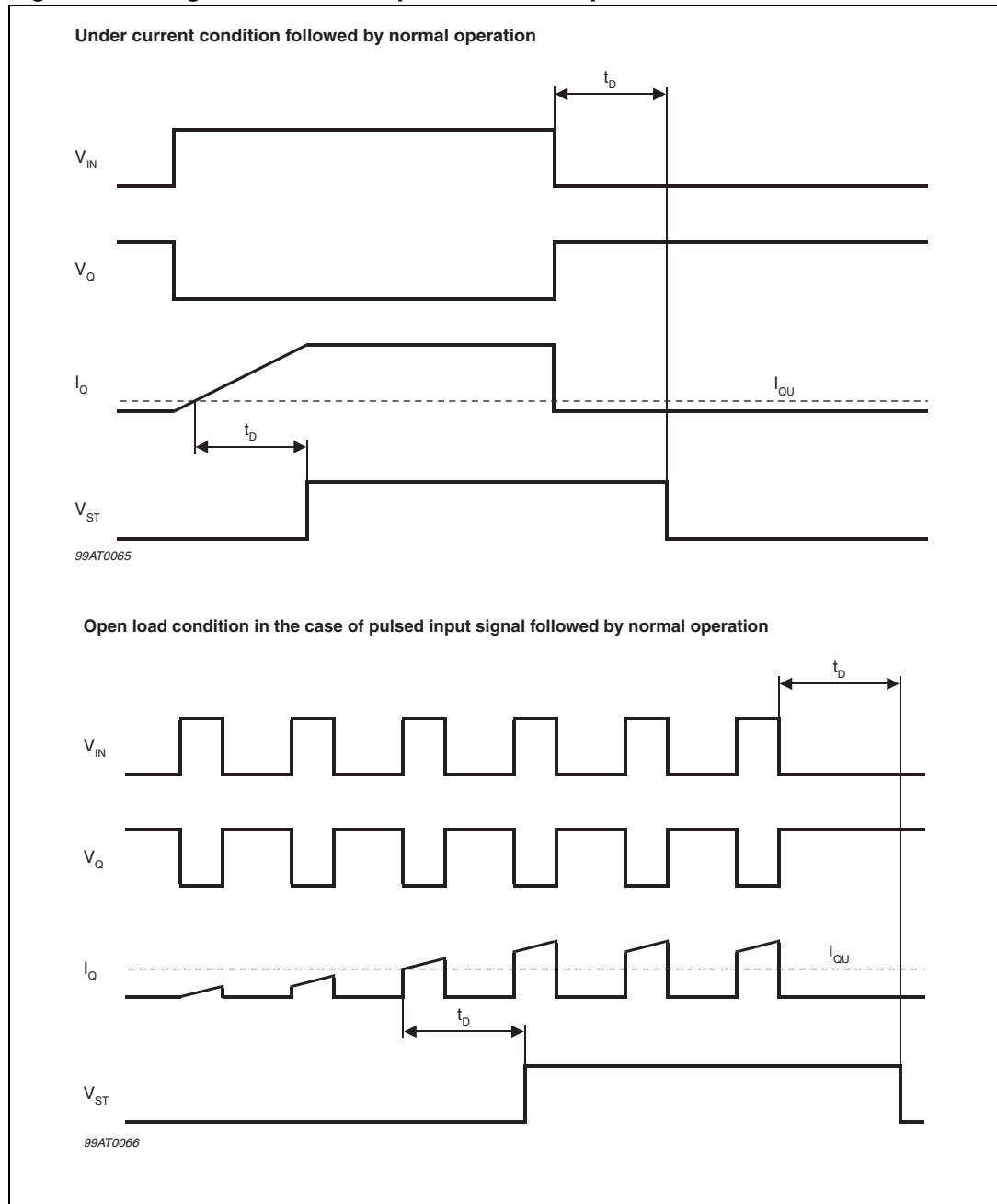
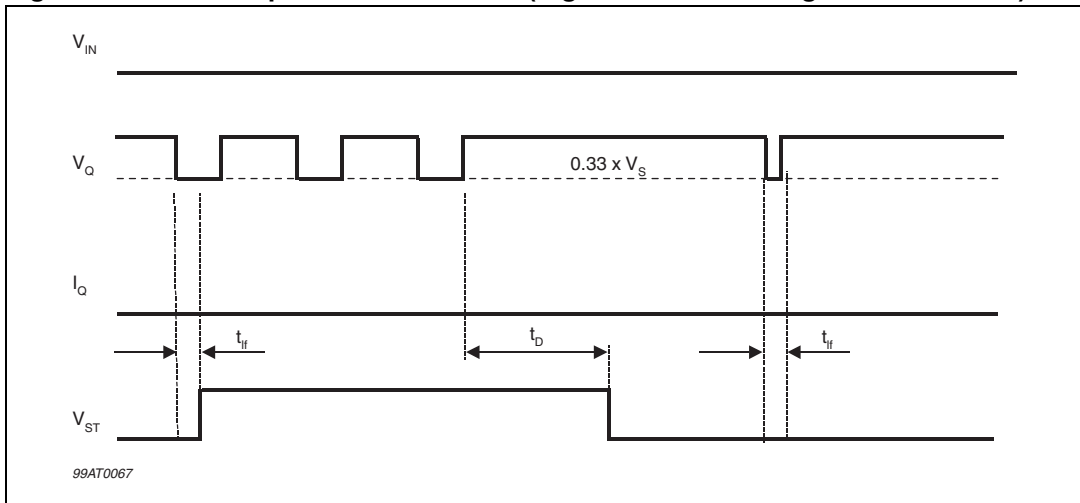


Figure 10. Pulsed open load conditions (regulated and non-regulated channels)



5.2 Regulated channels (timing diagrams of diagnostic with 2kHz PWM input signal)

Figure 11. Normal condition, inductive load

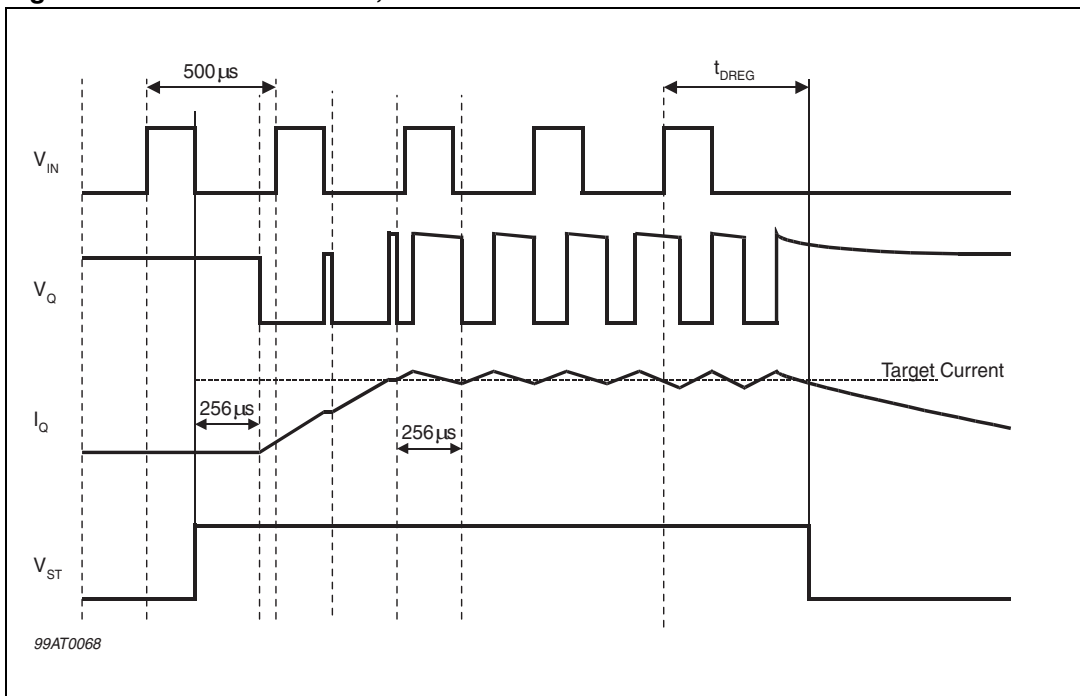


Figure 12. Current overload

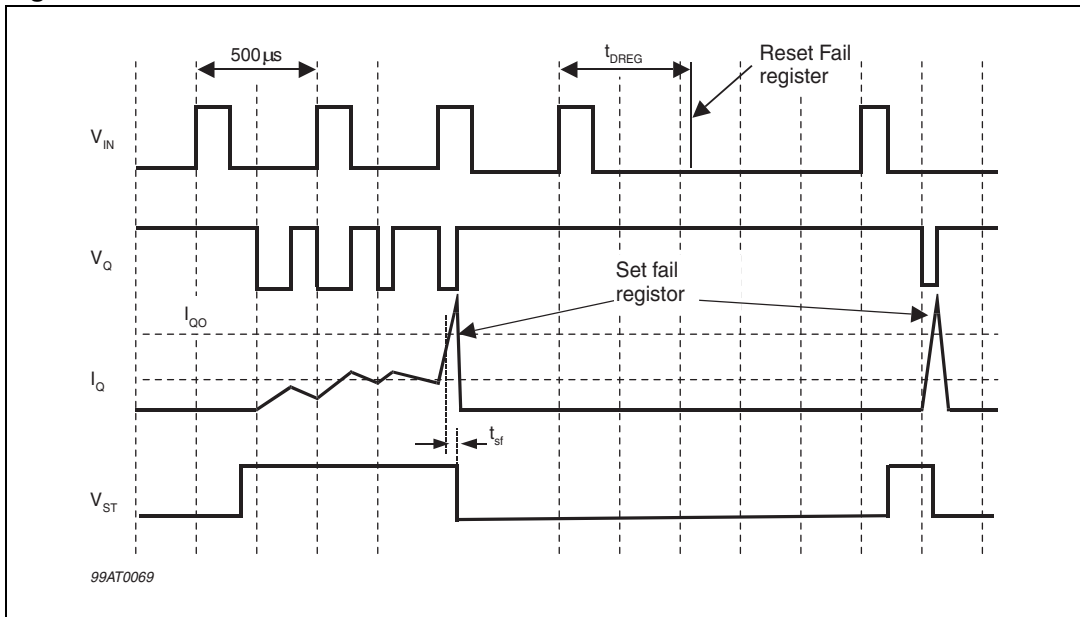


Figure 13. Recirculation error

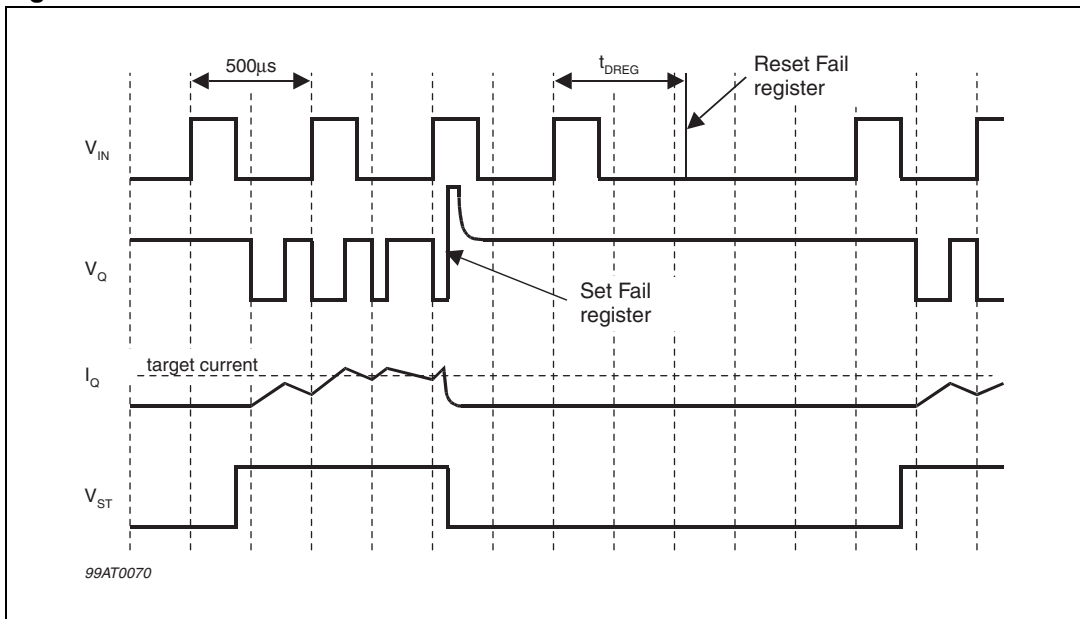


Figure 14. Current regulation error (e.g. as a result of voltage reduction)

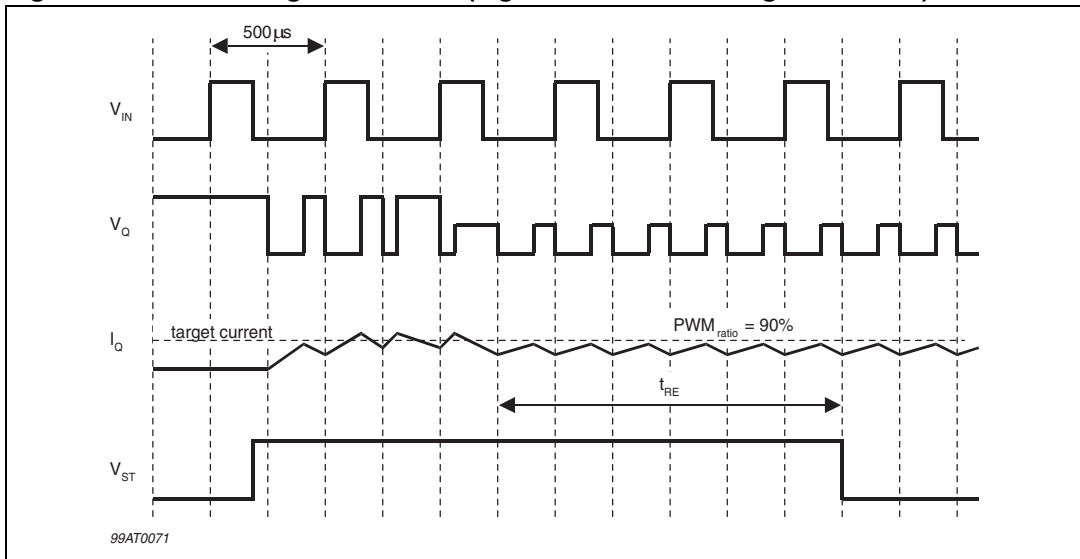


Figure 15. Over temperature

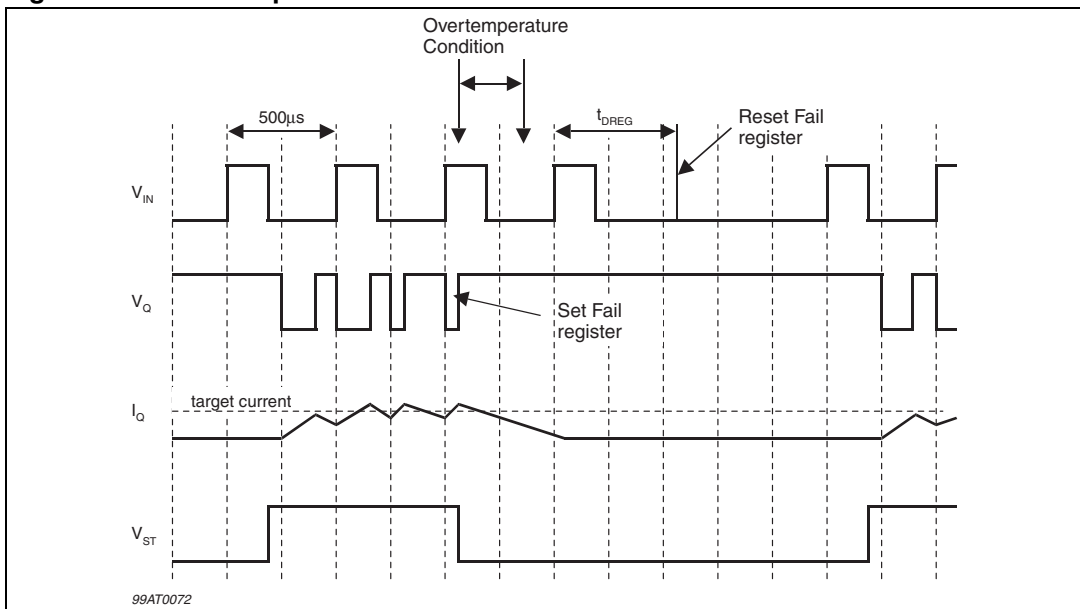
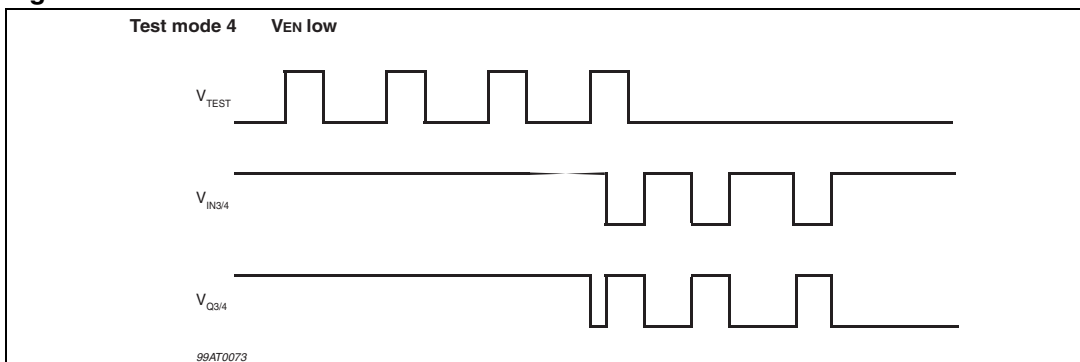


Figure 16. Test mode 4

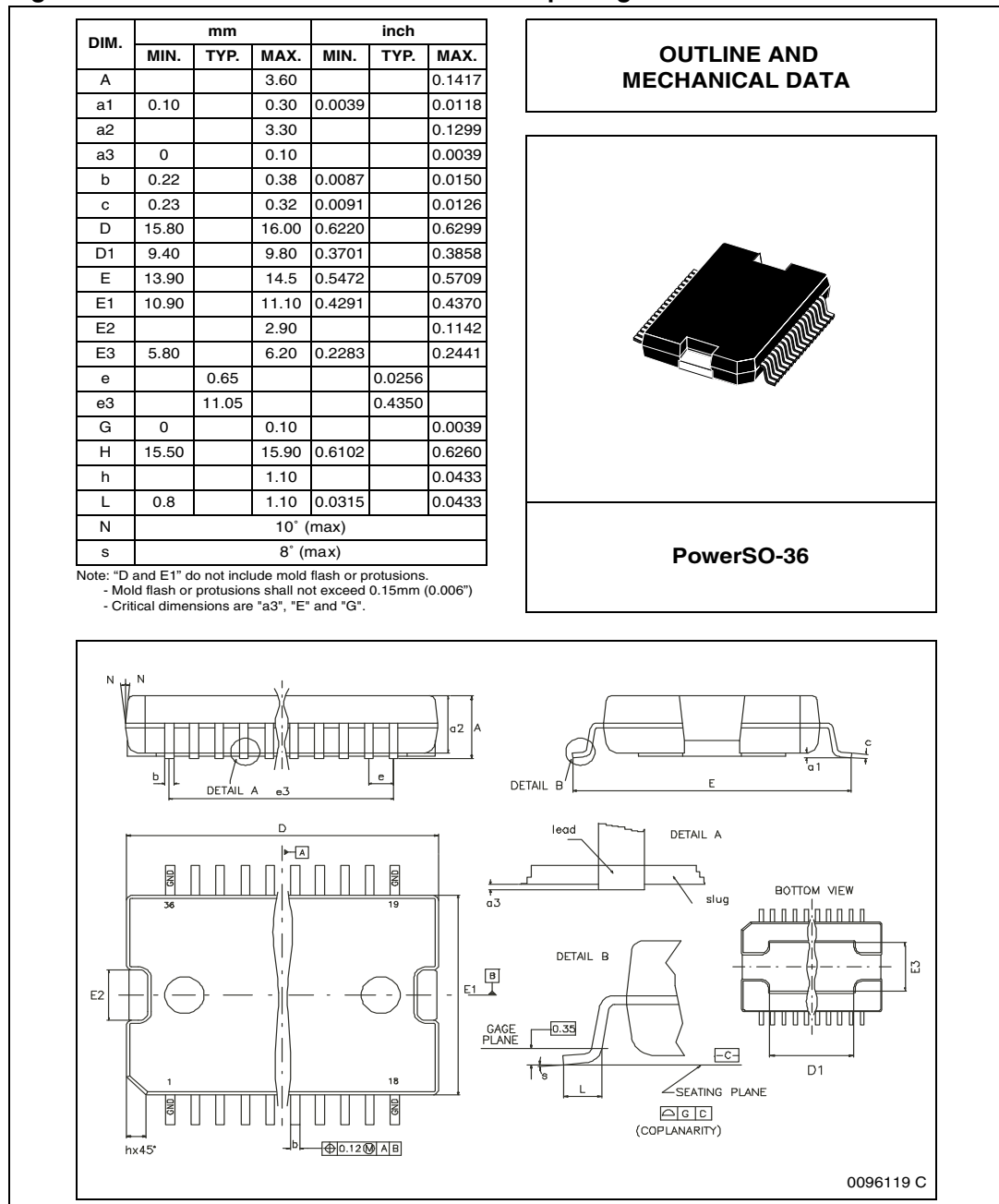


6 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK[®] packages. ECOPACK[®] packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 17. PowerSO-36 mechanical data and package dimensions



7 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 20-Feb-2004 | 5 | Initial release. |
| 05-Sep-2008 | 6 | Document reformatted. Updated the order codes in Table 1: Device summary . |
| 17-Sep-2013 | 7 | Updated Disclaimer |

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