# DATA SHEET

# 74ALVCH16841

## 20-bit bus interface D-type latch (3-State)

Product specification

1998 Jul 27

IC24 Data Handbook

Philips
Semiconductors

PHILIPS

# 20-bit bus interface D-type latch (3-State) 74ALVCH16841

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Wide supply voltage range of 1.2V to 3.6V
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple $V_{CC}$ and GND pins for minimum noise and ground bounce
- Current drive ±24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

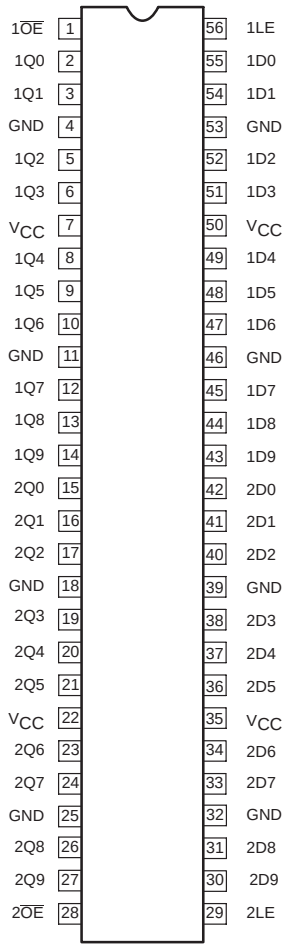
## DESCRIPTION

The 74ALVCH16841 has two 10-bit D-type latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE) and output enable ($n\overline{OE}$) control gates.

When $n\overline{OE}$ is LOW, the data in the registers appears at the outputs. When $n\overline{OE}$ is High the outputs are in High-impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16841 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## PIN CONFIGURATION




## QUICK REFERENCE DATA

GND = 0V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.5$ns

| SYMBOL | PARAMETER | CONDITIONS | | TYPICAL | UNIT |
|---|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay $nD_n$ to $nQ_n$ | $V_{CC}$ = 2.5V, $C_L$ = 30pF<br>$V_{CC}$ = 3.3V, $C_L$ = 50pF | | 2.5<br>2.4 | ns |
| $t_{PHL}/t_{PLH}$ | Propagation delay nLE to $nQ_n$ | $V_{CC}$ = 2.5V, $C_L$ = 30pF<br>$V_{CC}$ = 3.3V, $C_L$ = 50pF | | 2.5<br>2.4 | ns |
| $C_I$ | Input capacitance | | | 5.0 | pF |
| $C_{PD}$ | Power dissipation capacitance per buffer | $V_I$ = GND to $V_{CC}$[1] | Outputs enabled | 19 | pF |
| | | | Outputs disabled | 3 | |

**NOTES:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i$ = input frequency in MHz; $C_L$ = output load capacitance in pF; $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 56-Pin Plastic TSSOP Type II | –40°C to +85°C | 74ALVCH16841 DGG | ACH16841 DGG | SOT364-1 |

## PIN DESCRIPTION

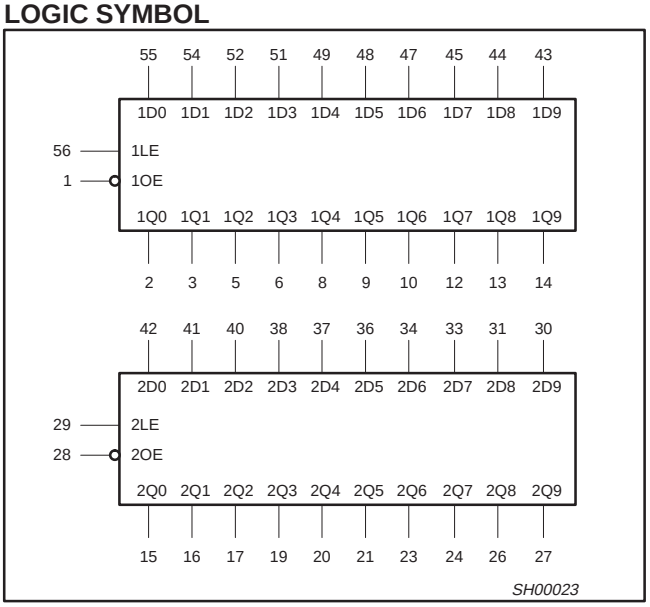
| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 1 | $1\overline{OE}$ | Output enable inputs (active-LOW) |
| 56 | 1LE | Latch enable inputs (active HIGH) |
| 55, 54, 52, 51, 49, 48, 47, 45, 44, 43 | 1D0 – 1D9 | Data inputs |
| 2, 3, 5, 6, 8, 9, 10, 12, 13, 14 | 1Q0 – 1Q9 | Data outputs |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0V) |
| 7, 22, 35, 50 | $V_{CC}$ | Positive supply voltage |
| 28 | $2\overline{OE}$ | Output enable inputs (active-LOW) |
| 29 | 2LE | Latch enable inputs (active HIGH) |
| 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | 2D0 – 2D9 | Data inputs |
| 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | 2Q0 – 2Q9 | Data outputs |

## FUNCTION TABLE

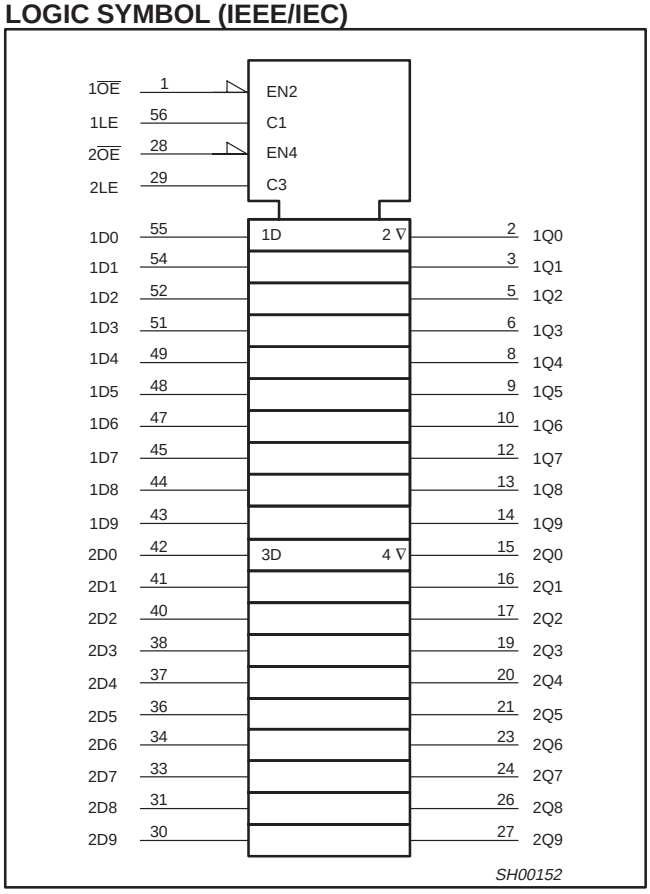
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $n\overline{OE}$ | LE | Dx | Q |
| L | H | L | L |
| L | H | H | H |
| L | L | X | $Q_0$ |
| H | X | X | Z |

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

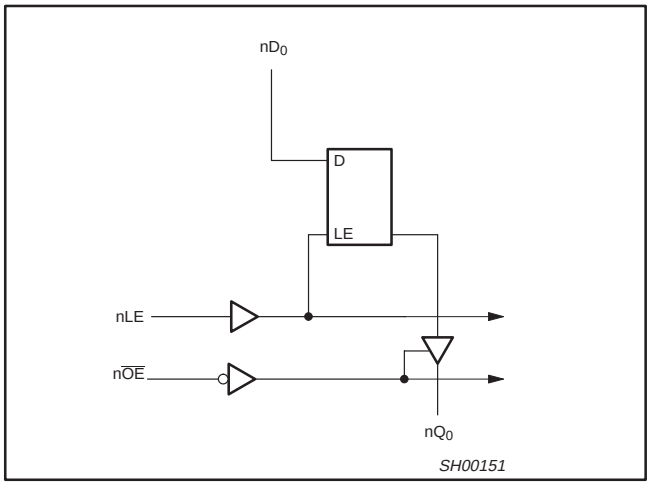
## LOGIC SYMBOL



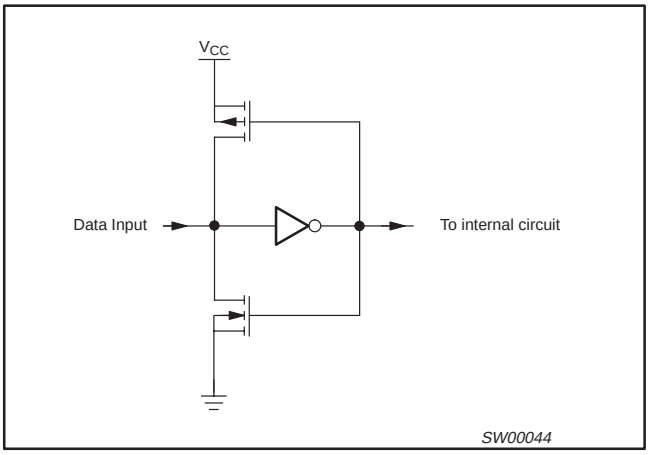

## LOGIC SYMBOL (IEEE/IEC)




## LOGIC DIAGRAM



## BUS HOLD CIRCUIT




## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load) | | 2.3 | 2.7 | V |
| | DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load) | | 3.0 | 3.6 | |
| $V_I$ | DC Input voltage range | | 0 | $V_{CC}$ | V |
| $V_O$ | DC output voltage range | | 0 | $V_{CC}$ | V |
| $T_{amb}$ | Operating free-air temperature range | | –40 | +85 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 2.3 to 3.0V<br>$V_{CC}$ = 3.0 to 3.6V | 0<br>0 | 20<br>10 | ns/V |

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +4.6 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –50 | mA |
| $V_I$ | DC input voltage | For control pins[1] | –0.5 to +4.6 | V |
| | | For data inputs[1] | –0.5 to $V_{CC}$ +0.5 | |
| $I_{OK}$ | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ±50 | mA |
| $V_O$ | DC output voltage | Note 1 | –0.5 to $V_{CC}$ +0.5 | V |
| $I_O$ | DC output source or sink current | $V_O$ = 0 to $V_{CC}$ | ±50 | mA |
| $I_{GND}$, $I_{CC}$ | DC $V_{CC}$ or GND current | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package<br>–plastic medium-shrink (SSOP)<br>–plastic thin-medium-shrink (TSSOP) | For temperature range: –40 to +125 °C<br>above +55°C derate linearly with 11.3 mW/K<br>above +55°C derate linearly with 8 mW/K | <br>850<br>600 | mW |

**NOTE:**
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{CC}$ = 2.3 to 2.7V | 1.7 | 1.2 | | V |
| | | $V_{CC}$ = 2.7 to 3.6V | 2.0 | 1.5 | | |
| $V_{IL}$ | LOW level Input voltage | $V_{CC}$ = 2.3 to 2.7V | | 1.2 | 0.7 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | | 1.5 | 0.8 | |
| $V_{OH}$ | HIGH level output voltage | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –100µA | $V_{CC}$ – 0.2 | $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –6mA | $V_{CC}$ – 0.3 | $V_{CC}$ – 0.08 | | |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –12mA | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.26 | | |
| | | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –12mA | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.14 | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –12mA | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.09 | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = –24mA | $V_{CC}$ – 1.0 | $V_{CC}$ – 0.28 | | |
| $V_{OL}$ | LOW level output voltage | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | GND | 0.20 | V |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 6mA | | 0.07 | 0.40 | V |
| | | $V_{CC}$ = 2.3V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 12mA | | 0.15 | 0.70 | V |
| | | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 12mA | | 0.14 | 0.40 | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 24mA | | 0.27 | 0.55 | |
| $I_I$ | Input leakage current | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{CC}$ or GND | | 0.1 | 5 | µA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | | 0.1 | 10 | µA |
| $I_{CC}$ | Quiescent supply current | $V_{CC}$ = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; $I_O$ = 0 | | 0.2 | 40 | µA |
| $\Delta I_{CC}$ | Additional quiescent supply current | $V_{CC}$ = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; $I_O$ = 0 | | 150 | 750 | µA |
| $I_{BHL}$[2] | Bus hold LOW sustaining current | $V_{CC}$ = 2.3V; $V_I$ = 0.7V | 45 | – | | µA |
| | | $V_{CC}$ = 3.0V; $V_I$ = 0.8V | 75 | 150 | | |
| $I_{BHH}$[2] | Bus hold HIGH sustaining current | $V_{CC}$ = 2.3V; $V_I$ = 1.7V | –45 | | | µA |
| | | $V_{CC}$ = 3.0V; $V_I$ = 2.0V | –75 | –175 | | |
| $I_{BHLO}$[2] | Bus hold LOW overdrive current | $V_{CC}$ = 3.6V | 500 | | | µA |
| $I_{BHHO}$[2] | Bus hold HIGH overdrive current | $V_{CC}$ = 3.6V | –500 | | | µA |

**NOTES:**
1. All typical values are at $T_{amb}$ = 25°C.
2. Valid for data inputs of bus hold parts.

## AC CHARACTERISTICS FOR $V_{CC}$ = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; $C_L$ = 30pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS $V_{CC}$ = 2.3 to 2.7V | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| $t_{PLH}/t_{PHL}$ | Propagation delay $nD_n$ to $nQ_n$ | 1, 5 | 1.0 | 2.5 | 5.0 | ns |
| $t_{PLH}/t_{PHL}$ | Propagation delay nLE to $nQ_n$ | 2, 5 | 1.0 | 2.5 | 5.6 | ns |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $n\overline{OE}_n$ to $nQ_n$ | 4, 5 | 1.0 | 2.7 | 6.2 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time $n\overline{OE}_n$ to $nQ_n$ | 4, 5 | 1.1 | 2.2 | 5.3 | ns |
| $t_W$ | nLE pulse width HIGH | 2, 5 | 3.3 | 1.5 | – | ns |
| $t_{SU}$ | Set up time $nD_n$ to nLE | 3, 5 | 1.3 | 0.1 | – | ns |
| $T_h$ | Hold time $nD_n$ to nLE | 3, 5 | 1.4 | 0.3 | – | ns |

**NOTE:**
1. All typical values are at $V_{CC}$ = 3.3V and $T_{amb}$ = 25°C.

## AC CHARACTERISTICS FOR $V_{CC}$ = 3.0V TO 3.6V RANGE AND $V_{CC}$ = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L$ = 50pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS $V_{CC} = 3.3 \pm 0.3$V | | | LIMITS $V_{CC}$ = 2.7V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[1, 2] | MAX | MIN | TYP[1] | MAX | |
| $t_{PLH}/t_{PHL}$ | Propagation delay $nD_n$ to $nQ_n$ | 1, 5 | 1.0 | 2.4 | 3.9 | 1.0 | 2.6 | 4.7 | ns |
| $t_{PLH}/t_{PHL}$ | Propagation delay nLE to $nQ_n$ | 2, 5 | 1.0 | 2.4 | 4.3 | 1.0 | 2.6 | 5.1 | ns |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $n\overline{OE}_n$ to $nQ_n$ | 4, 5 | 1.0 | 2.3 | 4.9 | 1.0 | 3.1 | 6.0 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time $n\overline{OE}_n$ to $nQ_n$ | 4, 5 | 1.3 | 2.9 | 4.1 | 1.3 | 3.1 | 4.3 | ns |
| $t_W$ | nLE pulse width HIGH | 2, 5 | 3.3 | 1.5 | – | 3.3 | 1.5 | – | ns |
| $t_{SU}$ | Set up time $nD_n$ to nLE | 3, 5 | 1.0 | 0.6 | – | 1.1 | 0.1 | – | ns |
| $t_h$ | Hold time $nD_n$ to nLE | 3, 5 | 1.4 | 0.2 | – | 1.7 | 0.2 | – | ns |

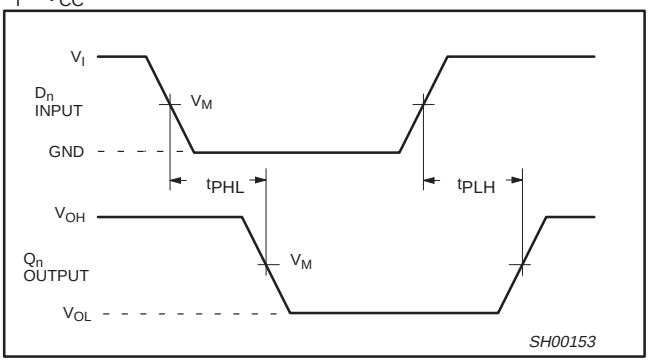
**NOTES:**
1. All typical values are measured $T_{amb}$ = 25°C.
2. Typical value is measured at $V_{CC}$ = 3.3V

## AC WAVEFORMS FOR $V_{CC}$ = 2.3V TO 2.7V AND $V_{CC}$ < 2.3V RANGE

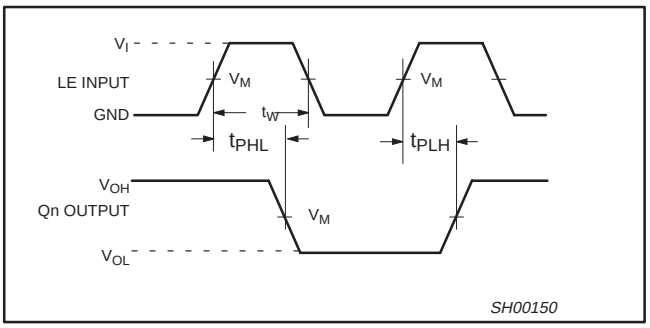
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} – 0.15V$
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

## AC WAVEFORMS FOR $V_{CC}$ = 3.0V TO 3.6V AND $V_{CC}$ = 2.7V RANGE

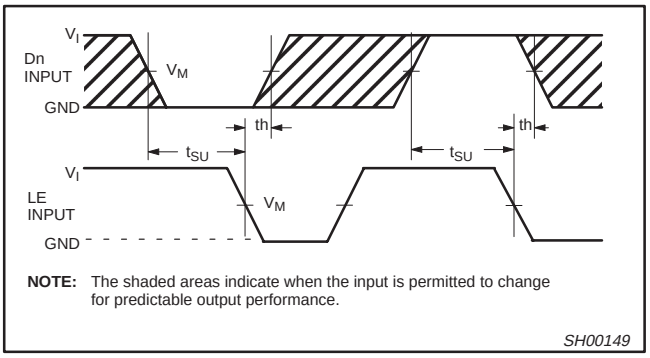
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} – 0.3V$
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$
$V_I = V_{CC}$



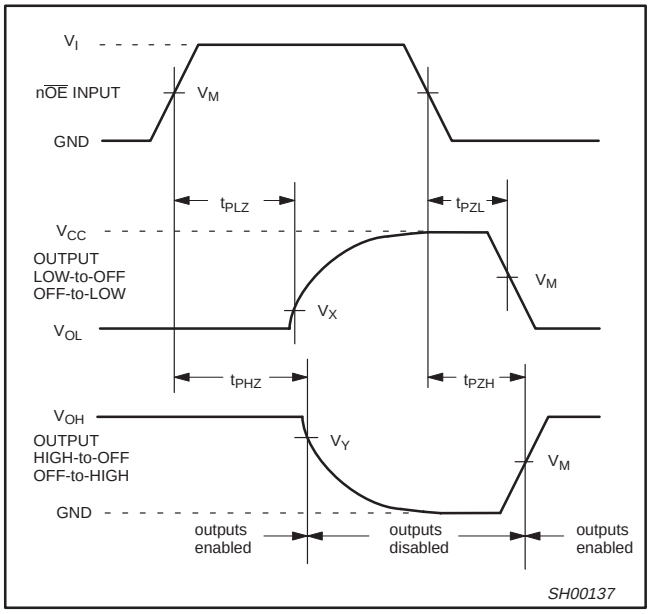

**Waveform 1. The input ($D_n$) to output ($Q_n$) propagation delay**




**Waveform 2. The latch enable (LE) pulse width, the latch enable input to output ($Q_n$) propagation delay**

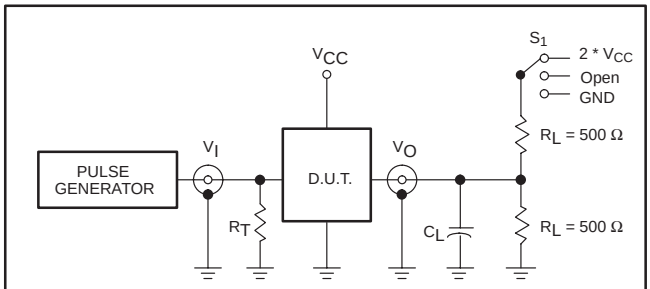



**Waveform 3. The data set up and hold times for the $D_n$ input to the LE input**




**Waveform 4. 3-State enable and disable times**

## TEST CIRCUIT




**Test Circuit for switching times**

### DEFINITIONS

$R_L$ = Load resistor
$C_L$ = Load capacitance includes jig and probe capacitance
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

### SWITCH POSITION

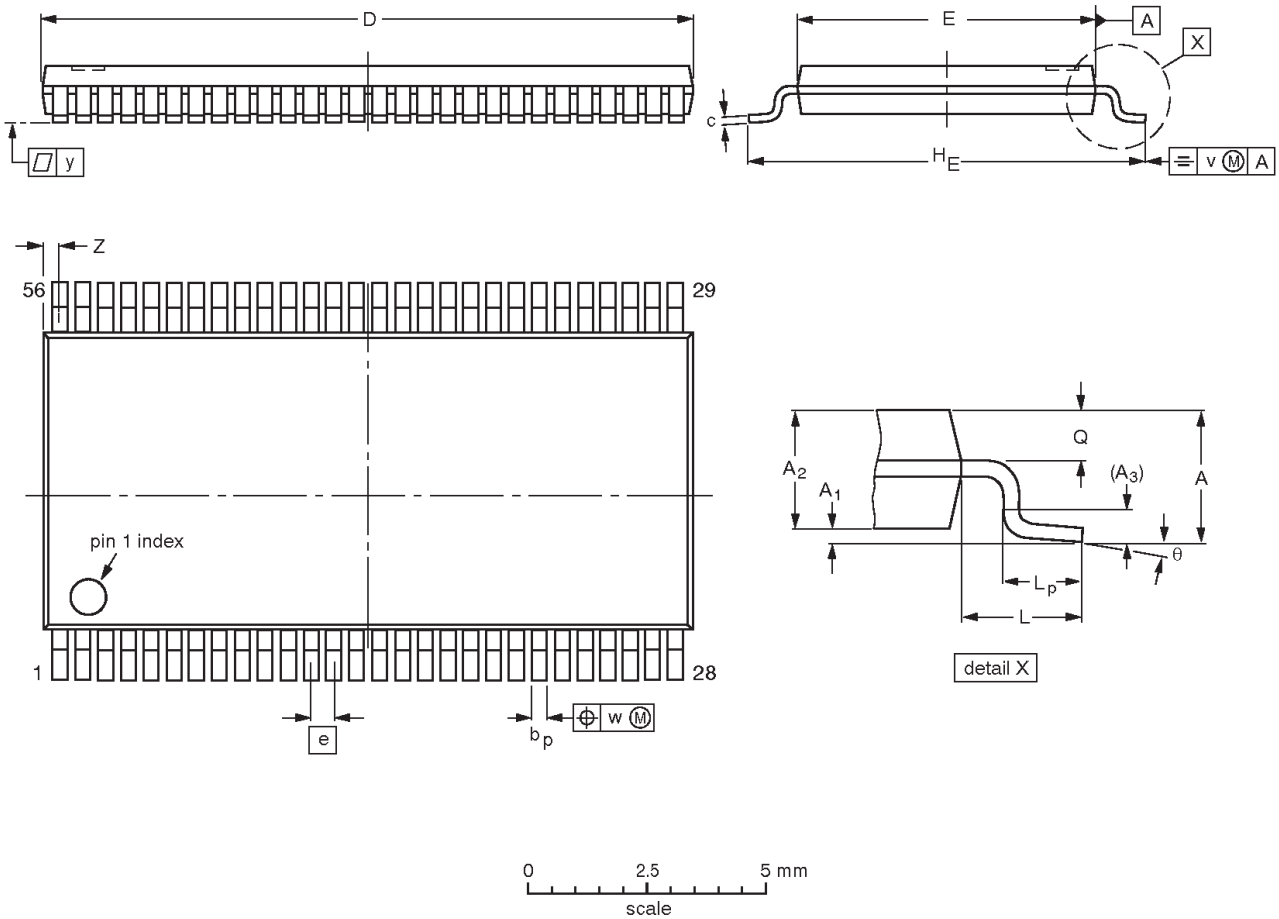
| TEST | $S_1$ |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 * $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $V_I$ |
|---|---|
| < 2.7V | $V_{CC}$ |
| 2.7–3.6V | 2.7V |

SV00906

**Waveform 5. Load circuitry for switching times**

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1.0 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT364-1 | | MO-153EE | | | | | ~~93-02-03~~<br>95-02-10 |

**NOTES**

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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