



2.5V ULTRA-PRECISION 1:4 LVDS FANOUT BUFFER/TRANSLATOR WITH INTERNAL TERMINATION

Precision Edge®
SY89832U

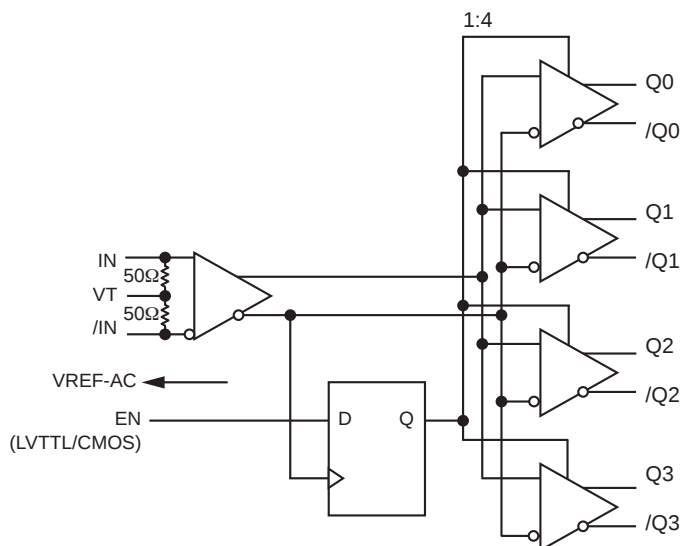
FEATURES

- **Guaranteed AC performance over temperature and voltage:**
 - DC-to >2.0GHz throughput
 - <570ps propagation delay (IN-to-Q)
 - <20ps within-device skew
 - <200ps rise/fall time
- **Ultra-low jitter design:**
 - <1ps_{RMS} cycle-to-cycle jitter
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
 - <10ps_{PP} total jitter (clock)
- **Unique, patent-pending input termination and VT pin accepts DC- and AC-coupled inputs**
- **High-speed LVDS outputs**
- **2.5V voltage supply operation**
- **Industrial temperature range: -40°C to +85°C**
- **Available in 16-pin (3mm x 3mm) MLF® package**

APPLICATIONS

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The SY89832U is a 2.5V, high-speed, 2GHz differential LVDS (Low Voltage Differential Swing) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

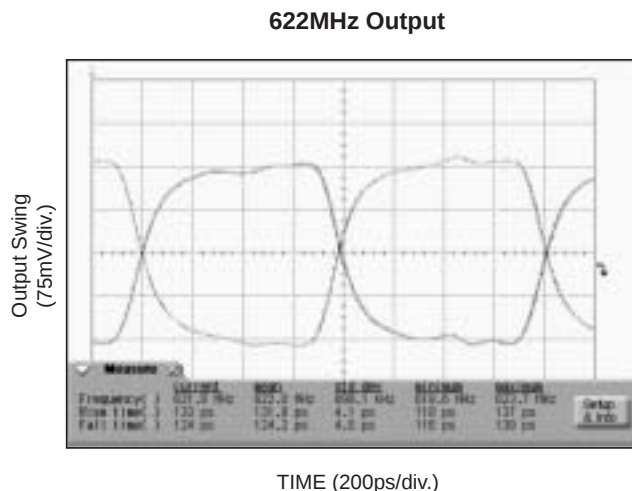
The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF-AC reference output is included for AC-coupled applications.

The SY89832U is a part of Micrel's high-speed clock synchronization family. For 3.3V applications, see SY89833L. For applications that require a different I/O combination, consult Micrel's website at www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

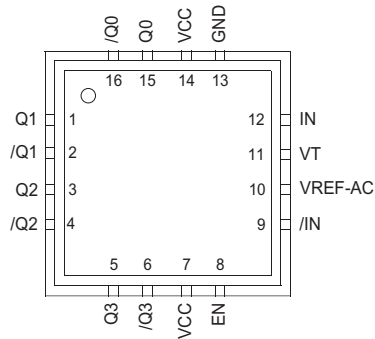


Precision Edge®

TYPICAL PERFORMANCE



PACKAGE/ORDERING INFORMATION



16-Pin MLF® (MLF-16)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89832UMI	MLF-16	Industrial	832U	Sn-Pb
SY89832UMITR ⁽²⁾	MLF-16	Industrial	832U	Sn-Pb
SY89832UMG ⁽³⁾	MLF-16	Industrial	832U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89832UMGTR ^(2, 3)	MLF-16	Industrial	832U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See "LVDS Outputs" section, Figure 2a. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a $25k\Omega$ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signals as small as 100mV . Each pin of a pair internally terminates to a VT pin through 50Ω . Note that these inputs will default to an intermediate state if left open. Please refer to the "Input Interface Applications" section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to $V_{CC}-1.4\text{V}$. They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with $0.01\mu\text{F}$ low ESR capacitor to V_{CC} . See "Input Interface Applications" section for more details. Maximum sink/source current is $\pm 1.5\text{mA}$. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with $0.1\mu\text{F}/0.01\mu\text{F}$ low ESR capacitors and place as close to each VCC pin as possible.

TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 ⁽¹⁾	1 ⁽¹⁾

Note 1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to $V_{CC} + 0.3V$
LVDS Output Current (I_{OUT})	±10mA
Input Current	
Source or Sink Current on (I_N , $/I_N$)	±50mA
VREF-AC Current	
Source or Sink Current on (I_{VT})	±2mA
Lead Temperature (soldering, 20sec.)	260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage Range	+2.375V to 2.625V
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance ⁽³⁾	
MLF®	
(θ_{JA}) Still-Air	60°C/W
(ψ_{JB})	32°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		75	100	mA
R_{IN}	Input Resistance (I_N -to- V_T)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (I_N -to- $/I_N$)		80	100	120	Ω
V_{IH}	Input HIGH Voltage (I_N , $/I_N$)		$V_{CC}-1.2$		V_{CC}	V
V_{IL}	Input LOW Voltage (I_N , $/I_N$)		0		$V_{IH}-0.1$	V
V_{IN}	Input Voltage Swing (I_N , $/I_N$)	see Figure 2c.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing $ I_N - /I_N $	see Figure 2d.	0.2			V
V_{REF-AC}	Output Reference Voltage		$V_{CC}-1.525$	$V_{CC}-1.425$	$V_{CC}-1.325$	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS⁽⁶⁾ $V_{CC} = 2.5V \pm 5\%$, $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 2c.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2d.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		-50		50	mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁶⁾ $V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		-125		30	μA
I_{IL}	Input LOW Current		-300			μA

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

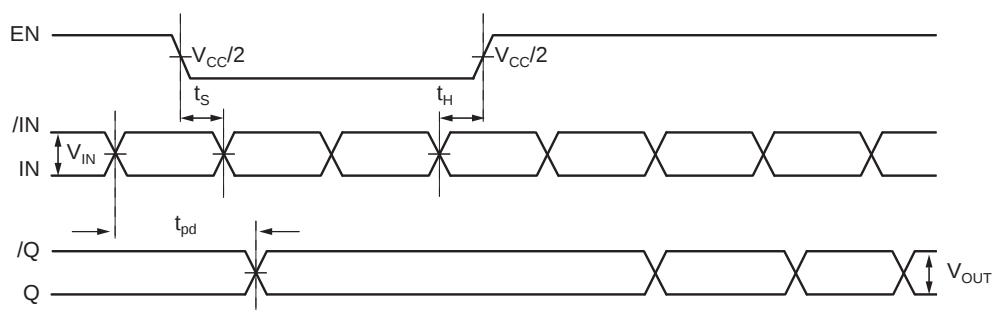
AC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = +2.5V \pm 5\%$ or $+3.3V \pm 10\%$; $R_L = 100\Omega$ across the outputs; $T_A = -40^\circ C$ to $+85^\circ C$ unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	$V_{OUT} \geq 200mV$	2.0	2.5		GHz
t_{pd}	Propagation Delay	IN-to-Q $V_{IN} < 400mV$	370	470	570	ps
		IN-to-Q $V_{IN} \geq 400mV$	300	410	500	ps
t_{SKEW}	Within-Device Skew	Note 8		5	20	ps
	Part-to-Part Skew	Note 9			200	ps
t_S	Set-Up Time	EN to IN, /IN	300			ps
t_H	Hold Time	EN to IN, /IN	300			ps
t_{JITTER}	Data					
	Random Jitter (RJ)	Note 11			1	ps _{RMS}
	Deterministic Jitter (DJ)	Note 12			10	ps _{PP}
	Clock					
	Cycle-to-Cycle Jitter	Note 13			1	ps _{RMS}
	Total Jitter (TJ)	Note 14			10	ps _{PP}
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	70	150	225	ps

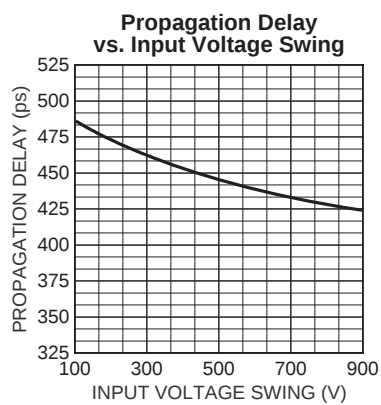
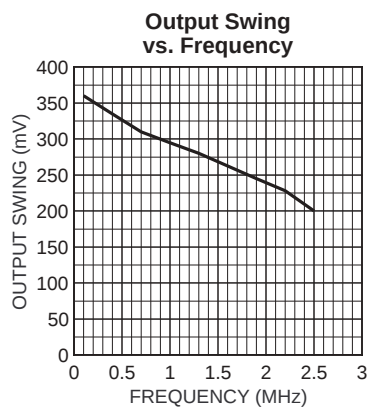
Notes:

- High-frequency AC parameters are guaranteed by design and characterization.
- Within device skew is measured between two different outputs under identical input transitions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
- Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.
- Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
- Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}-1$ PRBS pattern.
- Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs.
 $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TIMING DIAGRAM

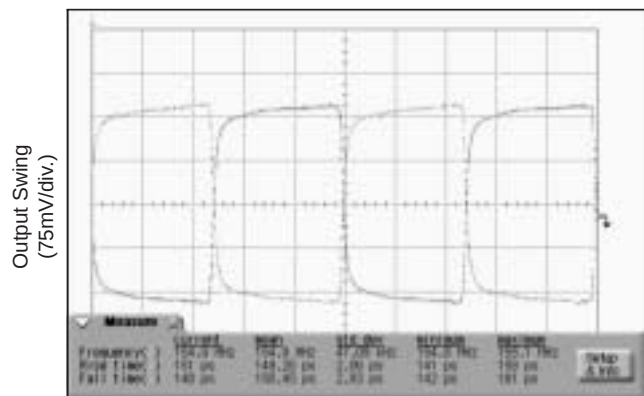
TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 2.5V$, $GND = 0V$, $R_L = 100\Omega$ across the outputs; $T_A = 25^\circ C$, $V_{IN} = 400mV$, unless otherwise stated.

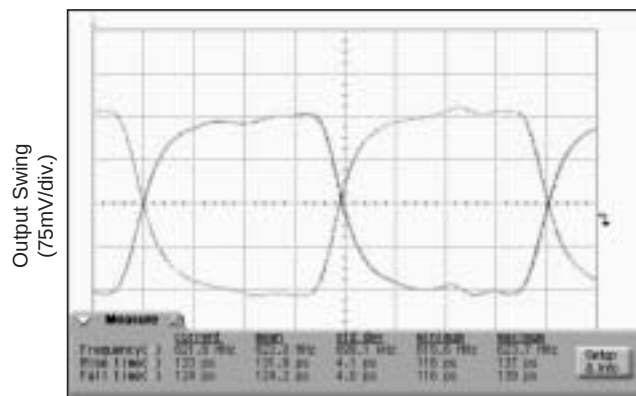


FUNCTIONAL CHARACTERISTICS

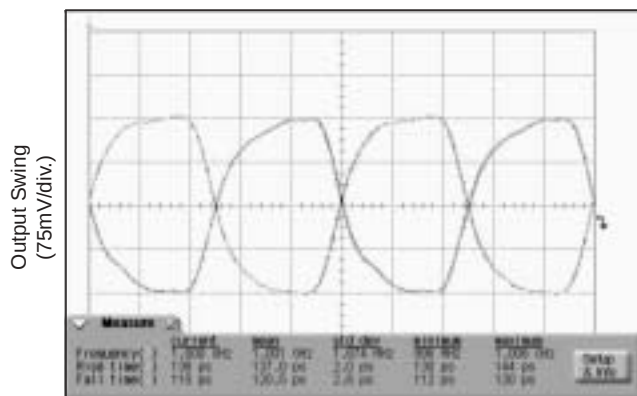
$V_{CC} = 2.5V$, $GND = 0V$, $V_{IN} = 400mV$, $R_L = 100\Omega$ across the outputs; $T_A = 25^\circ C$, unless otherwise stated.

155MHz Output

TIME (1.291ns/div.)

622MHz Output

TIME (200ps/div.)

1GHz Output

TIME (200ps/div.)

INPUT STAGE

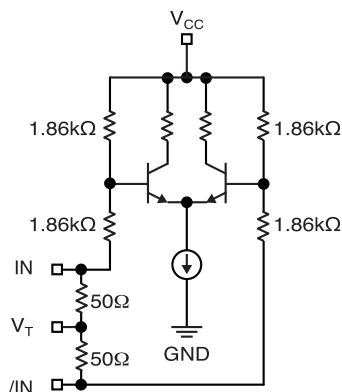


Figure 1. Simplified Differential Input Buffer

LVDS OUTPUTS

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receive

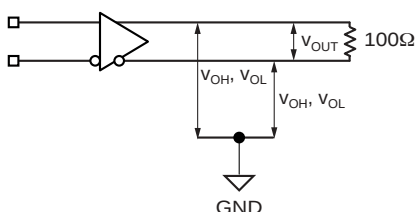


Figure 2a. LVDS Differential Measurement

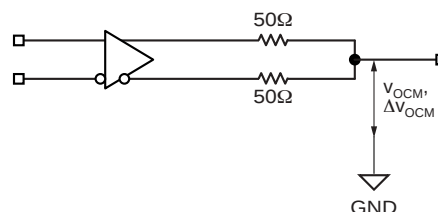


Figure 2b. LVDS Common Mode Measurement

SINGLE-ENDED AND DIFFERENTIAL SWINGS

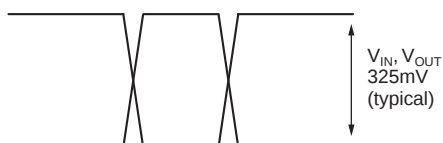


Figure 2c. Single-Ended Swing

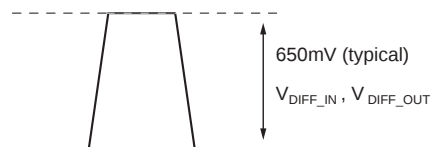


Figure 2d. Differential Swing

INPUT INTERFACE APPLICATIONS

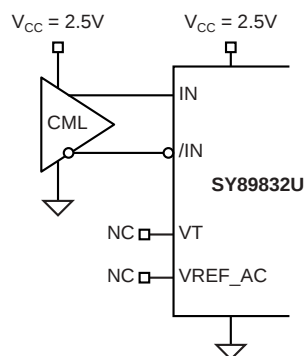


Figure 3a. DC-Coupled CML Input Interface

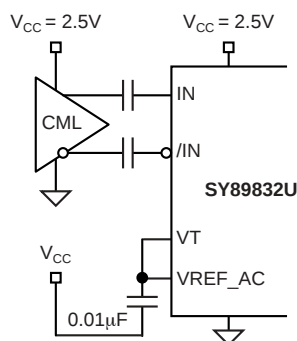


Figure 3b. AC-Coupled CML Input Interface

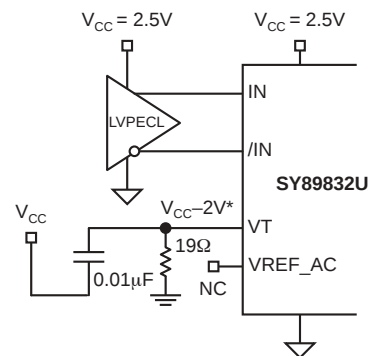


Figure 3c. DC-Coupled LVPECL Input Interface
(*Bypass with 0.01μF to GND)

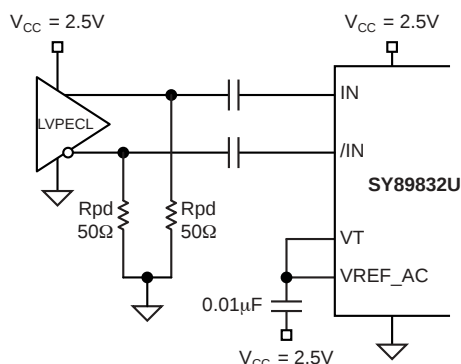


Figure 3d. AC-Coupled LVPECL Input Interface

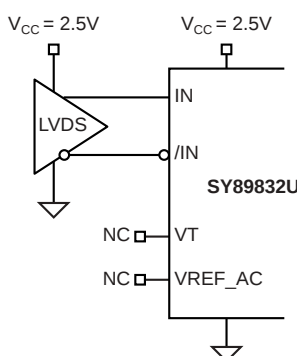
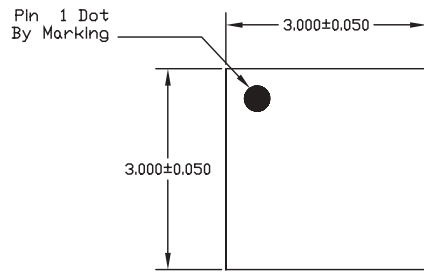
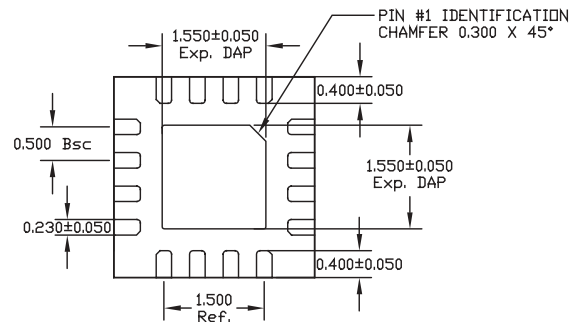
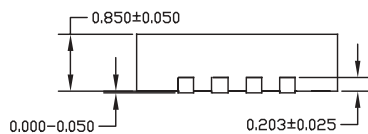


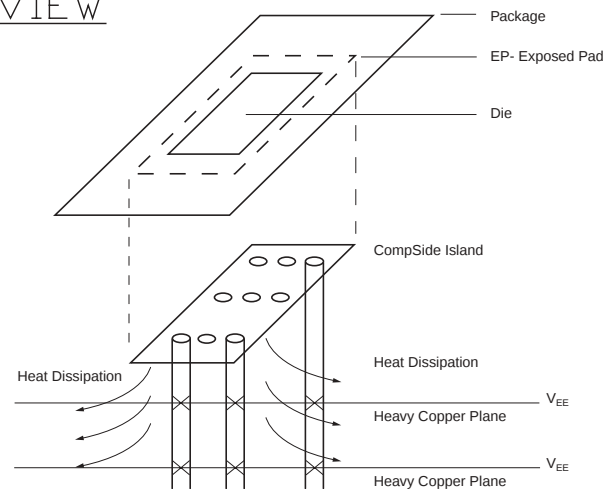
Figure 3e. LVDS Input Interface

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input MUX	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89833U	3.3V Ultra-Precision 1:4 LVDS Fanout Buffer with Internal Termination	http://www.micrel.com/product-info/products/sy89833u.shtml
SY89834U	2.5/3.3V Two Input, 1GHz LVTTTL/CMOS-to-LVPECL 1:4 Fanout Buffer/Translator	http://www.micrel.com/product-info/products/sy89834u.shtml
	16-MLF® Manufacturing Guidelines Exposed Pad Application Note	http://www.amkor.com/products/notes_papers/MLF_appnote_0301.pdf
HBW Solutions	New Products and Applications	http://www.micrel.com/product-info/as/solutions.shtml

16-PIN EPAD MicroLeadFrame® (MLF-16)TOP VIEWBOTTOM VIEWSIDE VIEW**NOTE:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

- Note 1.** Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
- Note 2.** Exposed pads must be soldered to a ground for proper thermal management.

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