

## MAX19005

# Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### General Description

The MAX19005 four-channel, ultra-low-power, pin-electronics IC includes a two-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections for each channel. The driver features a -1V to +5.2V voltage range, includes high-impedance modes, and is highly linear even at low voltage swings. The window comparator features 240MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Low leakage and high impedance are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

This device is available in an 80-pin, 12mm x 12mm body, 0.5mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package for efficient heat removal. The device is specified to operate over the 0°C to +70°C commercial temperature range and features a die temperature monitor output.

**Ordering Information** appears at end of data sheet.

### Features

- ◆ **Small Footprint: Four Channels in 0.3in<sup>2</sup>**
- ◆ **Low-Power Dissipation: 340mW/Channel (typ)**
- ◆ **High Speed: 200Mbps at 3V<sub>p-p</sub>**
- ◆ **-1V to +5.2V Operating Range**
- ◆ **Integrated Pin Switch (with -1V to +24V Off Range)**
- ◆ **Integrated PMU Switches with -1V to +24V Operating Range**
- ◆ **Passive Load**
- ◆ **Low-Leakage Mode by Pin Switch Off: 10nA (max)**
- ◆ **Low Gain and Offset Error**

### Applications

NAND Flash Testers  
DRAM Probe Testers  
Low-Cost Mixed-Signal/System-on-Chip (SoC) Testers  
Active Burn-In Systems  
Structural Testers

For related parts and recommended products to use with this part, refer to: [www.maxim-ic.com/MAX19005.related](http://www.maxim-ic.com/MAX19005.related)

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND.....	-0.3V to +9.4V
V <sub>SS</sub> to GND .....	-6.25V to +0.3V
V <sub>DD</sub> - V <sub>SS</sub> .....	+15.65V
V <sub>L</sub> to GND .....	-0.3V to +5V
DHV <sub>-</sub> , DLV <sub>-</sub> to GND with Integrated Pin Switch Off .....	V <sub>SS</sub> - 0.3V to V <sub>DD</sub> + 0.3V
DHV <sub>-</sub> , DLV <sub>-</sub> to GND with Integrated Pin Switch On .....	V <sub>SSSW</sub> - 0.3V to V <sub>DD</sub> + 0.3V
DATA <sub>-</sub> , RCV <sub>-</sub> , V <sub>BBI</sub> to GND.....	-0.3V to +5V
LDV <sub>-</sub> to GND.....	V <sub>SSSW</sub> - 0.3V to V <sub>DD</sub> + 0.3V
CHV <sub>-</sub> , CLV <sub>-</sub> , COMPHI, COMPL0 to GND.....	V <sub>SS</sub> - 0.3V to V <sub>DD</sub> + 0.3V
CMPL <sub>-</sub> , CMPL <sub>-</sub> , V <sub>BBO</sub> to GND .....	-0.3V to V <sub>DD</sub>
LD, DIN, SCLK, CS, SWEN to GND .....	-0.3V to +V <sub>L</sub>
CHV <sub>-</sub> , CLV <sub>-</sub> to DUT <sub>-</sub> with Integrated Pin Switch On.....	8V
DUT <sub>-</sub> to GND with Integrated Pin Switch Off...V <sub>SSSW</sub> to V <sub>DDSW</sub>	
DUT <sub>-</sub> to GND with Integrated Pin Switch On.....	V <sub>SSSW</sub> to V <sub>DD</sub>
FORCE, SENSE, PMU <sub>-</sub> to GND .....	V <sub>SSSW</sub> to V <sub>DDSW</sub>
V <sub>DDSW</sub> to V <sub>SSSW</sub> .....	+27V

V <sub>DDSW</sub> to V <sub>SS</sub> .....	+31.35V
V <sub>DDSW</sub> to GND.....	-0.3V to +26.1V
V <sub>SSSW</sub> to GND.....	-2.4V to +0.3V
DUT <sub>-</sub> , CMPL <sub>-</sub> , COMPL <sub>-</sub> Short-Circuit Duration.....	Continuous
DOUT to GND .....	-0.3V to +V <sub>L</sub>
TEMP to GND .....	-0.3V to V <sub>DD</sub>
TEMP Short-Circuit Duration .....	Continuous
PMU Force Switch Continuous Current .....	±35mA
PMU Force Switch Peak Current.....	±160mA
PMU Sense Switch Continuous Current.....	±1mA
PMU Sense Switch Peak Current.....	±30mA
All Digital Inputs .....	±30mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
TQFP (derate 35.7mW/°C above +70°C) .....	2857mW
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature .....	+150°C
Lead Temperature (soldering, 10s) .....	+300°C
Soldering Temperature (reflow) .....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +8V, V<sub>SS</sub> = -5V, V<sub>L</sub> = +3V, V<sub>DDSW</sub> = +24.6V, V<sub>SSSW</sub> = -1.25V, V<sub>COMP</sub> = +1V, V<sub>COMP</sub> = 0V, V<sub>LDV<sub>-</sub></sub> = 0V, LOAD EN LOW<sub>-</sub> = LOAD EN HIGH<sub>-</sub> = 0, SWEN = 1, T<sub>J</sub> = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T<sub>J</sub> = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DRIVER (all specifications apply when DUT<sub>-</sub> = DHV<sub>-</sub> or DUT<sub>-</sub> = DLV<sub>-</sub>)</b>						
<b>DC CHARACTERISTICS (R<sub>DUT<sub>-</sub></sub> ≥ 10MΩ, unless otherwise noted)</b>						
Voltage Range			-1.0		+5.2	V
Gain		Measured at 0V and +3V	0.995	1	1.005	V/V
Gain Temperature Coefficient				50		ppm/°C
Offset		V <sub>DHV<sub>-</sub></sub> = +2V, V <sub>DLV<sub>-</sub></sub> = 0V			±10	mV
Offset Temperature Coefficient		V <sub>DHV<sub>-</sub></sub> = +1.5V		±250		μV/°C
Power-Supply Rejection Ratio	PSRR	V <sub>DD</sub> , V <sub>SS</sub> independently varied over full range, V <sub>DHV<sub>-</sub></sub> = +1.5V			±18	mV/V
		V <sub>DDSW</sub> , V <sub>SSSW</sub> independently varied over full range, V <sub>DHV<sub>-</sub></sub> = +1.5V			±10	mV/V
Maximum DC Drive Current	I <sub>DUT<sub>-</sub></sub>		±40			mA
DC Output Resistance		I <sub>DUT<sub>-</sub></sub> = ±10mA, DATA <sub>-</sub> = 1, trim condition, target = 49.5Ω	47.5	49.5	51.5	Ω
DC Output Resistance (V <sub>DDSW</sub> = +15V)		I <sub>DUT<sub>-</sub></sub> = ±10mA, DATA <sub>-</sub> = 1	49.0	52.0	55.0	Ω

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW\_ = LOAD\ EN\ HIGH\_ = 0$ ,  $SWEN = 1$ ,  $T_J = +70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Output Resistance Variation		$I_{DUT\_} = -40mA$ to $+40mA$ , $DATA\_ = 1$ (Note 2)			5.0	$\Omega$
DC Output Resistance Variation ( $V_{DDSW} = +15V$ )		$I_{DUT\_} = -40mA$ to $+40mA$ , $DATA\_ = 1$ (Note 2)			8.0	$\Omega$
DC Crosstalk, $DHV\_$ to $DLV\_$ , $DLV\_$ to $DHV\_$		$V_{DLV\_} = +1.5V$ , $V_{DHV\_} = -1V$ , $+5.2V$			$\pm 5$	mV
		$V_{DHV\_} = +1.5V$ , $V_{DLV\_} = -1V$ , $+5.2V$			$\pm 5$	
Linearity Error		$+1.5V$ (Note 3)			$\pm 5$	mV
		$-1V$ and $+5.2V$ (Note 3)			$\pm 15$	
<b>AC CHARACTERISTICS (<math>R_{DUT\_} = 50\Omega</math> to GND, unless otherwise noted) (Note 4)</b>						
Dynamic Output Current		(Note 5)		$\pm 60$		mA
Drive Mode Overshoot, Undershoot, and Preshoot		$+0.2V$ to $4V_{P-P}$ swing (Note 6)		$5\% + 10$		mV
High-Impedance Mode Spike		$DHV\_/high-Z$ , $V_{DLV\_} = -1V$ , $V_{DHV\_} = 0V$		25		mV
		$DLV\_/high-Z$ , $V_{DLV\_} = 0V$ , $V_{DHV\_} = +1V$		25		
Propagation Delay, Data to Output		$V_{DHV\_} = +3V$ , $V_{DLV\_} = 0V$ , average of $t_{LH}$ and $t_{HL}$	2.5	3.5	5.1	ns
Propagation Delay Temperature Coefficient		$V_{DHV\_} = +3V$ , $V_{DLV\_} = 0V$		1		ps/ $^{\circ}C$
Propagation Delay Match, $t_{LH}$ vs. $t_{HL}$		$V_{DHV\_} = +3V$ , $V_{DLV\_} = 0V$		70		ps
Propagation Delay Skew, Drivers Within Package		$V_{DHV\_} = +3V$ , $V_{DLV\_} = 0V$		100		ps
Propagation Delay Change vs. Pulse Width		Relative to 12.5ns pulse	$3V_{P-P}$ , 40MHz, PW = 4ns to 21ns		$\pm 40$	ps
			$1V_{P-P}$ , 40MHz, PW = 2.5ns to 22.5ns		$\pm 90$	
Propagation Delay Change vs. Common-Mode Voltage		$1V_{P-P}$ , $V_{DLV\_} = 0V$ to $+3V$ , relative to delay at $V_{DLV\_} = +1V$		$\pm 80$		ps
Propagation Delay, Drive to High Impedance, High Impedance to Drive		$V_{DHV\_} = +1.5V$ , $V_{DLV\_} = -1V$ , average of both directions of $t_{LH}$ and $t_{HL}$		3.9		ns
Minimum Voltage Swing		(Note 7)		100		mV

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMP HI} = +1V$ ,  $V_{COMP LO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD EN LOW\_ = LOAD EN HIGH\_ = 0$ ,  $SWEN = 1$ ,  $T_J = +70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall Time (Average Rise/Fall Time)		$V_{D HV\_} = +0.2V$ , $V_{D LV\_} = 0V$ , 20% to 80%		0.8		ns
		$V_{D HV\_} = +1V$ , $V_{D LV\_} = 0$ , 20% to 80%		0.8		
		$V_{D HV\_} = +3V$ , $V_{D LV\_} = 0V$ , 10% to 90%	1.4	2.0	2.7	
		$V_{D HV\_} = +4V$ , $V_{D LV\_} = 0V$ , $R_{D UT\_} = 500\Omega$ , 10% to 90%		2.5		
		$V_{D HV\_} = +5V$ , $V_{D LV\_} = 0V$ , $R_{D UT\_} = 500\Omega$ , 10% to 90%		3.1		
Rise/Fall Time Matching		$V_{D HV\_} = +0.2V$		$\pm 50$		%
		$V_{D HV\_} = +1V$	$V_{D LV\_} = 0V$	$\pm 15$		
		$V_{D HV\_} = +3V$ and $+5V$		$\pm 5$		
Minimum Pulse Width (Average Positive/Negative Pulse) (Note 8)		$0.2V_{P-P}$ , $V_{D HV\_} = +0.2V$ , $V_{D LV\_} = 0V$		1.8		ns
		$1V_{P-P}$ , $V_{D HV\_} = +1V$ , $V_{D LV\_} = 0V$		2.0		
		$3V_{P-P}$ , $V_{D HV\_} = +3V$ , $V_{D LV\_} = 0V$		2.6		
<b>COMPARATOR (driver in high-impedance mode) (Note 9)</b>						
<b>DC CHARACTERISTICS</b>						
Input Voltage Range			-1.0		+5.2	V
Differential Input Voltage		$V_{D UT\_} - V_{CHV\_}$ , $V_{D UT\_} - V_{CLV\_}$	-6.2		+6.2	V
Hysteresis		$V_{CHV\_} = V_{CLV\_} = +1.5V$		8		mV
Input Offset Voltage		$V_{D UT\_} = +1.5V$ , $V_{COMP HI} = +0.8V$ , $V_{COMP LO} = +0.2V$ (Note 10)			$\pm 10$	mV
Input Offset Temperature Coefficient		(Note 10)		$\pm 25$		$\mu V/^{\circ}C$
Common-Mode Rejection Ratio	CMRR	$V_{D UT\_} = 0V$ and $+3V$ (Note 10)	60			dB
Linearity Error		$V_{D UT\_} = +1.5V$ (Notes 3, 10)			$\pm 5$	mV
		$V_{D UT\_} = -1V$ , $+5.2V$ (Notes 3, 10)			$\pm 10$	
Power-Supply Rejection Ratio	PSRR	$V_{D UT\_} = +1.5V$ , $V_{DD}$ , $V_{SS}$ , $V_{DDSW}$ , $V_{SSSW}$ supplies independently varied over full range (Note 10)			$\pm 5$	mV/V
<b>AC CHARACTERISTICS (Note 11)</b>						
Equivalent Input Bandwidth		$V_{D LV\_} = 0V$ termination mode, $V_{D UT\_} = 1V_{P-P}$ , $t_R = t_F = 500ps$ input, calculated from 10% to 90% redigitization waveform		300		MHz
Prop Delay		$V_{D UT\_} = 1V_{P-P}$ , $V_{CHV\_}$ or $V_{CLV\_} = +0.5V$	1.1	2.0	3.3	ns
Prop-Delay Temperature Coefficient		$V_{D UT\_} = 1V_{P-P}$ , $V_{CHV\_}$ or $V_{CLV\_} = +0.5V$		2		ps/ $^{\circ}C$
Prop-Delay Match, $t_{LH}$ to $t_{HL}$		Absolute value of delta for each comparator, $V_{D UT\_} = 1V_{P-P}$		$\pm 250$		ps

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW\_ = LOAD\ EN\ HIGH\_ = 0$ ,  $SWEN = 1$ ,  $T_J = +70^\circ C$  with an accuracy of  $\pm 15^\circ C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+90^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL), $V_{DUT\_} = 1V_{P-P}$		$\pm 100$		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 12)		$V_{CHV\_}$ or $V_{CLV\_} = 0$ to $+4.9V$ , $V_{DUT\_} = 0.2V_{P-P}$		$\pm 20$		ps
		$V_{CHV\_}$ or $V_{CLV\_} = -0.9$ to $+4.9V$ , $V_{DUT\_} = 0.2V_{P-P}$		$\pm 30$		
Prop-Delay Dispersions vs. Overdrive		$V_{DLV\_} = 0V$ termination mode, $V_{DUT\_} = 1V_{P-P}$ , $t_R = t_F = 500ps$ input, 90% (rising edge) and 10% (falling edge) relative to timing at 50% point		$\pm 600$		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width		$\pm 60$		ps
Prop-Delay Dispersions vs. Slew Rate		$+0.5V/ns$ to $+2V/ns$		$\pm 50$		ps
<b>LOGIC INPUTS AND OUTPUTS (COMPHI, COMPLO, CMPH_, CMPL_, V<sub>BBO</sub>)</b>						
Input Voltage Range, $V_{COMPHI}$ and $V_{COMPLO}$			0		3.6	V
Differential Input Voltage, $V_{COMPHI} - V_{COMPLO}$		$V_{COMPHI} \geq V_{COMPLO}$ , $CMPH\_ and$ $CMPL\_ with no load$	0		3.6	V
Differential Input Voltage, $V_{COMPHI} - V_{COMPLO}$		$V_{COMPHI} \geq V_{COMPLO}$ , $CMPH\_ and$ $CMPL\_ with 50\Omega to V_{TTCMP}, V_{COMPHI} \geqV_{TTCMP} \geq V_{COMPLO}$	0		1.0	V
Reference Output, $V_{BBO}$		Relative to $(V_{COMPHI} + V_{COMPLO})/2$ at $V_{COMPHI} = +1V$ and $V_{COMPLO} = 0V$			$\pm 50$	mV
Output High-Voltage Offset		$I_{OUT} = 0mA$ , relative to $V_{COMPHI}$ at $V_{COMPHI} = +1V$			$\pm 65$	mV
Output Low-Voltage Offset		$I_{OUT} = 0mA$ , relative to $V_{COMPLO}$ at $V_{COMPLO\_} = 0V$			$\pm 65$	mV
Output Resistance, $CMPH\_ and$ $CMPL\_$		$I_{CMPH\_} = I_{CMPL\_} = \pm 10mA$ , $V_{COMPHI} =$ $+1V$ , $V_{COMPLO} = 0V$ , $CMPH\_ ,$ $CMPL\_ at$ high-level output	40	50	60	$\Omega$
Maximum Current Limit, $CMPH\_ and$ $CMPL\_$		$V_{COMPHI} = +1.8V$ , $V_{COMPLO} = 0V$ , $CMPH\_ ,$ $CMPL\_ at$ high-level output, $V_{FORCE} = 0V, +3.6V$	-15		+15	mA
Maximum Current Limit, $V_{BBO}$		$V_{COMPHI} = +1V$ , $V_{COMPLO} = 0V$ , at $V_{BBO} = +0.5V$ output	-1		+1	mA

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW\_ = LOAD\ EN\ HIGH\_ = 0$ ,  $SWEN = 1$ ,  $T_J = +70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall Time, CMPH_ and CMPL_		20% to 80%, $V_{COMPHI\_} = +1V$ , $V_{COMPLO} = 0V$ , load = T-line, $50\Omega > 1ns$ , $50\Omega$ to GND		0.7		ns
<b>PASSIVE LOAD (driver in high-impedance mode) (Note 13)</b>						
<b>DC CHARACTERISTICS <math>R_{DUT\_} \geq 10M\Omega</math>, unless otherwise noted)</b>						
LDV_ Voltage Range			-1.0		+5.2	V
Gain		Measured at 0V and +3V	0.99		1.01	V/V
Gain Temperature Coefficient		Measured at 0V and +3V		50		ppm/ $^{\circ}C$
Offset		$V_{LDV\_} = +1.5V$			$\pm 100$	mV
Offset Temperature Coefficient				0.02		mV/ $^{\circ}C$
Power-Supply Rejection Ratio	PSRR	$V_{DD}$ and $V_{SS}$ independently varied over full range, $V_{LDV\_} = +1.5V$	-18		+18	mV/V
		$V_{DDSW}$ and $V_{SSSW}$ independently varied over full range, $V_{LDV\_} = +1.5V$	-10		+10	mV/V
Output Resistance Tolerance— High Value		$I_{DUT\_} = \pm 2mA$ , $V_{LDV\_} = +1.5V$	710	750	790	$\Omega$
Output Resistance Tolerance— Low Value		$I_{DUT\_} = \pm 4mA$ , $V_{LDV\_} = +1.5V$	335	375	415	$\Omega$
Output Resistance, Tolerance— High Value ( $V_{DDSW} = +15V$ )		$I_{DUT\_} = \pm 2mA$ , $V_{LDV\_} = +1.5V$	735	800	865	$\Omega$
Output Resistance, Tolerance— Low Value ( $V_{DDSW} = +15V$ )		$I_{DUT\_} = \pm 4mA$ , $V_{LDV\_} = +1.5V$	360	425	490	$\Omega$
Switch Resistance Variation		0 to +3V (relative to +1.5V)		$\pm 10$		%
		Full range (relative to +1.5V)		$\pm 30$		
Switch Resistance Variation ( $V_{DDSW} = +15V$ )		0 to +3V (relative to +1.5V)		$\pm 10$		%
		Full range (relative to +1.5V)		$\pm 30$		
Maximum Output Current		$V_{LDV\_} = -1V$ , $V_{DUT\_} = +5V$	-4			mA
		$V_{LDV\_} = +5V$ , $V_{DUT\_} = -1V$			+4	
Linearity Error, Full Range		Measured at -1V, +1.5V, and +5.2V (Notes 3, 14)			$\pm 25$	mV
<b>AC CHARACTERISTICS</b>						
Settling Time, LDV_ to Output		$V_{LDV\_} = -1V$ to +5V step, $R_{DUT\_} = 100k\Omega$ (Note 15)		0.5		$\mu s$
Output Transient Response		$V_{LDV\_} = +1.5V$ , $V_{DUT\_} = -1V$ to +5V square wave at 1MHz, $R_{DUT\_} = 50k\Omega$		20		ns

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPL0} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW\_ = LOAD\ EN\ HIGH\_ = 0$ ,  $SWEN = 1$ ,  $T_J = +70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>PMU SWITCHES (FORCE, SENSE, PMU_) (Note 13)</b>						
Voltage Range			-1.0		+24	V
Voltage Range ( $V_{DDSW} = +15V$ )			-1.0		+10	V
Force Switch Resistance		$V_{FORCE} = +1.5V$ , $I_{PMU\_} = \pm 10mA$			40	$\Omega$
Force Switch Resistance ( $V_{DDSW} = +15V$ )		$V_{FORCE} = +1.5V$ , $I_{PMU\_} = \pm 10mA$			47	$\Omega$
Force Path Current		$V_{PMU\_} = -1V$ to $+24V$ , $V_{FORCE} = -1V$ to $+24V$			$\pm 30$	mA
Force Path Current ( $V_{DDSW} = +15V$ )		$V_{PMU\_} = -1V$ to $+10V$ , $V_{FORCE} = -1V$ to $+10V$			$\pm 30$	mA
Force Switch Resistance Variation		0V to +3V (relative to $V_{FORCE} = +1.5V$ )		$\pm 10$		%
		Full range (Note 16)		$\pm 40$		
Force Switch Resistance Variation ( $V_{DDSW} = +15V$ )		0V to +3V (relative to $V_{FORCE} = +1.5V$ )		$\pm 15$		%
		Full range (Note 16)		$\pm 45$		
Sense Switch Resistance		$V_{SENSE} = +1.5V$ , $I_{PMU\_} = \pm 0.4mA$	650	1000	1350	$\Omega$
Sense Switch Resistance ( $V_{DDSW} = +15V$ )		$V_{SENSE} = +1.5V$ , $I_{PMU\_} = \pm 0.4mA$	850	1250	1800	$\Omega$
Sense Switch Resistance Variation		Relative to +11.5V, full range		$\pm 40$		%
Sense Switch Resistance Variation ( $V_{DDSW} = +15V$ )		Relative to +4.5V, full range		$\pm 40$		%
PMU_ Capacitance		Force and sense switches open		6		pF
FORCE Capacitance		All channels of force and sense switches open		36		pF
SENSE Capacitance		All channels of force and sense switches open		8		pF
FORCE External Capacitance		Allowable external capacitance		2		nF
SENSE External Capacitance		Allowable external capacitance		1		nF
FORCE and SENSE Switching Speed		Connect, $PMU\_ = +5V$ , FORCE or SENSE 10M $\Omega$    8pF		10		$\mu s$
		Disconnect, $PMU\_ = +5V$ , FORCE or SENSE 10M $\Omega$    8pF		100		
PMU_ Leakage		$SWEN = 0$ , or $PMU\ EN\_ = 0$ , $V_{FORCE\_} = V_{SENSE\_} = -1V$ to $+24V$		$\pm 0.5$	$\pm 5$	nA
PMU_ Leakage ( $V_{DDSW} = +15V$ )		$SWEN = 0$ , or $PMU\ EN\_ = 0$ , $V_{FORCE\_} = V_{SENSE\_} = -1V$ to $+10V$		$\pm 0.5$	$\pm 5$	nA

# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ , LOAD EN LOW\_ = LOAD EN HIGH\_ = 0, SWEN = 1,  $T_J = +70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>TOTAL FUNCTION</b>						
<b>DUT_</b>						
Leakage, High-Impedance Mode		Passive load switches open, pin switch short, $V_{DUT\_} = +5.2V$ , $V_{CLV\_} = V_{CHV\_} = -1V$ , $V_{DUT\_} = -1V$ , $V_{CLV\_} = V_{CHV\_} = +5.2V$ , full range			2	$\mu A$
Low-Leakage Recovery Time		Confirmed simulation only (Note 17)		10		$\mu s$
Combined Capacitance		High-impedance mode, passive load switches open, pin switch short		10		pF
Load Resistance Range		(Note 18)		1		$G\Omega$
Load Capacitance Range		(Note 18)		12		nF
Leakage, Pin Switch Off Mode		-1V to +24V, pin switch open		$\pm 1$	$\pm 10$	nA
Leakage, Pin Switch Off Mode ( $V_{DDSW} = +15V$ )		-1V to +10V, pin switch open		$\pm 1$	$\pm 10$	nA
Pin Switch Switching Speed		Connect or disconnect, $V_{DH\_} = +5V$ , $DUT\_ = 10M\Omega \parallel 8pF$		10		$\mu s$
<b>VOLTAGE REFERENCE INPUTS (DHV_, DLV_, CHV_, CLV_, LDV_, COMPHI, COMPLO)</b>						
Input Bias Current					$\pm 100$	$\mu A$
<b>SINGLE-ENDED CONTROL INPUTS (DATA_, RCV_)</b>						
Input High Voltage			$V_{BBI} + 0.2$		3.2	V
Input Low Voltage			0	$V_{BBI} - 0.2$		V
Voltage Between Inputs and $V_{BBI}$			$V_{BBI} - 1.6$	$V_{BBI} + 1.6$		V
Input Offset Voltage				$\pm 50$		mV
Input Bias Current					$\pm 100$	$\mu A$
<b>REFERENCE INPUT (<math>V_{BBI}</math>)</b>						
Input Voltage Range			0.2		3.0	V
Input Bias Current					$\pm 100$	$\mu A$
<b>DIGITAL INPUTS (<math>\overline{LD}</math>, DIN, SCLK, <math>\overline{CS}</math>)</b>						
Input High Voltage		(Note 19)	$2/3 (V_L)$		$V_L$	V
Input Low Voltage		(Note 19)	-0.1		$1/3 (V_L)$	V
Input Bias Current					$\pm 1$	$\mu A$
<b>SERIAL-DATA OUTPUT (DOUT)</b>						
Output High Voltage		$I_{OH} = -1mA$	$V_L - 0.4$		$V_L + 0.1$	V
Output Low Voltage		$I_{OL} = +1mA$	$V_{DGND} - 0.1$		$V_{DGND} + 0.4$	V
Output Rise-and-Fall Time		$C_L = 10pF$		5.0		ns



# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW\_ = LOAD\ EN\ HIGH\_ = 0$ ,  $SWEN = 1$ ,  $T_J = +70^\circ C$  with an accuracy of  $\pm 15^\circ C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+90^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Low to DOUT Delay		$C_L = 10pF$	4		45	ns
<b>SERIAL-INTERFACE TIMING</b>						
SCLK Frequency					20	MHz
SCLK Pulse-Width High	$t_{CH}$		20			ns
SCLK Pulse-Width Low	$t_{CL}$		20			ns
$\overline{CS}$ Low to SCLK High Setup	$t_{CSS0}$		5			ns
SCLK High to $\overline{CS}$ Low Hold	$t_{CSH0}$		0			ns
$\overline{CS}$ High to SCLK High Setup	$t_{CSS1}$		20			ns
SCLK High to $\overline{CS}$ High Hold	$t_{CSH1}$		20			ns
DIN to SCLK High Setup	$t_{DS}$		10			ns
DIN to SCLK High Hold	$t_{DH}$		10			ns
$\overline{CS}$ High to $\overline{LD}$ Low Hold	$t_{CSHLD}$		20			ns
$\overline{CS}$ High Pulse Width	$t_{CSWH}$		20			ns
$\overline{LD}$ Low Pulse Width	$t_{LDW}$		20			ns
$V_L$ Rising to $\overline{CS}$ Low		Power-on delay		2		$\mu s$
<b>TEMPERATURE SENSOR</b>						
Nominal Voltage		$T_J = +70^\circ C$ , $R_L \geq 10M\Omega$		3.43		V
Temperature Coefficient				+10		mV/ $^\circ C$
Output Resistance				17		k $\Omega$
<b>POWER SUPPLIES</b>						
Positive Supply Voltage	$V_{DD}$	(Note 20)	7.6	8	8.4	V
Negative Supply Voltage	$V_{SS}$	(Note 20)	-5.25	-5	-4.75	V
Logic Supply Voltage	$V_L$		2.3	3	3.6	V
Switch Positive Supply Voltage	$V_{DDSW}$	(Notes 20, 21)	24.1	24.6	25.1	V
Switch Positive Supply Voltage	$V_{DDSW}$	(Notes 20, 22)	14.5	15	15.5	V
Switch Negative Supply Voltage	$V_{SSSW}$	(Note 20)	-1.4	-1.25	-1.1	V
Positive Supply Current	$I_{DD}$	$f_{OUT} = 0MHz$		105	120	mA
Negative Supply Current	$I_{SS}$	$f_{OUT} = 0MHz$		105	120	mA
Logic Supply Current	$I_L$	$f_{OUT} = 0MHz$		1	4	mA
Switch Positive Supply Current	$I_{DDSW}$	$f_{OUT} = 0MHz$		2	6	mA
Switch Negative Supply Current	$I_{SSSW}$	$f_{OUT} = 0MHz$		1.5	5	mA
Static Power Dissipation		$f_{OUT} = 0MHz$		1.35	1.56	W
Operating Power Dissipation		$f_{OUT} = 100Mbps$ (Note 23)		1.45		W

# Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{DDSW} = +24.6V$ ,  $V_{SSSW} = -1.25V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ , LOAD EN LOW\_ = LOAD EN HIGH\_ = 0, SWEN = 1,  $T_J = +70^{\circ}C$  with an accuracy of  $\pm 15^{\circ}C$ . Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at  $T_J = +50^{\circ}C$  to  $+90^{\circ}C$ , unless otherwise noted.) (Note 1)

- Note 1:** All minimum and maximum DC, rise/fall time at +3V swing tests are 100% production tested. The propagation-delay data to output and propagation-delay comparator tests are guaranteed by design. All specifications are with DUT\_ and PMU\_ electrically isolated, unless otherwise noted.
- Note 2:** Resistance measurements are made using  $\pm 2.5mA$  current changes in the loading instrument about the noted value. Absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity. Test conditions are at  $I_{DUT\_} = \pm 1mA$ ,  $\pm 12mA$ , and  $\pm 40mA$ , respectively.
- Note 3:** Relative to a straight line through 0V and +3V.
- Note 4:**  $V_{DHFV\_} = +3V$ ,  $V_{DLV\_} = 0V$ , unless otherwise specified. DATA\_ and RCV\_  $V_{HIGH} = +2V$ ,  $V_{LOW} = 1V$ ,  $V_{BBI} = +1.5V$ .
- Note 5:** Current supplied for a minimum of 10ns. Verified to be greater than or equal to DC drive current by design and characterization.
- Note 6:** Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
- Note 7:** At the minimum voltage swing, undershoot is less than 20%. DHV\_ and DLV\_ references are adjusted to result in the specified swing.
- Note 8:** At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA\_.
- Note 9:** With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
- Note 10:** Measured by using a servo to locate comparator thresholds.
- Note 11:** Unless otherwise noted, all propagation delays are measured at 40MHz,  $V_{DUT\_} = 0$  to +1V,  $V_{CHV\_} = V_{CLV\_} = +0.5V$ ,  $t_R = t_F = 500ps$ ,  $Z_S = 50\Omega$ , driver in high-impedance mode. Comparator outputs are terminated with  $50\Omega$  to GND. Measured from  $V_{DUT\_}$  crossing calibrated CHV\_/CLV\_ threshold to midpoint of nominal comparator output swing.
- Note 12:**  $V_{DUT\_} = 200mV_{P-P}$ . Propagation delay is compared to a reference time at +2V.
- Note 13:** Operating output voltage/current range of passive load and PMU force switch at +24.6V supply. See Figure 1.
- Note 14:** LOAD EN LOW\_ = LOAD EN HIGH\_ = 1.
- Note 15:** Waveform settles to within 5% of final value into  $100k\Omega$  load.
- Note 16:**  $I_{PMU\_} = \pm 2mA$  at  $V_{FORCE} = -1V$ , +11.5V, and +24V. Percent variation relative to value calculated at  $V_{FORCE} = +11.5V$ .
- Note 17:** Time to return to the specified maximum leakage after a +3V, +4V/ns step at DUT\_.
- Note 18:** Load at end of 2ns transmission line; for stability only, AC performance could be degraded.
- Note 19:** The driver meets all of its timing specifications at the specified digital input voltages.
- Note 20:** Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
- Note 21:** DUT\_ (pin switch off), PMU\_ maximum voltage is +24V.
- Note 22:** DUT\_ (pin switch off), PMU\_ maximum voltage is +10V.
- Note 23:** All channels driven at  $3V_{P-P}$ , load = 2ns,  $50\Omega$  transmission line terminated with 3pF.

# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

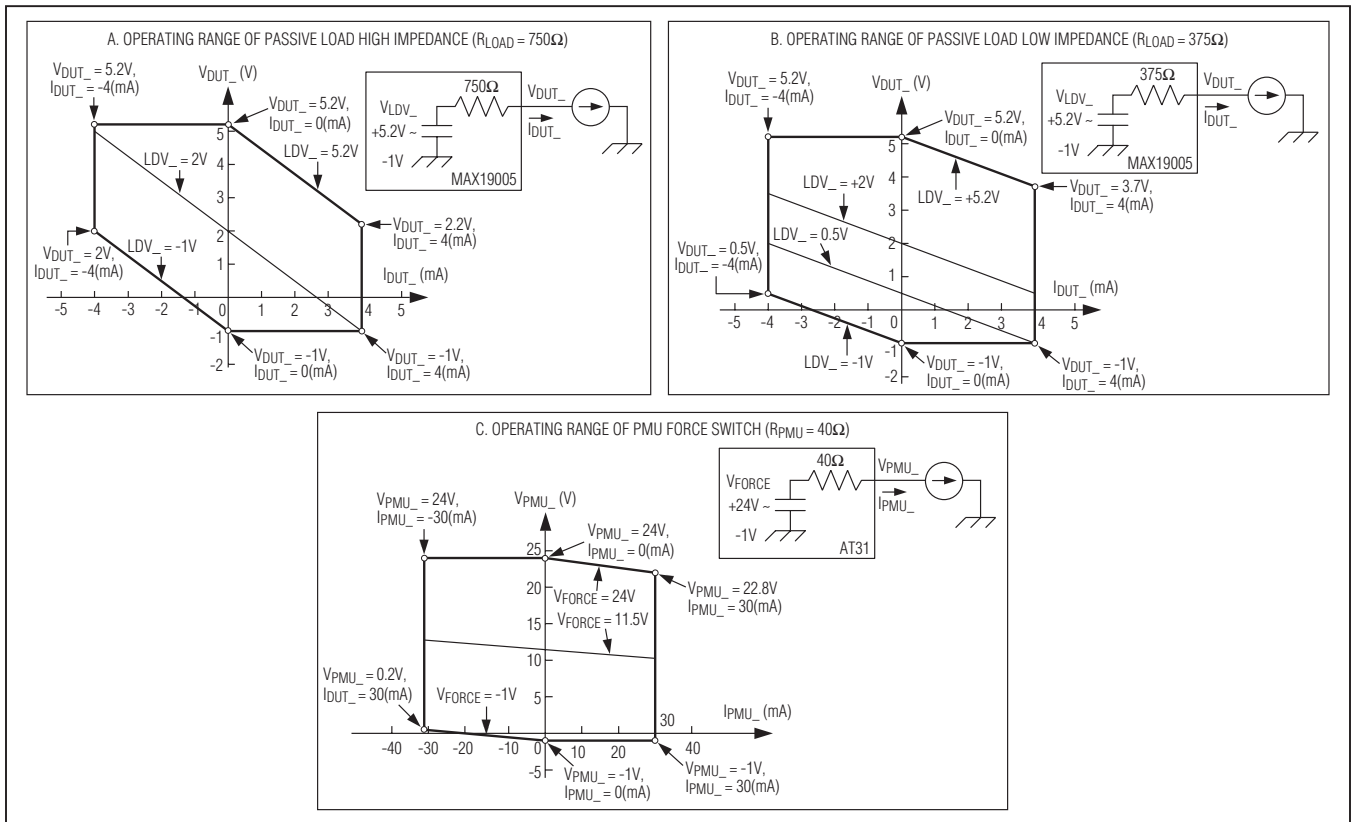


Figure 1. Operating Ranges

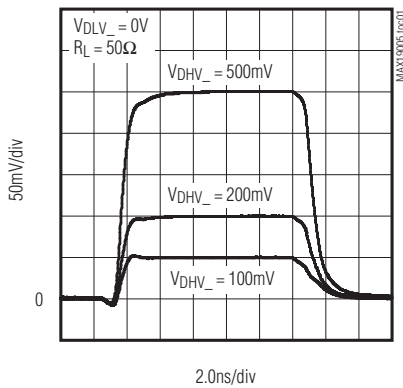
# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

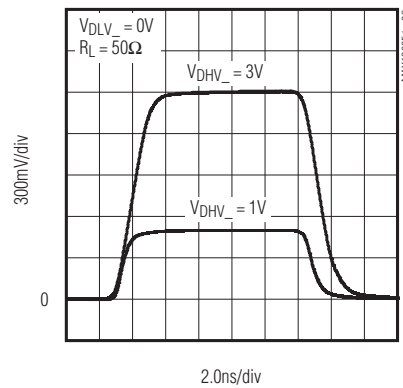
### Typical Operating Characteristics

( $V_{DD} = 8V$ ,  $V_{SS} = -5V$ ,  $V_L = 3V$ ,  $V_{DDSW} = 24.6V$ ,  $V_{SSSW} = 1.25V$ ,  $V_{COMPHI} = 1V$ ,  $V_{COMPL0} = 0V$ ,  $V_{LDV\_} = 0V$ , LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients  $T_J = +70^\circ C$  are measured at  $T_J = +50^\circ C$  to  $+90^\circ C$ , unless otherwise noted.)

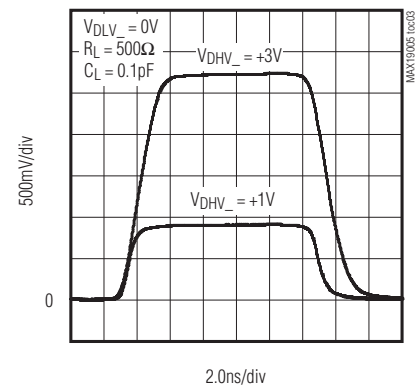
**DRIVER SMALL-SIGNAL RESPONSE**



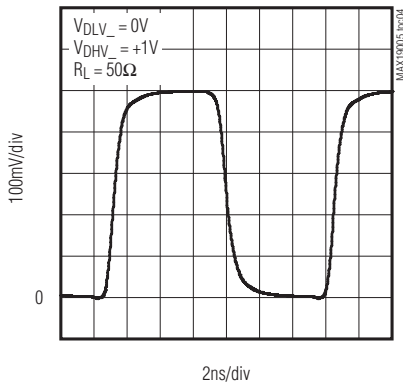
**DRIVER LARGE-SIGNAL RESPONSE**



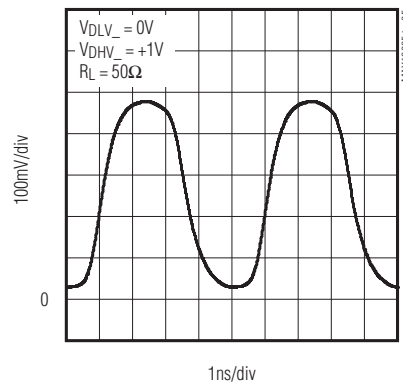
**DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω**



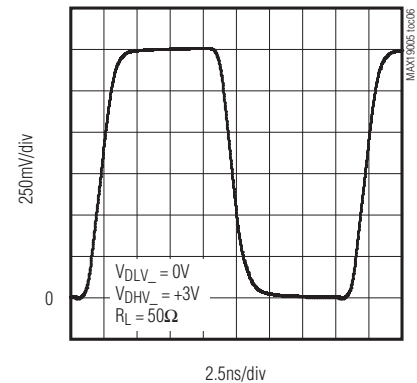
**DRIVER 1Vp-p, 150Mbps SIGNAL RESPONSE**



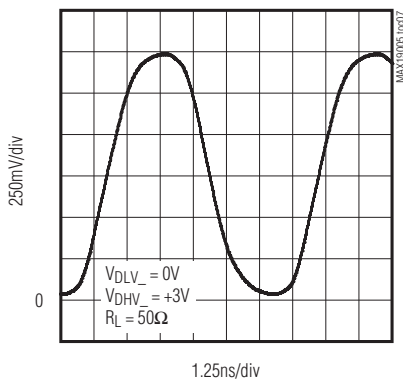
**DRIVER 1Vp-p, 400Mbps SIGNAL RESPONSE**



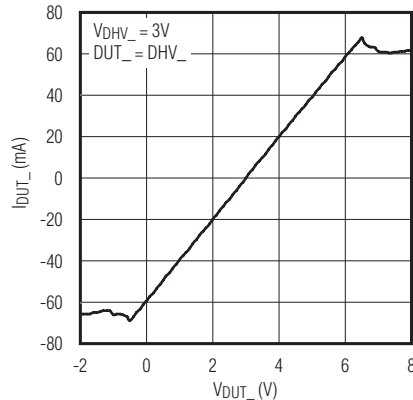
**DRIVER 3Vp-p, 100Mbps SIGNAL RESPONSE**



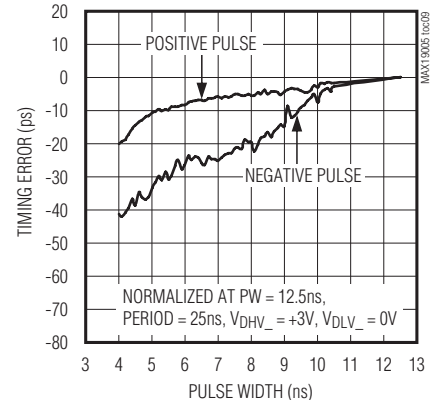
**DRIVER 3Vp-p, 250Mbps SIGNAL RESPONSE**



**DRIVER DC CURRENT—LIMIT RESPONSE**



**DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH**

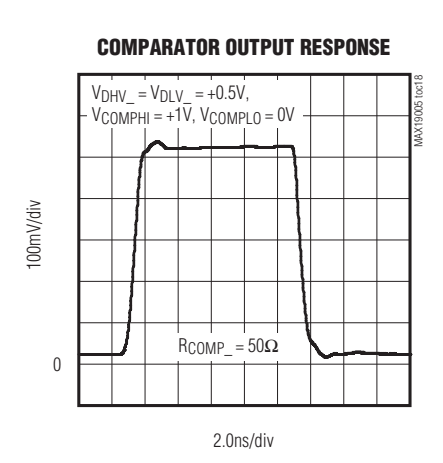
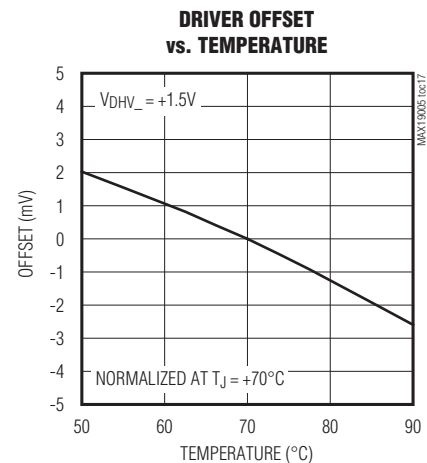
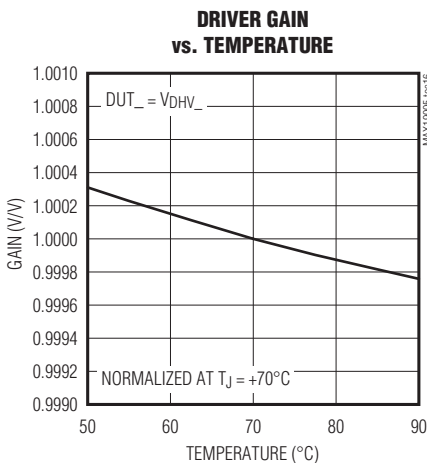
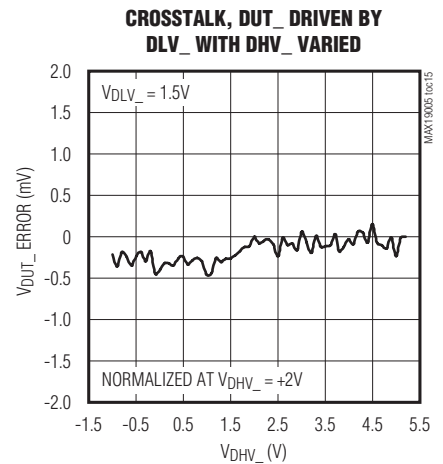
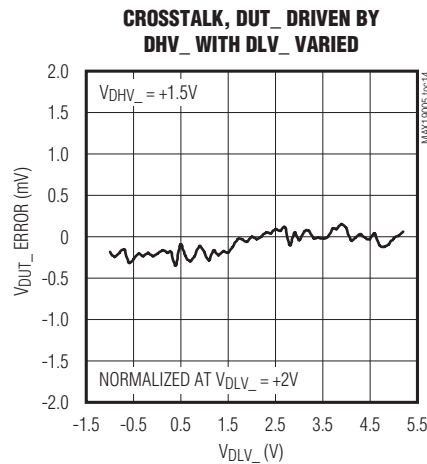
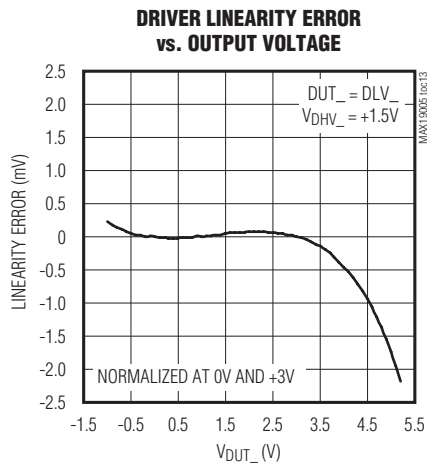
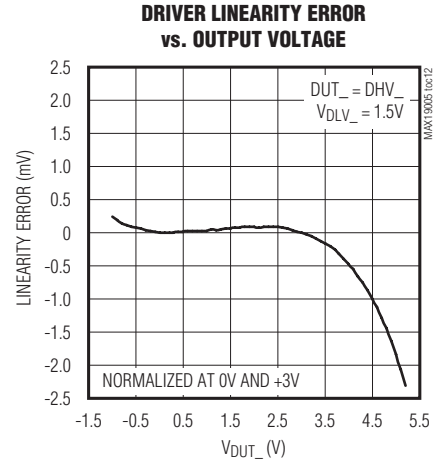
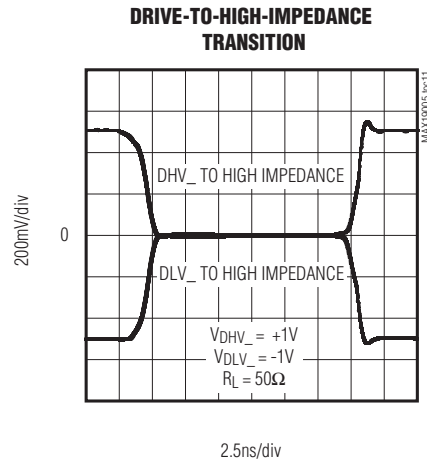
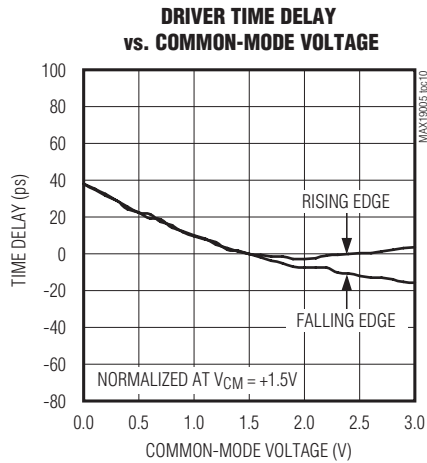


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## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Typical Operating Characteristics (continued)

( $V_{DD} = 8V$ ,  $V_{SS} = -5V$ ,  $V_L = 3V$ ,  $V_{DDSW} = 24.6V$ ,  $V_{SSSW} = 1.25V$ ,  $V_{COMPHI} = 1V$ ,  $V_{COMPL0} = 0V$ ,  $V_{LDV} = 0V$ , LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients  $T_J = +70^\circ C$  are measured at  $T_J = +50^\circ C$ , to  $+90^\circ C$  unless otherwise noted.)

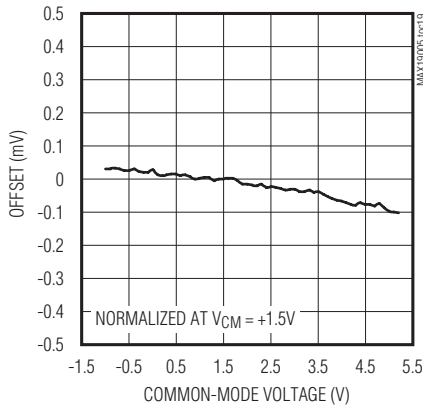


## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

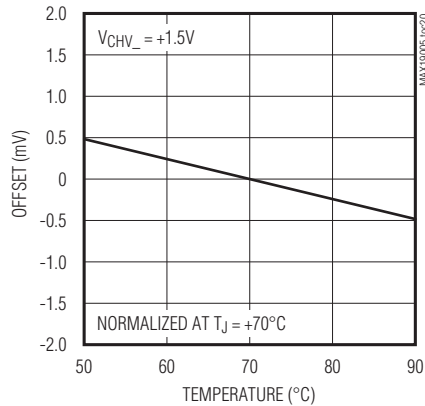
### Typical Operating Characteristics (continued)

( $V_{DD} = 8V$ ,  $V_{SS} = -5V$ ,  $V_L = 3V$ ,  $V_{DDSW} = 24.6V$ ,  $V_{SSSW} = 1.25V$ ,  $V_{COMPHI} = 1V$ ,  $V_{COMPL0} = 0V$ ,  $V_{LDV\_} = 0V$ , LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients  $T_J = +70^\circ C$  are measured at  $T_J = +50^\circ C$ , to  $+90^\circ C$  unless otherwise noted.)

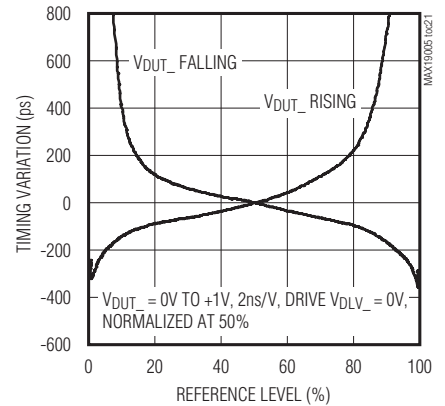
**COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE**



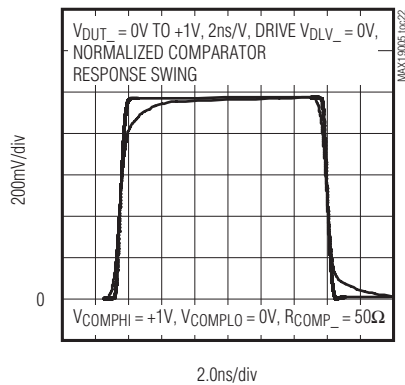
**COMPARATOR OFFSET vs. TEMPERATURE**



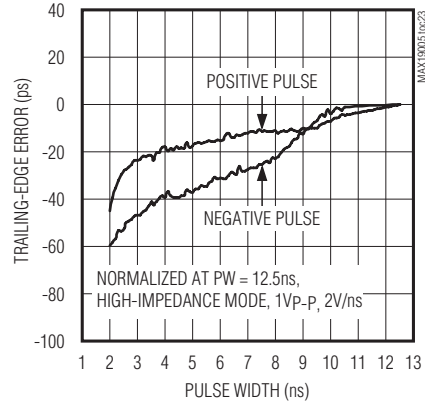
**COMPARATOR WAVEFORM TRACKING**



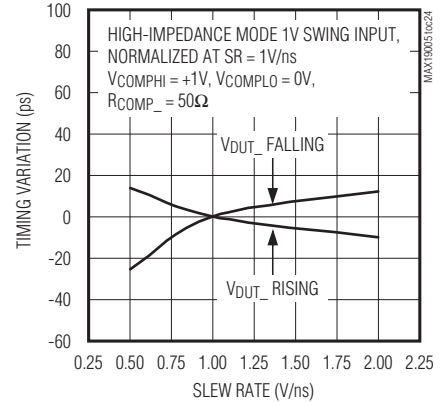
**COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE**



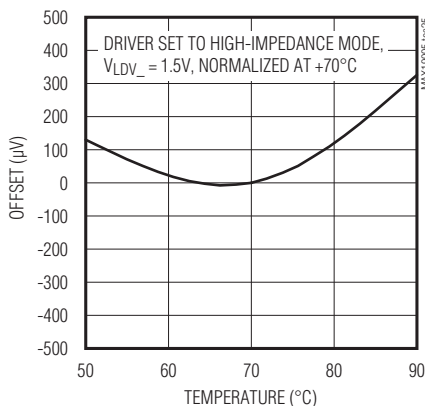
**COMPARATOR TIMING VARIATION vs. PULSE WIDTH**



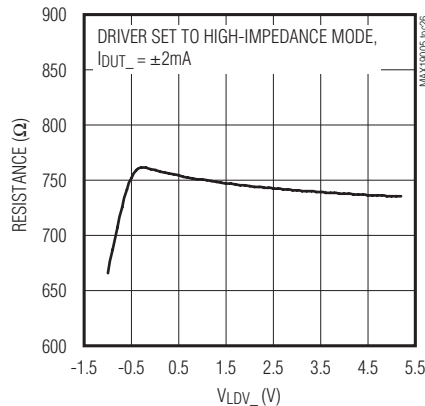
**COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE**



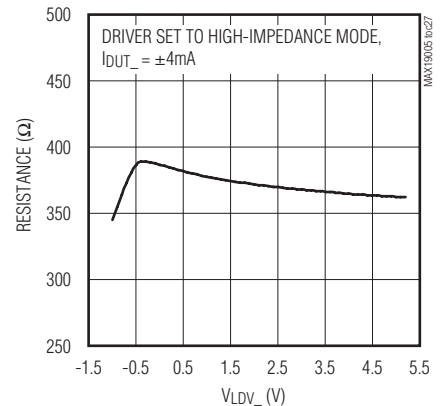
**PASSIVE LOAD OFFSET vs. TEMPERATURE**



**PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE**



**PASSIVE LOAD LOW RESISTOR vs. VOLTAGE**



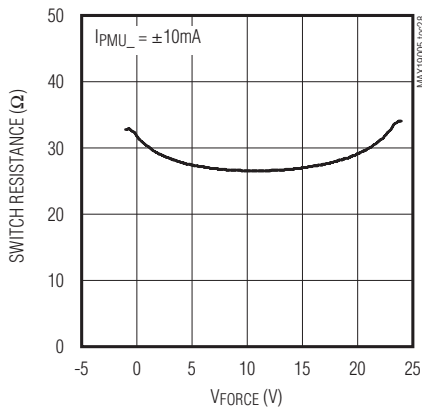
# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

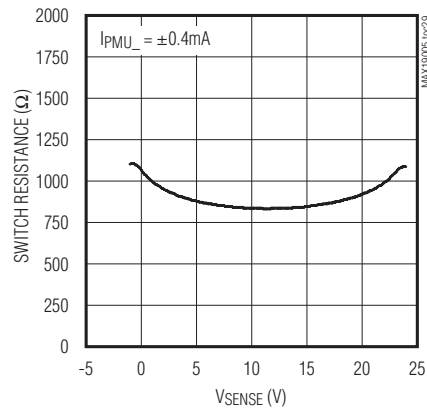
### Typical Operating Characteristics (continued)

( $V_{DD} = 8V$ ,  $V_{SS} = -5V$ ,  $V_L = 3V$ ,  $V_{DDSW} = 24.6V$ ,  $V_{SSSW} = 1.25V$ ,  $V_{COMPHI} = 1V$ ,  $V_{COMPLO} = 0V$ ,  $V_{LDV\_} = 0V$ , LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients  $T_J = +70^\circ C$  are measured at  $T_J = +50^\circ C$ , to  $+90^\circ C$  unless otherwise noted.)

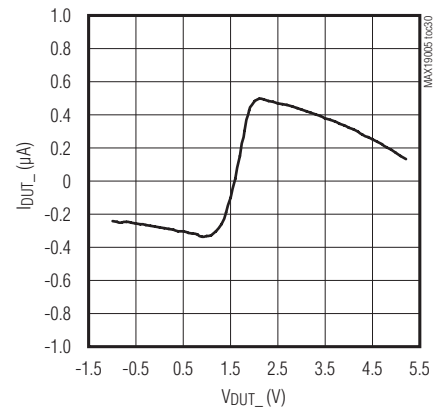
**PMU\_FORCE SWITCH RESISTANCE  
vs. FORCE VOLTAGE**



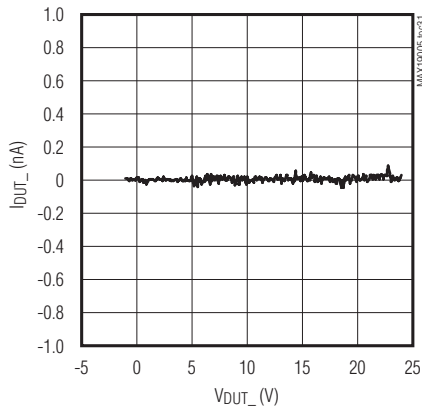
**PMU\_SENSE SWITCH RESISTANCE  
vs. SENSE VOLTAGE**



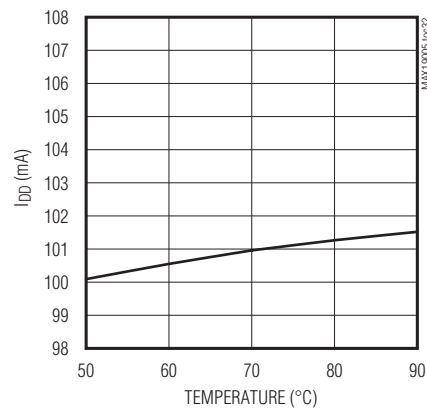
**HIGH-IMPEDANCE LEAKAGE AT DUT\_  
vs. DUT\_ VOLTAGE**



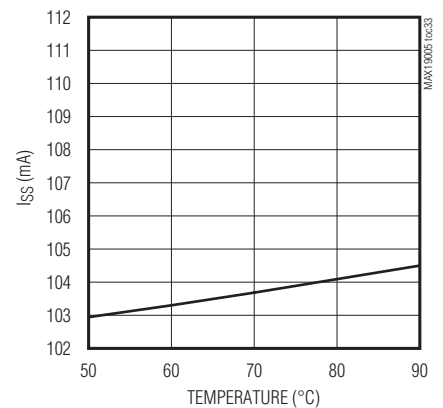
**LOW-LEAKAGE CURRENT  
vs. DUT\_ VOLTAGE**



**I<sub>DD</sub> SUPPLY CURRENT  
vs. TEMPERATURE**



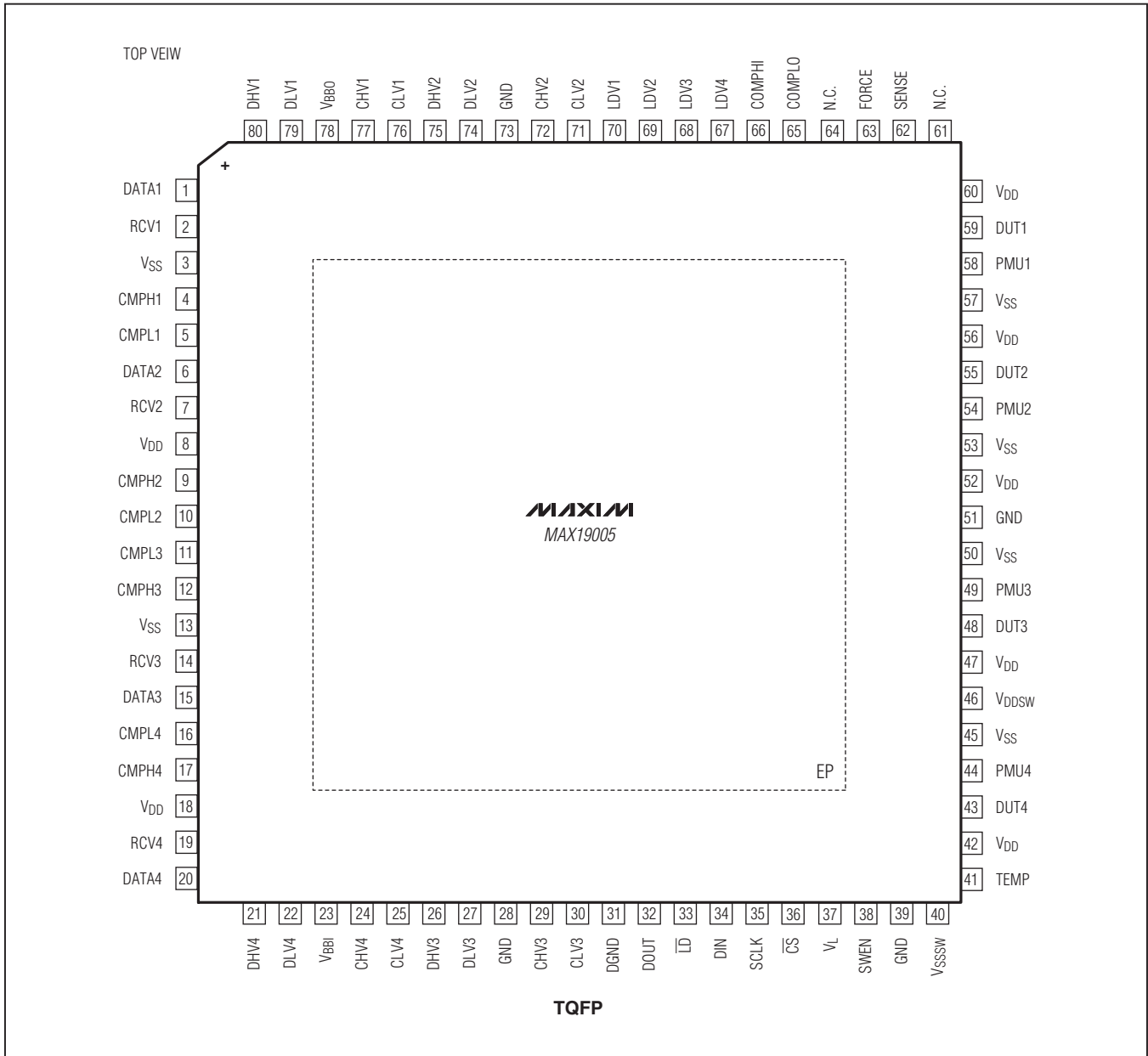
**I<sub>SS</sub> SUPPLY CURRENT  
vs. TEMPERATURE**



# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Pin Configuration





# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Pin Description

PIN	NAME	FUNCTION
1	DATA1	Channel 1 Multiplexer Control Input. Selects the driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	RCV1	Channel 1 Multiplexer Control Input. Sets the channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 13, 45, 50, 53, 57	V <sub>SS</sub>	Negative Power-Supply Input
4	CMPH1	Channel 1 High-Side Comparator Output
5	CMPL1	Channel 1 Low-Side Comparator Output
6	DATA2	Channel 2 Multiplexer Control Input. Selects the driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	RCV2	Channel 2 Multiplexer Control Input. Sets the channel 2 mode to drive or receive. See Table 1 and Figure 2.
8, 18, 42, 47, 52, 56, 60	V <sub>DD</sub>	Positive Power-Supply Input
9	CMPH2	Channel 2 High-Side Comparator Output
10	CMPL2	Channel 2 Low-Side Comparator Output
11	CMPL3	Channel 3 Low-Side Comparator Output
12	CMPH3	Channel 3 High-Side Comparator Output
14	RCV3	Channel 3 Multiplexer Control Input. Sets the channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	DATA3	Channel 3 Multiplexer Control Input. Selects the driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	CMPL4	Channel 4 Low-Side Comparator Output
17	CMPH4	Channel 4 High-Side Comparator Output
19	RCV4	Channel 4 Multiplexer Control Input. Sets the channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	DHV4	Channel 4 Driver High-Voltage Input
22	DLV4	Channel 4 Driver Low-Voltage Input
23	V <sub>BBI</sub>	DATA_/RCV_ Threshold Voltage Input
24	CHV4	Channel 4 High-Side Comparator Threshold Voltage Input
25	CLV4	Channel 4 Low-Side Comparator Threshold Voltage Input
26	DHV3	Channel 3 Driver High-Voltage Input
27	DLV3	Channel 3 Driver Low-Voltage Input
28, 39, 51, 73	GND	Analog Ground
29	CHV3	Channel 3 High-Side Comparator Threshold Voltage Input
30	CLV3	Channel 3 Low-Side Comparator Threshold Voltage Input
31	DGND	Digital Ground Connection

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## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Pin Description (continued)

PIN	NAME	FUNCTION
32	DOUT	Serial-Interface Data Output
33	$\overline{\text{LD}}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.
34	DIN	Serial-Interface Data Input
35	SCLK	Serial Clock
36	$\overline{\text{CS}}$	Chip Select
37	$V_L$	Logic Power-Supply Input
38	SWEN	PMU Switch and Pin Switch Enable Input
40	$V_{SSSW}$	PMU Switch and Pin Switch Negative Power-Supply Input
41	TEMP	Temperature Sensor Output
43	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	PMU4	Channel 4 Parametric Measurement Unit Connection. PMU switch I/O node for channel 4.
46	$V_{DDSW}$	Positive PMU Switch and Pin Switch Power-Supply Input
48	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	PMU3	Channel 3 Parametric Measurement Unit Connection. PMU switch I/O node for channel 3.
54	PMU2	Channel 2 Parametric Measurement Unit Connection. PMU switch I/O node for channel 2.
55	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	PMU1	Channel 1 Parametric Measurement Unit Connection. PMU switch I/O node for channel 1.
59	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61, 64	N.C.	No Connection. Not internally connected.
62	SENSE	PMU Sense Connection
63	FORCE	PMU Force Connection
65	COMPLO	Comparator Output Low-Voltage Reference Input
66	COMPHI	Comparator Output High-Voltage Reference Input
67	LDV4	Channel 4 Load Voltage Input
68	LDV3	Channel 3 Load Voltage Input
69	LDV2	Channel 2 Load Voltage Input
70	LDV1	Channel 1 Load Voltage Input
71	CLV2	Channel 2 Low-Side Comparator Threshold Voltage Input
72	CHV2	Channel 2 High-Side Comparator Threshold Voltage Input
74	DLV2	Channel 2 Driver Low-Voltage Input
75	DHV2	Channel 2 Driver High-Voltage Input
76	CLV1	Channel 1 Low-Side Comparator Threshold Voltage Input
77	CHV1	Channel 1 High-Side Comparator Threshold Voltage Input
78	$V_{BBO}$	Comparator Output Threshold Voltage Output
79	DLV1	Channel 1 Driver Low-Voltage Input
80	DHV1	Channel 1 Driver High-Voltage Input
—	EP	Exposed Pad. Leave unconnected or connect to GND.

# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

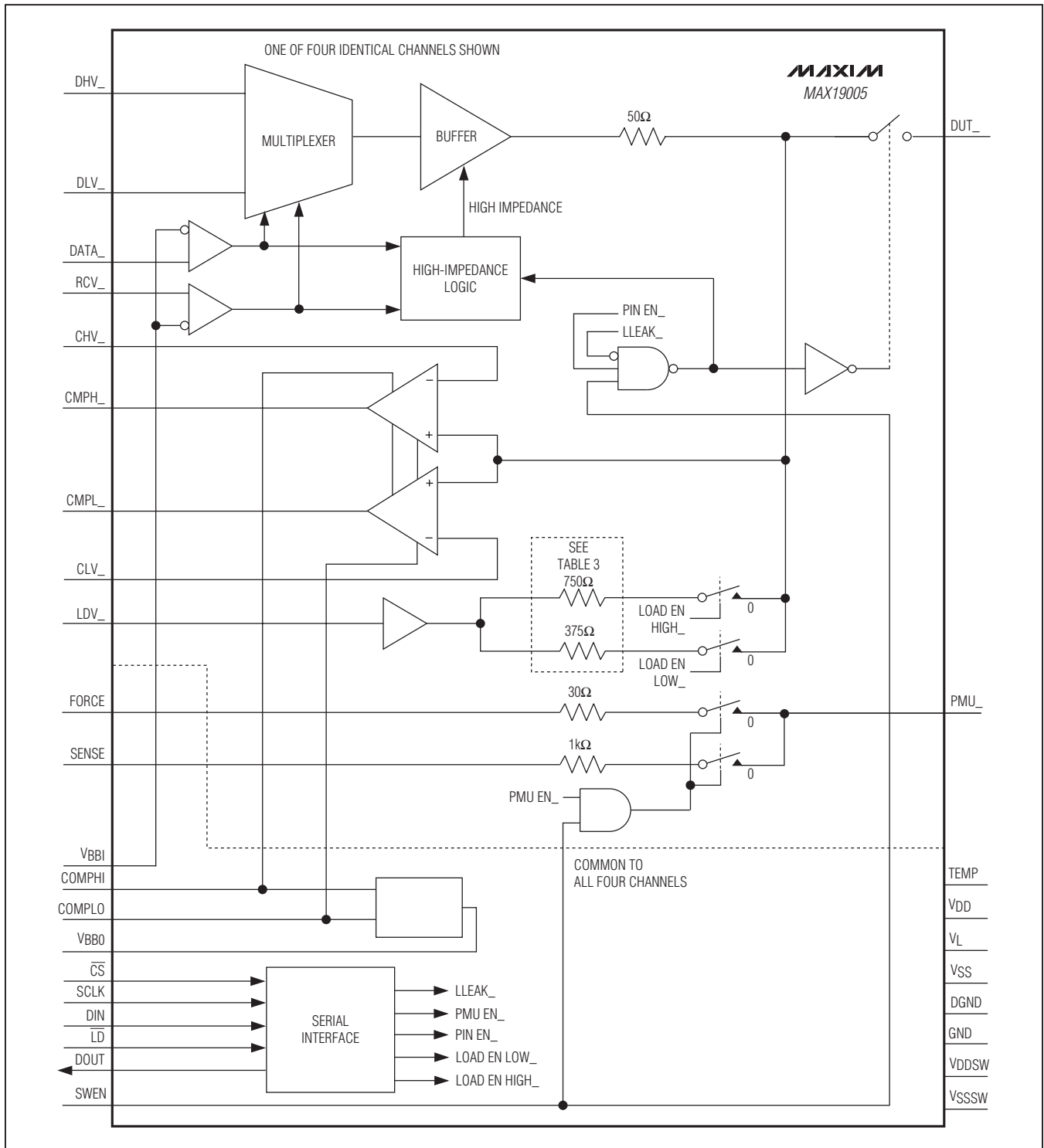


Figure 2. Block Diagram

# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Detailed Description

The MAX19005 is a four-channel, ultra-low-power, pin-electronics IC for automated test equipment that includes, for each channel, a two-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 2). All functions feature a -1V to +5.2V operating range and the drivers include a high-impedance mode. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT\_ current loading. The Kelvin paths allow accurate connection of an instrument with  $\pm 25\text{mA}$  source/sink capability. Additionally, the IC offers a low-leakage mode that reduces DUT\_ leakage current to less than 20nA.

Each of the four channels feature single-ended CMOS-compatible inputs (DATA\_ and RCV\_) for control of the driver signal path (Figure 3). The IC mode operations

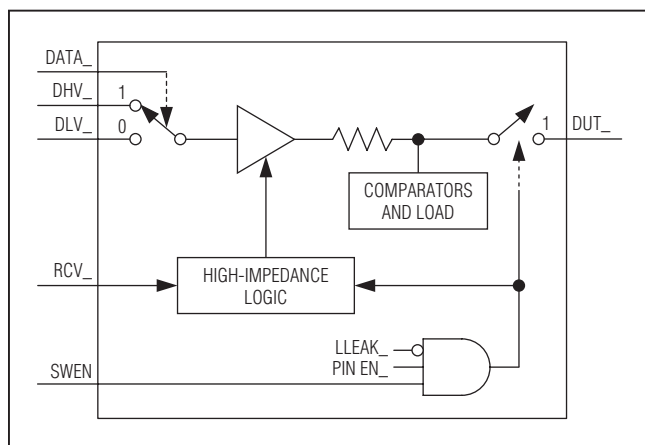


Figure 3. Multiplexer and Driver Channel

are programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

The driver input is a high-speed multiplexer that selects one of two voltage inputs: DHV\_ and DLV\_. This switching is controlled by high-speed inputs DATA\_ and RCV\_. DATA\_ and RCV\_ are single-ended inputs with threshold levels (VBBI). Each channel's threshold levels are independently buffered to minimize crosstalk.

DUT\_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 3, Table 1). High-speed input RCV\_ and mode-control bit LLEAK\_ control these modes. In high-impedance mode, the bias current at DUT\_ is less than 2 $\mu\text{A}$  over the -1V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT\_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is 49.5 $\Omega$ .

### Comparators

The IC provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT\_ and the other input connected to either CHV\_ or CLV\_ (Figure 2). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator 50 $\Omega$  output impedance provides source termination (Figure 4). VBBO output voltage is provided, (COMPHI + COMPLO)/2.

Table 1. Component List

EXTERNAL PIN CONNECTIONS			INTERNAL REGISTER CONTROL BITS		DRIVER STATUS	PIN SWITCH STATUS
RCV_	DATA_	SWEN	PIN EN_	LLEAK_		
0	0	1	1	0	DUT_ = DLV_	Short
0	1	1	1	0	DUT_ = DHV_	Short
1	X	1	1	0	High impedance	Short
X	X	0	X	0	0V	Open
X	X	X	0	0	0V	Open
X	X	X	X	1	0V (low power)	Open

X = Don't care.

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

**Table 2. Comparator Logic**

CONDITION		CMPH_	CMPL_
DUT_ < CHV_	DUT_ < CLV_	0	0
DUT_ < CHV_	DUT_ > CLV_	0	1
DUT_ > CHV_	DUT_ < CLV_	1	0
DUT_ > CHV_	DUT_ > CLV_	1	1

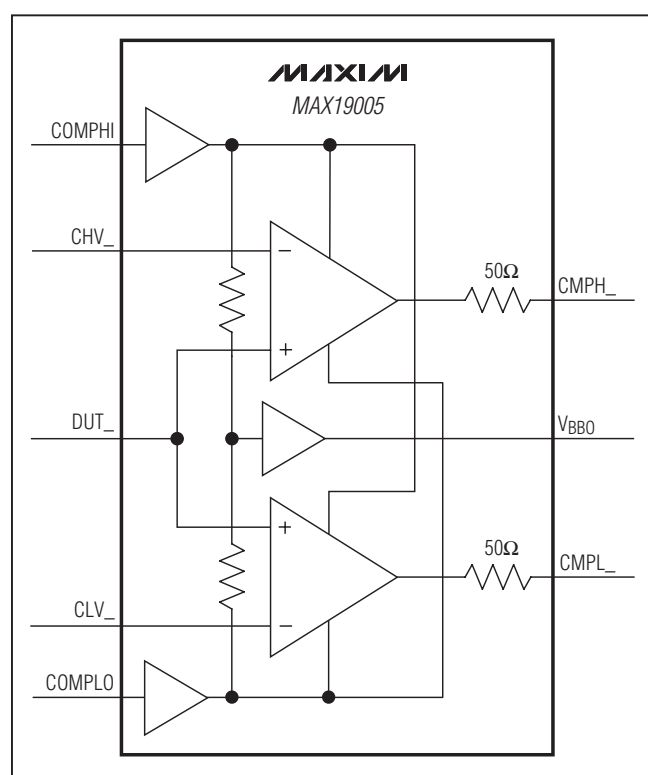


Figure 4. Complementary 50Ω Comparator Outputs

### Passive Load

The IC channels each feature a passive load consisting of a buffered input voltage (LDV\_) connected to DUT\_ through two resistive paths (Figure 2). Each path connects to DUT\_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT\_ outputs. See Table 3.

**Table 3. Passive Load Logic**

INTERNAL CONTROL BITS		PASSIVE LOAD STATUS
LOAD EN HIGH_	LOAD EN LOW_	
0	0	Disconnect
0	1	375Ω load connect
1	0	750Ω load connect
1	1	750Ω    375Ω load connect

**Table 4. PMU Switch Logic**

EXTERNAL CONNECTION	INTERNAL CONTROL BIT	PMU SWITCH STATUS
SWEN	PMU EN_	
0	X	Open
1	0	Open
1	1	Short

X = Don't care.

### Parametric Switches

Each of the four IC channels provide force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 2). Both force and sense switches are simultaneously controlled through the serial interface providing maximum application flexibility. PMU\_ and DUT\_ are provided on separate pins, allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU\_. It also allows PMU\_ to connect to DUT\_, either directly or with an impedance-matching network. See Table 4.

### Low-Leakage Mode (LLEAK\_)

Asserting LLEAK\_ through the serial port places the IC into a very-low-leakage state. See the Electrical Characteristics section. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK\_ control is independent for each channel.

When DUT\_ is driven with a high-speed signal while LLEAK\_ is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the Electrical Characteristics section indicates device behavior under this condition.

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## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Temperature Monitor

Each device supplies a single temperature output signal (TEMP) that asserts a nominal +3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 17kΩ (typ).

### Serial Interface and Device Control

A CMOS-compatible serial interface controls the IC modes (Figure 5). Control data flow into a 12-bit shift register (LSB first) and are latched when CS is taken high. Data from the shift register are then loaded to the per-channel control latches, as determined by bits D[8:11] (Figure 5 and Table 5). The latches contain the five mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA\_ and

RCV\_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing LD low. With LD always low, data transfer on the rising edge of CS.

### Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed pad, solder it to circuit-board copper. The exposed pad must be either left unconnected, isolated, or connected to GND.

### Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

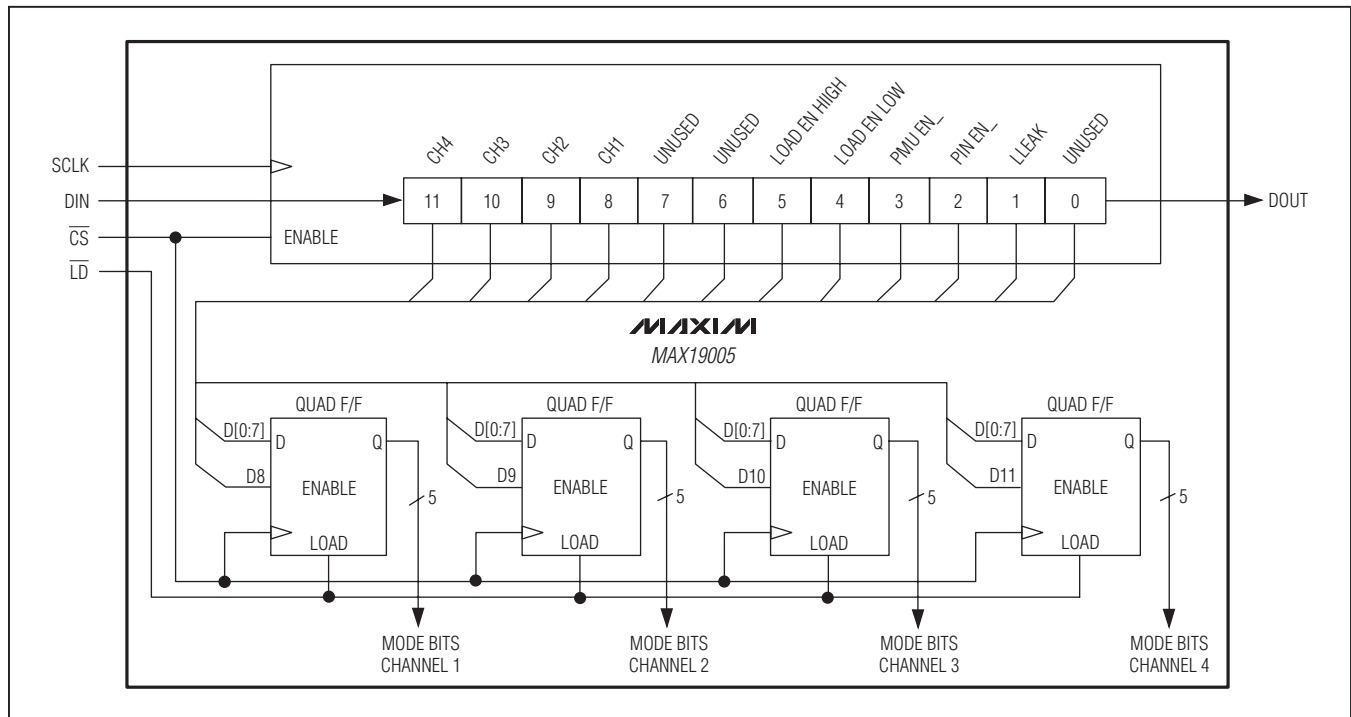


Figure 5. Serial Interface

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

**Table 5. Control Register Bits**

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
D0	—	Unused	X	X	0
D1	LLEAK	Assert low-leakage mode	Active	Low leakage	0
D2	PIN EN	Enable pin switch	Disabled	Enabled	0
D3	PMU EN	Enable PMU switch	Disabled	Enabled	0
D4	LOAD EN LOW	Enable low load resistor	Disabled	Enabled	0
D5	LOAD EN HIGH	Enable high load resistor	Disabled	Enabled	0
D6	—	Unused	X	X	0
D7	—	Unused	X	X	0
D8	CH1	Update channel 1 control register	Disabled	Enabled	1
D9	CH2	Update channel 2 control register	Disabled	Enabled	1
D10	CH3	Update channel 3 control register	Disabled	Enabled	1
D11	CH4	Update channel 4 control register	Disabled	Enabled	1

X = Don't care.

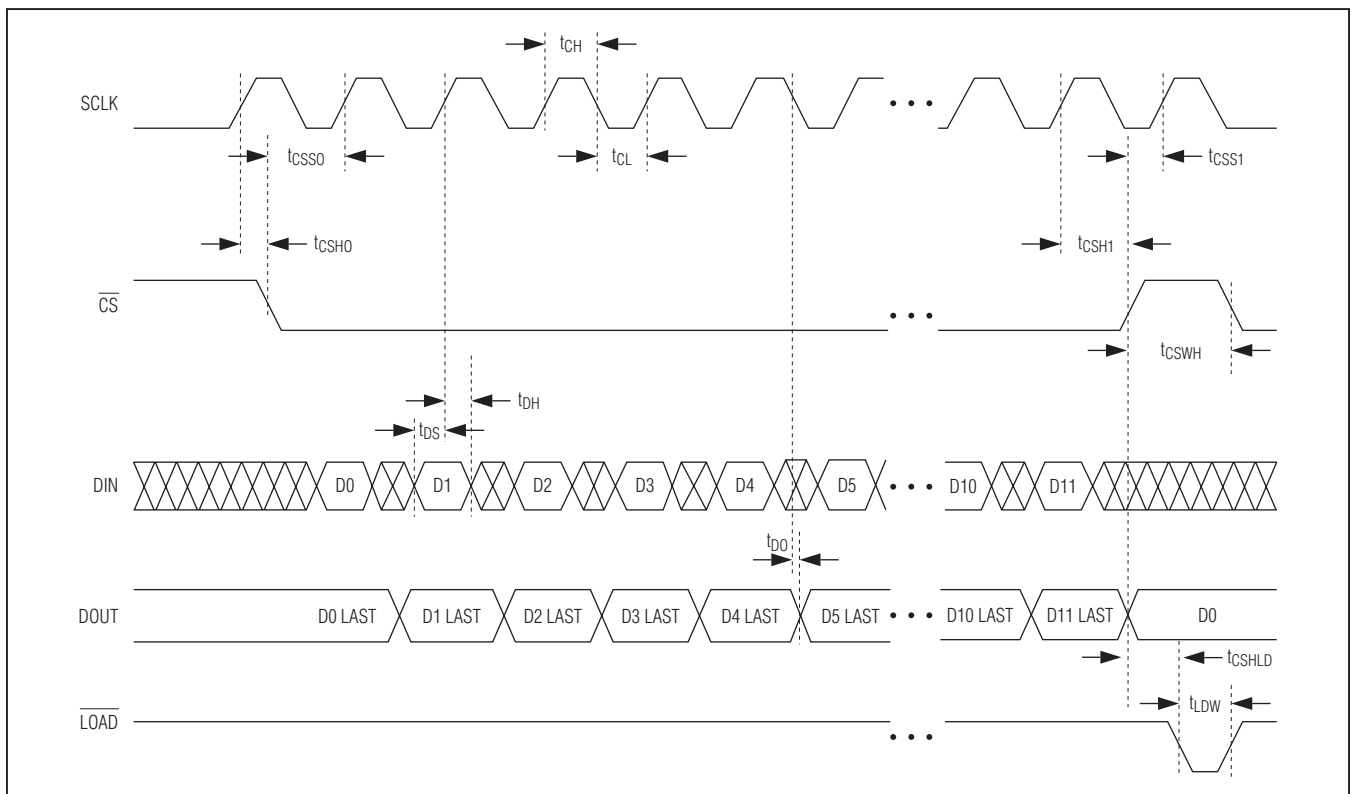


Figure 6. Serial-Interface Timing

# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	HEAT EXTRACTION
MAX19005CCS+	0°C to +70°C	80 TQFP-EP*	Bottom

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
80 TQFP-EP	C80E+4	<a href="#">21-0115</a>	<a href="#">90-0152</a>



# MAX19005

## Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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