

44 V, 5.5 A, quad power half-bridge

Datasheet - production data



Features

- Multipower BCD technology
- Minimum input/output pulse width distortion
- 150 mΩ R_{DS(on)} complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- · Short-circuit protection

Description

The STA510A is a monolithic, quad, half-bridge stage in multipower BCD technology. The device can be used as dual-bridge or reconfigured, by connecting the CONFIG pin to the VDD pin, as single-bridge with double current capability, or as half-bridge (binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo all-digital high-efficiency (DDX) amplifier, which employs a pulse-width modulator driver. The STA510A is capable of delivering an output power of 50 W into 3 Ω loads with THD = 10% and V_{CC} = 36 V. In single BTL configuration the device can deliver 200 W into a 3 Ω load with THD = 10% and V_{CC} = 36 V.

The input pins have a threshold proportional to $V_{\mbox{\scriptsize L}}$ pin voltage.

Table 1. Device summary

Order code	Operating temp. range	Package	Packing	
STA510A13TR	0° to 70° C	PSSO36 (slug up)	Tape and reel	

Contents STA510A

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1 Audio application circuit

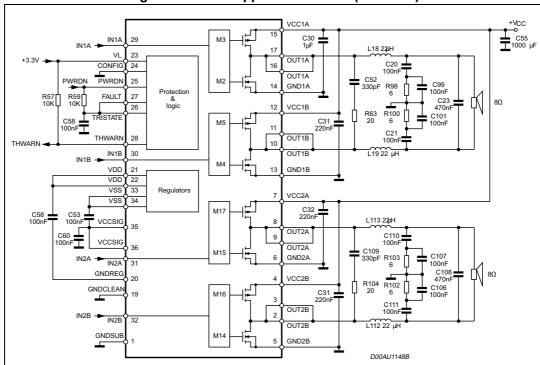


Figure 1. TAudio application circuit (dual BTL)

Pin description STA510A

2 Pin description

0 36 1 ☐ GND-SUB V_{CC}Sign [V_{CC}Sign [35 2 OUT2B 3 OUT2B V_{SS} [34 33 4 $V_{CC}2B$ V_{SS} IN2B 32 5 GND2B IN2A 31 6 GND2A IN1B 30 7 ☐ V_{CC}2A IN1A 29 8 OUT2A TH_WAR [28 9 OUT2A 27 OUT1B FAULT [10 TRI-STATE [26 11 OUT1B 25 **PWRDN** 12 V_{CC}1B CONFIG [24 GND1B 13 23 GND1A 14 V_L

Figure 2. Pin connections (top view)

Table 2. Pin list

15

16

17

18

 $V_{CC}1A$

OUT1A

OUT1A

N.C.

22

21

20

19

V_{DD} [

V_{DD}

GND-Reg [

GND-Clean

Pin	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half-bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	Vcc2A	Positive supply
8, 9	OUT2A	Output half-bridge 2A
10, 11	OUT1B	Output half-bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	Vcc1A	Positive supply
16, 17	OUT1A	Output half-bridge 1A
18	NC	Not connected

STA510A Pin description

Table 2. Pin list (continued)

Pin	Name	Description
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator V _{DD}
21, 22	V_{DD}	5-V regulator referred to ground
23	V_{L}	High logical state setting voltage
24	CONFIG	Configuration 0: normal operation 1: single BTL (mono) mode, join the pins OUT1A to OUT1B and OUT2A to OUT2B (if IN1A is joined to IN1B and IN2A to IN2B)
25	PWRDN	Standby (power down): 0: low power consumption mode 1: normal operation
26	TRI-STATE	High impedance control: 0: all power amplifiers in high-impedance state 1: normal operation
Fault advisor: 0: fault detected (short circuit or thermal) 1: normal operation		0: fault detected (short circuit or thermal)
28	Thermal warning advisor: 28 TH-WAR 0: junction temperature = 130 °C 1: normal operation	
29	IN1A	Input of half-bridge 1A
30	IN1B	Input of half-bridge 1B
31	IN2A	Input of half-bridge 2A
32	IN2B	Input of half-bridge 2B
33, 34	V _{SS}	5-V regulator referred to +V _{CC}
35, 36	VCCSIGN	Signal positive supply
-	EP	Exposed pad up

^{1.} The pin is open collector. To have a high logic value it needs to be pulled up by a resistor.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

	<u> </u>		
Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (pin 4, 7, 12, 15)	44	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
P _{tot}	Power dissipation (T _{case} = 70 °C)	21	W
T _{op}	Operating temperature range	90	°C
T _{stg} , T _j	Storage and junction temperature	-40 to 150	°C

3.2 Recommended operating conditions

Table 4. Recommended operating conditions⁽¹⁾

Symbol	Parameter		Тур.	Max.	Unit
V _{cc}	DC supply voltage	10		39.0	V
V_{L}	Input logic reference	2.7	3.3	5.0	V
T _{amb}	Ambient temperature	0		70	°C

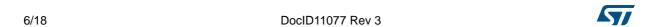
^{1.} Performance not guaranteed beyond recommended operating conditions.

3.3 Thermal data

The power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level. The PowerSO36 package of the STA510A includes an exposed pad or slug on the top of the device to provide a direct thermal path from the die to the heatsink.

Table 5. Thermal data

Symbol	Parameter	Min.	Тур.	Max.	Unit
T _{j-case}	Thermal resistance junction to case (thermal pad)		1	2.5	°C/W
T _{jSD}	Thermal shut-down junction temperature		150		°C
T _{warn}	Thermal warning temperature		130		°C
t _{hSD}	Thermal shutdown hysteresis		25		°C



3.4 Electrical specifications

The results in *Table 6* below are given for the conditions: $V_L = 3.3 \text{ V}$, $V_{CC} = 36 \text{ V}$, $R_L = 8 \Omega$, $f_{sw} = 384 \text{ kHz}$ and $T_{amb} = 25 ^{\circ}\text{C}$ unless otherwise specified. See also *Figure 3*.

Table 6. Electrical specifications

Symbol	Parameter Conditions			Тур.	Max.	Unit
R_{dsON}	Power P-channel/N-channel MOSFET R _{DS(on)}	Id = 1 A		150	200	mΩ
I _{dss}	Power P-channel/N-channel leakage current				100	μΑ
g _N	Power P-channel R _{DS(on)} matching	Id = 1 A	95			%
g _P	Power N-channel R _{DS(on)} matching	Id = 1 A	95			%
Dt_s	Low current deadtime (static)	See test circuit Figure 3		10	20	ns
Dt_d	High current deadtime (dynamic)	L = 22 μ H, C = 470 nF, R _L = 8 Ω , Id = 3 A, see test circuit <i>Figure 5</i>			50	ns
t _{d ON}	Turn-on delay time	Resistive load, V _{CC} = 30 V			100	ns
t _{d OFF}	Turn-off delay time	Resistive load, V _{CC} = 30 V			100	ns
t _r	Rise time	Resistive load, as Figure 3			25	ns
t _f	Fall time	Resistive load, as Figure 3			25	ns
V _{IN-High}	High level input voltage				V _L /2 + 300 mV	V
V _{IN-Low}	Low level input voltage		V _L /2 – 300 mV			V
I _{IN-H}	High level input current	Pin voltage = V _L		1		μΑ
I _{IN-L}	Low level input current	Pin voltage = 0.3 V		1		μΑ
I _{PWRDN-H}	High level PWRDN pin input current	V _L = 3.3 V		35		μΑ
		V _L = 2.7 V			0.70	
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE)	V _L = 3.3 V			0.80	V
	, , , , , , , , , , , , , , , , , , , ,	V _L = 5.0 V			0.85	
		V _L = 2.7 V	1.50			V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE)	V _L = 3.3 V	1.7			V
	, , , , , , , , , , , , , , , , , , , ,	V _L = 5.0 V	1.85			V
I _{VCC} - PWRDN	Supply current from V _{CC} in power down	PWRDN = 0			3	mA
I _{FAULT}	Output current pins FAULT -TH- WARN when FAULT CONDITIONS	V _{PIN} = 3.3 V		1		mA
I _{VCC-hiz}	Supply current from V _{CC} in tri-state	V _{CC} = 30 V, Pin TRI-STATE = 0		22		mA



Table 6. Electrical specifications (continued)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I _{vcc}	Supply current from V _{CC} in operation both channel switching)	V _{CC} = 30 V, input pulse width duty cycle = 50%, switching frequency = 384 kHz, no LC filters;		70		mA
I _{SCP}	Short-circuit current limit		5.5	6		Α
V _{UV}	Undervoltage protection threshold			7		V
t _{pw_min}	Output minimum pulse width	No load	25		40	ns
ESD	ESD maximum withstanding voltage range, test condition CDF-AEC-Q100-002-"Human Body Model"			± 1500		V

Not used

1

1

1

INxB TRI-STATE INxA Q1 Q3 Q4 **Output mode** OFF OFF OFF Hi-Z 0 Х Х OFF 0 OFF OFF **DUMP** 1 0 ON ON 1 0 1 OFF ON ON **OFF NEGATIVE** 1 1 0 ON **OFF OFF** ON **POSITIVE**

ON

OFF

OFF

Table 7. Logic truth table

Figure 3. Test circuit for low current deadtime for single-ended applications

ON

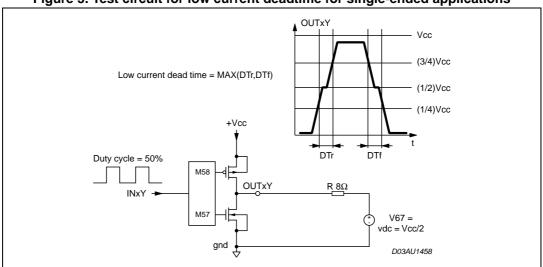
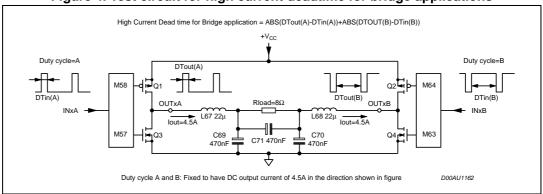


Figure 4. Test circuit for high current deadtime for bridge applications



INXA OUTXB INXB

GND D00AU1134

Figure 5. Block diagram for high current dead time for bridge applications



STA510A Technical information

4 Technical information

The STA510A is a dual channel H-bridge that is able to deliver 100 W per channel (into $R_L = 6~\Omega$ with THD = 10% and $V_{CC} = 36~V$) of audio output power very efficiently. It operates in conjunction with a pulse-width modulator driver such as the STA321 or STA309A.

The STA510A converts ternary-, phase-shift- or binary-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and thermal and short-circuit protection circuitry. In differential mode (ternary, phase-shift or binary differential), two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to the damped ternary modulation operation.

In binary mode, both full bridge and half bridge modes are supported. The STA510A includes overcurrent and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

Figure 6. Block diagram of full-bridge DDX® or binary mode

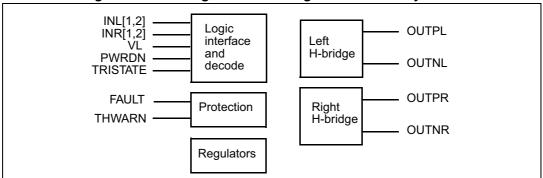
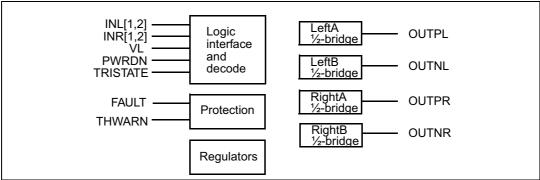


Figure 7. Block diagram of f binary half-bridge mode



4.1 Logic interface and decode

The STA510A power outputs are controlled using one or two logic-level timing signals. In order to provide a proper logic interface, the VL input must operate at the same voltage as the DDX control logic supply.

Technical information STA510A

4.2 Protection circuitry

The STA510A includes protection circuitry for overcurrent and thermal overload conditions. A thermal warning pin (THWARN, pin 28, open drain MOSFET) is activated low when the IC temperature exceeds 130 °C, just in advance of thermal shutdown. When a fault condition is detected an internal fault signal immediately disables the output power MOSFETs, placing both H-bridges in a high-impedance state. At the same time the open-drain MOSFET of pin FAULT (pin 27) is switched on.

There are two possible modes subsequent to activating a fault.

- **Shutdown mode**: with pins FAULT (with pull-up resistor) and TRISTATE separate, an activated fault disables the device, signalling a low at pin FAULT output. The device may subsequently be reset to normal operation by toggling pin TRISTATE from high to low to high using an external logic signal.
- Automatic recovery mode: This is shown in the applications circuits below where pins
 FAULT and TRISTATE are connected together to a time-constant circuit (R59 and
 C58). An activated fault forces a reset on pin TRISTATE causing normal operation to
 resume following a delay determined by the time constant of the circuit. If the fault
 condition persists, the circuit operation repeats until the fault condition is cleared. An
 increase in the time constant of the circuit produces a longer recovery interval. Care
 must be taken in the overall system design not to exceed the protection thesholds
 under normal operation.

4.3 Power outputs

The STA510A power and output pins are duplicated to provide a low-impedance path for the device bridged outputs. All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRISTATE pin should be used to set all power MOSFETs to the high-impedance state during power-up until the logic power supply, VL, has settled.

4.4 Parallel output / high current operation

When using the DDX mode output, the STA510A outputs can be connected in parallel in order to increase the output current capability to a load. In this configuration the STA510A can provide up to 200 W into a $3-\Omega$ load.

This mode of operation is enabled with the pin CONFIG (pin 24) connected to pin VDD. The inputs are joined so that IN1A = IN1B, IN2A = IN2B and similarly the outputs OUT1A = OUT1B, OUT2A = OUT2B as shown in *Figure 9*.

4.5 Output filtering

A passive 2^{nd} -order filter is used on the STA510A power outputs to reconstruct the analog audio signal. System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6- or 8- Ω loads is shown in the application circuit of *Figure 8*, and for 4- Ω loads in *Figure 9* and *Figure 10*.

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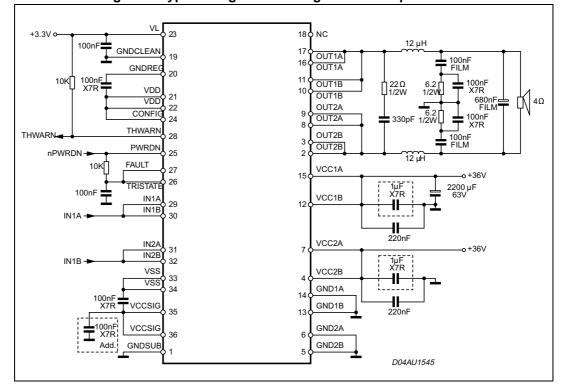
STA510A **Technical information**

Application circuits 4.6

C55 1000 µF L18 22µH VL 23 OUT1A OUT1A PWRDN 25 M2 GND1A Protection FAULT 27 C23 470nF 12 VCC1B M5 OUT1B 10 IN1B → VDD 13 VDD 22 VSS 33 Regulators VSS 7 34 L113 22 µH OUT2A OUT2A C107 GND2A GNDREG C108 470nF R104 R102 20 6 C31 1 M16 OUT2B OUT2B L112 22 uH GNDSUB M14 D00+AU1148B

Figure 8. Typical stereo full bridge configuration for up to 2x 100 W





Technical information STA510A

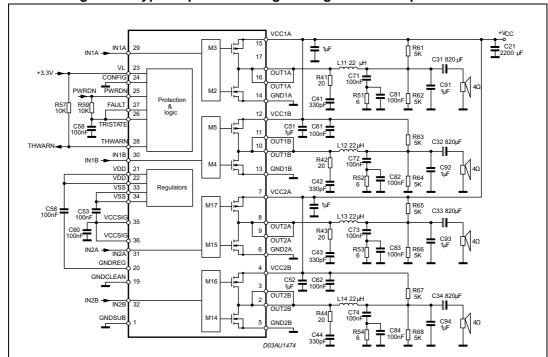


Figure 10. Typical quad half-bridge configuration for up to 4x 50 W

Note:

In the above three circuits a PWM modulator as driver is needed.

The power estimations were made using the STA321+STA510A demo board. The peak power duration is for $t \le 1$ s.

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STA510A Package information

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

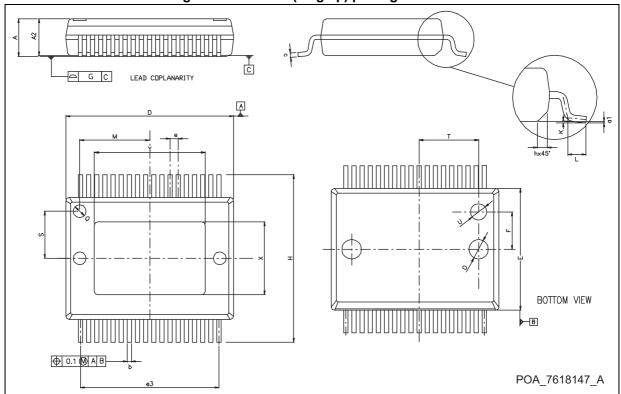


Figure 11. PSSO36 (slug up) package outline

Package information STA510A

Table 8. PSSO36 (slug up) mechanical data

Dim		mm			inches	
Dim.	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
С	0.23		0.32	0.009		0.012
D ⁽¹⁾	10.10		10.50	0.398		0.413
E ⁽¹⁾	7.4		7.6	0.291		0.299
е		0.50			0.020	
e3		8.50			0.035	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
Н	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
М		4.3			0.169	
N		10° (max.)			10° (max.)	
0		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
Т		3.65			0.144	
U		1.0			0.039	
Х	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

 [&]quot;D and E" do not include mold flash or protrusion. Mold flash or protrusion shall not exceed 0.15 mm (0.006").

STA510A Revision history

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Oct-2004	1	Initial release.
11-Mar-2010	2	Updated description and applications circuits
15-Jan-2019	3	Removed the order code STA510A from the device summary table in cover page.

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