# PCA8565

## Real time clock/calendar

Rev. 4 — 5 December 2014

**Product data sheet**

## 1. General description

The PCA8565 is a CMOS[1] real time clock and calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All address and data are transferred serially via a two-line bidirectional I²C-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

For a selection of NXP Real-Time Clocks, see Table 36 on page 40

## 2. Features and benefits

- AEC-Q100 compliant (PCA8565TS) for automotive applications
- Provides year, month, day, weekday, hours, minutes and seconds based on a 32.768 kHz quartz crystal
- Clock operating voltage: 0.9 V to 5.5 V at room temperature
- Extended operating temperature range: −40 °C to +125 °C
- Low current; typical 0.65 µA at $V_{DD}$ = 3.0 V and $T_{amb}$ = 25 °C
- 400 kHz two-wire I²C-bus interface (at $V_{DD}$ = 1.8 V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz and 1 Hz)
- Alarm and timer functions
- Internal power-on reset
- I²C-bus slave address: read A3h and write A2h
- Open-drain interrupt pin
- One integrated oscillator capacitor

## 3. Applications

- Automotive
- Industrial
- Other applications that require a wide operating temperature range

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 22.

## 4. Ordering information

**Table 1.** **Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | **Name** | **Description** | | **Version** |
| PCA8565TS | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | | SOT505-1 |

### 4.1 Ordering options

**Table 2.** **Ordering options**

| Product type number | Orderable part number | Sales item (12NC) | Delivery form | IC revision |
|---|---|---|---|---|
| PCA8565TS/1 | PCA8565TS/1,118 | 935272132118 | tape and reel, 13 inch | 1 |
| PCA8565TS/S410/1 | PCA8565TS/S410/1,5 | 935273247518 | tape and reel, 13 inch, dry pack | 1 |

## 5. Marking

**Table 3.** **Marking codes**

| Type number | Marking code |
|---|---|
| PCA8565TS | 8565 |

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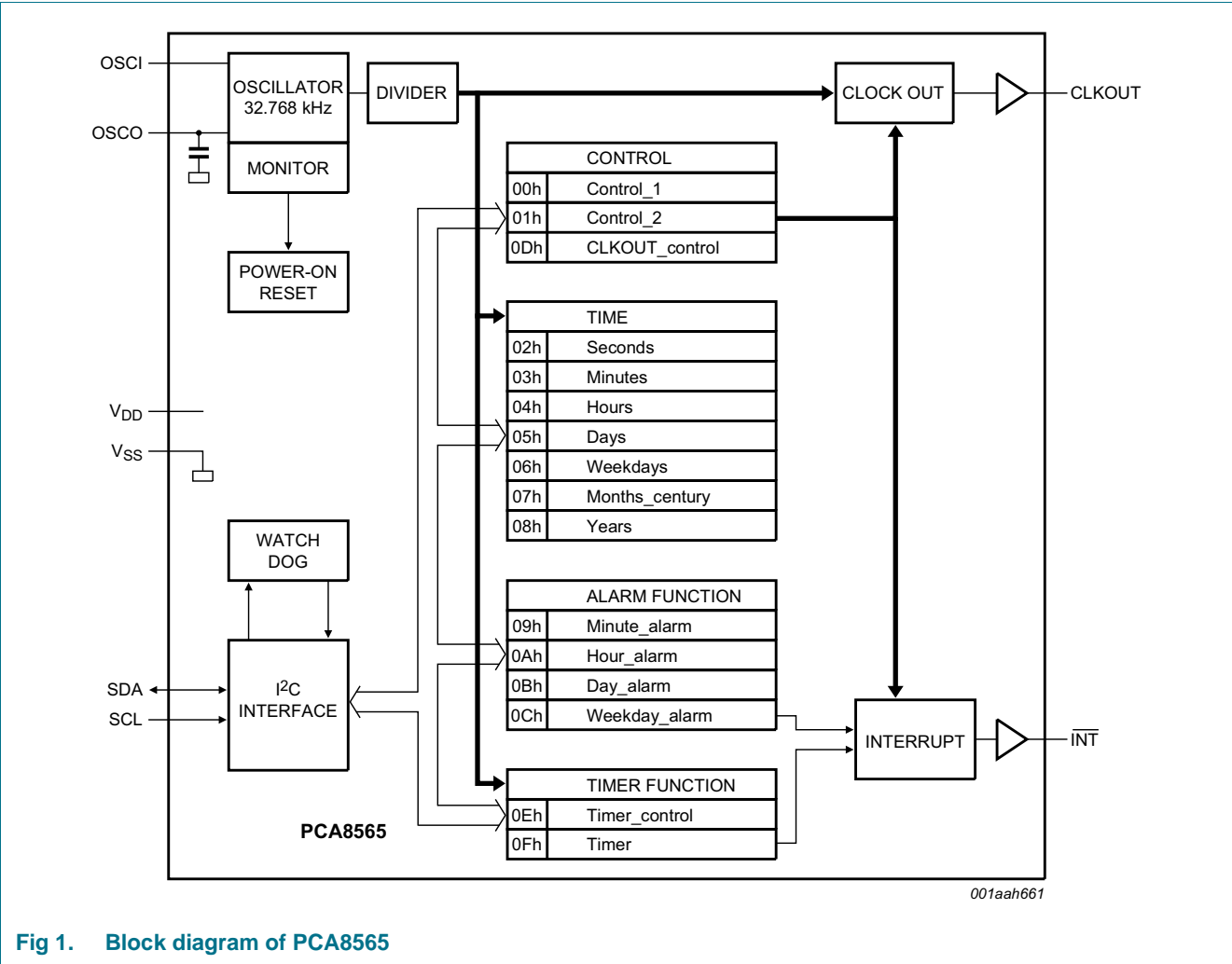
## 6. Block diagram



**Fig 1.    Block diagram of PCA8565**

# 7. Pinning information

## 7.1 Pinning



Top view. For mechanical details see Figure 28.

**Fig 2.** **Pin configuration of PCA8565TS (TSSOP8)**
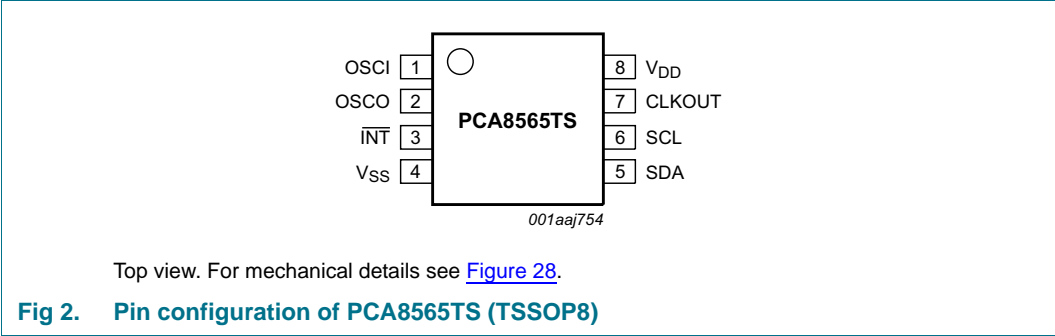
## 7.2 Pin description

**Table 4.** **Pin description**
*Input or input/output pins must always be at a defined level ($V_{SS}$ or $V_{DD}$) unless otherwise specified.*

| Symbol | Pin | Description |
|--------|-----|-------------|
|        | **PCA8565TS** | |
| OSCI | 1 | oscillator input |
| OSCO | 2 | oscillator output |
| $\overline{INT}$ | 3 | interrupt output (open-drain; active LOW) |
| $V_{SS}$ | 4 | ground |
| SDA | 5 | serial data I/O |
| SCL | 6 | serial clock input |
| CLKOUT | 7 | clock output, open-drain |
| $V_{DD}$ | 8 | positive supply voltage |

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## 8. Functional description

The PCA8565 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz $I^2C$-bus interface.

All 16 registers are designed as addressable 8-bit registers although not all bits are implemented:

- The first two registers (memory address 00h and 01h) are used as control and status registers
- The registers at memory addresses 02h through 08h are used as counters for the clock function (seconds up to years counters)
- Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm
- The register at address 0Dh controls the CLKOUT output frequency
- At address 0Eh is the timer control register and address 0Fh contains the timer value

The arrays SECONDS, MINUTES, HOURS, DAYS, WEEKDAYS, MONTHS, YEARS as well as the bit fields MINUTE_ALARM, HOUR_ALARM, DAY_ALARM and WEEKDAY_ALARM are all coded in Binary Coded Decimal (BCD) format.

When one of the RTC registers is written or read the contents of all time counters are frozen. This prevents faulty writing or reading of the clock or calendar during a carry condition (see Section 9.5.3).

## 8.1  Register overview

**Table 5.  Register overview and control bits default values**

*Bit positions labeled as - are not implemented. Bit positions labeled as N should always be written with logic 0. Reset values are shown in Table 8.*

| Address | Register name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Control registers** | | | | | | | | | |
| 00h | Control_1 | TEST1 | N | STOP | N | TESTC | N | N | N |
| 01h | Control_2 | N | N | N | TI_TP | AF | TF | AIE | TIE |
| **Time and date registers** | | | | | | | | | |
| 02h | Seconds | VL | SECONDS (0 to 59) | | | | | | |
| 03h | Minutes | - | MINUTES (0 to 59) | | | | | | |
| 04h | Hours | - | - | HOURS (0 to 23) | | | | | |
| 05h | Days | - | - | DAYS (1 to 31) | | | | | |
| 06h | Weekdays | - | - | - | - | - | WEEKDAYS (0 to 6) | | |
| 07h | Months_century | C | - | - | MONTHS (1 to 12) | | | | |
| 08h | Years | YEARS (0 to 99) | | | | | | | |
| **Alarm registers** | | | | | | | | | |
| 09h | Minute_alarm | AE_M | MINUTE_ALARM (0 to 59) | | | | | | |
| 0Ah | Hour_alarm | AE_H | - | HOUR_ALARM (0 to 23) | | | | | |
| 0Bh | Day_alarm | AE_D | - | DAY_ALARM (1 to 31) | | | | | |
| 0Ch | Weekday_alarm | AE_W | - | - | - | - | WEEKDAY_ALARM (0 to 6) | | |
| **CLKOUT control register** | | | | | | | | | |
| 0Dh | CLKOUT_control | FE | - | - | - | - | - | FD | |
| **Timer registers** | | | | | | | | | |
| 0Eh | Timer_control | TE | - | - | - | - | - | TD | |
| 0Fh | Timer | COUNTDOWN_TIMER | | | | | | | |

## 8.2 Control registers

### 8.2.1 Register Control_1

**Table 6.    Register Control_1 (address 00h) bits description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 | TEST1 | 0[1] | normal mode |
|   |       | 1 | EXT_CLK test mode |
| 6 | N | 0[2] | default value |
| 5 | STOP | 0[1] | RTC source clock runs |
|   |      | 1 | all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available) |
| 4 | N | 0[2] | default value |
| 3 | TESTC | 0 | power-on reset override facility is disabled; set to logic 0 for normal operation |
|   |       | 1[1] | power-on reset override may be enabled |
| 2 to 0 | N | 000[2] | default value |

[1]    Default value.

[2]    Bits labeled as N should always be written with logic 0.

### 8.2.2 Register Control_2

**Table 7.    Register Control_2 (address 01h) bits description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 to 5 | N | 000[1] | default value |
| 4 | TI_TP | 0[2] | $\overline{\text{INT}}$ is active when TF is active (subject to the status of TIE) |
|   |       | 1 | $\overline{\text{INT}}$ pulses active according to Table 29 (subject to the status of TIE); **Remark:** note that if AF and AIE are active then $\overline{\text{INT}}$ will be permanently active |
| 3 | AF | 0[2] | alarm flag inactive |
|   |    | 1 | alarm flag active |
| 2 | TF | 0[2] | timer flag inactive |
|   |    | 1 | timer flag active |
| 1 | AIE | 0[2] | alarm interrupt disabled |
|   |     | 1 | alarm interrupt enabled |
| 0 | TIE | 0[2] | timer interrupt disabled |
|   |     | 1 | timer interrupt enabled |

[1]    Bits labeled as N should always be written with logic 0.

[2]    Default value.

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## 8.3 Reset

The PCA8565 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I²C-bus logic is initialized including the address pointer. All other registers are set according to Table 8.

**Table 8.    Register reset values[1]**

| Address | Register name | Bit | | | | | | | |
|---------|---------------|-----|---|---|---|---|---|---|---|
| | | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 00h | Control_1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 01h | Control_2 | x | x | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Seconds | 1 | x | x | x | x | x | x | x |
| 03h | Minutes | 1 | x | x | x | x | x | x | x |
| 04h | Hours | x | x | x | x | x | x | x | x |
| 05h | Days | x | x | x | x | x | x | x | x |
| 06h | Weekdays | x | x | x | x | x | x | x | x |
| 07h | Months_century | x | x | x | x | x | x | x | x |
| 08h | Years | x | x | x | x | x | x | x | x |
| 09h | Minute_alarm | 1 | x | x | x | x | x | x | x |
| 0Ah | Hour_alarm | 1 | x | x | x | x | x | x | x |
| 0Bh | Day_alarm | 1 | x | x | x | x | x | x | x |
| 0Ch | Weekday_alarm | 1 | x | x | x | x | x | x | x |
| 0Dh | CLKOUT_control | 1 | x | x | x | x | x | 0 | 0 |
| 0Eh | Timer_control | 0 | x | x | x | x | x | 1 | 1 |
| 0Fh | Timer | x | x | x | x | x | x | x | x |

[1]    Registers labeled 'x' are undefined at power-on and unchanged by subsequent resets.

### 8.3.1 Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I²C-bus pins, SDA and SCL, be toggled in a specific order as shown in Figure 3. All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I²C-bus access. The override mode may be cleared by writing a logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.
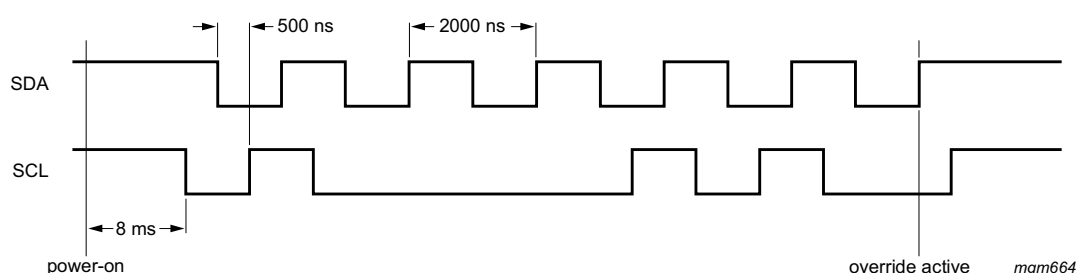
**Fig 3.    POR override sequence**

## 8.4  Time and date registers

The majority of the registers are coded in the BCD format to simplify application use.

### 8.4.1  Register Seconds

**Table 9.    Register Seconds (address 02h) bits description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | VL | 0 | - | clock integrity is guaranteed |
| | | 1[1] | - | integrity of the clock information is not guaranteed |
| 6 to 4 | SECONDS | 0 to 5 | ten's place | actual seconds coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1]    Start-up value.

**Table 10.    Seconds coded in BCD format**

| Seconds value in decimal | Upper-digit (ten's place) | | | Digit (unit place) | | | |
|---|---|---|---|---|---|---|---|
| | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| : | | | | | | | |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| : | | | | | | | |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

#### 8.4.1.1  Voltage-low detector

The PCA8565 has an on-chip voltage-low detector. When $V_{DD}$ drops below $V_{low}$, bit VL in the Seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag is cleared by command.

Bit VL is intended to detect the situation when $V_{DD}$ is decreasing slowly, for example under battery operation. Should $V_{DD}$ reach $V_{low}$ before power is re-asserted then bit VL is set. This indicates that the time may be corrupt (see Figure 4).

**Fig 4.  Voltage-low detection**
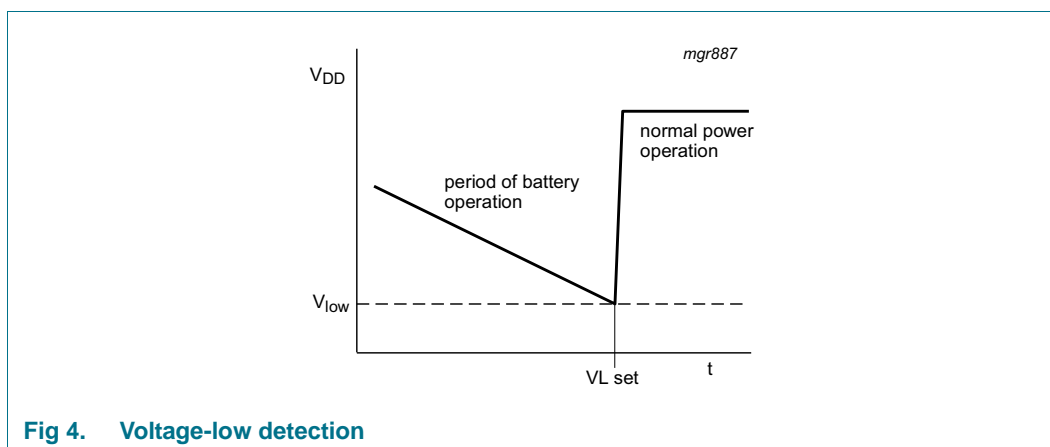
### 8.4.2  Register Minutes

**Table 11.    Register Minutes (address 03h) bits description**

| Bit | Symbol | Value | Place value | Description |
|-----|--------|-------|-------------|-------------|
| 7 | - | - | - | unused |
| 6 to 4 | MINUTES | 0 to 5 | ten's place | actual minutes coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 8.4.3  Register Hours

**Table 12.    Register Hours (address 04h) bits description**

| Bit | Symbol | Value | Place value | Description |
|-----|--------|-------|-------------|-------------|
| 7 to 6 | - | - | - | unused |
| 5 to 4 | HOURS | 0 to 2 | ten's place | actual hours coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 8.4.4  Register Days

**Table 13.    Register Days (address 05h) bits description**

| Bit | Symbol | Value | Place value | Description |
|-----|--------|-------|-------------|-------------|
| 7 to 6 | - | - | - | unused |
| 5 to 4 | DAYS[1] | 0 to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1]    The PCA8565 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

### 8.4.5  Register Weekdays

**Table 14.    Register Weekdays (address 06h) bits description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 to 3 | - | - | unused |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday values, see Table 15 |

**Table 15.    Weekday assignments**

| Day[1] | Bit | | |
|---|---|---|---|
| | **2** | **1** | **0** |
| Sunday | 0 | 0 | 0 |
| Monday | 0 | 0 | 1 |
| Tuesday | 0 | 1 | 0 |
| Wednesday | 0 | 1 | 1 |
| Thursday | 1 | 0 | 0 |
| Friday | 1 | 0 | 1 |
| Saturday | 1 | 1 | 0 |

[1]    Definition may be re-assigned by the user.

### 8.4.6  Register Months_century

**Table 16.    Register Months_century (address 07h) bits description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 | C[1] | 0[2] | - | indicates the century is x |
| | | 1 | - | indicates the century is x + 1 |
| 6 to 5 | - | - | - | unused |
| 4 | MONTHS | 0 to 1 | ten's place | actual month coded in BCD format, see Table 17 |
| 3 to 0 | | 0 to 9 | unit place | |

[1]    This bit may be re-assigned by the user.

[2]    This bit is toggled when the years register overflows from 99 to 00.

**Table 17.    Month assignments coded in BCD format**

| Month | Upper-digit (ten's place) | Digit (unit place) | | | |
|---|---|---|---|---|---|
| | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| January | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 1 | 0 | 0 | 1 |
| October | 1 | 0 | 0 | 0 | 0 |
| November | 1 | 0 | 0 | 0 | 1 |
| December | 1 | 0 | 0 | 1 | 0 |

### 8.4.7 Register Years

**Table 18.    Register Years (08h) bits description**

| Bit | Symbol | Value | Place value | Description |
|---|---|---|---|---|
| 7 to 4 | YEARS | 0 to 9 | ten's place | actual year coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

## 8.5 Setting and reading the time

Figure 5 shows the data flow and data dependencies starting from the 1 Hz clock tick.
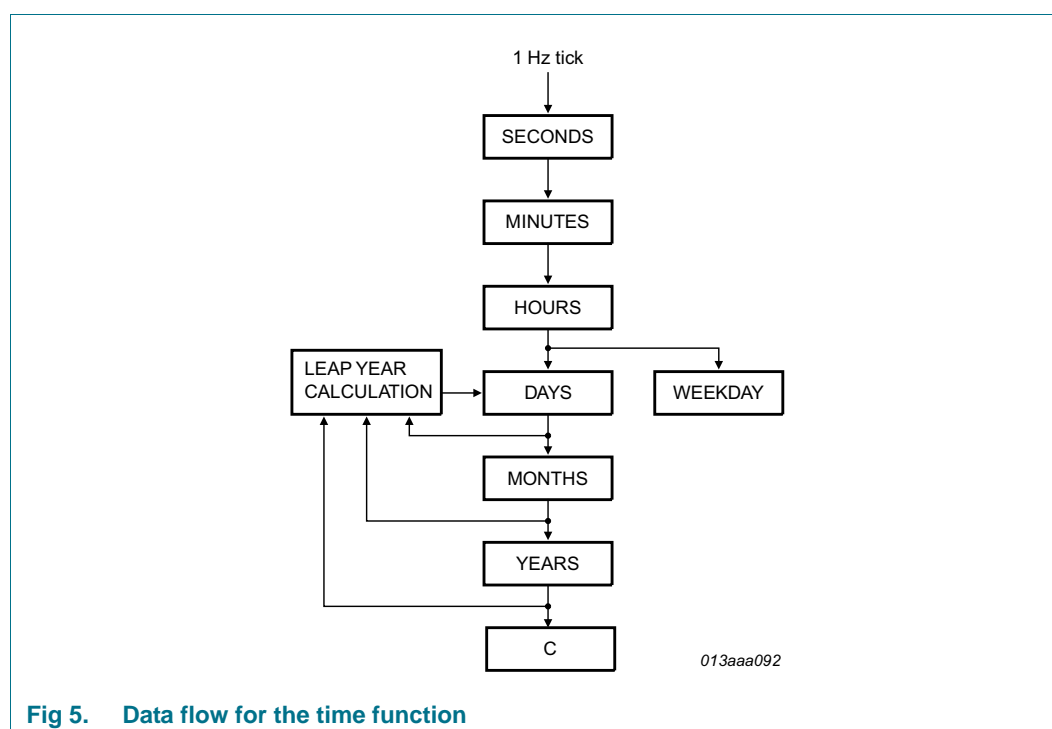


**Fig 5.    Data flow for the time function**

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers, during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 6).

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.
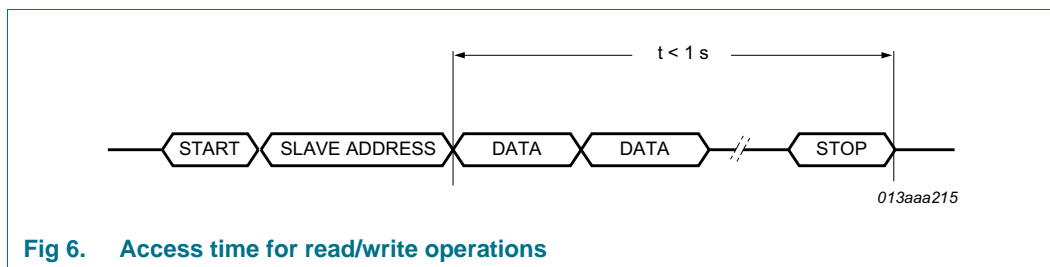
**Fig 6.    Access time for read/write operations**

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h).

2. Set the address pointer to registers Seconds (02h).

3. Send a RESTART condition or STOP followed by START.

4. Send the slave address for read (A3h).

5. Read the register Seconds.

6. Read the register Minutes.

7. Read the register Hours.

8. Read the register Days.

9. Read the register Weekdays.

10. Read the register Months_century.

11. Read the register Years.

12. Send a STOP condition.

## 8.6  Alarm registers

When one or more of the alarm registers are loaded with a valid minute, hour, day or weekday and its corresponding bit alarm enable (AE_x) is logic 0, then that information is compared with the actual minute, hour, day and weekday.

When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by command. **Once AF has been cleared it is only set again when the time increments to match the alarm condition once more.** (For clearing the AF, see Section 8.9.1.1 on page 18.)

Alarm registers which have their bit AE_x at logic 1 are ignored.

(1) Only when all enabled alarm settings are matching.

It's only on increment to a matched case that the alarm is set, see Section 8.9.1.1.

**Fig 7.    Alarm function block diagram**
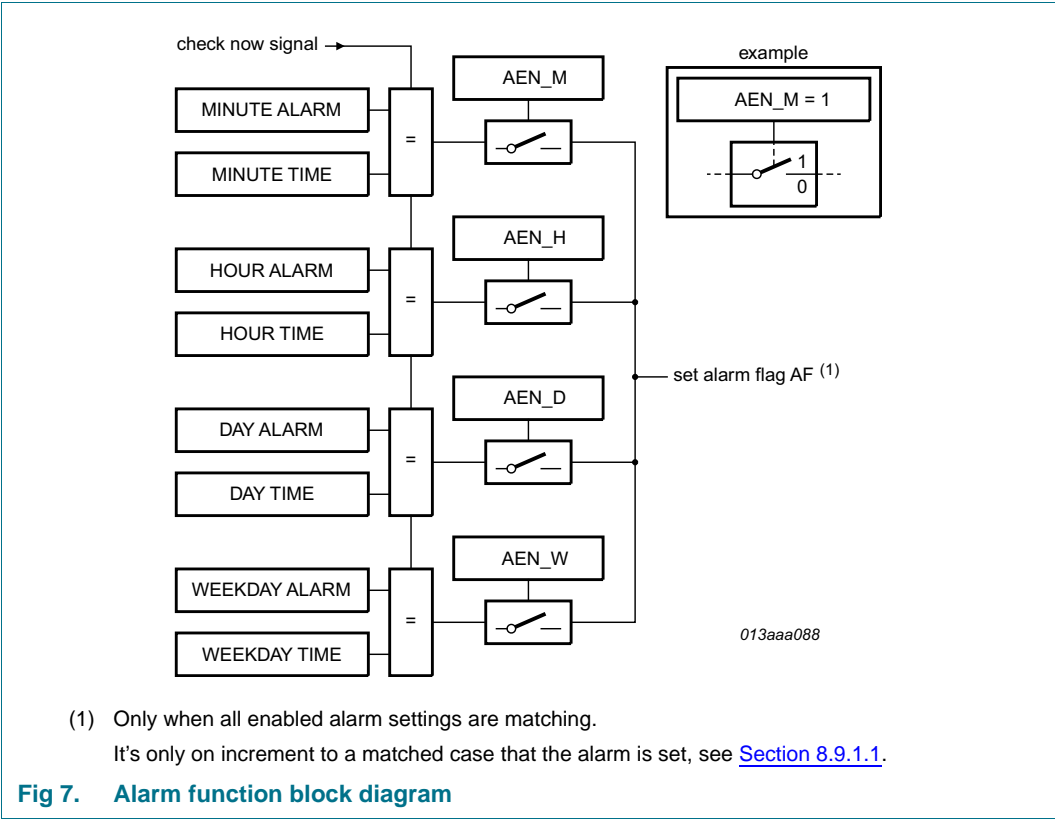
### 8.6.1  Register Minute_alarm

**Table 19.    Register Minute_alarm (address 09h) bits description**

| Bit | Symbol | Value | Place value | Description |
|-----|--------|-------|-------------|-------------|
| 7 | AE_M | 0 | - | minute alarm is enabled |
|   |      | 1[1] | - | minute alarm is disabled |
| 6 to 4 | MINUTE_ALARM | 0 to 5 | ten's place | minute alarm information coded in BCD format |
| 3 to 0 |            | 0 to 9 | unit place |  |

[1]   Default value.

### 8.6.2  Register Hour_alarm

**Table 20.    Register Hour_alarm (address 0Ah) bits description**

| Bit | Symbol | Value | Place value | Description |
|-----|--------|-------|-------------|-------------|
| 7 | AE_H | 0 | - | hour alarm is enabled |
|   |      | 1[1] | - | hour alarm is disabled |
| 6 | - | - | - | unused |
| 5 to 4 | HOUR_ALARM | 0 to 2 | ten's place | hour alarm information coded in BCD format |
| 3 to 0 |            | 0 to 9 | unit place |  |

[1]   Default value.

### 8.6.3 Register Day_alarm

**Table 21.  Register Day_alarm (address 0Bh) bits description**

| Bit | Symbol | Value | Place value | Description |
|-----|--------|-------|-------------|-------------|
| 7 | AE_D | 0 | - | day alarm is enabled |
|   |        | 1[1] | - | day alarm is disabled |
| 6 | - | - | - | unused |
| 5 to 4 | DAY_ALARM | 0 to 3 | ten's place | day alarm information coded in BCD format |
| 3 to 0 |  | 0 to 9 | unit place |  |

[1]    Default value.

### 8.6.4 Register Weekday_alarm

**Table 22.  Register Weekday_alarm (address 0Ch) bits description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 | AE_W | 0 | weekday alarm is enabled |
|   |       | 1[1] | weekday alarm is disabled |
| 6 to 3 | - | - | unused |
| 2 to 0 | WEEKDAY_ALARM | 0 to 6 | weekday alarm information coded in BCD format |

[1]    Default value.

## 8.7  Timer functions

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $\frac{1}{60}$ Hz) and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag (TF) in the register Control_status_2. The TF may only be cleared by command. The asserted TF can be used to generate an interrupt (on pin $\overline{\text{INT}}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the state of TF. Bit TI_TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

### 8.7.1  Register Timer_control

The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the bit TE in register Timer_control. The source clock for the timer is also selected by the TD[1:0] in register Timer_control. Other timer properties such as interrupt generation are controlled via register Control_2.

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**Table 23.    Register Timer_control (address 0Eh) bits description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | TE | 0[1] | timer is disabled |
| | | 1 | timer is enabled |
| 6 to 2 | - | - | unused |
| 1 to 0 | TD[1:0] | | timer source clock frequency select[2] |
| | | 00 | 4.096 kHz |
| | | 01 | 64 Hz |
| | | 10 | 1 Hz |
| | | 11[2] | $\frac{1}{60}$ Hz |

[1]    Default value.

[2]    These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to $\frac{1}{60}$ Hz for power saving.

### 8.7.2  Register Countdown_Timer

**Table 24.    Timer (address 0Fh) bits description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 0 | COUNTDOWN_TIMER | 00h to FFh | countdown period in seconds:<br><br>$$CountdownPeriod = \frac{n}{SourceClockFrequency}$$<br><br>where n is the countdown value |

**Table 25.    Timer register bits value range**

| Bit | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

The timer register is an 8-bit binary countdown timer. It is enabled or disabled via the Timer_control register. The source clock for the timer is also selected by the Timer_control register. Other timer properties such as single or periodic interrupt generation are controlled via the register Control_status_2 (address 01h).

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

## 8.8  Register CLKOUT_control and clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the CLKOUT_control register at address 0Dh. Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

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**Table 26.    Register CLKOUT_control (address 0Dh) bits description**

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 7 | FE | 0 | the CLKOUT output is inhibited and CLKOUT output is set to high-impedance |
| | | 1[1] | the CLKOUT output is activated |
| 6 to 2 | - | - | unused |
| 1 to 0 | FD[1:0] | | frequency output at pin CLKOUT |
| | | 00[1] | 32.768 kHz |
| | | 01 | 1.024 kHz |
| | | 10 | 32 Hz |
| | | 11 | 1 Hz |

[1]    Default value.

## 8.9  Interrupt output

### 8.9.1  Bits TF and AF

When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value until overwritten by command. If both timer and alarm interrupts are required in the application, the source of the interrupt is determined by reading these bits.



Example where only the minute alarm is used and no other interrupts are enabled.

**Fig 8.    AF timing**

When bits TIE and AIE are disabled, pin INT will remain high-impedance.

**Fig 9.    Interrupt scheme**
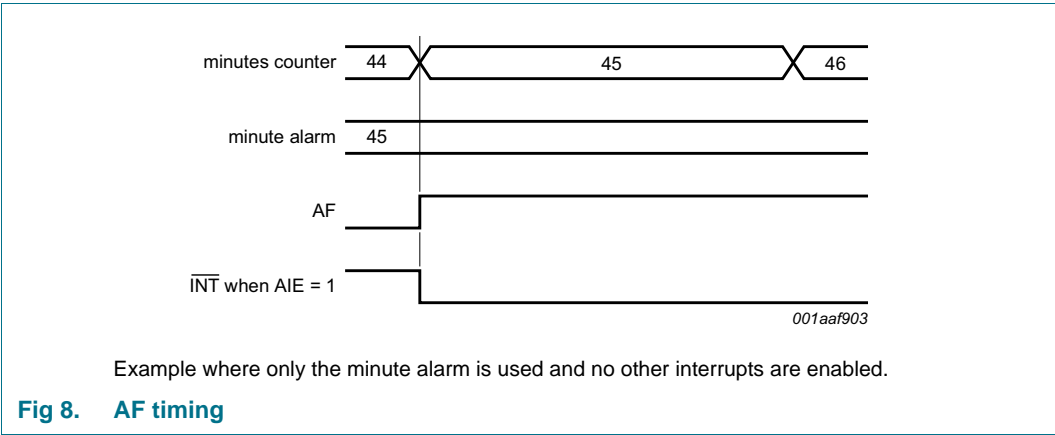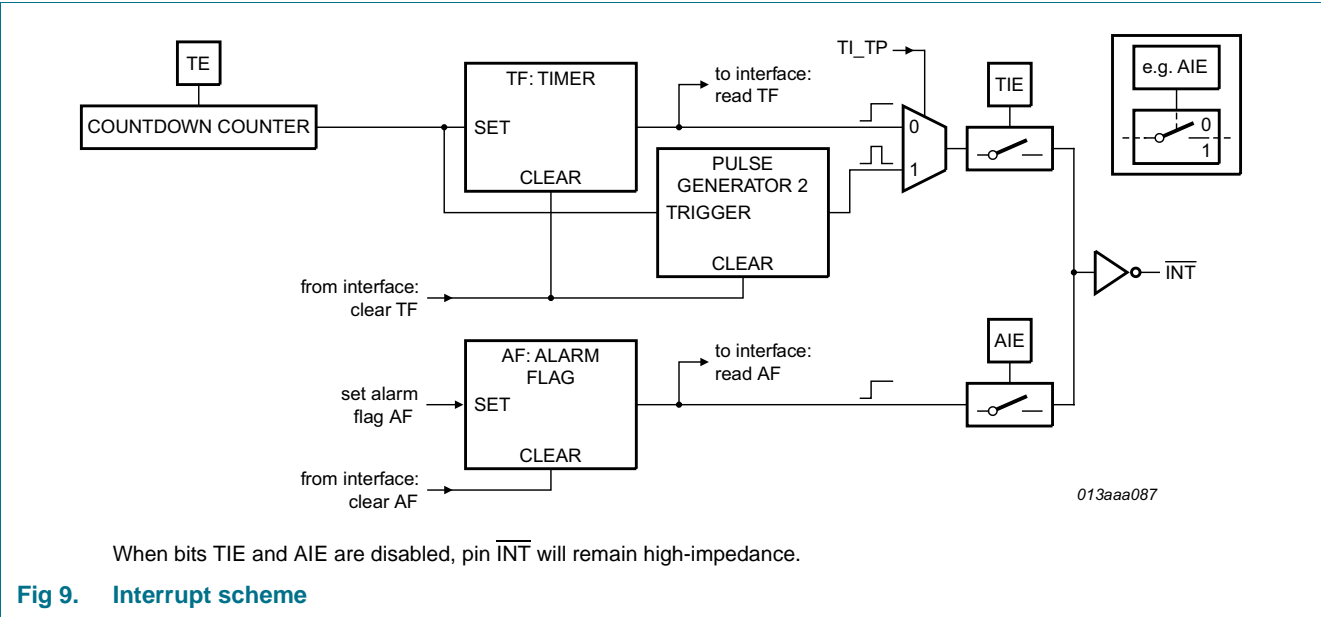
#### 8.9.1.1   Clearing the alarm flag (AF)

Table 28 shows an example for clearing bit AF but leaving bit TF unaffected. Clearing the flags is made by a write command; therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

To prevent the timer flags being overwritten while clearing AF, a logical AND is performed during a write access. Writing a logic 1 will cause the flag to maintain its value, whereas writing a logic 0 will cause the flag to be reset.

**Table 27.    Flag location in register Control_2**

| Register | Bit | | | | | | | |
|----------|-----|---|---|---|---|---|---|---|
|          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Control_2 | -  | - | - | - | AF | TF | - | - |

The following table shows what instruction must be sent to clear bit AF. In this example bit TF is unaffected.

**Table 28.    Example to clear only AF (bit 3) in register Control_2**

| Register | Bit | | | | | | | |
|----------|-----|---|---|---|---|---|---|---|
|          | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Control_2 | -  | - | - | - | 0 | 1 | - | - |

### 8.9.2   Bits TIE and AIE

These bits activate or deactivate the generation of an interrupt when TF or AF is asserted respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

### 8.9.3 Countdown timer interrupts

The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies (see Table 29).

**Table 29.** $\overline{\text{INT}}$ **operation (bit TI_TP = 1)**

| Source clock (Hz) | $\overline{\text{INT}}$ period (s) | |
|---|---|---|
| | n = 1[1] | n > 1 |
| 4096 | $^1/_{8192}$ | $^1/_{4096}$ |
| 64 | $^1/_{128}$ | $^1/_{64}$ |
| 1 | $^1/_{64}$ | $^1/_{64}$ |
| $^1/_{60}$ | $^1/_{64}$ | $^1/_{64}$ |

[1]  n = loaded countdown value. Timer stopped when n = 0.

## 8.10 External clock (EXT_CLK) test mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1 000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a $2^6$ divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0 (STOP must be cleared before the prescaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

**Remark:** Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_CLK test mode (Control_1, bit TEST1 = 1).
2. Set STOP (Control_1, bit STOP = 1).
3. Clear STOP (Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

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## 8.11 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler ($F_2$ to $F_{14}$) to be held in reset and thus no 1 Hz ticks will be generated (see Figure 10). The time circuits can then be set and will not increment until the STOP bit is released (see Figure 11 and Table 30).
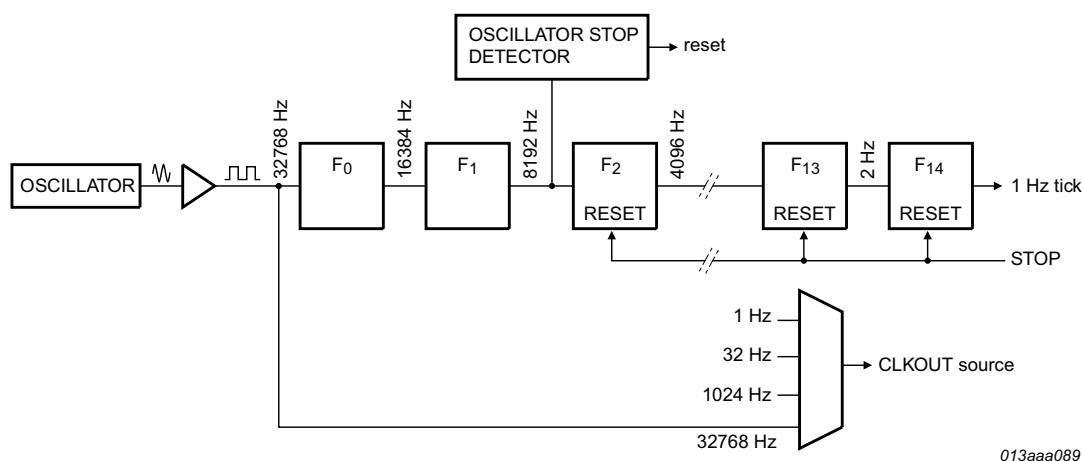


**Fig 10.   STOP bit functional diagram**

The STOP bit function will not affect the output of 32.768 kHz but will stop 1.024 kHz, 32 Hz and 1 Hz.

The lower two stages of the prescaler ($F_0$ and $F_1$) are not reset and because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 8.192 kHz cycle (see Figure 11).
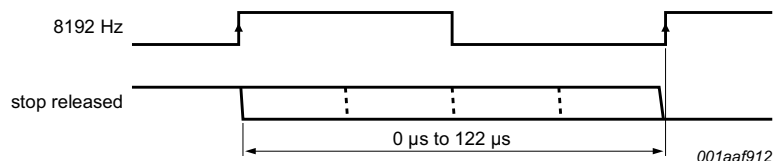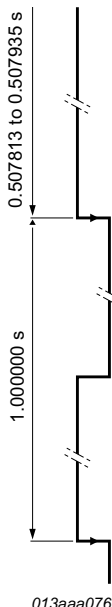


**Fig 11.   STOP bit release timing**

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**Table 30. First increment of time circuits after STOP bit release**

| Bit STOP | Prescaler bits $F_0F_1$-$F_2$ to $F_{14}$ | [1]  1 Hz tick | Time hh:mm:ss | Comment |
|---|---|---|---|---|
| **Clock is running normally** | | | | |
| 0 | 01-0 0001 1101 0100 | | 12:45:12 | prescaler counting normally |
| **STOP bit is activated by user. $F_0F_1$ are not reset and values cannot be predicted externally** | | | | |
| 1 | XX-0 0000 0000 0000 | | 12:45:12 | prescaler is reset; time circuits are frozen |
| **New time is set by user** | | | | |
| 1 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is reset; time circuits are frozen |
| **STOP bit is released by user** | | | | |
| 0 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is now running |
| | XX-1 0000 0000 0000 | | 08:00:00 | - |
| | XX-0 1000 0000 0000 | | 08:00:00 | - |
| | XX-1 1000 0000 0000 | | 08:00:00 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:00 | - |
| | 00-0 0000 0000 0001 | | 08:00:01 | 0 to 1 transition of $F_{14}$ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1111 | | 08:00:01 | - |
| | 00-0 0000 0000 0000 | | 08:00:01 | - |
| | 10-0 0000 0000 0000 | | 08:00:01 | - |
| | : | | : | - |
| | 11-1 1111 1111 1110 | | 08:00:01 | - |
| | 00-0 0000 0000 0001 | | 08:00:02 | 0 to 1 transition of $F_{14}$ increments the time circuits |



0.507813 to 0.507935 s; 1.000000 s; 013aaa076

[1]  $F_0$ is clocked at 32.768 kHz.

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits $F_0$ and $F_1$ not being reset (see Table 30) and the unknown state of the 32 kHz clock.

# 9. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

## 9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 12).
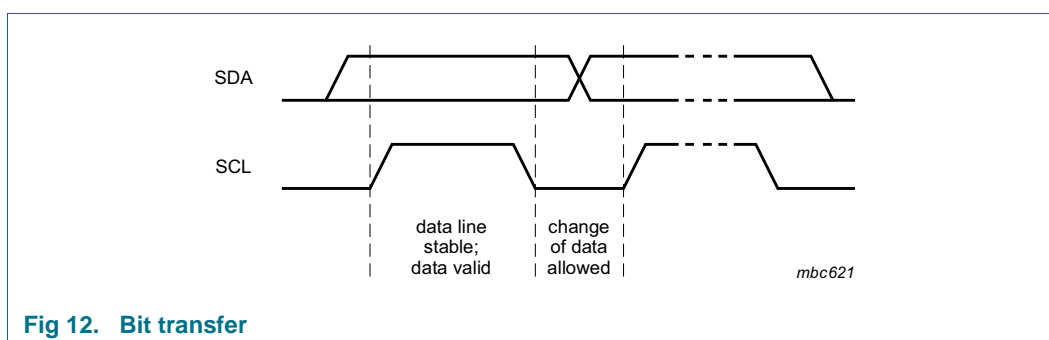


**Fig 12. Bit transfer**

## 9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P), see Figure 13.
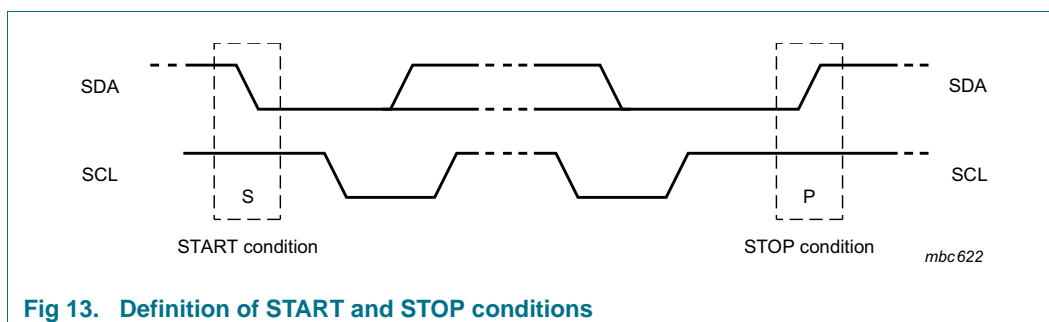


**Fig 13. Definition of START and STOP conditions**

## 9.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 14).
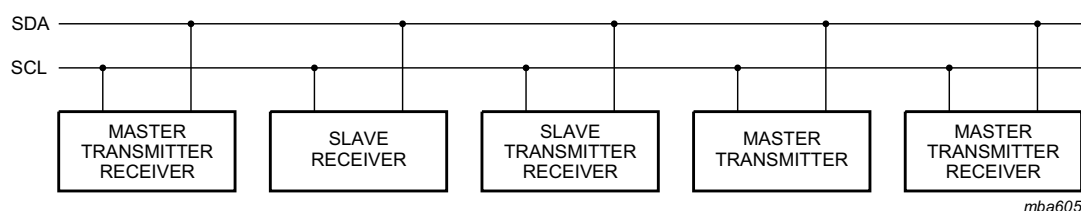
**Fig 14. System configuration**

## 9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.

- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I$^2$C-bus is shown in Figure 15.
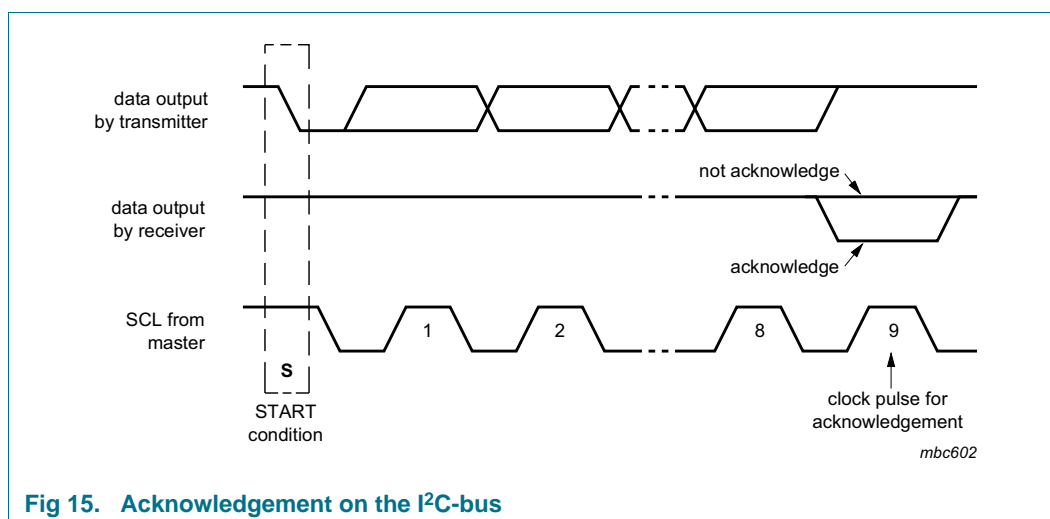


**Fig 15. Acknowledgement on the I$^2$C-bus**

### 9.5 I²C-bus protocol

#### 9.5.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCA8565 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCA8565 slave address is shown in Figure 16.
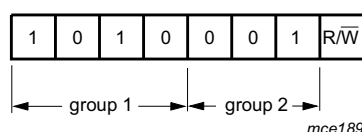


**Fig 16. Slave address**

#### 9.5.2 Clock and calendar read/write cycles

The I²C-bus configuration for the different PCA8565 read and write cycles is shown in Figure 17, Figure 18 and Figure 19. The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.
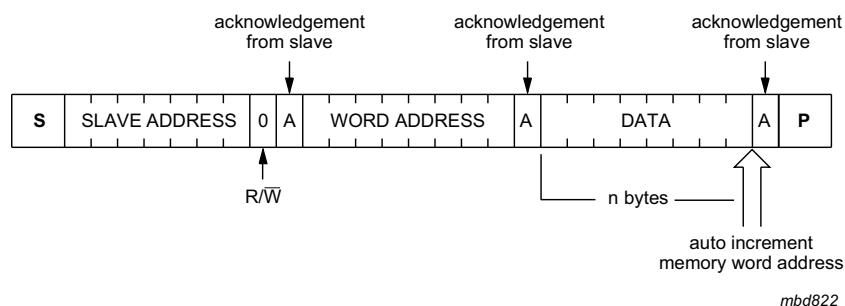


**Fig 17. Master transmits to slave receiver (write mode)**

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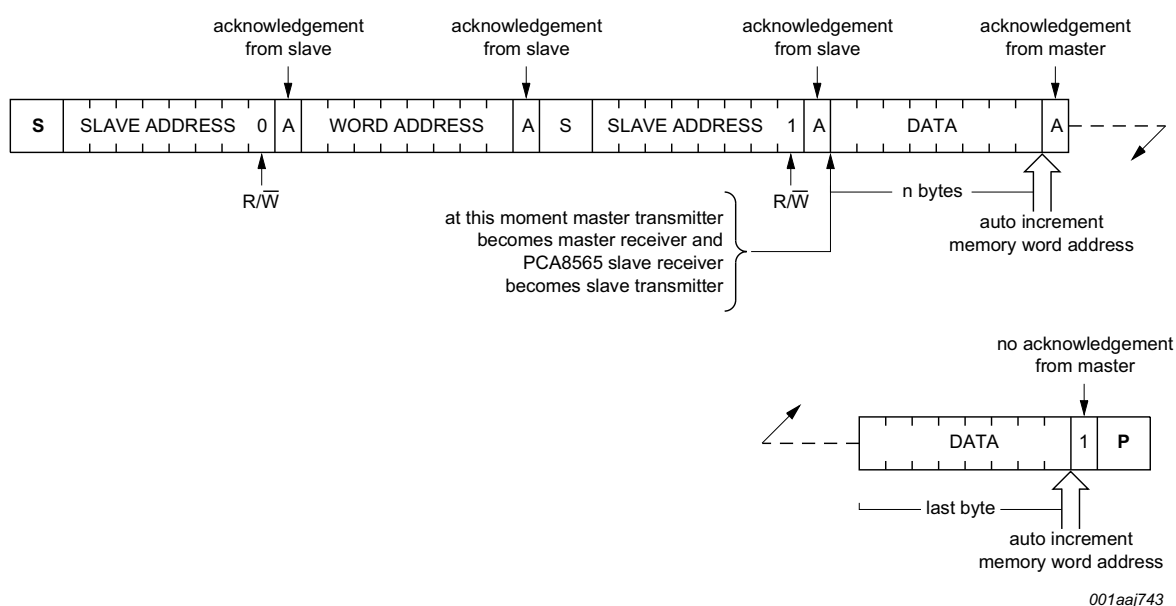
**Fig 18.  Master reads after setting word address (write word address; read data)**
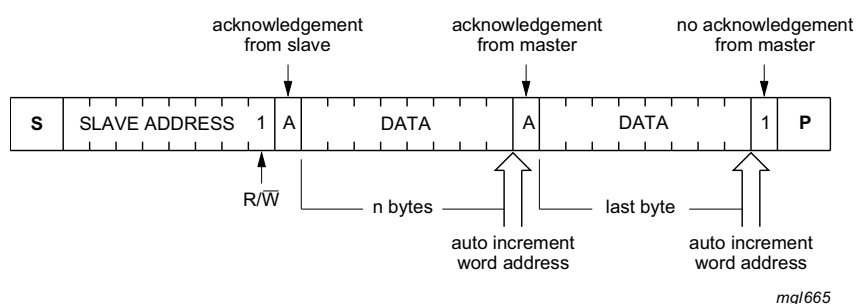


**Fig 19.  Master reads slave immediately after first byte (read mode)**

### 9.5.3  Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface, the PCA8565 has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid slave address is transmitted, then the PCA8565 will automatically clear the interface and allow the time counting circuits to continue counting. Under a correct data transfer, the watchdog timer is stopped on receipt of a START or STOP condition.

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s will be lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid slave address.

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a. Correct data transfer: read or write



b. Incorrect data transfer: read or write

**Fig 20.  Interface watchdog timer**
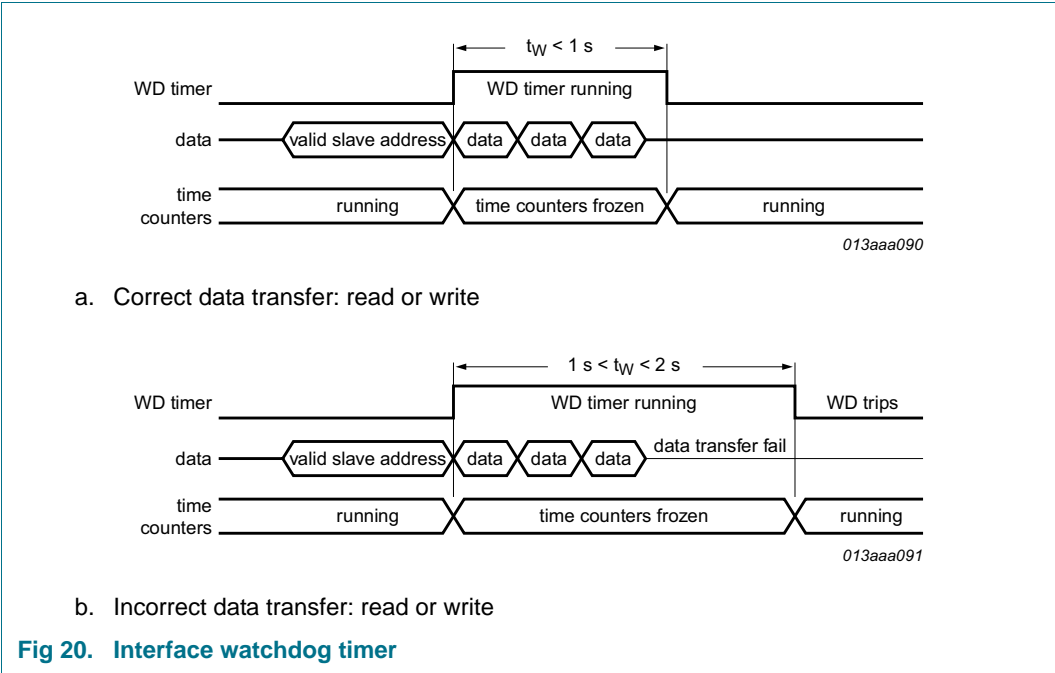
# 10. Internal circuitry
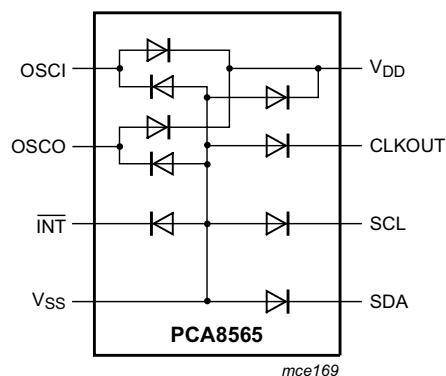


**Fig 21.   Device diode protection diagram of PCA8565**

# 11. Safety notes

| CAUTION |
| --- |
| This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards. |

## 12. Limiting values

**Table 31. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | −0.5 | +6.5 | V |
| $I_{SS}$ | ground supply current | | | −50 | +50 | mA |
| $I_{DD}$ | supply current | | | −50 | +50 | mA |
| $V_I$ | input voltage | | | −0.5 | +6.5 | V |
| $I_I$ | input current | | | −10 | +10 | mA |
| $I_O$ | output current | | | −10 | +10 | mA |
| $P_{tot}$ | total power dissipation | | | - | 300 | mW |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [1] | - | ±3000 | V |
| | | CDM | [2] | - | ±1100 | V |
| $I_{lu}$ | latch-up current | | [3] | - | 250 | mA |
| $T_{stg}$ | storage temperature | | [4] | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +125 | °C |

[1] Pass level; Human Body Model (HBM) according to Ref. 6 "JESD22-A114".

[2] Pass level; Charged-Device Model (CDM), according to Ref. 7 "JESD22-C101".

[3] Pass level; latch-up testing, according to Ref. 8 "JESD78".

[4] According to the store and transport requirements (see Ref. 14 "UM10569") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

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## 13. Static characteristics

**Table 32.  Static characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +125 °C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 40 kΩ; $C_L$ = 8 pF; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DD}$ | supply voltage | | 1.8 | - | 5.5 | V |
| | | for clock data integrity | $V_{low}$ | - | 5.5 | V |
| $V_{low}$ | low voltage | for low voltage detection | - | 0.9 | 1.7 | V |
| $I_{DD}$ | supply current | interface active | | | | |
| | | $f_{SCL}$ = 400 kHz | - | - | 820 | µA |
| | | $f_{SCL}$ = 100 kHz | - | - | 220 | µA |
| | | interface inactive ($f_{SCL}$ = 0 Hz); $T_{amb}$ = 25 °C [1] | | | | |
| | | CLKOUT disabled | | | | |
| | | $V_{DD}$ = 5.0 V | - | 750 | 1500 | nA |
| | | $V_{DD}$ = 4.0 V | - | 700 | 1400 | nA |
| | | $V_{DD}$ = 3.0 V | - | 650 | 1300 | nA |
| | | $V_{DD}$ = 2.0 V | - | 600 | 1200 | nA |
| | | $V_{DD}$ = 5.0 V; $T_{amb}$ = 125 °C [2] | - | 750 | 5000 | nA |
| | | CLKOUT enabled at 32 kHz [1] | | | | |
| | | $V_{DD}$ = 5.0 V | - | 1000 | 2000 | nA |
| | | $V_{DD}$ = 4.0 V | - | 900 | 1800 | nA |
| | | $V_{DD}$ = 3.0 V | - | 800 | 1600 | nA |
| | | $V_{DD}$ = 2.0 V | - | 700 | 1400 | nA |
| | | $V_{DD}$ = 5.0 V; $T_{amb}$ = 125 °C [2] | - | 1000 | 6000 | nA |
| **Inputs** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | $V_{SS}$ − 0.3 | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | on pins SCL and SDA | $0.7V_{DD}$ | - | 5.5 | V |
| | | on pin OSCI | $0.7V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| $I_{LI}$ | input leakage current | on pins SCL and SDA; $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | 0 | +1 | µA |
| $C_i$ | input capacitance | [3] | - | - | 7 | pF |

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**Table 32.   Static characteristics** *…continued*

$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 ℃ to +125 ℃; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 40 kΩ; $C_L$ = 8 pF; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Outputs** | | | | | | |
| $I_{OL}$ | LOW-level output current | output sink current | | | | |
| | | $V_{OL}$ = 0.4 V; $V_{DD}$ = 5 V | | | | |
| | | on pin SDA | 3 | - | - | mA |
| | | on pin $\overline{INT}$ | 1 | - | - | mA |
| | | $V_O$ = $V_{DD}$ or $V_{SS}$ | | | | |
| | | on pin CLKOUT | 1 | - | - | mA |
| $I_{LO}$ | output leakage current | | −1 | 0 | +1 | µA |

[1]   Timer source clock = $\frac{1}{60}$ Hz, level of pins SCL and SDA is $V_{DD}$ or $V_{SS}$.

[2]   Worst case is at high temperature and high supply voltage.

[3]   Tested on sample basis.



$T_{amb}$ = 25 °C; Timer = 1 minute; CLKOUT disabled.

**Fig 22.   $I_{DD}$ as a function of $V_{DD}$**



$T_{amb}$ = 25 °C; Timer = 1 minute; CLKOUT = 32 kHz.

**Fig 23.   $I_{DD}$ as a function of $V_{DD}$**

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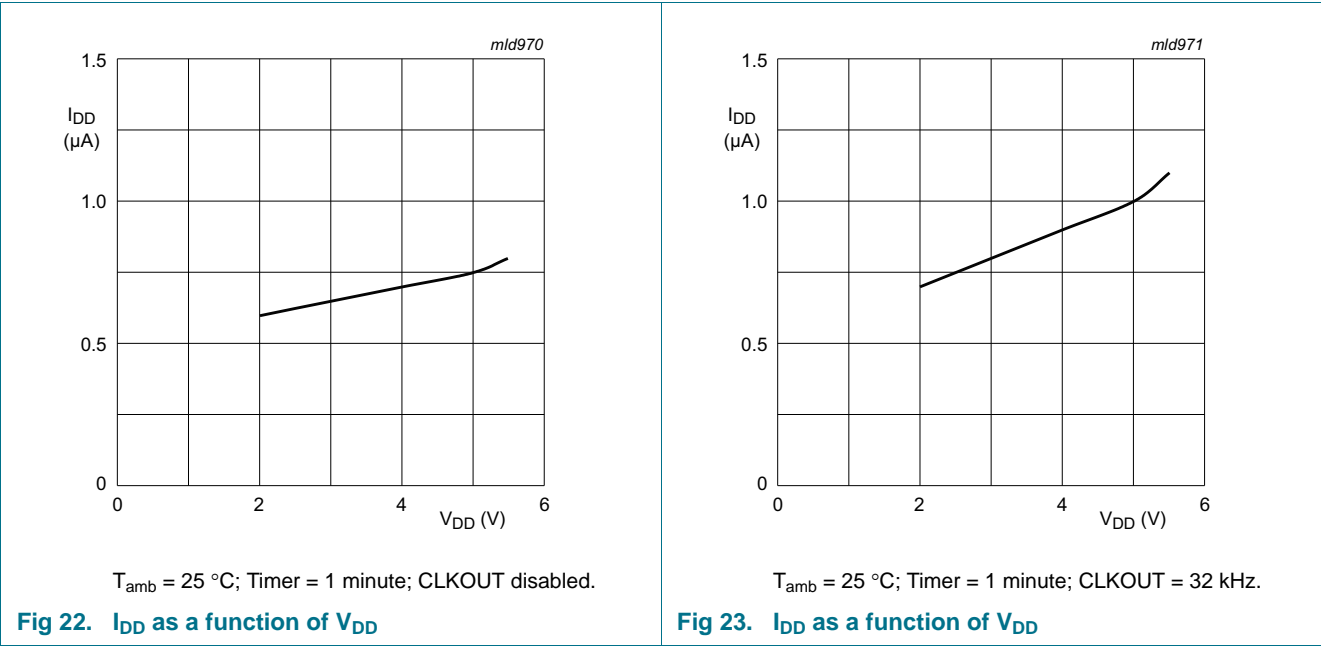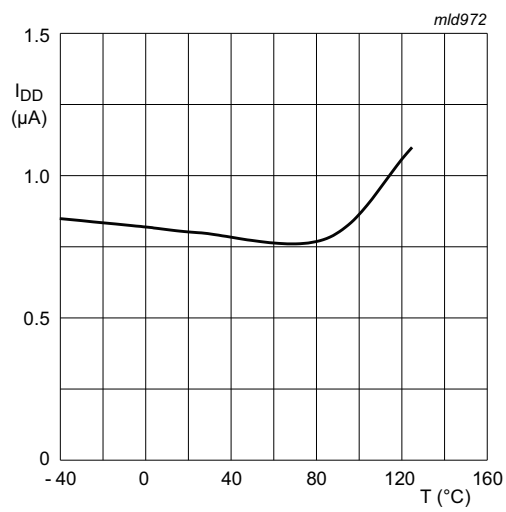
V<sub>DD</sub> = 3 V; Timer = 1 minute; CLKOUT = 32 kHz.

**Fig 24.   I_DD as a function of temperature**
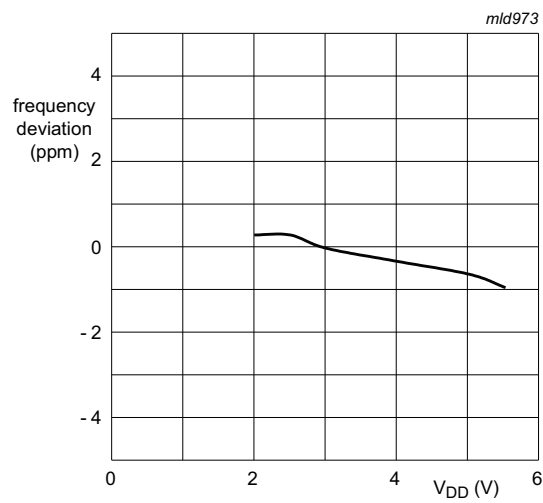


T<sub>amb</sub> = 25 °C; normalized to V<sub>DD</sub> = 3 V.

**Fig 25.   Frequency deviation as a function of V_DD**

## 14. Dynamic characteristics

**Table 33.   Dynamic characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +125 °C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 40 kΩ; $C_L$ = 8 pF; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Oscillator** | | | | | | |
| $C_{L(itg)}$ | integrated load capacitance | [1] | 15 | 25 | 35 | pF |
| $\Delta f_{osc}/f_{osc}$ | relative oscillator frequency variation | $\Delta V_{DD}$ = 200 mV; $T_{amb}$ = 25 °C | - | 0.2 | - | ppm |
| **Quartz crystal parameters (f = 32.768 kHz)** | | | | | | |
| $R_s$ | series resistance | | - | - | 100 | kΩ |
| $C_L$ | load capacitance | | - | 10 | - | pF |
| $C_{trim}$ | trimmer capacitance | | 5 | - | 25 | pF |
| **CLKOUT output** | | | | | | |
| $\delta_{CLKOUT}$ | duty cycle on pin CLKOUT | [2] | - | 50 | - | % |
| **I²C-bus timing characteristics** | | [3][4] | | | | |
| $f_{SCL}$ | SCL clock frequency | [5] | - | - | 400 | kHz |
| $t_{HD;STA}$ | hold time (repeated) START condition | | 0.6 | - | - | μs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 0.6 | - | - | μs |
| $t_{LOW}$ | LOW period of the SCL clock | | 1.3 | - | - | μs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | 0.6 | - | - | μs |
| $t_r$ | rise time of both SDA and SCL signals | | - | - | 0.3 | μs |
| $t_f$ | fall time of both SDA and SCL signals | | - | - | 0.3 | μs |
| $t_{SU;DAT}$ | data set-up time | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | - | - | ns |
| $t_{BUF}$ | bus free time between a STOP and START condition | | 4.7 | - | - | μs |
| $t_{SU;STO}$ | set-up time for STOP condition | | 0.6 | - | - | μs |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | | - | - | 50 | ns |
| $C_b$ | capacitive load for each bus line | | - | - | 400 | pF |

[1]   Integrated load capacitance, $C_{L(itg)}$, is a calculation of $C_{OSCI}$ and $C_{OSCO}$ in series. $C_{L(itg)} = \dfrac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$

[2]   For $f_{CLKOUT}$ = 1.024 kHz, 32 Hz and 1 Hz.

[3]   All timing values are valid within the operating supply voltage at ambient temperature and referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.

[4]   A detailed description of the I²C-bus specification is given in the document Ref. 12 "UM10204".

[5]   I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.
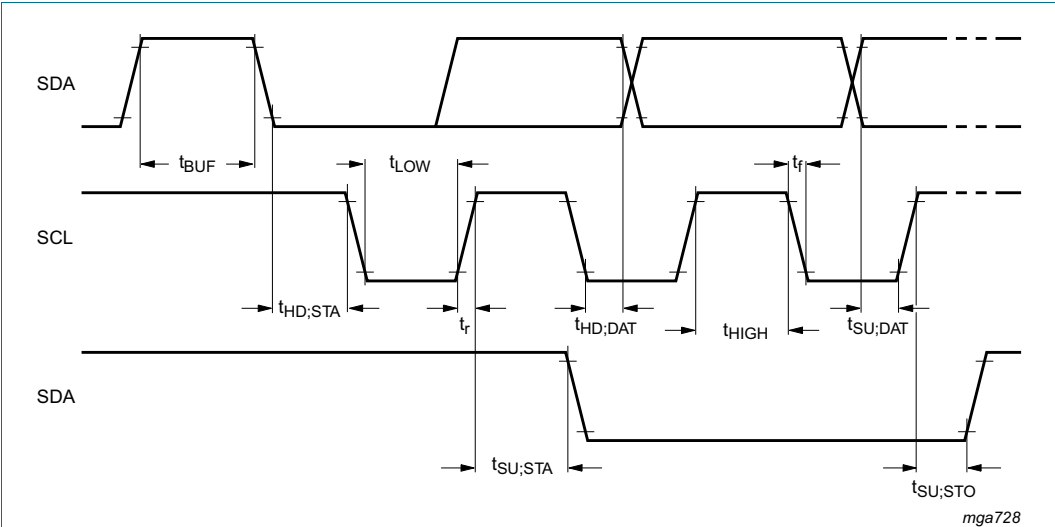
**Fig 26.** **I²C-bus timing waveforms**

## 15. Application information
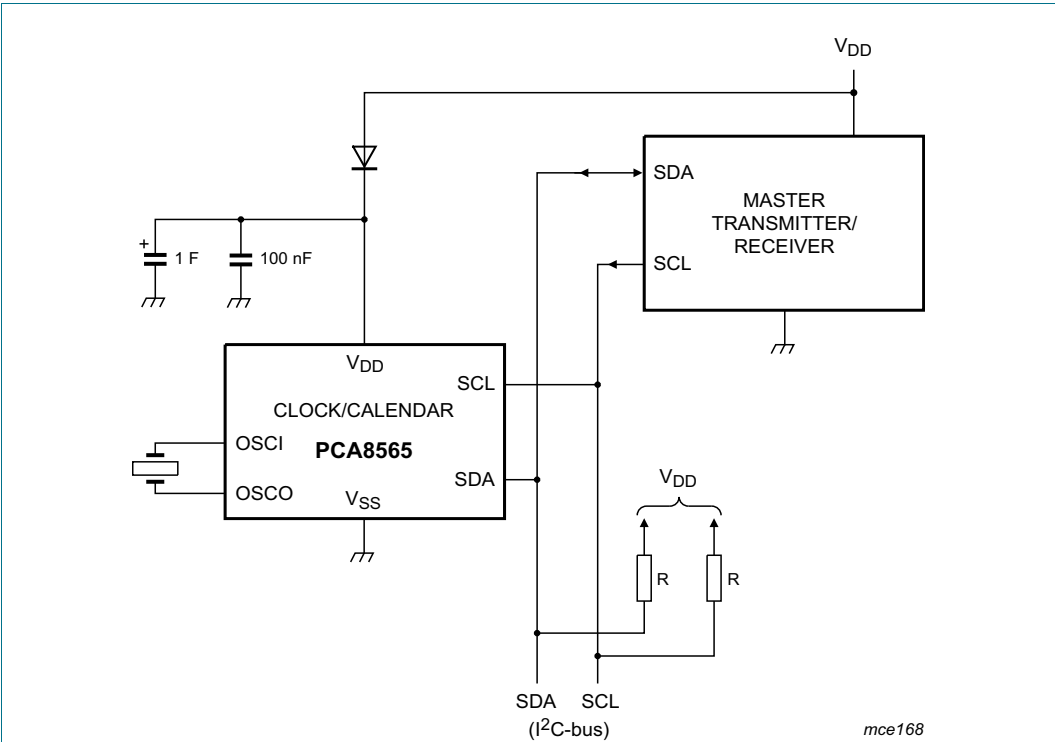


**Fig 27.** **Application diagram of PCA8565**

### 15.1 Quartz frequency adjustment

#### 15.1.1 Method 1: fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout, a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at pin CLKOUT. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\Delta f/f = \pm 5 \times 10^{-6}$). Average deviations of $\pm 5$ minutes per year can be easily achieved.

#### 15.1.2 Method 2: OSCI trimmer

Using the 32.768 kHz signal available after power-on at pin CLKOUT, fast setting of a trimmer is possible.

#### 15.1.3 Method 3: OSCO output

Direct measurement of OSCO out (allowing for test probe capacitance).

## 16. Test information

### 16.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

## 17. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm**

**SOT505-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D⁽¹⁾ | E⁽²⁾ | e | Hₑ | L | Lₚ | v | w | y | Z⁽¹⁾ | θ |
|------|--------|----|----|----|----|----|------|------|----|----|----|----|----|----|----|------|----|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.45 0.25 | 0.28 0.15 | 3.1 2.9 | 3.1 2.9 | 0.65 | 5.1 4.7 | 0.94 | 0.7 0.4 | 0.1 | 0.1 | 0.1 | 0.70 0.35 | 6° 0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~ 03-02-18 |
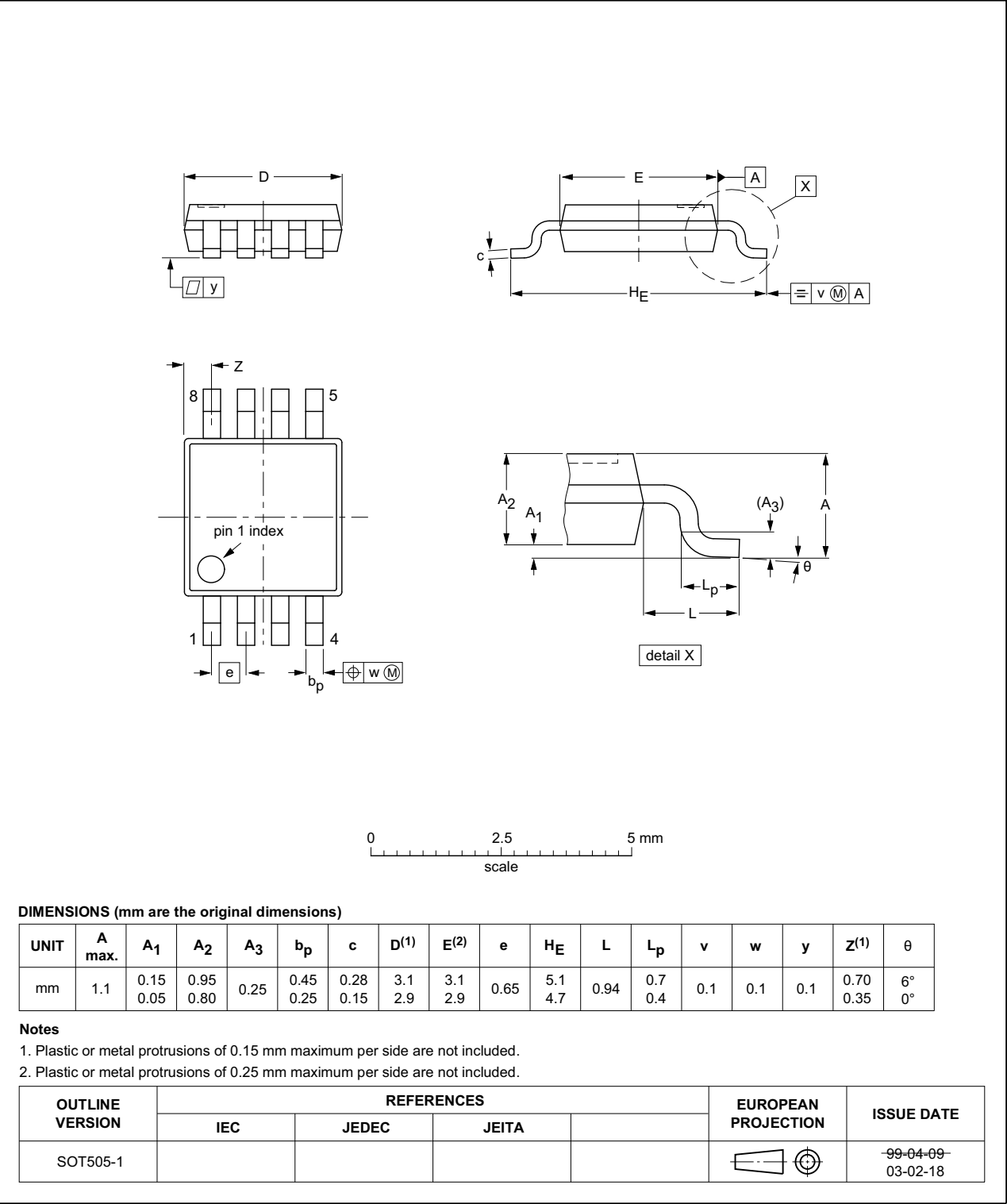
**Fig 28.   Package outline SOT505-1 (TSSOP8) of PCA8565TS**

# 18. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

# 19. Packing information

## 19.1 Tape and reel information

For tape and reel packing information, please see Ref. 10 "SOT505-1_118" and Ref. 11 "SOT505-1_518" on page 42

# 20. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 20.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 20.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 20.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 20.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 34 and 35

**Table 34. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
| --- | --- | --- |
| | Volume (mm$^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 35. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
| --- | --- | --- | --- |
| | Volume (mm$^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.

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MSL: Moisture Sensitivity Level

**Fig 29. Temperature profiles for large and small components**
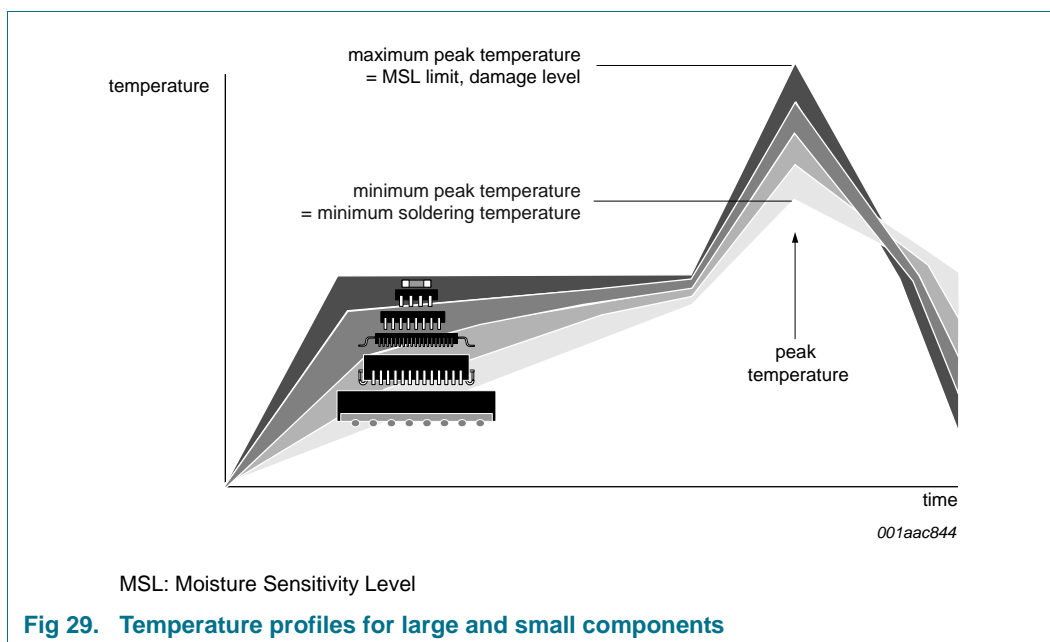
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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Real time clock/calendar

# 21. Appendix

## 21.1 Real-Time Clock selection

**Table 36. Selection of Real-Time Clocks**

| Type name | Alarm, Timer, Watchdog | Interrupt output | Interface | $I_{DD}$, typical (nA) | Battery backup | Timestamp, tamper input | AEC-Q100 compliant | Special features | Packages |
|---|---|---|---|---|---|---|---|---|---|
| PCF8563 | X | 1 | I²C | 250 | - | - | - | - | SO8, TSSOP8, HVSON10 |
| PCF8564A | X | 1 | I²C | 250 | - | - | - | integrated oscillator caps | WLCSP |
| PCA8565 | X | 1 | I²C | 600 | - | - | grade 1 | high robustness, $T_{amb}$= −40 °C to 125 °C | TSSOP8, HVSON10 |
| PCA8565A | X | 1 | I²C | 600 | - | - | - | integrated oscillator caps, $T_{amb}$= −40 °C to 125 °C | WLCSP |
| PCF85063 | - | 1 | I²C | 220 | - | - | - | basic functions only, no alarm | HXSON8 |
| PCF85063A | X | 1 | I²C | 220 | - | - | - | tiny package | SO8, DFN2626-10 |
| PCF85063B | X | 1 | SPI | 220 | - | - | - | tiny package | DFN2626-10 |
| PCF85263A | X | 2 | I²C | 230 | X | X | - | time stamp, battery backup, stopwatch $1/100$ s | SO8, TSSOP10, TSSOP8, DFN2626-10 |
| PCF85263B | X | 2 | SPI | 230 | X | X | - | time stamp, battery backup, stopwatch $1/100$ s | TSSOP10, DFN2626-10 |
| PCF85363A | X | 2 | I²C | 230 | X | X | - | time stamp, battery backup, stopwatch $1/100$ s, 64 Byte RAM | TSSOP10, DFN2626-10 |
| PCF85363B | X | 2 | SPI | 230 | X | X | - | time stamp, battery backup, stopwatch $1/100$ s, 64 Byte RAM | TSSOP10, DFN2626-10 |
| PCF8523 | X | 2 | I²C | 150 | X | - | - | lowest power 150 nA in operation, FM+ 1 MHz | SO8, HVSON8, TSSOP14, WLCSP |
| PCF2123 | X | 1 | SPI | 100 | - | - | - | lowest power 100 nA in operation | TSSOP14, HVQFN16 |
| PCF2127 | X | 1 | I²C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated, 512 Byte RAM | SO16 |

**Table 36.** **Selection of Real-Time Clocks** *…continued*

| Type name | Alarm, Timer, Watchdog | Interrupt output | Interface | $I_{DD}$, typical (nA) | Battery backup | Timestamp, tamper input | AEC-Q100 compliant | Special features | Packages |
|---|---|---|---|---|---|---|---|---|---|
| PCF2127A | X | 1 | I²C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated, 512 Byte RAM | SO20 |
| PCF2129 | X | 1 | I²C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated | SO16 |
| PCF2129A | X | 1 | I²C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated | SO20 |
| PCA2129 | X | 1 | I²C and SPI | 500 | X | X | grade 3 | temperature compensated, quartz built in, calibrated | SO16 |
| PCA21125 | X | 1 | SPI | 820 | - | - | grade 1 | high robustness, $T_{amb}$= −40 °C to 125 °C | TSSOP14 |

## 22. Abbreviations

**Table 37.    Abbreviations**

| Acronym | Description |
|---------|-------------|
| BCD | Binary Coded Decimal |
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| HBM | Human Body Model |
| I$^2$C | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| MSB | Most Significant Bit |
| MSL | Moisture Sensitivity Level |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| RC | Resistance and Capacitance |
| RTC | Real Time Clock |
| SMD | Surface Mount Device |

## 23. References

[1]   **AN10365 —** Surface mount reflow soldering description

[2]   **AN10853 —** ESD and EMC sensitivity of IC

[3]   **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4]   **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5]   **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[6]   **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7]   **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8]   **JESD78 —** IC Latch-Up Test

[9]   **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10]  **SOT505-1_118 —** TSSOP8; Reel pack; SMD, 13", packing information

[11]  **SOT505-1_518 —** TSSOP8; Reel dry pack; SMD, 13", packing information

[12]  **UM10204 —** I$^2$C-bus specification and user manual

[13]  **UM10301 —** User Manual for NXP Real Time Clocks PCF85x3, PCA8565 and PCF2123, PCA2125

[14]  **UM10569 —** Store and transport requirements

## 24. Revision history

**Table 38. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA8565 v.4 | 20141205 | Product data sheet | - | PCA8565 v.3 |
| Modifications: | • Corrected Figure 27 | | | |
| PCA8565 v.3 | 20140901 | Product data sheet | - | PCA8565 v.2 |
| PCA8565 v.2 | 20090616 | Product data sheet | - | PCA8565 v.1 |
| PCA8565 v.1 | 20030331 | Product data sheet | - | - |

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 27. Tables

## 28. Figures

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# 29. Contents