The ISL22102 integrates two digitally controlled potentiometers (DCP) with buffered wiper outputs and an internal bias voltage generator (VB) on a monolithic CMOS integrated circuit. The wiper position is adjusted by the user through simple Up and Down push buttons, ideal for stereo volume control in audio applications.

Each potentiometer is implemented using 31 polysilicon resistors in a logarithmic array. Between each of the resistors are tap points connected to the wiper terminal through switches. When powered up, the wipers are reset to the -20 dB position.

In addition to the ISL22102's low noise design, the ISL22102 also contains a zero-crossing detection circuitry to further minimize click and pop noise during volume transition.

The internal VB generator of the ISL22102 provides a precision middle scale voltage reference that reduces external circuitry and simplifies application design.

The ISL22102 implements two power saving techniques for power critical applications. It is a Standby Mode that can be enabled to reduce the power consumption of the part when DCP is not in use. The part also has Audio Detection circuitry that provides an indication FLAG to external devices and services. The FLAG can be delayed through D0, D1 and D2 pin configuration. By connecting the FLAG to the standby pin ( $\overline{\mathrm{SB}}$ ), it will automatically put the part into Standby Mode.

## Pinout



## Features

- Dual Audio Control - Two 32 Taps Log Pots
- Buffered Wiper Outputs
- Audio Detection with Threshold Input and Controlled Delay
- Zero Amplitude Wiper Switching (ZAWS)
- Simple Push-button Interface
- Auto Increment/decrement After 1s Button Press
- Standby Mode
- Mute Function
- Total Resistance: $18.5 \mathrm{k} \Omega$ each DCP (Typical)
- Voltage Operation
- $\mathrm{VCC}=2.7 \mathrm{~V}$ to 5.5 V
- $\mathrm{AVCC}=2.7 \mathrm{~V}$ to 5.5 V
- Temp Range $=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
- Package Options
- 20 Ld TSSOP
- 20 Ld QFN
- Pb-Free (RoHS Compliant)


## Audio Performance

- OdB to -72dB Volume Control
- -90dB Mute
- SNR: -90dB
- THD+N: 0.01\% @ 1kHz
- Crosstalk Rejection: -100dB @ 1kHz
- Channel-to-Channel Variation: $\pm 0.1 \mathrm{~dB}$
- Mid point 3dB-Cutoff: 100kHz


## Applications

- Set Top Boxes
- Stereo Amplifiers
- DVD Players
- Portable Audio Products


## Ordering Information

| PART NUMBER <br> (Note) | PART MARKING | TOTAL RESISTANCE <br> $(\mathbf{k} \Omega)$ | TEMP RANGE <br> $\left({ }^{\circ} \mathbf{C}\right)$ | PACKAGE <br> (Pb-Free) | PKG. <br> DWG.\# |
| :--- | :--- | :---: | :---: | :---: | :---: |
| ISL22102IV2OZ* (No longer <br> available or supported) | 22102 IVZ | 18.5 | -40 to +85 | 20 Ld TSSOP | M20.173 |
| ISL22102IR20Z* | 22102 IRZ | 18.5 | -40 to +85 | 20 Ld QFN | L20.4×4C |

## Block Diagram



## Pinouts



## Pin Description

| $\begin{gathered} \text { PIN } \\ \text { (QFN) } \end{gathered}$ | $\begin{gathered} \text { PIN } \\ \text { (TSSOP) } \end{gathered}$ | SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1 | 4 | DN | Active low volume decrement input with internal pull-up. |
| 2 | 5 | MUTE | Active low mute input with internal pull-up. |
| 3 | 6 | VCC | Digital Power Supply. |
| 4 | 7 | AVCC | Analog Power Supply. |
| 5 | 8 | LEFT_IN | Input terminal of the Left Channel Potentiometer. Referenced to VB. |
| 6 | 9 | LEFT_OUT | Left channel output. Referenced to VB. |
| 7 | 10 | CB | Terminal for external bypass capacitor to GND. |
| 8 | 11 | VB | AVCC/2 reference output. Can be used as a signal reference for other system components. |
| 9 | 12 | RIGHT_OUT | Right channel output. Referenced to VB. |
| 10 | 13 | RIGHT_IN | Input terminal of the Right Channel Potentiometer. Referenced to VB. |
| 11 | 14 | HPA | Terminal A of audio-detector high pass filter capacitor. |
| 12 | 15 | HPB | Terminal B of audio-detector high pass filter capacitor. |
| 13 | 16 | GND | System Ground. Overall for analog and digital power supply. |
| 14 | 17 | $\mathrm{V}_{\text {TH }}$ | Analog Input threshold for audio detection. Require an external resistor to VB. |
| 15 | 18 | D0 | Programming bit (LSB) input for delayed FLAG low output. |
| 16 | 19 | D1 | Programming bit input for delayed FLAG low output. |
| 17 | 20 | D2 | Programming bit (MSB) input for delayed FLAG low output. |
| 18 | 1 | FLAG | Output signal indicates audio input detection. |
| 19 | 2 | SB | Active low Standby Mode input with internal pull-up. |
| 20 | 3 | UP | Active low volume increment input with internal pull-up. |
| EPAD* |  |  | Exposed Die Pad internally connected to GND |

*Note: PCB thermal land for QFN/TDFN EPAD should be connected to GND plane or left floating. For more information refer to http://www.intersil.com/data/tb/TB389.pdf

| Absolute Maximum Ratings |  |
| :---: | :---: |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Voltage on $\overline{\mathrm{UP}}, \overline{\mathrm{DN}}, \overline{\mathrm{MUTE}}$ or $\overline{\mathrm{SB}}$ with Respect to GND | -0.3V to VCC + 0.3 |
| Voltage on AVCC (referenced to GND) | -0.3 V to +6 V |
| Voltage on VCC (referenced to GND) | -0.3V to +6 V |
| Any Audio Inputs (referenced to VB) | $\pm A V C C / 2 \pm 0.3$ |
| Any Outputs (referenced to GND) | -0.3V to AVCC + 0.3 |
| $\mathrm{l}_{\text {Out }} \mathrm{max}$ (10s). | .$\pm 30 \mathrm{~mA}$ |
| Latchup | II, Level A at $+85^{\circ} \mathrm{C}$ |
| ESD Rating |  |
| Human Body Model | 2.5 kV |
| Machine Model. | .250V |

Thermal Information
Thermal Resistance (Typical)

| 20 Lead TSSOP (Note 1) $\ldots \ldots \ldots .$. | 85 | N/A |
| :--- | :--- | :--- |
| 20 Lead QFN (Notes 2,3$) \ldots \ldots . .$. | 40 | 4 |

Maximum Junction Temperature (Plastic Package). . . . . . . . $+150^{\circ} \mathrm{C}$
Pb-free Reflow Profile . . . . . . . . . . . . . . . . . . . . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Temperature Range (Industrial) . . . . . . . . . . . . . . . . . . $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$
Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2.7 V to 5.5 V
Analog Supply Voltage ( $\mathrm{AV}_{\mathrm{CC}}$ ) . . . . . . . . . . . . . . . . . . . . . 2.7 V to 5.5 V
Power Rating of each DCP . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15mW

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

## NOTES:

1. $\theta_{\mathrm{JA}}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. $\theta_{\mathrm{JA}}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For $\theta_{\mathrm{Jc}}$, the "case temp" location is the center of the exposed metal pad on the package underside.

Analog Specifications Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 8) | TYP <br> (Note 4) | MAX <br> (Note 8) | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DYNAMIC PERFORMANCE (Notes 5, 6) |  |  |  |  |  |  |
|  | Volume Control Range |  | -72 |  | 0 | dB |
|  | Mute Mode | @1V ${ }_{\text {RMS }}$ |  | -90 |  | dB |
| SNR <br> (Note 7) | Signal Noise Ratios (Unweighted) | @1V $\mathrm{RMS}^{\text {@ }} 1 \mathrm{kHz}, \mathrm{AVCC}=5 \mathrm{~V}$ |  | -90 |  | dB |
| THD + N <br> (Note 7) | Total Harmonic Distortion + Noise | @1V RMs @ 1kHz, AVCC = 5V Tap position from 0 to 10 |  | 0.01 |  | \% |
| XTalk (Note 7) | DCP Isolation | @1kHz, @ tap 10 |  | -100 |  | dB |
| PSRR <br> (Note 7) | Power Supply Rejection | $A V C C=5 V$ |  | -90 |  | dB |
| (Note 7) | -3db Cutoff Frequency | Tap position from 0 to 25 |  | 100 |  | kHz |
| (Note 7) | Noise | 20 Hz to 20 kHz , VB Input |  | 3 |  | $\mu \mathrm{V}_{\text {RMS }}$ |
| DCP ACCURACY |  |  |  |  |  |  |
| $\mathrm{R}_{\text {TOTAL }}$ | End-to-end Resistance |  |  | 18.5 |  | $\mathrm{k} \Omega$ |
|  | End-to-end Resistance Tolerance |  | -20 |  | +20 | \% |
|  | DCP Input Resistance Matching |  | -2 |  | +2 | \% |
|  | Wiper Step Size | Tap position from 0 to 26 |  | -2 |  | dB |
|  |  | Tap position from 27 to 31 |  | -4 |  | dB |
|  | Wiper Step Size Error | Tap position from 0 to 26 |  | $\pm 0.1$ | $\pm 0.5$ | dB |
|  |  | Tap position from 27 to 29 |  |  | $\pm 1$ | dB |
|  |  | Tap position from 30 to 31 |  |  | $\pm 2$ | dB |
|  | DCP-to-DCP Matching | Tap position from 0 to 26 |  |  | $\pm 0.5$ | dB |
|  |  | Tap position from 27 to 29 |  |  | $\pm 1$ | dB |
|  |  | Tap position from 30 to 31 |  |  | $\pm 2$ | dB |
|  | Power-up Attenuation (Default Wiper Position at Tap 10) |  |  | -20 |  | dB |
| TCV (Note 7) | Ratiometric Temperature Coefficient | Tap position 15 |  | $\pm 10$ |  | ppm/ ${ }^{\circ} \mathrm{C}$ |

Analog Specifications Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN <br> (Note 8) | TYP <br> (Note 4) | MAX <br> (Note 8) | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

DC ELECTRICAL SPECIFICATION

| AVCC | Analog Power Supply |  | 2.7 |  | 5.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VCC | Digital Power Supply |  | 2.7 |  | 5.5 | V |
| $t_{R}$ | AVCC and VCC Ramp Rate |  | 0.2 |  | 50 | V/ms |
| $\mathrm{I}_{\text {AVCC }}$ | Analog Supply Current | $\mathrm{AVCC}=5.5 \mathrm{~V}, \mathrm{I}_{\mathrm{BIAS}}=0 \mathrm{~mA}, \mathrm{I}_{\mathrm{OUT}}=0 \mathrm{~mA}$ for both channels |  |  | 750 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {ASB }}$ | Analog Standby Current | $\mathrm{AVCC}=5.5 \mathrm{~V}, \mathrm{I}_{\mathrm{BIAS}}=0 \mathrm{~mA}$ |  |  | 360 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{V}_{\text {CC }}$ Supply Current | All Inputs $=5.5 \mathrm{~V}, \mathrm{VCC}=5.5 \mathrm{~V}, \mathrm{AVCC}=5.5 \mathrm{~V}$ |  |  | 60 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {SB }}$ | $\mathrm{V}_{\text {CC }}$ Current (Standby) | $\mathrm{VCC}=5.5 \mathrm{~V}$ |  |  | 35 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IN }}$ | Input Signal on LEFT_IN, RIGHT_IN Pins | Reference to VB pin | -AVCC/2 |  | AVCC/2 | V |
| $\mathrm{V}_{\text {OUT }}$ | Output Signal on LEFT_OUT, RIGHT_OUT Pins | Reference to GND | 0 |  | AVCC | V |
| lout (Note 5) | LEFT_OUT, RIGHT_OUT Buffer Current | $V C C=5.5 \mathrm{~V}$ | -15 |  | 15 | mA |
| $\mathrm{R}_{\text {OUT }}$ | Buffer Output Impedance |  |  |  | 25 | $\Omega$ |
| $\mathrm{C}_{\text {IN }}$ (Note 7) | Input Capacitance LEFT_IN, RIGHT_IN |  |  | 10 |  | pF |
| VB | Bias Output Voltage |  |  | AVCC/2 |  | V |
|  | VB Accuracy |  | -50 |  | 50 | mV |
| $\mathrm{I}_{\text {BIAS }}$ | VB Output Current | $\mathrm{VCC}=5.5 \mathrm{~V}$ | -5 |  | 5 | mA |
|  | VB Output Impedance |  |  |  | 20 | $\Omega$ |

Digital Specifications Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN <br> (Note 8) | TYP <br> (Note 4) | MAX <br> (Note 8) | UNITS |
| :---: | :--- | :--- | :---: | :---: | :---: | :---: |

AC Timing Over recommended operating conditions

| SYMBOL | PARAMETER | MIN (Note 8) | TYP <br> (Note 4) | MAX <br> (Note 8) | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {PU }}$ (Note 7) | Power-up Time to Wiper Stable |  | 10 |  | ms |
| $t_{\text {WRPO }}$ (Note 7) | Wiper Response Time (include $\mathrm{t}_{\text {DB }}$ and $\mathrm{t}_{\text {ZAWS }}$ ) |  | 35 |  | ms |
|  | Auto Increment Starts after $\overline{\mathrm{UP}}$ or $\overline{\mathrm{DN}}$ Input is Keeping Low |  | 1 |  | S |
|  | Auto Increment Rate for the First 4s |  | 4 |  | Hz |
|  | Auto Increment Rate After 4s |  | 8 |  | Hz |
| $t_{\text {DB }}$ | Debounce Time |  |  | 50 | ms |
| $\begin{aligned} & t_{\text {LOCK }} \\ & \text { (Note 7) } \end{aligned}$ | Lockout Time after Debounce Time, when any New Command will be Ignored |  | 40 |  | ms |
| $t_{\text {FLAG_HIGH }}$ (Note 7) | FLAG Delay Time from when Audio Input is Detected to FLAG Asserted HIGH |  | 1 |  | $\mu \mathrm{s}$ |

AC Timing Over recommended operating conditions (Continued)

| SYMBOL | PARAMETER | MIN (Note 8) | TYP (Note 4) | MAX <br> (Note 8) | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {FLAG_LOW }}$ | FLAG Delay Time Interval Step Size, from D2:D0 = 001b to 111b. FLAG is Asserted LOW when Audio Input is Below Threshold. (See Table 1, page 7) |  | 30 |  | S |
| tzaws (Note 7) | Zero Amplitude Detection Time for Wiper Switching |  | 32 |  | ms |
| t LOW | Active LOW $\overline{\text { PU, }} \overline{\mathrm{DN}}$ or $\overline{\text { MUTE }}$ Pulse | 20 |  |  | ms |
| $\mathrm{t}_{\text {GAP }}$ | Time Between Two Separate Push-Button Events | 80 |  |  | ms |

NOTES:
4. Typical values are for $\mathrm{AVCC}=\mathrm{VCC}=2.7 \mathrm{~V}$ to $5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
5. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{AVCC}=5.0 \mathrm{~V} ; 2 \mathrm{~Hz}$ to 20 kHz Measurement Bandwidth, input signal $1 \mathrm{~V}_{\mathrm{RMS}}, 1 \mathrm{kHz}$ Sine Wave.
6. When pin is open, voltage is pulled up through current source to VCC.
7. Limits should be considered typical and are not production tested.
8. Parameters with MIN and/or MAX limits are $100 \%$ tested at $+25^{\circ} \mathrm{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Timing Diagrams



FIGURE 1. DIGITAL INPUT TIMING


FIGURE 2. AUTO INCREMENT TIMING
NOTE:
9. MI in these timing diagrams refers to the minimum incremental change of the output (wiper) voltage.

## Pin Descriptions

## LEFT_IN, RIGHT_IN

The LEFT_IN and RIGHT_IN pins of the ISL22102 are equivalent to the fixed terminals of a mechanical potentiometer. The stereo audio signal applied to these pins are referenced to VB and may have $\pm \mathrm{AVCC} / 2$ maximum amplitude.

## LEFT_OUT, RIGHT_OUT

The LEFT_OUT and RIGHT_OUT pins are the buffered wiper terminals of the potentiometers which are equivalent to the movable terminals of a mechanical potentiometers with attached unity gain operational amplifiers (Op Amp). The default output position of wiper terminals preset to -20 dB attenuation of input signals.

## VB

This is reference voltage output equal AVCC/2. It is used as common point for audio inputs, as well as reference signal for other system components.

## $\overline{U P}$

The debounced active low $\overline{U P}$ input is increment the wipers position of both channels. An on-chip $2 \mu \mathrm{~A}$ current source pullup holds the UP input High. A switch closure to ground or a Low logic level will after a debounce time and Zero Amplitude Crossing Detection, move the wiper to the next adjacent higher tap position. If the $\overline{U P}$ input signal is held down for 1 s , the wipers will auto increment their position with a 4 Hz frequency rate for 4 s , and then a 8 Hz frequency rate (see Figure 2). When the wipers reach their top position of 0 dB attenuation, they will stay at this position ignoring any further Up commands.

## $\overline{D N}$

The debounced $\overline{\mathrm{DN}}$ input is decrement the wipers position of both channels. An on-chip $2 \mu \mathrm{~A}$ current source pull-up holds the $\overline{\mathrm{DN}}$ input High. A switch closure to ground or a Low logic level will, after a debounce time and Zero Amplitude Crossing Detection, move the wiper to the next adjacent lower tap position. If $\overline{\mathrm{DN}}$ input signal is held down for 1 s , the wipers will auto decrement their position with a 4 Hz frequency rate for 4 s , and then a 8 Hz frequency rate. When the wipers reach their bottom position of -90 dB attenuation, they will stay at this position ignoring any further Down or Mute commands.

## MUTE

The first active low MUTE input pulse allows both wipers to move, after a debounce time and Zero Amplitude Crossing Detection, to the highest attenuation level of -90 dB in one step. The second active low $\overline{\text { MUTE }}$ pulse will return both wipers to their original position, prior to MUTE command. An on-chip $2 \mu \mathrm{~A}$ current source pull-up holds the MUTE input High.

## $\overline{S B}$

The active low $\overline{\mathrm{SB}}$ input allows totally disconnect DCP arrays from their LEFT_IN and RIGHT_IN pins, and move both wipers to position closest to VB pin (as shown in Figure 3). It also sets ISL22102 in low power Standby mode. When $\overline{\mathrm{SB}}$ will be released, the both wipers will be set at position they have prior Standby.


FIGURE 3. DCP CONNECTION IN STANDBY MODE

## FLAG

This output pin provides status information to the rest of the system about audio activity. It is High when at least one audio input exceeds $\mathrm{V}_{\mathrm{TH}}$ threshold, otherwise its output level is Low. The FLAG output can be directly connected to $\overline{\mathrm{SB}}$ pin for automatical setting the ISL22102 in Standby mode.

D0-D2
These three digital input pins allow to program a delay time for FLAG Low output up to 240s. Table 1 lists the D0-D2 settings and corresponding delay times (typical values).
table 1. FLAG PROGRAMMED DELAY SETTINGS

| D2 | D1 | D0 | DELAY, (s) |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 60 |
| 0 | 1 | 0 | 90 |
| 0 | 1 | 1 | 120 |
| 1 | 0 | 0 | 150 |
| 1 | 0 | 1 | 180 |
| 1 | 1 | 0 | 210 |
| 1 | 1 | 1 | 240 |

## CB

This low pass filter terminal requires an external capacitor to GND. The value of this capacitor, together with $5 \mathrm{M} \Omega$ internal resistor divider, directly determines the PSRR (Power Supply Rejection Ratio) of audio and VB outputs. A $1 \mu \mathrm{~F}$ to $10 \mu \mathrm{~F}$ capacitor is recommended.

## HPA, HPB

These two high pass filter terminals require an external capacitor of 100 nF or higher in-between.

## $V_{T H}$

This terminal allows to set up the threshold level of audio input to be detected. When audio input to either Left or Right channel is below this threshold - the FLAG output is Low; when audio input is above this threshold - the FLAG output is High. The threshold level is maintained over an external resistor $\mathrm{R}_{\mathrm{TH}}$ placed between $V_{T H}$ pin, which is a source of $\pm 10 \mu \mathrm{~A}$ current, and VB pin. To calculate the actual threshold we need to multiply $10 \mu \mathrm{~A}$ by a resistor value and divide the result by 1000 . For example, a $100 \mathrm{k} \Omega$ resistor is a subject of 1 mV audio detection threshold, e.g. $10 \mu \mathrm{~A}^{*} 100 \mathrm{k} / 1000=1 \mathrm{mV}$. Note, the $\mathrm{V}_{\mathrm{TH}}$ threshold multiplied by 1000 should not exceed $1 / 2$ of AVCC. The maximum resistor value for detection threshold can be found in Table 2.

TABLE 2. $\mathrm{R}_{\mathrm{TH}}$ vs AVCC

| AVCC (V) | MAX $\mathbf{R H}_{\mathbf{T H}}(\mathbf{k} \Omega)$ |
| :---: | :---: |
| 5.5 | 188 |
| 5.25 | 177 |
| 5.0 | 167 |
| 4.75 | 156 |
| 4.5 | 146 |
| 4.25 | 135 |
| 4.0 | 125 |
| 3.75 | 115 |
| 3.5 | 104 |
| 3.25 | 94 |
| 3.0 | 83 |
| 2.75 | 73 |

## Device Operation

There are four sections in the ISL22102: the input control, counter and decode section, two resistor arrays with buffered wiper outputs, reference voltage generator of VB output, and audio detection block with programmable delay FLAG output. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch, connecting a point on the resistor array to the wiper output. Each resistor array is comprised of 31 individual resistors connected in series and its wiper output pass an attenuated audio input to the power amplifier. Both resistor arrays have logarithmic taper with -72dB dynamic range as shown in Table 2.

The ISL22102 is designed to interface directly to two push-button switches for effectively moving the wipers up or down. The $\overline{U P}$ and $\overline{D N}$ inputs increment or decrement 5-bit counters respectively. The output of these counters are decoded to select one of the thirty-two wiper positions along the resistive array. The wiper increment input, $\overline{U P}$, and the wiper decrement input, $\overline{\mathrm{DN}}$, are both connected to an internal
pull-up so that they normally remain High. When pulled Low by an external push button switch or a logic Low level input, the wipers will be switched to the next adjacent tap position.

Internal debounce circuitry prevents inadvertent switching of the wipers position if $\overline{\mathrm{UP}}$ or $\overline{\mathrm{DN}}$ remain Low for less than 15 ms , typical. Each of the buttons can be pushed either once for a single increment/decrement or continuously for a multiple increments/decrements. When making a continuous push, after the first second, the device is going to auto increment/decrement mode. If the button is held for longer than 1s, the wiper position will be auto incremented/decremented with a rate of 4 Hz for 4 s , and with a rate of 8 Hz after that. As soon as the button is released, the ISL22102 will return to a low power standby condition.

Each wiper acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

Table 3 contains information about attenuation level for each tap position.

TABLE 3. WIPER TAP POSITION vs ATTENUATION

| TAP POSITION | ATtENUATION |
| :---: | :---: |
| 0 | 0 |
| 1 | -2dB |
| 2 | -4dB |
| 3 | -6dB |
| 4 | -8dB |
| 5 | -10dB |
| 6 | -12dB |
| 7 | -14dB |
| 8 | -16dB |
| 9 | -18dB |
| 10 | -20dB |
| 11 | -22dB |
| 12 | -24dB |
| 13 | -26dB |
| 14 | -28dB |
| 15 | -30dB |
| 16 | -32dB |
| 17 | -34dB |
| 18 | -36dB |
| 19 | -38dB |
| 20 | -40dB |
| 21 | -42dB |
| 22 | -44dB |
| 23 | -46dB |
| 24 | -48dB |
| 25 | -50dB |

TABLE 3. WIPER TAP POSITION vs ATTENUATION (Continued)

| TAP POSITION | ATTENUATION |
| :---: | :---: |
| 26 | -52 dB |
| 27 | -56 dB |
| 28 | -60 dB |
| 29 | -64 dB |
| 30 | -68 dB |
| 31 | -72 dB |
| 32 | MUTE (-90dB) |

Once an $\overline{\mathrm{UP}}, \overline{\mathrm{DN}}$ or $\overline{\text { MUTE }}$ button has been validly pushed, the left and right inputs are examined for Zero Amplitude

Crossing. When either audio input exhibits a zero crossing prior to 32 ms , that command is immediately applied to appropriate wiper. If the zero crossing does not occur before the end of 32 ms , the command is executed at the end of 32 ms period. Zero crossing determines for each channel independently.
There is a 40 ms lockout time after any of the $\overline{\mathrm{UP}}, \overline{\mathrm{DN}}$ or $\overline{\text { MUTE }}$ button has been validly pushed, when any new command is ignored. If two or more buttons are pressed simultaneously, all commands are ignored upon release of ALL buttons.

## Typical Application Diagram


*FLAG LOW OUTPUT DELAY IS 240s

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION |  |
| :---: | :---: | :--- |
| September 21, 2015 | FN6788.2 | - Updated Ordering Information Table on page 2. <br> - Added Revision History. <br> - Added About Intersil Verbiage. |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets. For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

## L20.4x4C

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE Rev 0, 11/06


## NOTES:

1. Dimensions are in millimeters.

Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal $\pm 0.05$
4. Dimension $b$ applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin \#1 identifier is optional, but must be located within the zone indicated. The pin \#1 indentifier may be either a mold or mark feature.

## Thin Shrink Small Outline Plastic Packages (TSSOP)



## NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15 mm ( 0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. " $L$ " is the length of terminal for soldering to a substrate.
7. " N " is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm ( 0.003 inch ) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm ( 0.0027 inch ).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M20.173
20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | - | 0.047 | - | 1.20 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.031 | 0.051 | 0.80 | 1.05 | - |
| b | 0.0075 | 0.0118 | 0.19 | 0.30 | 9 |
| c | 0.0035 | 0.0079 | 0.09 | 0.20 | - |
| D | 0.252 | 0.260 | 6.40 | 6.60 | 3 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 | 4 |
| e | 0.026 | BSC | 0.65 | BSC | - |
| E | 0.246 | 0.256 | 6.25 | 6.50 | - |
| L | 0.0177 | 0.0295 | 0.45 | 0.75 | 6 |
| N | 20 |  | 20 |  | 7 |
| $\alpha$ | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ | - |

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