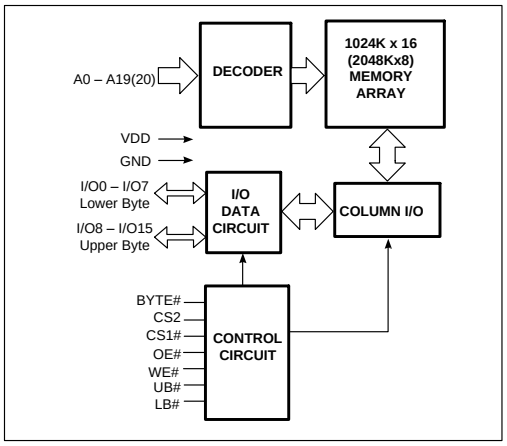
FEBURARY 2020

1024Kx16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - – Operating Current: 35mA (max.)
  - – CMOS standby Current: 5.5uA (typ.)
- TTL compatible interface levels
- Single power supply
  - –1.65V-2.2V VDD (IS62/65WV102416GALL)
  - – 2.2V-3.6V VDD (IS62/65WV102416GBLL)
- Three state outputs
- Commercial, Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL Block Diagram



DESCRIPTION

The *ISSI* IS62/65WV102416GALL/BLL are high-speed, low power, 16M bit static RAMs organized as 1024K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology.

This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices. When CS1# is HIGH (deselected) or when CS2 is LOW (deselected) or when CS1# is LOW, CS2 is HIGH and both LB# and UB# are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The device supports 16 I/Os when BYTE# is High, and 8 I/Os when BYTE# is Low. In x8 mode, UB#, LB#, and I/O8~I/O14 are not used, and I/O15 becomes A20.

The IS62/65WV102416GALL/BLL are packaged in the JEDEC standard 48-Pin TSOP (TYPE I)

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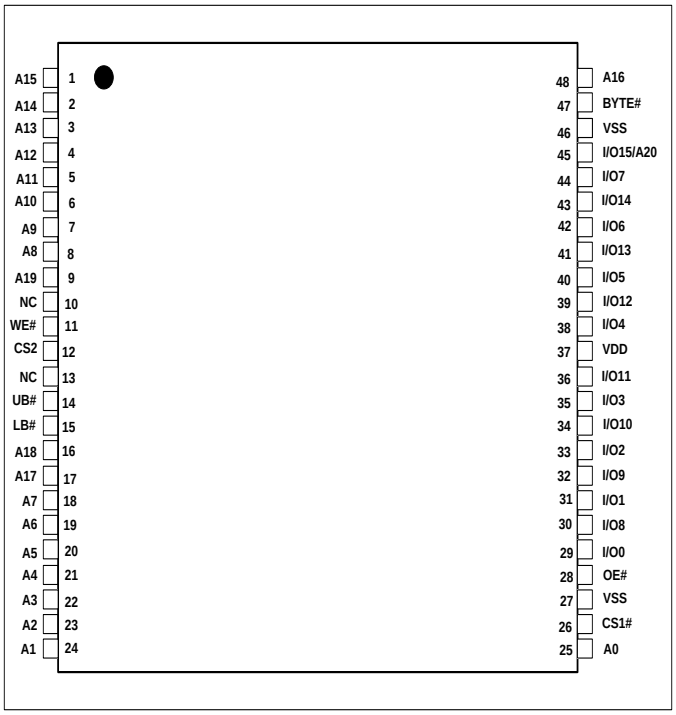
PIN CONFIGURATIONS

48-Pin TSOP (TYPE I)



PIN DESCRIPTIONS

A0-A19	Address Inputs
I/O0-I/O14	Data Inputs/Outputs
I/O15/A20	I/O15, when used in a x16 mode, A20 when used in a x8 mode.
CS1#, CS2	Chip Enable Inputs
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
BYTE#	Must be tied to V_{DD} to use as x16 or VSS to use as x8. UB#,LB#, I/O 8~I/O14 are not used and I/O 15 become A20 in x8 mode.
NC	No Connection
V_{DD}	Power
VSS	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different operating modes supported. Each function is described below with Truth Table. The device supports x16 mode and x8 mode, based on BYTE# condition. Following descriptions are based on x16 mode.

STANDBY MODE
Device enters standby mode when deselected (CS1# HIGH or CS2 LOW or both UB# and LB# are HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1 or ISB2. CMOS input in this mode will maximize saving power.

WRITE MODE
Write operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE
Read operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE(1)

Mode	CS1#	CS2	WE#	OE#	LB#	UB#	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	X	X	X	X	X	High-Z	High-Z	ISB2
	X	L	X	X	X	X	High-Z	High-Z	
	X	X	X	X	H	H	High-Z	High-Z	
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	ICC,ICC1
	L	H	H	H	X	L	High-Z	High-Z	
Read	L	H	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	H	L	H	L	High-Z	DOUT	
	L	H	H	L	L	L	DOUT	DOUT	
Write	L	H	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	H	L	X	H	L	High-Z	DIN	
	L	H	L	X	L	L	DIN	DIN	

Note:
1. The truth table is based on x16 mode, and UB#, LB#, and IO8~I/O15 are not used in x8 mode when BYTE# is Low. Also I/O 15 becomes A20 in x8 mode.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to GND	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

2. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	SPEED (MAX)	VDD(MIN)	VDD(TYP)	VDD(MAX)
Commercial	0°C to +70°C	~ALL	55 ns	1.65V	1.8V	2.2V
Industrial	-40°C to +85°C		55 ns	1.65V	1.8V	2.2V
Automotive	-40°C to +125°C		55 ns	1.65V	1.8V	2.2V
Commercial	0°C to +70°C	~BLL	45ns	2.2V	3.0V	3.6V
Industrial	-40°C to +85°C		45ns	2.2V	3.0V	3.6V
Automotive	-40°C to +125°C		55ns	2.2V	3.0V	3.6V

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)	Unit (2.2V~3.6V)
Input Pulse Level	0V to V_{DD}	0V to V_{DD}
Input Rise and Fall Time	1V/ns	1V/ns
Output Timing Reference Level	0.9V	½ V_{DD}
R1	13500	1005
R2	10800	820
V_{TM}	1.8V	V_{DD}
Output Load Conditions	Refer to Figure 1 and 2	

OUTPUT LOAD CONDITIONS FIGURES

FIGURE 1

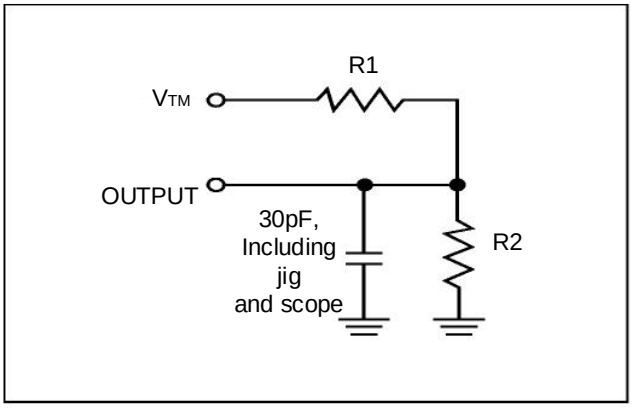
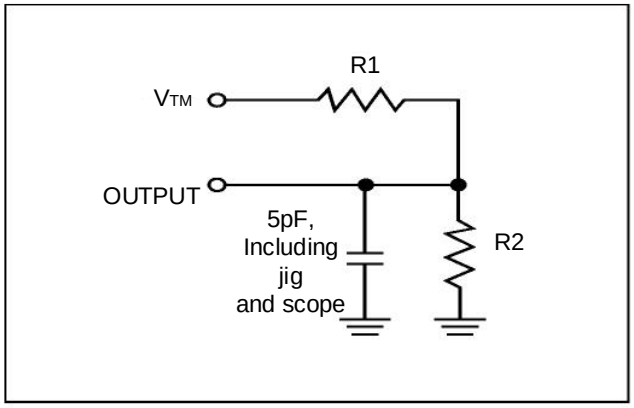


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

IS62(5)WV102416GALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE) VDD = 1.65V ~ 2.2V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV102416GBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE) VDD = 2.2V ~ 3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	—	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	—	0.4	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage	2.2 ≤ V_{DD} < 2.7	1.8	V_{DD} + 0.3	V
		2.7 ≤ V_{DD} ≤ 3.6	2.0	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage	2.2 ≤ V_{DD} < 2.7	–0.3	0.6	V
		2.7 ≤ V_{DD} ≤ 3.6	–0.3	0.8	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV102416GALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade		Typ(1)	Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD}(max)$, I_{OUT} = 0mA, f = f_{max},	Com.		-	35	mA
			Ind.		-	35	
			Auto. A3		-	35	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD} = V_{DD}(max)$, I_{OUT} = 0mA, f = 0	Com.		-	5	mA
			Ind.		-	5	
			Auto. A3		-	5	
ISB2	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD}(max)$, f = 0, CS1# ≥ V_{DD} - 0.2V or CS2 < 0.2V or (LB# and UB#) ≥ V_{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	25°C	5.5	9(2)	µA
				40°C	6.0	10(2)	
				70°C	7.5	14	
			Ind.	85°C	10.5	20	
			Auto. A3	125°C	25	55	

Notes:
1. Typical value indicates the value for the center of distribution at VDD=VDD (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested

IS62(5)WV102416GBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade		Typ(1)	Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD}(max)$, I_{OUT} = 0mA, f = f_{max},	Com.		-	35	mA
			Ind.		-	35	
			Auto. A3		-	35	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD} = V_{DD}(max)$, I_{OUT} = 0mA, f = 0	Com.		-	5	mA
			Ind.		-	5	
			Auto. A3		-	5	
ISB2	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD}(max)$, f = 0, CS1# ≥ V_{DD} - 0.2V or CS2 < 0.2V or (LB# and UB#) ≥ V_{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	25°C	5.5	9(2)	µA
				40°C	6.0	10(2)	
				70°C	7.5	14	
			Ind.	85°C	10.5	20	
			Auto. A3	125°C	25	55	

Notes:
1. Typical value indicates the value for the center of distribution at VDD=VDD (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested

AC CHARACTERISTICS[6] (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address Access Time	tAA	-	45	-	55	ns	1
Output Hold Time	tOHA	10	-	10	-	ns	1
CS1#, CS2 Access Time	tACS1/ACS2	-	45	-	55	ns	1
UB#, LB# Access Time	tBA	-	45	-	55	ns	1
OE# Access Time	tDOE	-	20	-	25	ns	1
OE# to High-Z Output	tHZOE	-	15	-	20	ns	2
OE# to Low-Z Output	tLZOE	5	-	5	-	ns	2
CS1#, CS2 to High-Z Output	tHZCS	-	15	-	20	ns	2
CS1#, CS2 to Low-Z Output	tLZCS	10	-	10	-	ns	2
UB#, LB# to High-Z Output	tHZB	-	15	-	20	ns	2
UB#, LB# to Low-Z Output	tLZB	10	-	10	-	ns	2

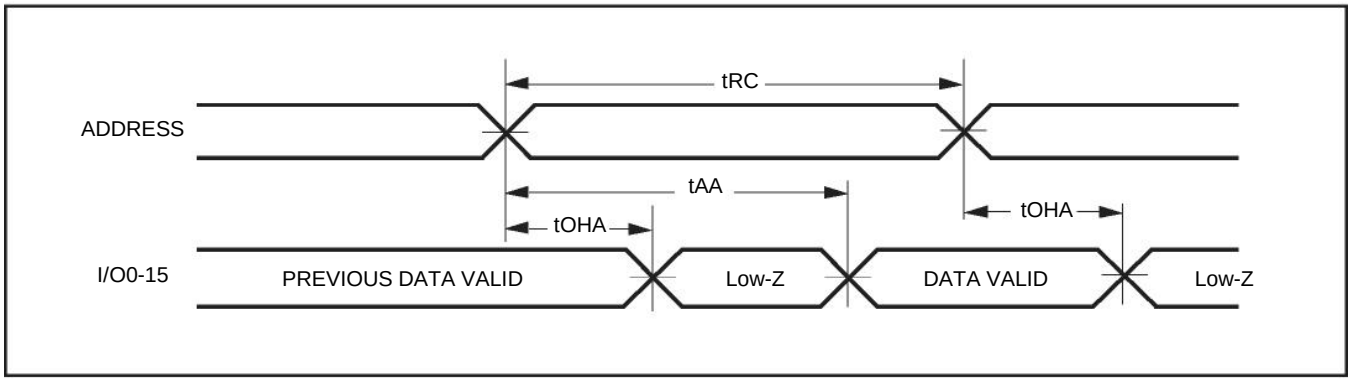
WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Min		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
CS1#, CS2 to Write End	tSCS1/SCS2	35	-	40	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	40	-	ns	1,3
UB#,LB# to Write End	tPWB	35	-	40	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
WE# Pulse Width	tPWE	35	-	40	-	ns	1,3,4
Data Setup to Write End	tSD	20	-	25	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
WE# LOW to High-Z Output	tHZWE	-	15	-	20	ns	2,3
WE# HIGH to Low-Z Output	tLZWE	5	-	5	-	ns	2,3

Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS1# = LOW, CS2=HIGH, UB# or LB# = LOW, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

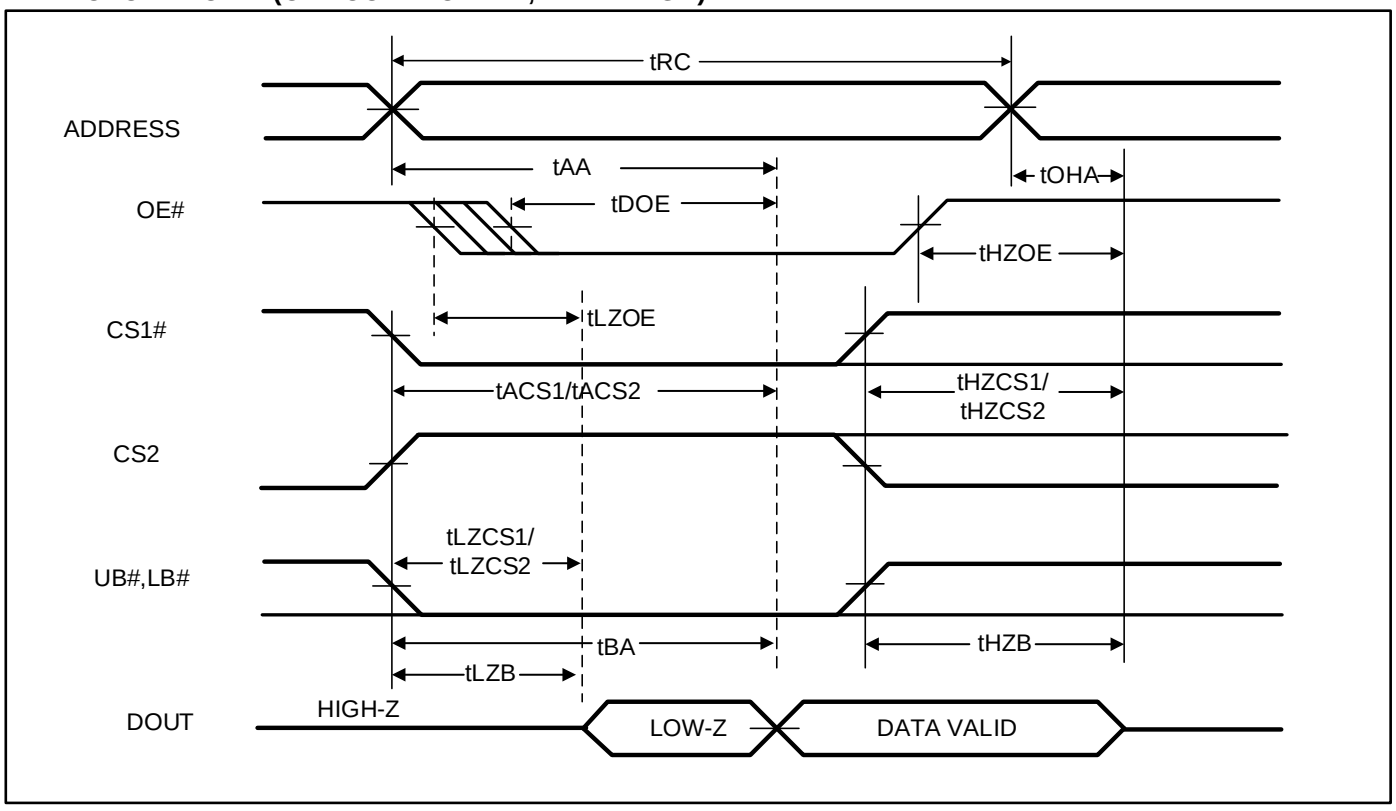
Timing Diagram

READ CYCLE NO. 1[1] (ADDRESS CONTROLLED, CS1# = OE# = UB# = LB# = LOW, CS2 = WE# = HIGH)



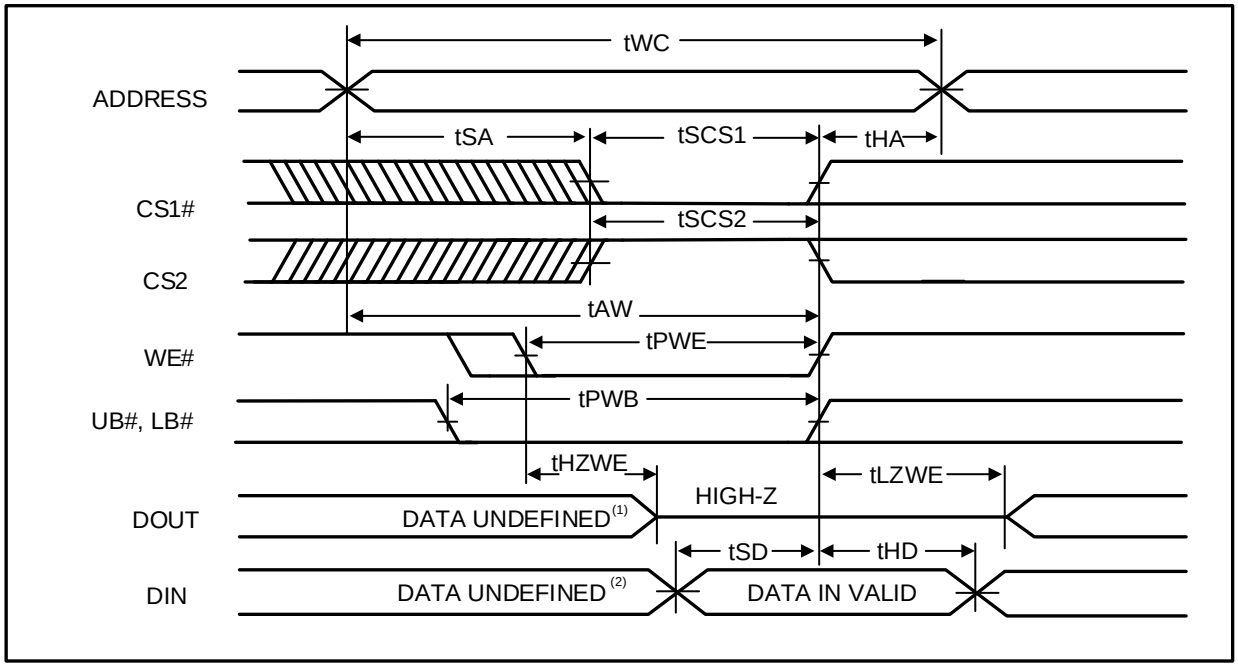
Notes:
1. The device is continuously selected.

READ CYCLE NO.2[1] (OE# CONTROLLED, WE# = HIGH)



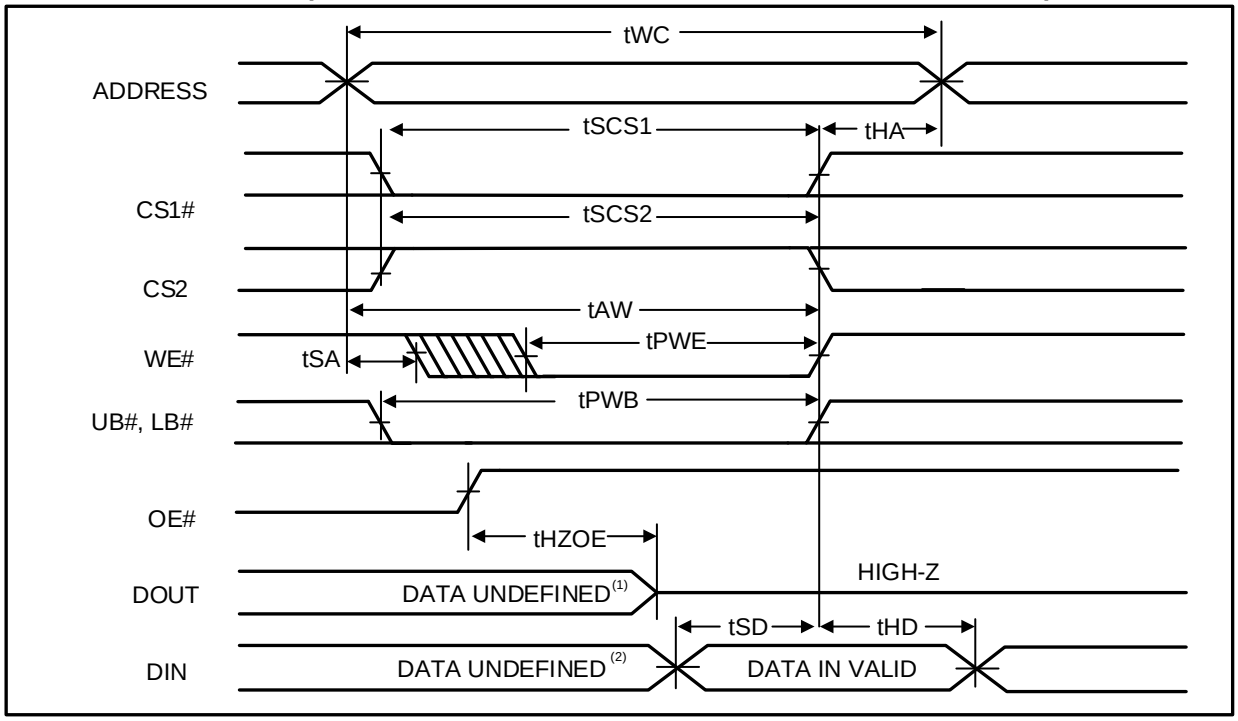
Notes:
1. Address is valid prior to or coincident with CS1# LOW or CS2 HIGH transition.

WRITE CYCLE NO.1[1,2] (CS1#, CS2 CONTROLLED, OE# = HIGH OR LOW)



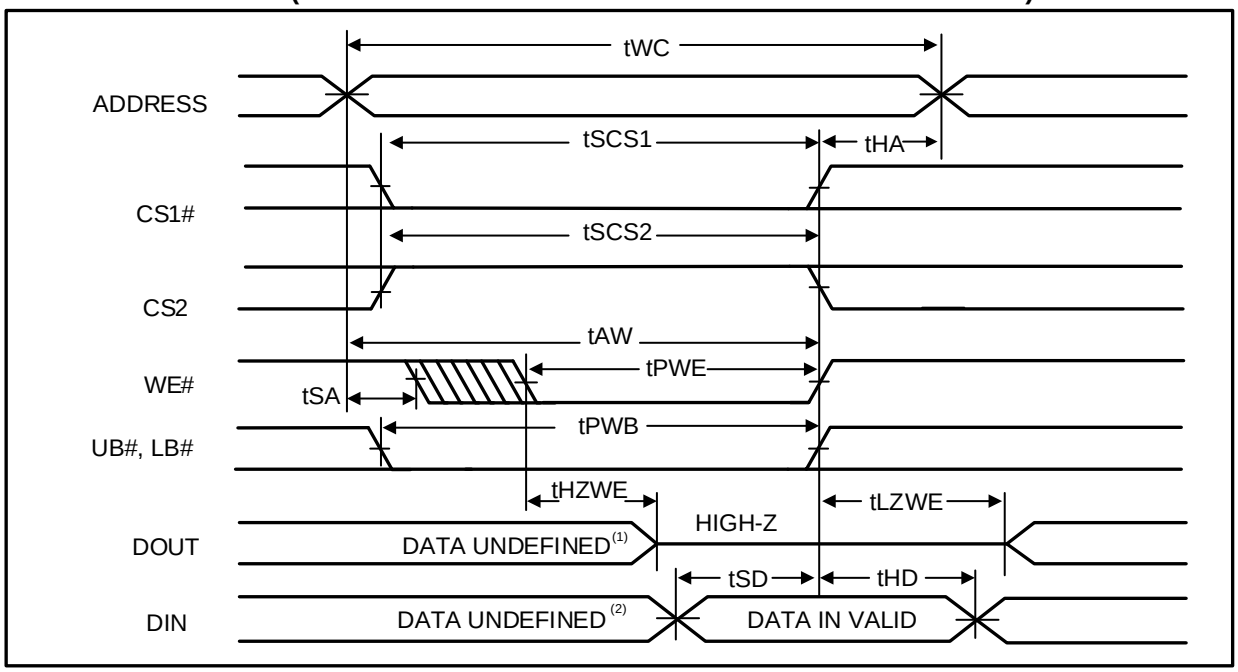
Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2[1,2] (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



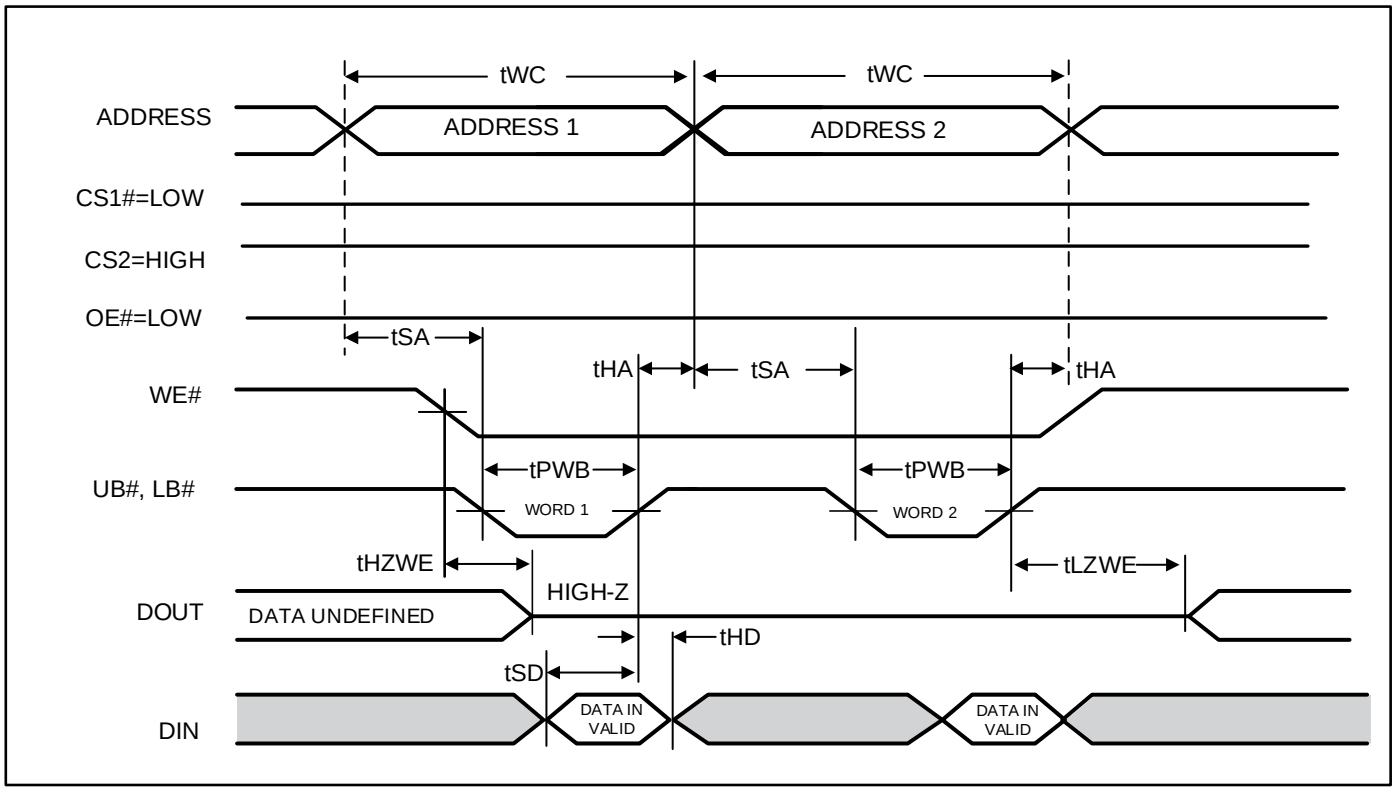
Notes:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3[1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Notes:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4[1, 2, 3] (UB# & LB# Controlled, OE# = LOW)



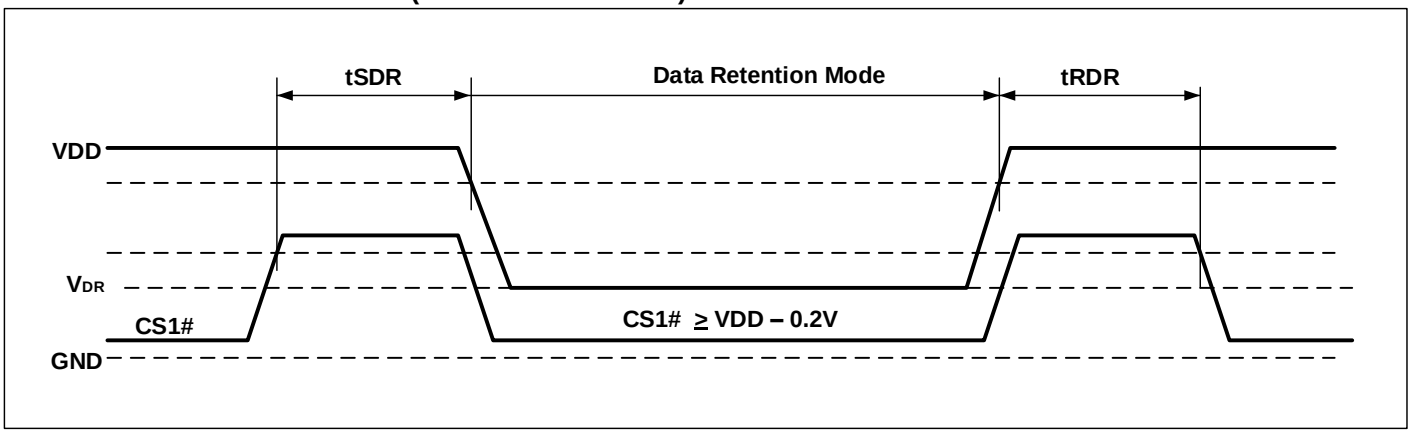
Notes:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, OE# is recommended to be HIGH during write period.
3. WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

DATA RETENTION CHARACTERISTICS

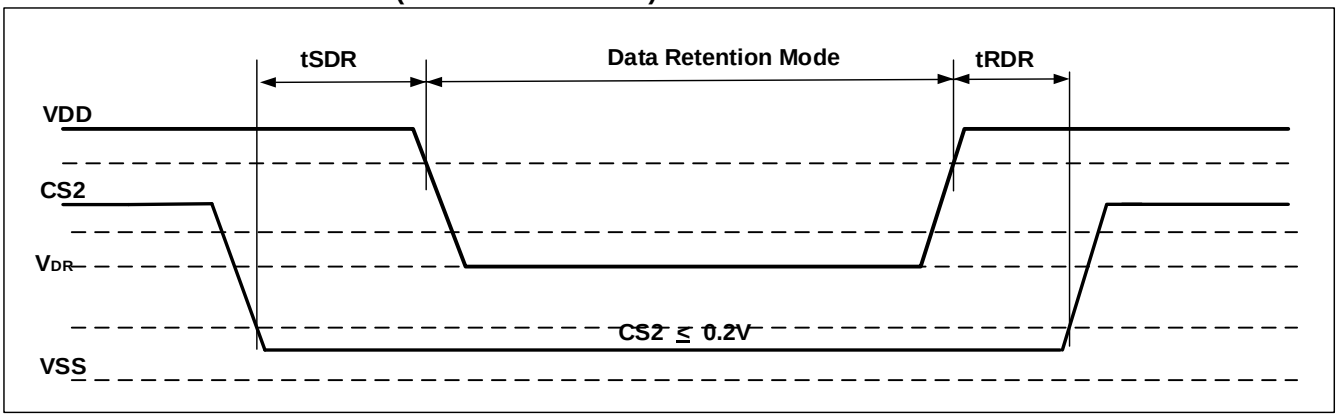
Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.5	-	-	V
I_{DR}	Data Retention Current	$V_{DD} = V_{DR}$ (min), CS1# ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V or (LB# and UB#) ≥ V_{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	25°C	-	5.5	13	uA
			85°C	-	-	19	
			125°C	-	-	52	
t_{SDR} (2)	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. Typical value indicates the value for the center of distribution at $V_{DD} = V_{DR}$ (min.), and not 100% tested.
2. VDD power down slope must be longer than 100 us/volt when enter into Data Retention Mode.

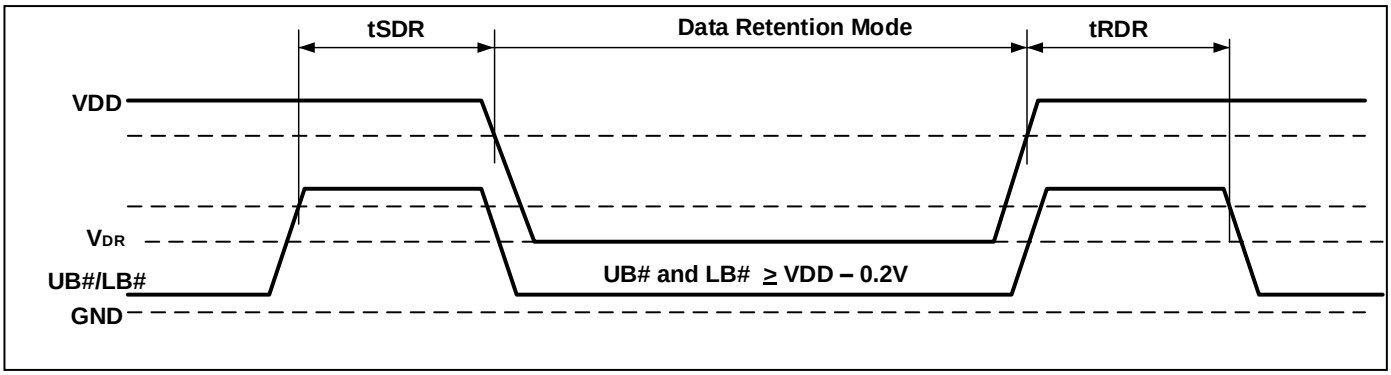
DATA RETENTION WAVEFORM (CS1# CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



DATA RETENTION WAVEFORM (UB# AND LB# CONTROLLED)



ORDERING INFORMATION

IS62/65WV102416GALL (1.65V - 2.2V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV102416GALL-55TLI	TSOP (Type I), Lead-free

AUTOMOTIVE RANGE (A3): –40°C TO +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV102416GALL-55CTLA3	TSOP (Type I), Copper Leadframe, Lead-free

IS62/65WV51216GBLL (2.2V - 3.6V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62WV102416GBLL-45TLI	TSOP (Type I), Lead-free

AUTOMOTIVE RANGE (A3): –40°C TO +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV102416GBLL-55CTLA3	TSOP (Type I), Copper Leadframe, Lead-free

PACKAGE INFORMATION