Six Current Channels, One Voltage Channel, Energy Metering IC

Data Sheet

ADE7816

FEATURES

- **Measures active and reactive energy, sampled waveforms, and current and voltage rms**
- **6 current input channels and 1 voltage channel**
- **<0.1% error in active and reactive energy over a dynamic range of 1000:1**
- **Supports current transformer and Rogowski coil sensors**
- **Provides instantaneous current and voltage readings**
- **Angle measurements on all 6 channels**
- **2 kHz bandwidth operation**
- **Reference: 1.2 V (drift 10 ppm/°C typical) with external overdrive capability**
- **Flexible I²C, SPI, and HSDC serial interfaces**

GENERAL DESCRIPTION

The ADE7816 is a highly accurate, multichannel metering device that is capable of measuring one voltage channel and up to six current channels. It measures line voltage and current and calculates active and reactive energy, as well as instantaneous rms voltage and current. The device incorporates seven sigma-delta (Σ-Δ) ADCs with a high accuracy energy measurement core. The six current input channels allow multiple loads to be measured simultaneously. The voltage channel and the six current channels each have a complete signal path allowing for a full range of measurements. Each input channel supports a flexible gain stage and is suitable for use with current transformers (CTs). Six on-chip digital integrators facilitate the use of the Rogowski coil sensors.

The ADE7816 provides access to on-chip meter registers via either the SPI or I²C interface. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I²C to provide access to real-time ADC output information. A full range of power quality information, such as overcurrent, overvoltage, peak, and sag detection, is accessible via the two external interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$.

The ADE7816 energy metering IC operates from a 3.3 V supply voltage and is available in a 40-lead LFCSP that is Pb free and RoHS compliant.

FUNCTIONAL BLOCK DIAGRAM

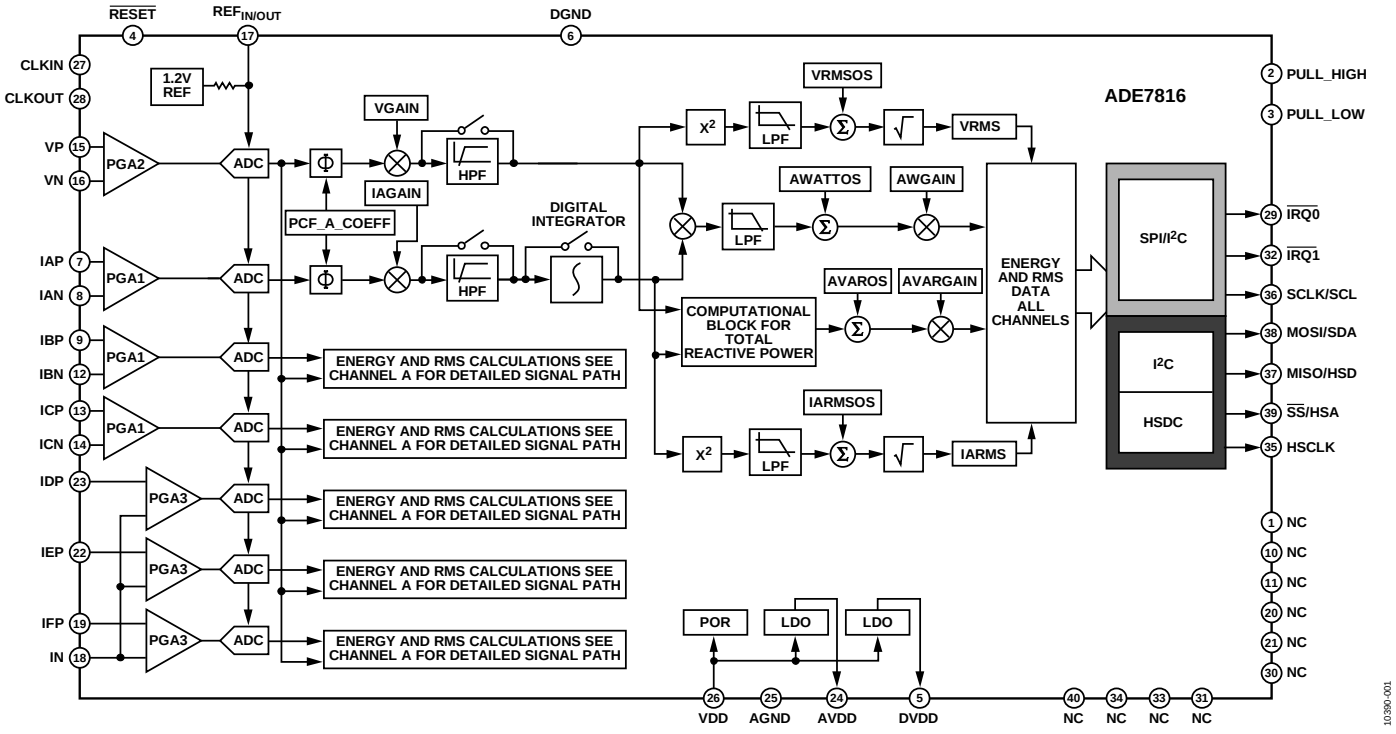

Figure 1.

Rev. B Document Feedback

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2/2012—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
Active Energy Measurement					
Active Energy Measurement Error (per Channel)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8,16; integrator on
Phase Error Between Channels					Line frequency = 45 Hz to 65 Hz, HPF on
Power Factor (PF) = 0.8 Capacitive			±0.05	Degrees	Phase lead = 37°
PF = 0.5 Inductive			±0.05	Degrees	Phase lag = 60°
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IxP = VP = ±100 mV rms
Energy Register Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Energy Register Variation		0.01		%	
Total Active Energy Measurement Bandwidth		2		kHz	
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (per Channel)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8,16; integrator on
Phase Error Between Channels					Line frequency = 45 Hz to 65 Hz, HPF on
PF = 0.8 Capacitive			±0.05	Degrees	Phase lead = 37°
PF = 0.5 Inductive			±0.05	Degrees	Phase lag = 60°
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IxP = VP = ±100 mV rms
Energy Register Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Energy Register Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		2		kHz	
RMS MEASUREMENTS					
I_{RMS} and V_{RMS} Measurement Bandwidth		2		kHz	
I_{RMS} and V_{RMS} Measurement Error		0.1		%	Over a dynamic range of 500 to 1; one second of averaging (100 samples)
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	Single-ended inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, IDP and IN, IEP and IN, IFP and IN.
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, IDP, IEP, and IFP Pins	400			kΩ	
IN Pin	130			kΩ	
ADC Offset Error		±2		mV	PGA = 1, uncalibrated error, see the Terminology section
Gain Error		±4		%	External 1.2 V reference

Parameter [1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Instantaneous Waveforms section
Signal-to-Noise Ratio, SNR		70		dB	PGA = 1
Signal-to-Noise-and-Distortion Ratio, SINAD		60		dB	PGA = 1
Bandwidth (−3 dB)		2		kHz	
TIME INTERVAL BETWEEN CHANNELS					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 1.207 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
Reference Error		±2		mV	
Output Impedance	1.2			kΩ	
Temperature Coefficient		10	50	ppm/°C	Maximum value across full temperature range of −40°C to +85°C
CLKIN, CLKOUT					All specifications are for CLKIN, CLKOUT of 16.384 MHz
Input Clock Frequency	16.22	16.384	16.55	MHz	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$/HSA, $\overline{RESET}$, PULL_HIGH, PULL_LOW					
Input High Voltage, V_{INH}	2.0			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			−8.7	µA	Input = 0 V, VDD = 3.3 V
			3	µA	Input = VDD = 3.3 V
		100		nA	Input = VDD = 3.3 V
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD					VDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			800	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			2	mA	
POWER SUPPLY					For specified performance
VDD Pin	3.0		3.6	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		25	27.8	mA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that, within the timing tables and diagrams, the dual function pin names are referenced by the relevant function only; see the Pin Configuration and Function Descriptions section for full pin mnemonics and function descriptions.

I²C-Compatible Interface Timing

Table 2. I²C-Compatible Interface Timing Parameters

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

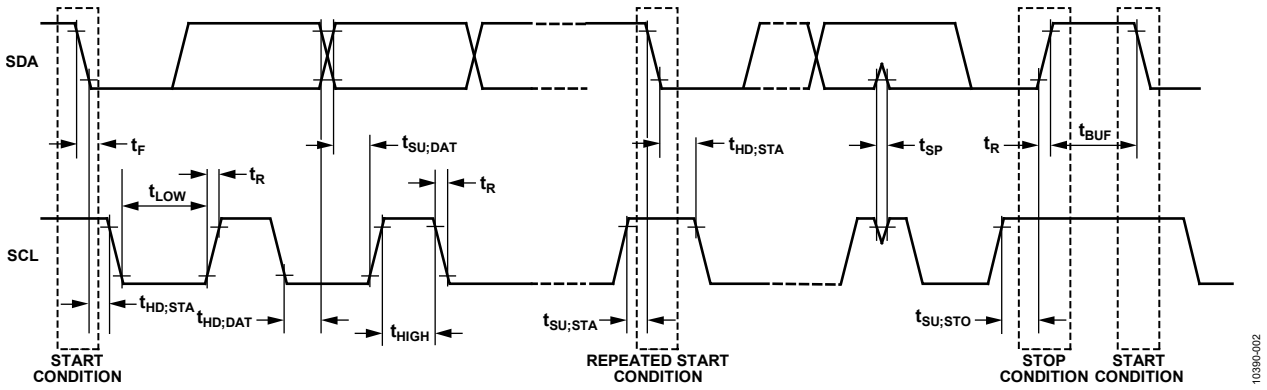


Figure 2. I²C-Compatible Interface Timing

SPI Interface Timing

Table 3. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

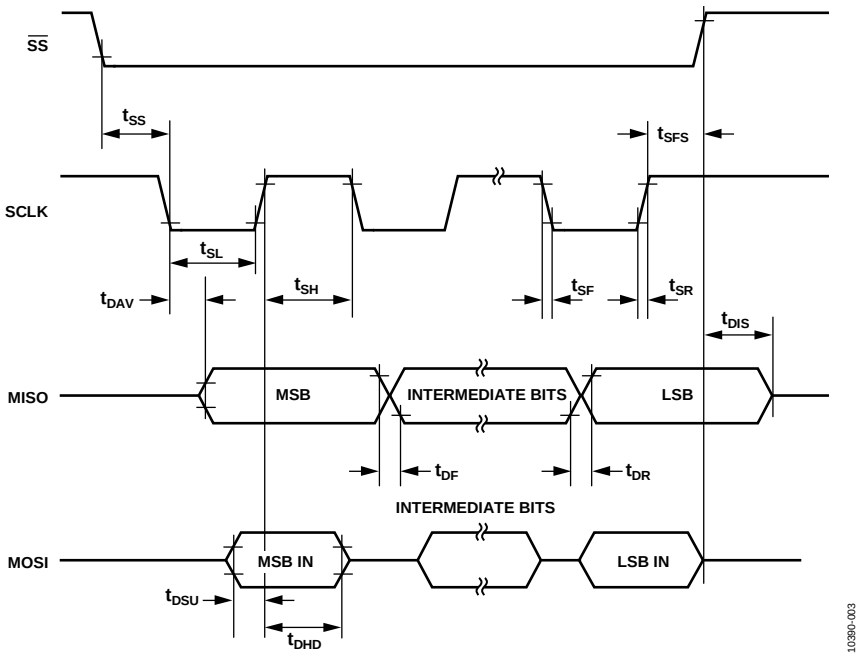


Figure 3. SPI Interface Timing

HSDC Interface Timing

Table 4. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

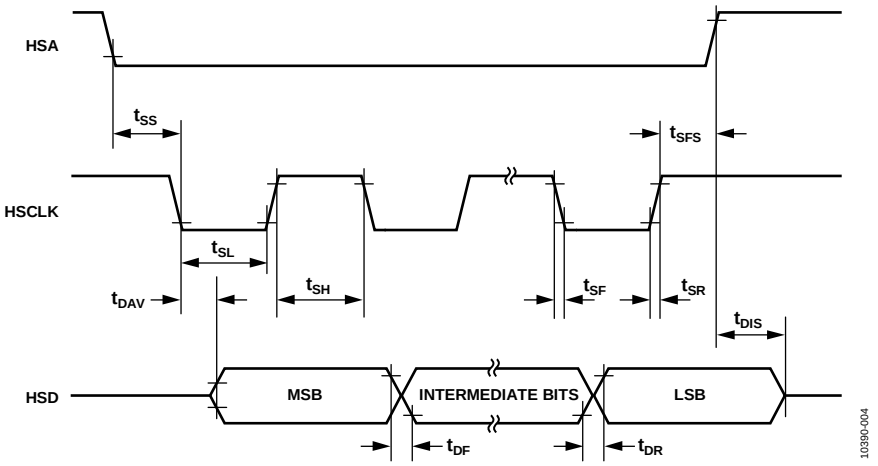


Figure 4. HSDC Interface Timing

Load Circuit for All Timing Specifications

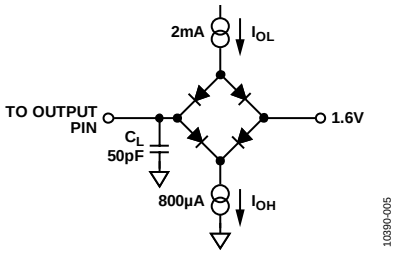


Figure 5. Load Circuit for All Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, IDP, IEP, IFP, IN	−2 V to +2 V
Analog Input Voltage to VP and VN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Regarding the temperature profile used in soldering RoHS-compliant parts, Analog Devices, Inc., advises that reflow profiles should conform to J-STD-20 from JEDEC. Refer to the JEDEC website for the latest revision.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

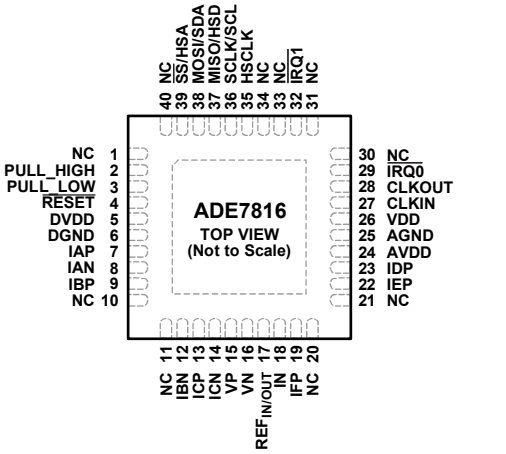
Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. PINS 1, 10, 11, 20, 21, 30, 31, 40 ARE NC PINS THAT MUST BE CONNECTED TO GND. SEE THE LAYOUT GUIDELINES SECTION.
2. NC = NO CONNECT. PIN 33 AND PIN 34 ARE NC PINS THAT MUST BE LEFT FLOATING. SEE THE LAYOUT GUIDELINES SECTION.
3. EXPOSED PAD. CREATE A SIMILAR PAD AND CONNECT THE PADS TO AGND AND DGND. SEE THE LAYOUT GUIDELINES SECTION.

10390-006

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. These pins must be connected to GND. See the Layout Guidelines section.
33, 34	NC	No Connect. These pins must be left floating. Do not connect to ground.
2	PULL_HIGH	Connect this pin to VDD for proper operation.
3	PULL_LOW	Connect this pin to AGND for proper operation.
4	$\overline{\text{RESET}}$	Active Low Reset Input. Hold this pin low for at least 10 µs to trigger a hardware reset.
5	DVDD	On-Chip 2.5 V Digital LDO Access. Do not connect any external active circuitry to this pin. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7, 8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this data sheet as Current Channel A. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IAN.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this data sheet as Current Channel B. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IBN.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this data sheet as Current Channel C. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to ICN.
15, 16	VP, VN	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this data sheet. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to VN. This channel also has an internal PGA.
17	$\text{REF}_{\text{IN/OUT}}$	On-Chip Voltage Reference Access. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
18	IN	Analog Input Common Pin for Current Channel D, Current Channel E, and Current Channel F. See the pin descriptions for Pin 19, Pin 22, and Pin 23 for more details.
19	IFP	Analog Input for Current Channel F. This channel is used with the current transducers and is referenced in this data sheet as Current Channel F. Connect this input in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IN.
22	IEP	Analog Input for Current Channel E. This channel is used with the current transducers and is referenced in this data sheet as Current Channel E. Connect this input in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IN.

Pin No.	Mnemonic	Description
23	IDP	Analog Input for Current Channel D. This channel is used with the current transducers and is referenced in this data sheet as Current Channel D. Connect this input in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IN.
24	AVDD	On-Chip 2.5 V Analog Low Dropout (LDO) Regulator Access. Do not connect external active circuitry to this pin. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, such as antialiasing filters and current and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage and should be set at 3.3 V ± 10% for specified operation. Decouple this pin to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT-cut crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7816. The clock frequency for specified operation is 16.384 MHz. Use ceramic load capacitors of a few tens of picofarads (pF) with the gate oscillator circuit. Refer to the crystal manufacturer data sheet for load capacitance requirements.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as stated in the description for Pin 27) to provide a clock source for the ADE7816. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
35	HSCLK	Serial Clock Output for the HSDC Port.
36	SCLK/SCL	Serial Clock Input for the SPI Port/Serial Clock Input for the I^2C Port. All serial data transfers are synchronized to this clock (see the Communication section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time (for example, opto-isolator outputs).
37	MISO/HSD	Data Output for SPI Port/Data Output for HSDC Port.
38	MOSI/SDA	Data Input for SPI Port/Data Output for I^2C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Exposed Pad. Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

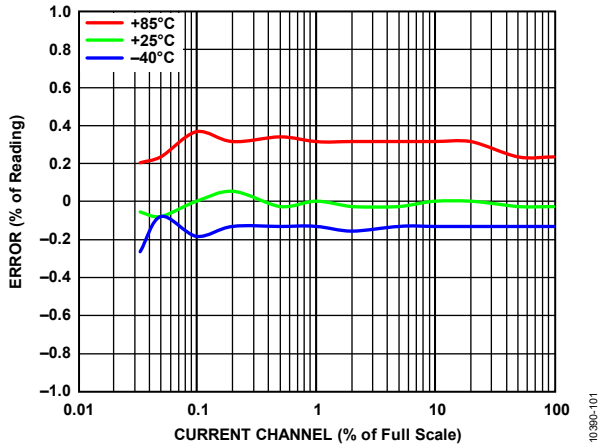


Figure 7. Active Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 1) over Temperature with Internal Reference, Integrator Off

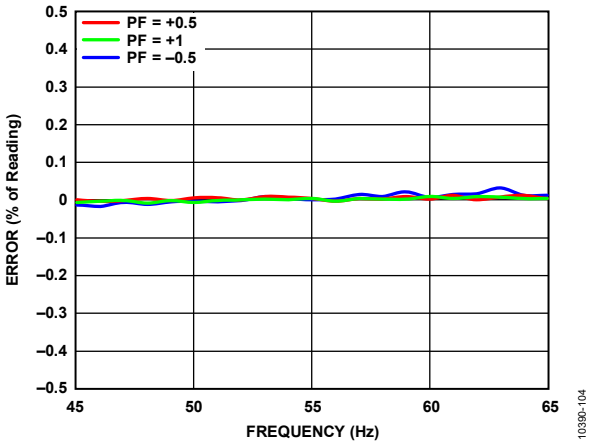


Figure 10. Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Frequency and Power Factor with Internal Reference, Integrator Off

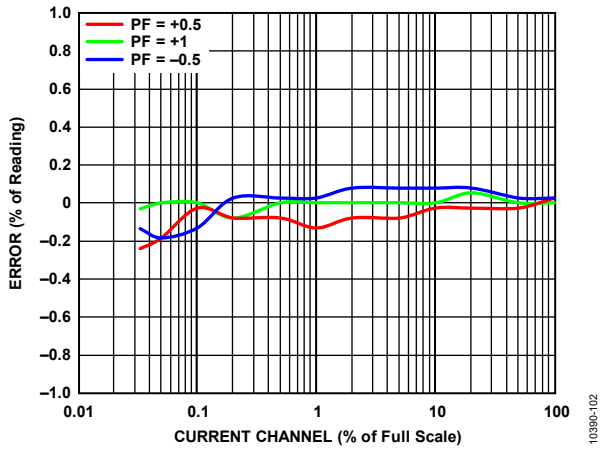


Figure 8. Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

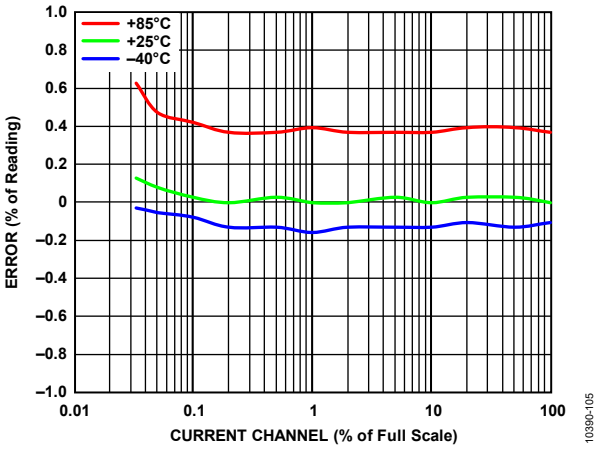


Figure 11. Reactive Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 0) over Temperature with Internal Reference, Integrator Off

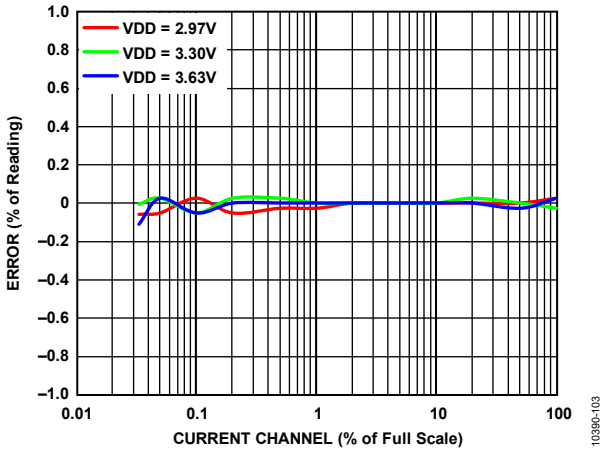


Figure 9. Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) over Supply Voltage with Internal Reference, Integrator Off

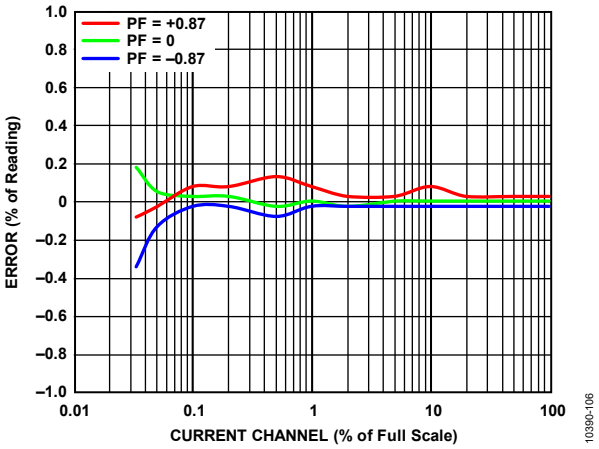


Figure 12. Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

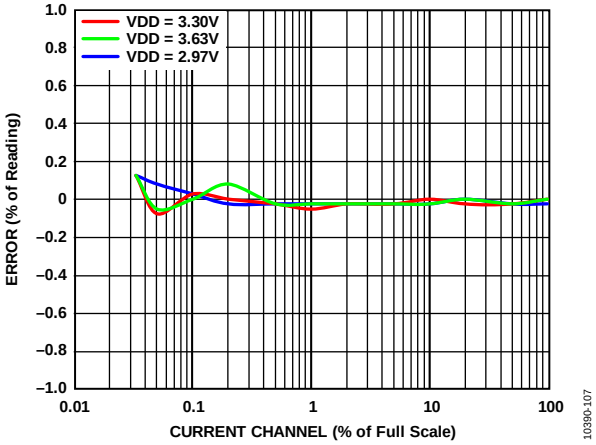


Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 0) over Supply Voltage with Internal Reference, Integrator Off

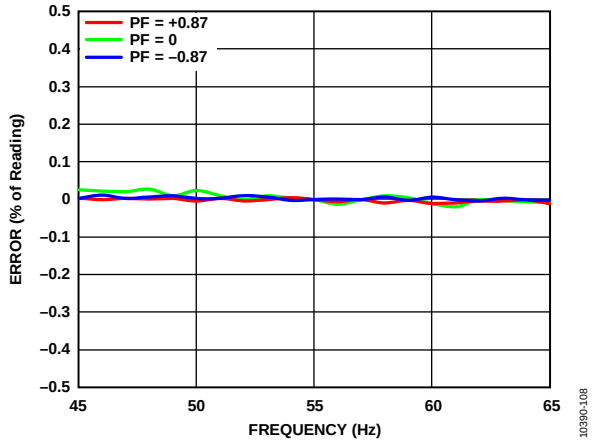


Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Frequency and Power Factor with Internal Reference

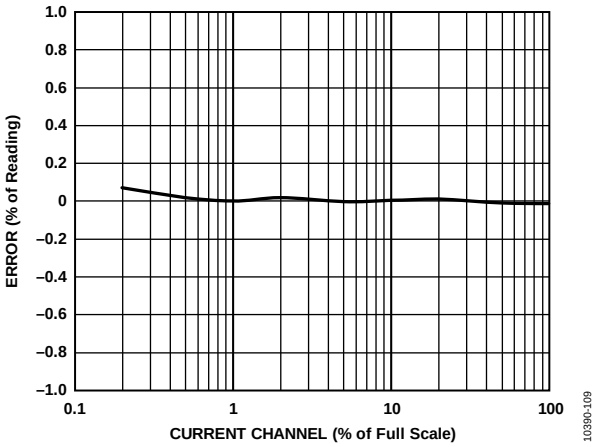


Figure 15. I_{RMS} Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator Off

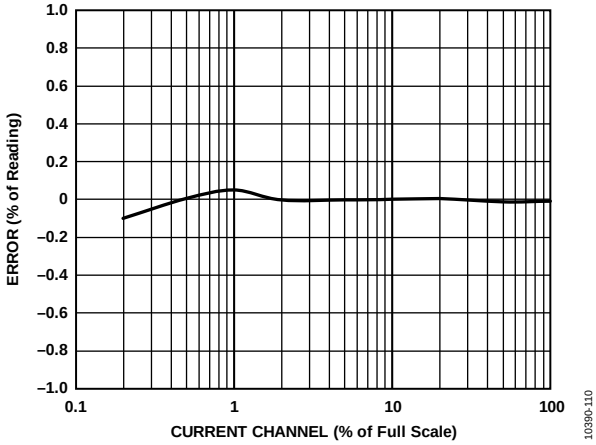


Figure 16. V_{RMS} Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator Off

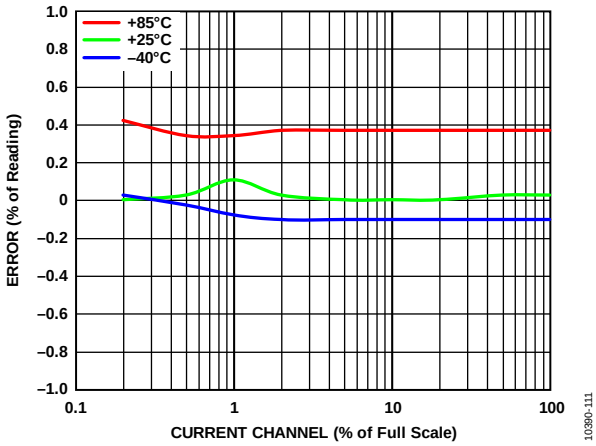


Figure 17. Active Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 1) over Temperature with Internal Reference, Integrator On

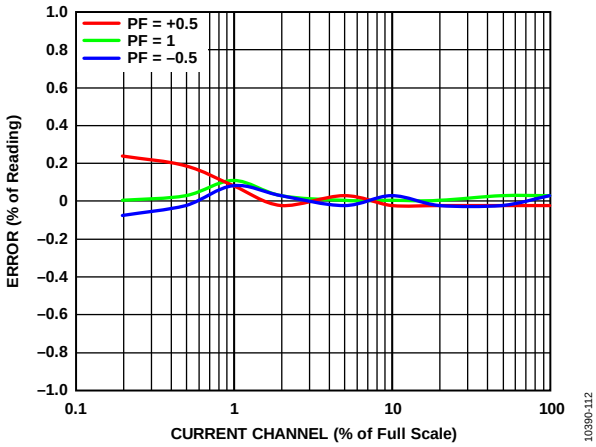


Figure 18. Active Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

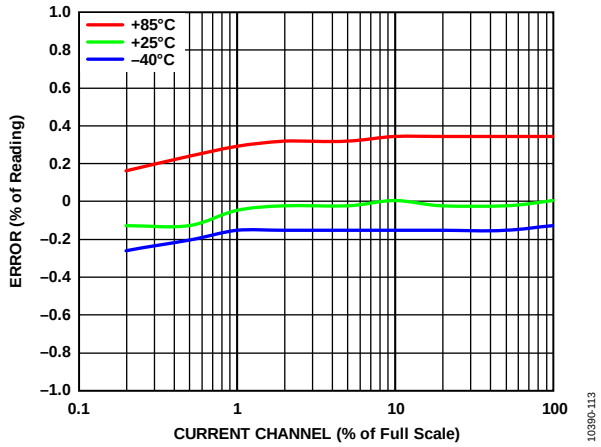


Figure 19. Reactive Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 0) over Temperature with Internal Reference, Integrator On

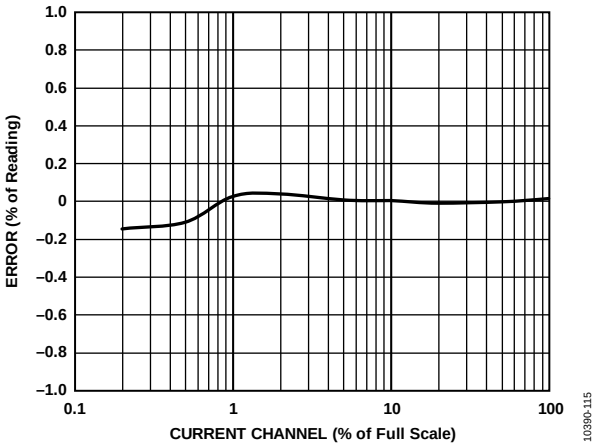


Figure 21. I_{RMS} Error as a Percentage of Reading (Gain = 16, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator On

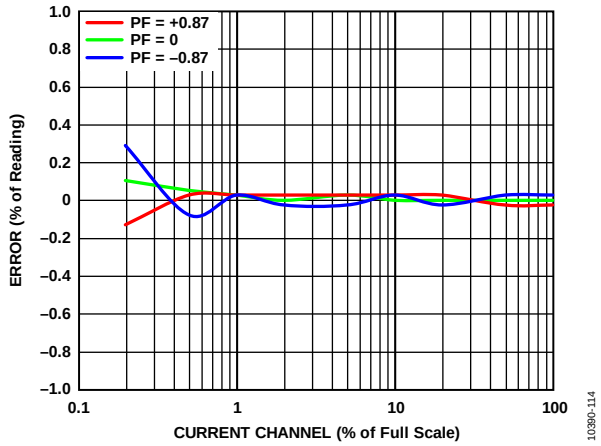


Figure 20. Reactive Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

TEST CIRCUIT

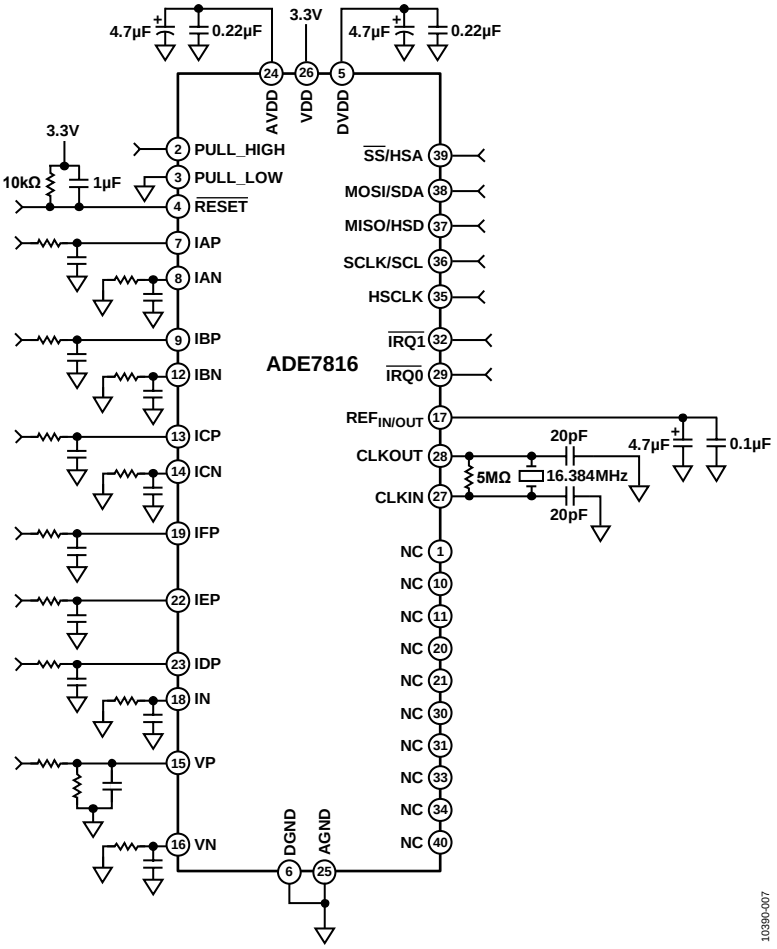


Figure 22. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7816 is defined by the following equation:

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7816 - True\ Energy}{True\ Energy} \times 100\%$$

Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current channels and the voltage channel. The all digital design ensures that the phase matching between the current channels and voltage channel in all three phases is within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

Power Supply Rejection (PSR)

PSR quantifies the ADE7816 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

ADC Offset Error

ADC offset error refers to the dc offset that is associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, the HPF removes the offset from the current channels and voltage channel, and the power calculation remains unaffected by this offset.

Gain Error

The gain error in the ADCs of the ADE7816 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code. The difference is expressed as a percentage of the ideal code.

QUICK START

This section outlines the procedure for powering up and initializing the ADE7816. Figure 23 shows a flow diagram of the initialization steps. For detailed information, refer to the section of the data sheet that pertains to each step, as indicated in Figure 23.

After power is supplied to the ADE7816 and communication is established, a set of registers must be written (see Figure 23). Table 8 lists details about each register.

The registers listed in Table 8 are essential for correct operation. After these registers are set, enable any meter-specific features before enabling the DSP to begin the energy calculations.

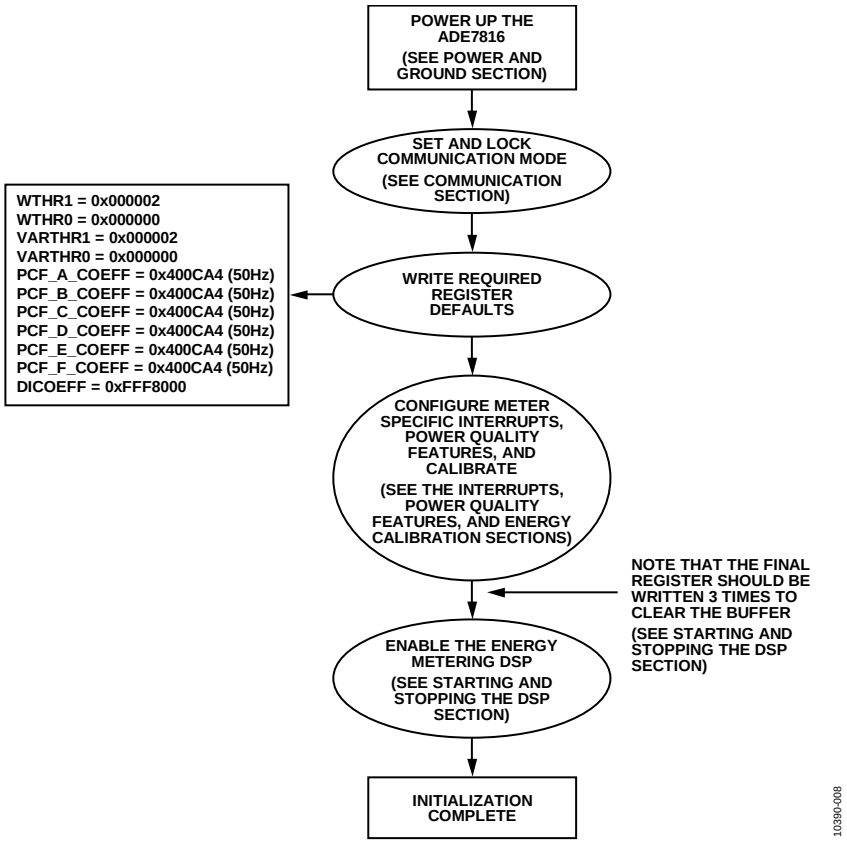


Figure 23. Quick Start

Table 8. Required Register Defaults

Register Address	Register Name	Register Description	Required Value	Reference Information
0x43AB	WTHR1	Threshold register for active energy	0x000002	Refer to the Active Energy Threshold section.
0x43AC	WTHR0	Threshold register for active energy	0x000000	Refer to the Active Energy Threshold section.
0x43AD	VARTHR1	Threshold register for reactive energy	0x000002	Refer to the Reactive Energy Threshold section.
0x43AE	VARTHR0	Threshold register for reactive energy	0x000000	Refer to the Reactive Energy Threshold section.
0x43B1	PCF_A_COEFF	Phase calibration for Current Channel A	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B2	PCF_B_COEFF	Phase calibration for Current Channel B	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B3	PCF_C_COEFF	Phase calibration for Current Channel C	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B4	PCF_D_COEFF	Phase calibration for Current Channel D	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B5	PCF_E_COEFF	Phase calibration for Current Channel E	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B6	PCF_F_COEFF	Phase calibration for Current Channel F	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x4388	DICOEFF	Digital integrator algorithm; required only if using di/dt sensors	0xFFF8000	Refer to the Digital Integrator section.

INPUTS

The following section provides details on the ADE7816 input connections that are required for correct functionality.

POWER AND GROUND

VDD and AGND, DGND

To power the ADE7816, a 3.3 V dc input voltage should be provided between the VDD pin and the AGND and DGND pins. In addition, the PULL_HIGH and PULL_LOW pins must be connected to 3.3 V and AGND, respectively. This configuration is shown in Figure 24.

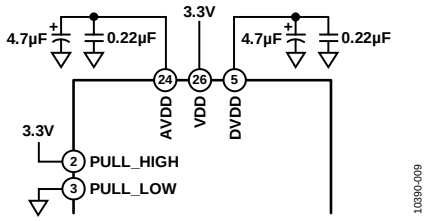


Figure 24. Applying Power to the ADE7816

The ADE7816 contains an on-chip power supply monitor that supervises the power supply (VDD). When the voltage applied to the VDD pin is below 2 V ± 10%, the chip is in an inactive state. After VDD crosses the 2 V ± 10% threshold, the power supply monitor keeps the ADE7816 in an inactive state for an additional 26 ms. This time delay allows VDD to reach the minimum specified operating voltage of 3.3 V − 10%. When the minimum specified operating voltage is met and the PULL_HIGH and PULL_LOW pins are tied to VDD and AGND, respectively, the internal circuitry is enabled. This process is accomplished in approximately 40 ms.

When the start-up sequence is complete and the ADE7816 is ready to receive communication from a microcontroller, the RSTDONE flag is set in the STATUS1 register (Address 0xE503). An external interrupt is triggered on the $\overline{\text{IRQ1}}$ pin. The RSTDONE interrupt is enabled by default and cannot be disabled; therefore, an external interrupt always occurs at the end of a power-up procedure or hardware or software reset.

It is highly recommended that the RSTDONE interrupt be used by the microcontroller to gate the first communication with the ADE7816. If the interrupt is not used, a timeout can be implemented. However, because the start-up sequence can vary from part to part and over temperature, a timeout of a least 100 ms is recommended. The RSTDONE interrupt provides the most time-efficient way of monitoring the completion of the ADE7816 start-up sequence.

The AVDD and DVDD output pins provide access to the on-chip analog and digital LDOs. When the ADE7816 is fully powered up, these pins are at 2.5 V. If the internal reference is being used, the $\text{REF}_{\text{IN/OUT}}$ pin outputs 1.2 V (see the Reference Circuit section).

When the start-up sequence is complete, all registers are at their default value, and the I²C port is the active serial port. Communication with the ADE7816 can begin. See the Communication section for more details.

To start the energy and rms computations, the internal DSP must be powered up after all configuration registers are set to their desired values. The DSP is started by setting the run register (Address 0xE228) to 0x0001. See the Starting and Stopping the DSP section for more information.

REFERENCE CIRCUIT

$\text{REF}_{\text{IN/OUT}}$

The nominal reference voltage at the $\text{REF}_{\text{IN/OUT}}$ pin is 1.2 V ± 0.075%. The $\text{REF}_{\text{IN/OUT}}$ pin can be overdriven by an external 1.2 V reference source. If Bit 0 (EXTREFEN) in the CONFIG2 register (Address 0xEC01) is cleared to 0 (the default value), the ADE7816 uses the internal voltage reference. If Bit 0 is set to 1, the external voltage reference is used.

The voltage of the ADE7816 internal reference drifts slightly with temperature; see the Specifications section for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for all ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy.

RESET

Hardware Reset

To initiate a hardware reset of the ADE7816, the $\overline{\text{RESET}}$ pin must be pulled low for at least 10 µs. After the $\overline{\text{RESET}}$ pin returns high, all registers return to their default values. The ADE7816 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is set to 0 during the transition period and changes to 1 when the transition ends.

Software Reset Functionality

Bit 7 (SWRST) in the CONFIG register (Address 0xE618) manages the software reset functionality in the ADE7816. The default value of this bit is 0. If Bit 7 is set to 1, the ADE7816 enters the software reset state. In this state, all internal registers are set to their default values, with the exception of the CONFIG2 register, which retains its existing value. In addition, the choice of which serial port is in use (I²C or SPI) remains unchanged if the lock-in procedure was executed previously (see the Communication section for details).

When the software reset ends, Bit 7 (SWRST) in the CONFIG register is cleared to 0, the $\overline{\text{IRQ1}}$ interrupt pin is set low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1. RSTDONE is set to 0 during the transition period and changes to 1 when the transition ends.

It is recommended that all meters be designed to have both software and hardware reset capability.

CLKIN AND CLKOUT

An external clock or parallel resonant crystal is required to clock the ADE7816. If an external clock source is being used, it should be connected to the CLKIN pin. The required clock frequency for specified operation is 16.384 MHz. Alternatively, a parallel resonant AT-cut crystal can be connected across the CLKIN and CLKOUT pins. The ADE7816 has no internal load capacitance and, therefore, load capacitors based on the data sheet of the crystal manufacturer should be added on each pin.

ANALOG INPUTS

Input Pins

The ADE7816 has seven analog inputs that form six current channels and one voltage channel. Current Channel A, Current Channel B, and Current Channel C each consist of a pair of differential input pins: IAP and IAN, IBP and IBN, and ICP and ICN. Current Channel D, Current Channel E, and Current Channel F all share a common reference, IN, and, therefore, are single-ended. For consistency, it is recommended that all six current inputs be connected in a single-ended configuration (see Figure 26 and Figure 27). The voltage channel is a fully differential input that consists of a pair of inputs: VP and VN. The voltage channel is typically connected in a single-ended configuration.

The maximum input voltage that should be applied to any input channel is ±500 mV. The maximum common-mode signal that is allowed on the inputs is ±25 mV. Figure 25 shows a schematic of the inputs and their relation to the maximum common-mode voltage.

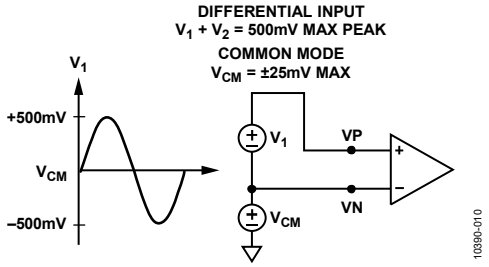


Figure 25. Maximum Input Level

PGA Gain

The ADE7816 has three internal PGA gain amplifiers that can be used to amplify the input signals by ×2, ×4, ×8 or ×16. The PGA gain stage is often required when using a current sensor that produces a low output voltage, such as Rogowski coils. PGA1 affects Current Channel A, Current Channel B, and Current Channel C and is controlled by Bits[2:0] (PGA1) of the gain register (Address 0xE60F). PGA2 affects the voltage channel and is controlled by Bits[5:3] (PGA2) of the gain register. PGA3 affects Current Channel D, Current Channel E, and Current Channel F and is controlled by Bits[8:6] (PGA3) of the gain register.

Table 9 lists details on how the PGA gain affects the full-scale input voltage.

Table 9. PGA Gain

Gain	Full-Scale Single-Ended Input (mV)	Gain Register (Address 0xE60F)		
		PGA1[2:0]	PGA2[5:3]	PGA3[8:6]
1	±500	000	000	000
2	±250	001	001	001
4	±125	010	010	010
8	±62.5	011	011	011
16	±31.25	100	100	100

Digital Integrator

The ADE7816 includes a digital integrator that must be enabled when using a di/dt sensor such as a Rogowski coil. This integrator is enabled by setting the INTEN bit (Bit 0) of the CONFIG register (Address 0xE618) to 1. When using the digital integrator, the DICOEFF register (Address 0x4388) should be written to 0xFFF8000. For more details on the theory behind the digital integrator, refer to the AN-1137 Application Note.

Antialiasing Filters

Each analog input pin requires that a simple RC filter be connected to the input. The role of the RC filter is to prevent aliasing. The aliasing effect is caused by frequency components (which are higher than half the sampling rate of the ADC) folding back and appearing in the sampled signal at a frequency that is below half the sampling rate. Aliasing is an artifact of all sampled systems. For conventional current sensors, it is recommended that one RC filter with a corner frequency of 5 kHz be used for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing for conventional current sensors (see Figure 26).

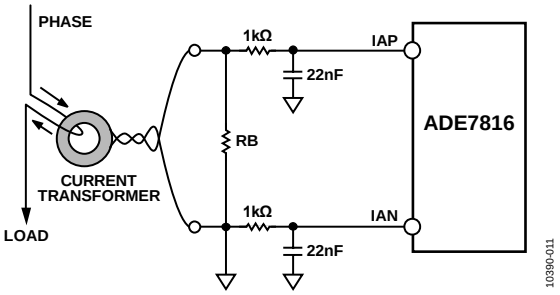


Figure 26. Current Transformer Input Connections

However, a di/dt sensor, such as a Rogowski coil, has a 20 dB per decade gain. This neutralizes the 20 dB per decade attenuation produced by the low-pass filter (LPF). Therefore, when using a di/dt sensor, a second pole is required. One simple approach is to cascade one additional RC filter, thereby producing a −40 dB per decade attenuation (see Figure 27).

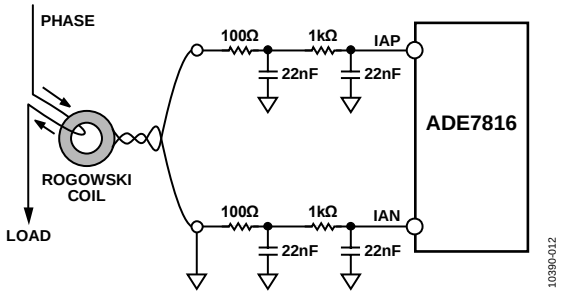


Figure 27. Rogowski Coil Input Connections

ENERGY MEASUREMENTS

This section describes the energy measurements available in the ADE7816. For information about the theory behind these measurements, refer to the AN-1137 Application Note.

STARTING AND STOPPING THE DSP

To obtain energy measurements, the internal processor must first be started by setting the run register (Address 0xE228) to 0x0001. It is recommended that all registers be initialized before starting the DSP and that the last register in the queue be written three times to flush the pipeline. When this procedure is complete, the DSP should be started. There is no reason to stop the DSP, once started, because all of the registers can be modified while the DSP is running. The DSP can be stopped, however, by writing 0x0000 to the run register.

Within the DSP core, there is a two-stage pipeline. This means that when a single register must be initialized, two or more writes are required to ensure that the value has been written. If two or more registers must be initialized, the last register must be written two more times to ensure that the value is written into the RAM. It is recommended that the last register be written three times to ensure successful communication. See the Register Protection section for details on protecting these registers.

ACTIVE ENERGY MEASUREMENT

Definition of Active Power and Active Energy

Active power is the product of voltage and current and is the power dissipated in a purely resistive load. Active energy is the accumulation of active power over time and is measured in watts.

The average power over an integral number of line cycles (n) is given by the following expression:

$$P = \frac{1}{nT}\int_0^{nT} P(t)dt = VI \quad (1)$$

where:
V is the rms voltage.
I is the rms current.
P is the active or real power.
T is the line cycle period.

Active Energy Registers

The ADE7816 has six active energy registers, where the active energy is accumulated for each of the six channels separately: AWATTHR (Address 0xE400), BWATTHR (Address 0xE401), CWATTHR (Address 0xE402), DWATTHR (Address 0xE403), EWATTHR (Address 0xE404) and FWATTHR (Address 0xE405). All active energy registers are in 32-bit, signed format. The ADE7816 accumulates both positive and negative power. Negative power indicates that the angle between the voltage and current is greater than 90°, and power is being injected back into the grid. The ADE7816 provides a signed accumulation of the power; positive power is added and negative power is subtracted. Figure 28 shows the configurations of the active energy signal path.

Active Energy Threshold

The ADE7816 accumulates energy in two steps (see Figure 28). The first step occurs internally, using the two threshold registers, WTHR1 (Address 0x43AB) and WTHR0 (Address 0x43AC). These registers make up the most significant and least significant 24 bits, respectively, of an internal threshold register that is used to control the frequency at which the external xWATTHR registers are updated. The WTHR1 and WTHR0 registers affect all six active energy measurements. For standard operation, the WTHR1 register should be set to 0x2 and the WTHR0 register set to 0x0. Thus, the update rate of the xWATTHR registers is set to slightly below the maximum of 8 kHz with full-scale inputs. If the rate at which energy is accumulated in the xWATTHR registers must be reduced, the WTHR1and WTHR0 registers can be modified.

$$Threshold = 0x2000000 \times \frac{8\text{ kHz}}{Required\ Update\ Rate\ (\text{kHz})} \quad (2)$$

Note that the maximum output with full scale inputs is 8 kHz. Do not adjust the threshold to try to produce more than 8 kHz. Such an adjustment may result in saturation of the output frequency and, therefore, a loss of accuracy.

The second stage of the accumulation occurs in the external registers, xWATTHR. With the recommended values provided in Equation 2, the energy updates at a rate of 8 kHz with full-scale inputs (see Figure 28).

Energy Accumulation and Register Roll-Over

As shown in Equation 2, the active energy accumulates at a maximum rate of 8 kHz with full-scale inputs. The maximum positive value that the 32-bit, signed xWATTHR registers can store before they overflow is 0x7FFFFFFF. Assuming steady accumulation with full-scale inputs, the accumulation time is

$$Time = 0x7FFFFFFF \times 125\ \mu s = 74\text{ hr, }33\text{ min, }55\text{ sec}$$

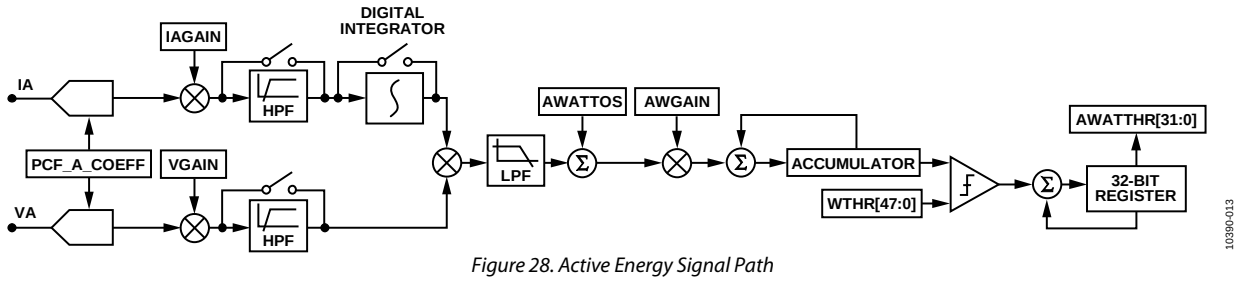


Figure 28. Active Energy Signal Path

The content of the active energy register overflows from full-scale positive (0x7FFFFFFF) to full-scale negative (0x80000000) and continues to increase in value when the active power is positive. Conversely, if the active power is negative, the energy register underflows from full-scale negative (0x80000000) to full-scale positive (0x7FFFFFFF) and continues decreasing in value. Bit 0 (AEHF1) in the STATUS0 register (Address 0xE502) is set when Bit 30 in the AWATTHR, BWATTHR, or CWATTHR register changes, signifying that one of these registers is half full. Similarly, Bit 1 (AEHF2) in the STATUS0 register is set when Bit 30 in the DWATTHR, EWATTHR, or FWATTHR register changes, signifying that one of these registers is half full.

Setting Bit 6 (RSTREAD) in the LCYCMODE register (Address 0xE702) enables a read-with-reset for all watt-hour accumulation registers. When this bit is set, all energy accumulation registers are set to 0 following a read operation.

REACTIVE ENERGY MEASUREMENT

Definition of Reactive Power and Reactive Energy

Reactive power is the product of the voltage and current when all harmonic components of one of these signals are phase shifted by 90°. Reactive power is the power dissipated in an induc-tive or capacitive load and is measured as volt-ampere reactive (var). Reactive energy is the accumulation of reactive power over time.

$$RP = \frac{1}{nT}\int_{0}^{nT} RP(t)dt = VI \times \sin(\theta) \quad (3)$$

where:
V is the rms voltage.
I is the rms current.
RP is the reactive or real power.
T is the line cycle period.

Reactive Energy Registers

The ADE7816 has six reactive energy registers that accumulate active energy for each of the six channels separately: AVARHR (Address 0xE406), BVARHR (Address 0xE407), CVARHR (Address 0xE408), DVARHR (Address 0xE409), EVARHR (Address 0xE40A), and FVARHR (Address 0xE40B). All reactive energy registers are in 32-bit, signed format. The ADE7816 accumulates both positive and negative reactive power. Negative reactive power indicates that the current is leading the voltage by up to 180°. The ADE7816 provides a signed accumulation of the power, where positive power is added and negative is subtracted.

Reactive Energy Threshold

The ADE7816 accumulates energy in two steps. The first is done internally using the threshold registers, VARTHR1 (Address 0x43AD) and VARTHR0 (Address 0x43AE). These registers make up the most significant and least significant 24 bits, respectively, of an internal threshold register that is used to control the frequency at which the external xVARHR registers are updated. The VARTHR1 and VARTHR0 registers affect all six reactive energy measurements. For standard operation, the VARTHR1 register should be set to 0x2 and the VARTHR0 register set to 0x0. This sets the update rate of the xVARHR registers to the maximum of 8 kHz with full-scale inputs.

If the rate at which energy is accumulated in the xVARHR registers must be reduced, VARTHR1 and VARTHR0 can be modified as follows:

$$Threshold = 0x2000000 \times \frac{8\text{ kHz}}{Required\ Update\ Rate\ (\text{kHz})} \quad (4)$$

Note that the maximum output with full scale inputs is 8 kHz. The threshold should not be adjusted to try to produce more than 8 kHz. Such an adjustment could result in saturation of the output frequency and, therefore, a loss of accuracy.

The second stage of the accumulation is done in the external registers, xVARHR. With the recommended values provided in Equation 4, the reactive energy updates at a rate of 8 kHz with full-scale inputs (see Figure 29).

Reactive Energy Accumulation and Register Roll-Over

The reactive energy accumulates at a maximum rate of 8 kHz with full-scale inputs. The maximum positive value that the 32-bit, signed xVARHR registers can store before they overflow is 0x7FFFFFFF. Assuming steady accumulation with full-scale reactive energy inputs, the accumulation time is

$$Time = 0x7FFFFFFF \times 125\ \mu s = 74\text{ hr, }33\text{ min, }55\text{ sec}$$

Conversely, if the reactive power is negative, the energy register underflows from full-scale negative (0x80000000) to full-scale positive (0x7FFFFFFF) and continues decreasing in value. Bit 2 (REHF1) in the STATUS0 register is set when Bit 30 of the AVARHR, BVARHR, or CVARHR register changes, signifying that one of these registers is half full. Similarly, Bit 3 (REHF2) in the STATUS0 register is set when Bit 30 of the DVARHR, EVARHR, or FVARHR register changes, signifying that one of these registers is half full.

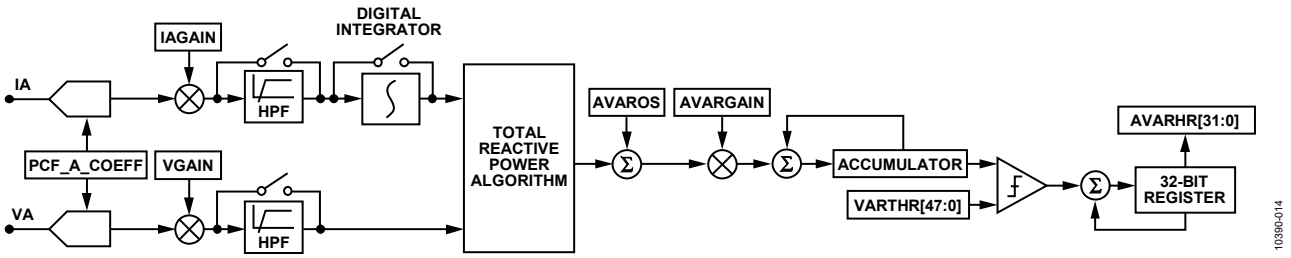


Figure 29. Reactive Energy Signal Path

The reactive energy register content overflows from full-scale positive (0x7FFFFFFF) to full-scale negative (0x80000000) and continues to increase in value when the reactive power is positive.

Setting Bit 6 (RSTREAD) of the LCYCMODE (Address 0xE702) register enables a read-with-reset for all reactive energy accumulation registers. When this bit is set, all energy accumulation registers are set to 0 following a read operation.

LINE CYCLE ACCUMULATION MODE

In the active and reactive line cycle accumulation mode, the energy accumulation of the ADE7816 is synchronized to the voltage channel zero crossing, so that the active and reactive energy can be accumulated over an integral number of half line cycles. This feature is available for the active and reactive energy accumulation on all six channels. The advantage of summing the active and reactive energy over an integral number of half line cycles is that the sinusoidal component of the energy is reduced to 0. This eliminates any ripple in the energy calculation. Accurate energy is calculated in a shorter time because the integration period can be shortened. The line cycle accumulation mode can be used for fast calibration and to obtain the average power over a specified time period. Figure 30 shows a diagram of the active energy line cycle accumulation mode signal path.

Active and reactive energy line cycle accumulation modes are disabled by default and can be enabled on all six channels by setting Bit 0 (LWATT) and Bit 1 (LVAR), respectively, in the LCYCMODE register. Bit 3 (ZX_SEL) of the LCYCMODE register must also be set to enable the voltage channel zero-crossing counter to be used in the line cycle accumulation measurement. The accumulation time should be written to the LINECYC register (Address 0xE60C) as an integer number of half line cycles. The ADE7816 can accumulate energy for up to 65,535 half line cycles. This equates to an accumulation period of approximately 655 sec with 50 Hz inputs, and 546 sec with 60 Hz inputs.

The number of half line cycles written to the LINECYC register is used for the active and reactive line cycle accumulation on all six channels. At the end of a line cycle accumulation period, the xWATTHR and xVARHR registers are updated and the LENERGY flag is set in the STATUS0 register (Address 0xE502). If the LENERGY bit in the MASK0 register (Address 0xE50A) is set, an external interrupt is issued on the IRQ0 pin. Another accumulation cycle begins immediately, as long as the LWATT and LVAR bits in the LCYCMODE register remain set.

The contents of the xWATTHR and xVARHR registers are updated synchronous to the LENERGY flag. The xWATTHR and xVARHR registers hold their current values until the end of the next line cycle period, when the contents are replaced with the new reading (see Figure 30 and Figure 31). When using the line cycle accumulation mode, Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because the read-with-reset function of the energy registers is not available in this mode.

Note that, when line cycle accumulation mode is first enabled, the reading after the first LENERGY flag should be ignored because it may be inaccurate. This inaccuracy is due to the line cycle accumulation mode not being synchronized to the zero crossing. As a result, the first reading may not be taken over a complete number of half line cycles. After the first line cycle accumulation is completed, all successive readings are correct.

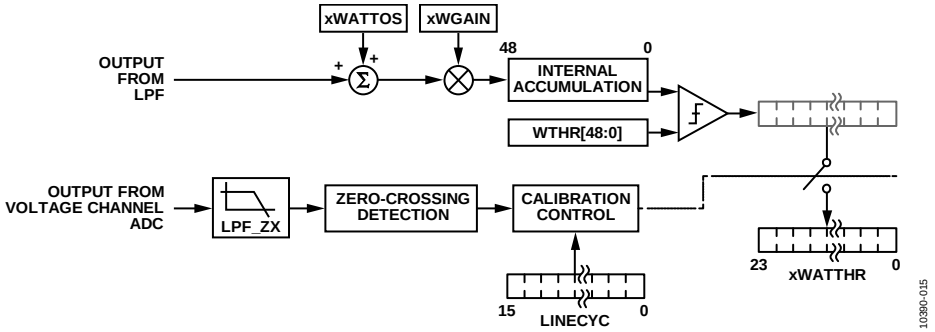


Figure 30. Line Cycle Accumulation for xWATTHR

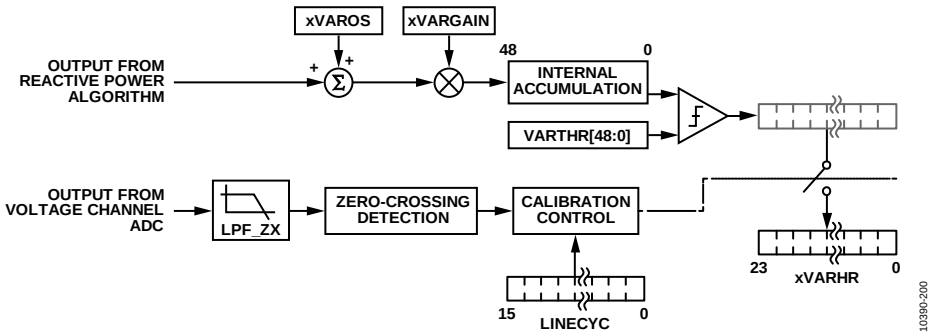


Figure 31. Line Cycle Accumulation for xVARHR

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Specifically, the rms of an ac signal is equal to the amount of dc required to produce an equivalent amount of power in the load. The ADE7816 provides rms measurements on the six current channels and the voltage channel simultaneously. These measurements have a settling time of approximately 440 ms with the integrator off and 500 ms with the integrator on. The registers are updated every 125 µs. The rms value is measured over a 2 kHz bandwidth.

The 24-bit, unsigned voltage rms measurement is available in the VRMS register (Address 0x43C0). Similarly, the six current channel rms measurements are available in the IARMS (Address 0x43C1), IBRMS (Address 0x43C2), ICRMS (Address 0x43C3), IDRMS (Address 0x43C4), IERMS (0x43C5), and IFRMS (Address 0x43C6) registers. All registers are updated at a rate of 8 kHz. Figure 32 shows the IxRMS signal path. A similar signal path is used on the voltage channel to compute the VRMS measurement.

Due to nonidealities in the internal filtering, it is recommended that the IxRMS registers be read synchronously to the zero-crossing signal (see the Zero-Crossing Detection section). This helps to stabilize reading-to-reading variation by removing the effect of any 2ω ripple that is present on the rms measurement.

With the specified full-scale analog input signal of 0.5 V, the rms value of a sinusoidal signal is 4,191,910 (0x3FF6A6), independent of line frequency. If the integrator is enabled on the current channels, the equivalent current rms value of a full-scale sinusoidal signal at 50 Hz is 4,191,910 (0x3FF6A6). At 60 Hz, it is 3,493,258 (0x354D8A).

NO LOAD DETECTION

The ADE7816 includes a no load detection feature that eliminates meter creep. Meter creep is defined as excess energy that is accumulated by the meter when there is no load attached. The ADE7816 warns of this condition and stops energy accumulation if the energy falls below a programmable threshold. The ADE7816 includes a no load feature on the active and reactive energy measurements. This allows a true no load condition to be detected.

The no load condition is triggered when the absolute values of the active and reactive powers are less than or equal to a threshold that is specified in the APNOLOAD (Address 0x43AF) and VARNOLOAD (Address 0x43B0) registers. When in the no load condition, the active and reactive energies are no longer accumulated in the energy registers. Note that each of the six channels has a separate no load circuit.

Setting the No Load Thresholds

The APNOLOAD and VARNOLOAD registers are compared to the active and reactive powers, respectively, to set the no load threshold. With full-scale inputs on both the current and voltage channel, the maximum power is 0x1FF6A6B. The no load threshold should, therefore, be set with respect to this maximum power, as follows:

$$APNOLOAD = 0x1FF6A6B \times V_{\%\ of\ Full\_Scale} \times I_{(noload)\%\ of\ Full\_Scale} \quad (5)$$

For example, if the nominal voltage is set to 50% of full scale and the current channel no load threshold is required to be at 0.01% of full scale, the APNOLOAD threshold is

$$APNOLOAD = 0x1FF6A6B \times 50\% \times 0.01\% = 0x68C \quad (6)$$

The VARNOLOAD register is usually set to the same value as that of the APNOLOAD register. When the APNOLOAD and VARNOLOAD registers are set to negative values, the no load detection circuit is disabled.

Bit 0 (NLOAD1) in the STATUS1 register (Address 0xE503) is set when the no load condition occurs on the A, B, or C current channel. Bit 1 (NLOAD2) in the STATUS1 register is set when the load condition occurs on the D, E, or F current channel. Bits[5:0] (NOLOADx) in the CHNOLOAD register (Address 0xE608) can be used to determine which channel caused the no load condition. When NOLOADx is cleared to 0, the channel is not in a no load condition. When NOLOADx is set to 1, the channel is in a no load condition.

No Load Interrupt

The ADE7816 includes two interrupts that are associated with the no load feature. The first is associated with the A, B, and C current channels, and it can be enabled by setting Bit 0 (NLOAD1) in the MASK1 register (Address 0xE50B). The second interrupt is associated with the D, E, and F current channels; it can be enabled by setting Bit 1 (NLOAD2) in the MASK1 register. If the corresponding interrupt is enabled, the no load condition causes the external $\overline{\text{IRQ1}}$ pin to go low (see the Interrupts section).

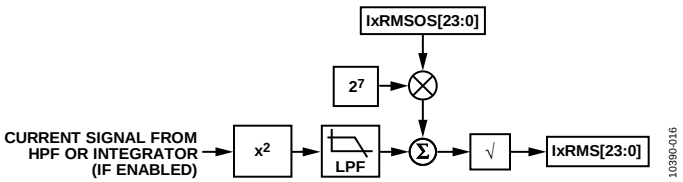


Figure 32. IxRMS Signal Path

ENERGY CALIBRATION

CHANNEL MATCHING

The ADE7816 provides individual channel gain registers that allow the six current channels and the voltage channel to be matched. Matching the channels simplifies the calibration process. The IAGAIN (Address 0x4381), IBGAIN (Address 0x4382), ICGAIN (Address 0x4383), IDGAIN (Address 0x4384), IEGAIN (Address 0x4385), and IFGAIN (Address 0x4386) registers adjust the A through F current channels, respectively, whereas the VGAIN register (Address 0x4380) can be used to adjust the voltage channel. The default value of the IxGAIN registers is 0x00000, which corresponds to no channel gain. The IxGAIN can adjust the channel gain by up to ±100%. The channel is scaled by −50% by writing 0xC00000 to the corresponding IxGAIN register, and it is increased by +50% by writing 0x400000. Equation 7 shows the relationship between the IxGAIN register and the rms measurement.

$$I_{rms} = I_{rms_0} \times \left(1 + \frac{IxGAIN}{2^{23}}\right) \quad (7)$$

$$V_{rms} = V_{rms_0} \times \left(1 + \frac{VGAIN}{2^{23}}\right)$$

where I_{rms_0} and V_{rms_0} are the current and voltage rms measurements, respectively, without offset correction.

Changing the content of the IxGAIN registers affects all calculations based off that channel, including the active and reactive energy. Therefore, it is recommended that the channel matching be performed first in the calibration procedure.

ENERGY GAIN CALIBRATION

The active and reactive energy measurements can be calibrated on all six channels separately. This separate calibration allows compensation for meter-to-meter gain variation.

The AWGAIN register (Address 0x4391) controls the active power gain calibration on Current Channel A. The BWGAIN (Address 0x4393), CWGAIN (Address 0x4395), DWGAIN (Address 0x4397), EWGAIN (Address 0x4399), and FWGAIN (Address 0x439B) registers control the active power gain calibration on the B through F current channels, respectively. The default value of the xWGAIN registers is 0x00000, which corresponds to no gain calibration. The xWGAIN registers can adjust the active power by up to ±100%. The output is scaled by −50% by writing 0xC00000 to the watt gain registers, and it is increased by +50% by writing 0x400000 to them. Equation 8 shows the relationship between the gain adjustment and the xWGAIN registers.

$$Active\ Power = Active\ Power_0 \times \left(\frac{xWGAIN}{0x800000} + 1\right) \quad (8)$$

Similar gain calibration registers are available for the reactive power. The reactive power on Current Channel A can be gain calibrated using the AVARGAIN (Address 0x439D) register. The BVARGAIN (Address 0x439F), CVARGAIN (Address 0x43A1), DVARGAIN (Address 0x43A3), EVARGAIN (Address 0x43A5), and FVARGAIN (Address 0x43A7) registers control the reactive power gain calibration on the B through F current channels, respectively. The xVARGAIN registers affect the reactive power in the same way that the xWGAIN registers affect the active power. Equation 9 shows the relationship between gain adjustment and the xVARGAIN registers.

$$Reactive\ Power = Reactive\ Power_0 \times \left(\frac{xVARGAIN}{0x800000} + 1\right) \quad (9)$$

ENERGY OFFSET CALIBRATION

The ADE7816 includes offset calibration registers for the active and reactive powers on all six channels. Offsets can exist in the power calculations due to crosstalk between channels on the PCB and in the ADE7816. The offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input levels.

The active power offset can be corrected on Current Channel A by adjusting the AWATTOS (Address 0x4392) register. The BWATTOS (Address 0x4394), CWATTOS (Address 0x4396), DWATTOS (Address 0x4398), EWATTOS (Address 0x439A), and FWATTOS (Address 0x439C) registers control the active power offset calibration on the B through F current channels, respectively. The xWATTOS registers are 24-bit, signed, twos complement registers with default values of 0. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full-scale current and voltage inputs, the maximum power output is equal to 1FF6A6B = 33,516,139. At −80 dB down from full scale (active power scaled down 10^4 times), one LSB of the xWATTOS registers represents 0.0298%. Equation 10 shows the relationship between the xWATTOS registers and the active energy reading.

$$xWATTHR = xWATTHR_0 + \left(\frac{8000}{WTHR} \times xWATTOS \times AccumulationTime(s)\right) \quad (10)$$

Similar offset calibration registers are available for the reactive power. The reactive power on Current Channel A can be offset calibrated using the AVAROS (Address 0x439E). The BVAROS (Address 0x43A0), CVAROS (Address 0x43A2), DVAROS (Address 0x43A4), EVAROS (Address 0x43A6), and FVAROS (Address 0x43A8) registers control the reactive power gain calibration on the B through F current channels, respectively. The xVAROS registers affect the reactive powers in the same way that the xWATTOS registers affect the active power. Equation 11 shows the relationship between the xVAROS registers and the reactive energy reading.

$$xVARHR = xVARHR_0 + \left(\frac{8000}{VARTHR} \times xVAROS \times AccumulationTime(s)\right) \quad (11)$$

ENERGY PHASE CALIBRATION

The ADE7816 is designed to function with a variety of current transducers, including those that induce inherent phase errors. A phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected to achieve accurate power readings. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7816 provides a means of digitally calibrating these small phase errors by introducing a time delay or a time advance.

Because different sensors can be used on each channel, separate phase calibration registers are included all six channels. The PCF_A_COEFF register (Address 0x43B1) can be used to correct phase errors on Current Channel A. The PCF_B_COEFF (Address 0x43B2), PCF_C_COEFF (Address 0x43B3), PCF_D_COEFF (Address 0x43B4), PCF_E_COEFF (Address 0x43B5), and PCF_F_COEFF (Address 0x43B6) registers control the phase calibration on the B through F current channels, respectively. All registers are 24-bit, unsigned.

The ADE7816 uses all pass filters to accurately add time advances and delays to the current channels with respect to the voltage channels. A separate filter is included on each of the six current channels. To adjust the time delay or advance, the coefficient of these filters must be adjusted. Equation 12, Equation 13, and Equation 14 show how the coefficients correspond to the phase offset in radians.

$$PCF\_x\_COEFF_{FRACTION} = \frac{\sin(\theta + 3\omega) - \sin\omega}{\sin(\theta + 4\omega)} \quad (12)$$

If PCF_x_COEFF ≥ 0, then

$$PCF\_x\_COEFF = 2^{23} \times PCF\_x\_COEFF_{FRACTION} \quad (13)$$

If PCF_x_COEFF < 0, then

$$PCF\_x\_COEFF = (2^{23} + 23^{28}) \times PCF\_x\_COEFF_{FRACTION} \quad (14)$$

where θ is the required current-to-voltage phase adjustment.

$$\omega = 2\pi \frac{Linefreq(Hz)}{8000}$$

To simplify this calculation, Analog Devices has a spreadsheet file that calculates this value. To obtain this spreadsheet, contact a representative of Analog Devices.

By default, the PCF_x_COEFF registers are set to 0. This setting does not, however, result in a 0° phase shift. On startup, the PCF_x_COEFF registers should be set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.

RMS OFFSET CALIBRATION

The ADE7816 includes an rms offset compensation register for each channel, as follows: IARMSOS (Address 0x438B), IBRMSOS (Address 0x438C), ICRMSOS (Address 0x438D), IDRMSOS (Address 0x438E), IERMSOS (Address 0x438F), IFRMSOS (Address 0x4390), and VRMSOS (Address 0x438A). These 24-bit, signed registers are used to remove offsets in the current and voltage rms calculations. The rms offset compensation register is added to the squared current and voltage signal before the square root is executed. Equation 15 shows the relationship between the rms measurement and the offset adjustment.

$$I_{rms} = \sqrt{I_{rms_0^2} + 128 \times IxRMSOS} \quad (15)$$

$$V_{rms} = \sqrt{V_{rms_0^2} + 128 \times VRMSOS}$$

where I_{rms_0} and V_{rms_0} are the current and voltage rms measurement, respectively, without offset correction.

POWER QUALITY FEATURES

This section describes the power quality features that are available in the ADE7816.

SELECTING A CURRENT CHANNEL GROUP

When using the power quality features on the current channels, the group of channels to be monitored must be selected. Bit 14 (CHANNEL_SEL) of the COMPMODE register (Address 0xE60E) can be used to make this selection. To select the A, B, and C current channels for the current channel power quality measurements, CHANNEL_SEL must be set to 0 (default). To select the D, E, and F current channels for the current channel power quality measurements, CHANNEL_SEL must be set to 1. If all channels require monitoring, the monitoring must be done in series by modifying the CHANNEL_SEL bit after data is obtained. The settling time of each power quality measurement is provided in the section that pertains to each power quality feature.

INSTANTANEOUS WAVEFORMS

The ADE7816 provides access to the current and voltage channel waveform data. This information allows the instantaneous data to be analyzed in more detail, including reconstruction of the current and voltage input for harmonic analyses. These measurements are available from a set of 24-bit, signed registers. The voltage channel has a dedicated register, VWV (Address 0xE510), whereas the current channels share three registers: IAWV/IDWV (Address 0xE50C), IBWV/IEWV (Address 0xE50D), and ICWV/IFWV (Address 0xE50E). A group of current channels (A, B, C or D, E, F) must be selected by Bit 14 (CHANNEL_SEL) of the COMPMODE register (see the Selecting a Current Channel Group section).

All measurements are updated at a rate of 8 kHz. The ADE7816 provides an interrupt status bit, DREADY (Bit 17 of the STATUS0 register, Address 0xE502), that is triggered at a rate of 8 kHz, allowing measurements to be synchronized with the instantaneous update signal rate. The instantaneous update signal can also be configured to trigger an interrupt on the external pin by setting the DREADY bit (Bit 17) in the MASK0 register (Address 0xE50A). With the specified full-scale analog input signal of 0.5 V, the expected reading on the current and voltage waveform register is approximately ±5,989,256 (dec).

The instantaneous waveforms have no additional settling time, and, therefore, if the CHANNEL_SEL bit is modified to change the group of current channels being measured, the new result is available in 125 µs (8 kHz).

ZERO-CROSSING DETECTION

Zero-Crossing Detection

The ADE7816 has a zero-crossing (ZX) detection circuit on the voltage and current channels. Zero-crossing detection allows measurements to be synchronized to the frequency of the incoming waveforms.

The zero-crossing events are filtered internally by an LPF. The LPF is intended to eliminate all harmonics of 50 Hz and 60 Hz systems, and to help identify the zero-crossing events on the fundamental components of both current and voltage channels. The digital filter has a pole at 80 Hz and is clocked at 256 kHz. As a result, there is a phase lag between the analog input signal and the output of the LPF. The error in ZX detection is 0.0703° for 50 Hz systems and 0.0843° for 60 Hz systems. The phase lag response of the LPF results in a time delay of approximately 1.74 ms (at 50 Hz) between its input and output. The overall delay between the zero crossing on the analog inputs and the ZX detection that is obtained after LPF1 is about 2.6 ms (at 50 Hz). Figure 33 shows how the zero-crossing signal is detected.

To provide further protection from noise, input signals to the voltage channel with an amplitude of <10% of full scale do not generate zero-crossing events at all. The ZX detection circuit of the current channels is active for all input signals, independent of their amplitudes.

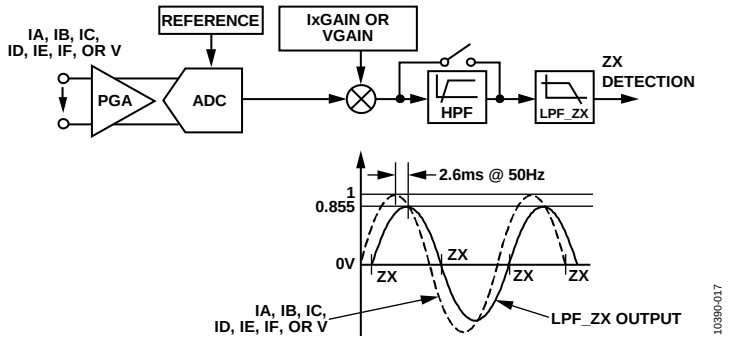


Figure 33. Zero-Crossing Detection

The ADE7816 contains four zero-crossing detection circuits, one dedicated for the voltage channel and three for the current channels. A group of current channels (A, B, C or D, E, F) must be selected by Bit 14 (CHANNEL_SEL) of the COMPMODE register, Address 0xE60E (see the Selecting a Current Channel Group section). When switching between channel groups, a settling time of 10 ms (50 Hz) or 8 ms (60 Hz) is required. Each circuit drives one flag in the STATUS1 register (Address 0xE503). For example, if a zero crossing occurs on the voltage channel, Bit 9 (ZXV) in the STATUS1 register goes high. If a zero-crossing event occurs on Current Channel A and the CHANNEL_SEL bit in the COMPMODE register is set to 0, Bit 12 (ZXI1) in the STATUS1 register is set to 1.

Zero-Crossing Timeout

Each zero-crossing detection circuit has an associated timeout register. This register is loaded with the value that is written into the 16-bit ZXTOUT register (Address 0xE60D) and is decremented by 1 LSB every 62.5 µs (16 kHz clock). The register is reset to the ZXTOUT value every time a zero crossing is detected. The default value of this register is 0xFFFF. If the timeout register decrements to 0 before a zero crossing is detected, the corresponding STATUS1 bit is set.

There is a zero-crossing timeout circuit that is dedicated to the voltage channel. For example, if a zero-crossing timeout event occurs on the voltage channel, Bit 3 (ZXTOV) in the STATUS1 register is set. There are three zero-crossing timeout circuits for the six current channels. A group of current channels, A, B, C or D, E, F, must be selected by the CHANNEL_SEL bit of the COMPMODE register (see the Selecting a Current Channel Group section). For example, if a zero-crossing timeout event occurs on Current Channel D and the CHANNEL_SEL bit in the COMPMODE register is set to 1, Bit 6 (ZXTOI1) in the STATUS1 register is set to 1.

The resolution of the ZXTOUT register is 62.5 µs (16 kHz clock) per LSB. Therefore, the maximum timeout period for an interrupt is 4.096 sec (2^{16}/16 kHz).

PEAK DETECTION

The ADE7816 includes an instantaneous peak detection feature that stores the maximum absolute value reached on the current and voltage channels over a fixed number of half line cycles. The PEAKCYC register (Address 0xE703) stores the number of half line cycles used for all peak measurements.

The peak detection feature is available on the voltage channel and three of the current channels. A group of current channels (A, B, C or D, E, F) must be selected by the CHANNEL_SEL bit of the COMPMODE register (see the Selecting a Current Channel Group section). When switching between current channel groups, no additional settling time is required. However, the PEAKCYC register should be rewritten to reset the measurement. By default, all three current channels are included in the peak detection measurement. If only one or two current channels are required, Bits[4:2] (PEAKSELx) of the MMODE register (Address 0xE700) can be set to 0 to disable a channel. Note that one PEAKSELx bit must always be set to 1 to enable the feature.

The results of the current and voltage peak detection are stored in the lowest 24 bits of two 32-bit, unsigned registers, IPEAK (Address 0xE500) and VPEAK (Address 0xE501). The peak detection measurements are updated at the end of the peak cycle specified in the PEAKCYC register. At that time, Bit 24 (PKV) and Bit 23 (PKI) in the STATUS1 register go high, signaling a peak event. To determine which current channel caused the peak event, Bits[26:24] (IPCHANNELx) in the IPEAK register must be read.

Setting the PEAKCYC Register

The 8-bit, unsigned PEAKCYC register contains the programmable peak detection period. The peak detection period is the number of half line cycles over which the peak measurement is measured. Each LSB of the PEAKCYC register corresponds to one half line cycle period. The PEAKCYC register holds a maximum value of 255.

At 50 Hz, the maximum peak cycle time is 2.55 seconds.

$$\left(\frac{1}{50} \div 2\right) \times 255 = 2.55 \text{ sec}$$

At 60 Hz, the maximum peak cycle time is 2.125 seconds.

$$\left(\frac{1}{60} \div 2\right) \times 255 = 2.125 \text{ sec}$$

OVERCURRENT AND OVERVOLTAGE DETECTION

The ADE7816 provides an overcurrent and overvoltage feature that detects whether the absolute value of the current or voltage waveform exceeds a programmable threshold. This feature uses the instantaneous voltage and current signals. The two registers used to set the voltage and current channel threshold are OVLVL (Address 0xE508) and OILVL (Address 0xE507), respectively. The OILVL threshold register determines the threshold for all current channels. The default value of the OVLVL and OILVL registers is 0xFFFFFF, which effectively disables the feature. Figure 34 shows the operation of the overvoltage detection feature.

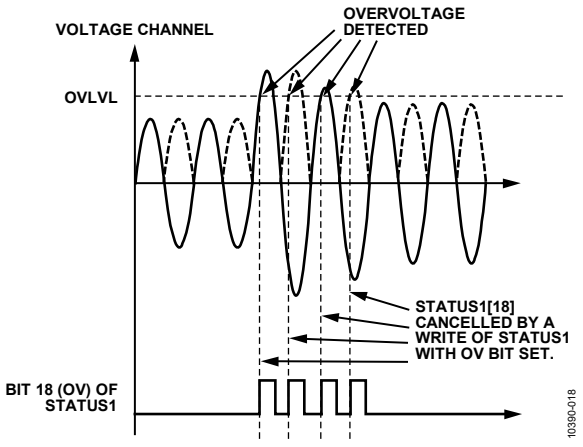


Figure 34. Overvoltage Detection

As shown in Figure 34, the OV bit (Bit 18) in the STATUS1 register (Address 0xE503) is set to 1 if the ADE7816 detects an overvoltage condition. The overcurrent detection feature works in a similar manner; however, a group of current channels (A, B, C or D, E, F) must be selected by Bit 14 (CHANNEL_SEL) of the COMPMODE register, Address 0xE60E (see the Selecting a Current Channel Group section). When switching between current channel groups, no additional settling time is required and the feature continues to monitor at an 8 kHz rate. If an overcurrent condition is detected on any of the selected current channels, the OI bit (Bit 17) of the STATUS1 register is set to 1. To determine the current channel(s) causing the overcurrent event, the OICHANNELx bits (Bit 3, Bit 4, and Bit 5) of the CHSTATUS register are used.

Setting the OVLVL and OILVL Registers

The content of the overvoltage (OVLVL) and overcurrent (OILVL), 24-bit, unsigned registers is compared to the absolute value of the voltage and current channels. The maximum value of these registers is 5,928,256 (0x5A7540) with full scale inputs. When either the OVLVL or OILVL register is equal to this value, the overvoltage or overcurrent conditions are never detected. Writing 0x0 to these registers signifies that the overvoltage or overcurrent conditions are continuously detected, and the corresponding interrupts are permanently triggered.

Overvoltage and Overcurrent Interrupts

Two interrupts are associated with the overvoltage and overcurrent features. The first interrupt is associated with the overvoltage feature; it is enabled by setting the OV bit (Bit 18) of the MASK1 register (Address 0xE50B). When this bit is set, an overvoltage condition causes the external $\overline{\text{IRQ1}}$ pin to be pulled low. A second interrupt is associated with the overcurrent detection feature. This interrupt is enabled by setting the OI bit (Bit 17) of the MASK1 register. When this bit is set, an overcurrent condition on any of the selected current channels causes the external $\overline{\text{IRQ1}}$ pin to be pulled low.

INDICATION OF POWER DIRECTION

The ADE7816 includes sign indication on the active and reactive power measurements. Sign indication allows positive and negative energy to be identified and billed separately, if required. It also helps detect a miswiring condition. This feature is available on three channels at a time. A group of current channels (A, B, C or D, E, F) must be selected by Bit 14 (CHANNEL_SEL) of the COMPMODE register at Address 0xE60E, Bit 6 (REVAPSEL) and Bit 7 (REVRPSEL) of the ACCMODE register at Address 0xE701 (see the Selecting a Current Channel Group section).

The three-sign indication bits that indicate the polarity of the active power are Bit 0 (W1SIGN), Bit 1 (W2SIGN), and Bit 2 (W3SIGN) of the CHSIGN register (Address 0xE617). W1SIGN indicates the direction of power on the A or D current channel, W2SIGN indicates the direction of power on the B or E current channel, and W3SIGN indicates the direction of power on the C or F current channel. An additional three bits, VAR1SIGN (Bit 4), VAR2SIGN (Bit 5), and VAR3SIGN (Bit 6), also in the CHSIGN register, provide the direction of the reactive power. All of these bits are unlatched and read only. A low reading (0) on any of these bits indicates that the corresponding power reading is positive; a high reading (1) indicates that the corresponding power reading is negative.

In addition to the sign indication bits, the ADE7816 also includes reverse power status bits and associated interrupts. The status bits are located in the STATUS0 register (Address 0xE502). The reverse power bits are set to 1 when the sign of the power changes. Bit 6 (REVAP1) monitors the A or D current channel, Bit 7 (REVAP2) monitors the B or E channel, and Bit 8 (REVAP3) monitors the C or F current channel. Similarly, Bit 10 (REVRP1), Bit 11 (REVRP2), and Bit 12 (REVRP3) monitor the reactive power. Both positive-to-negative and negative-to-positive changes result in the corresponding status bit being set. Each status bit has a corresponding interrupt enable bit that is located in the MASK0 register (Address 0xE50A). If the corresponding MASK0 bit is set, a change in active energy power direction causes the external $\overline{\text{IRQ0}}$ pin to be pulled low (see the Interrupts section for more details).

ANGLE MEASUREMENTS

The ADE7816 can measure the time delay between the current and voltage inputs. It can also be configured to measure the time between the six current channels. The negative to positive transitions identified by the zero-crossing detection circuit are used as a start and stop for the measurement (see Figure 35).

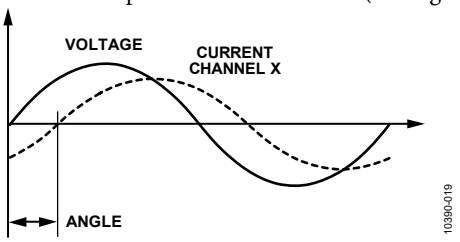


Figure 35. Voltage to Current Time Delay

There are three angle registers that store the results of the time delay. A group of current channels (A, B, C or D, E, F) must be selected by Bit 14 (CHANNEL_SEL) of the COMPMODE register (see the Selecting a Current Channel Group section).

When Bits[10:9] (ANGLESEL) of the COMPMODE register are set to 00b (default), the time delays between the current channels and the voltage channel are measured. The ANGLE0 register (Address 0xE601) stores the delay between the voltage and the A or D current channel. The ANGLE1 register (Address 0xE602) stores the delay between the voltage and the B or E current channel. The ANGLE2 register (Address 0xE603) stores the delay between the voltage and the C or F current channel. The time delay between the current and voltage inputs can be used to characterize how balanced the load is. The delays between phase voltages and currents can be used to compute the power factor, as shown in Equation 16.

$$\cos\theta_x = \cos\left(ANGLEx \times \frac{360^\circ \times f_{LINE}}{256\text{ kHz}}\right) \quad (16)$$

where f_{LINE} is 50 Hz or 60 Hz.

This method of determining the power factor does not take into account the effect of any harmonics.

When Bits[10:9] (ANGLESEL) of the COMPMODE register are set to 10b, the time delays (angles) between current channels are measured. Table 10 shows the current channel-to-channel delay measurements that are available.

Table 10. Available Channel-to-Channel Measurements (ANGLESEL = 10b)

CHANNEL_SEL (COMPMODE[14])	Channel-to-Channel Measurements		
	ANGLE0	ANGLE1	ANGLE2
0	A to B	A to C	B to C
1	A to E	D to F	E to F

The ANGLE0 (Address 0xE601), ANGLE1 (Address 0xE602), and ANGLE2 (Address 0xE603) registers are 16-bit, unsigned registers with 1 LSB corresponding to 3.90625 µs (256 kHz clock), which corresponds to a resolution of 0.0703° (360° × 50 Hz/256 kHz) for 50 Hz systems and 0.0843° (360° × 60 Hz/256 kHz) for 60 Hz systems.

PERIOD MEASUREMENT

The ADE7816 provides the period measurement of the line in the voltage channel. The period register (Address 0xE607) is a 16-bit, unsigned register that updates every line period. Due to internal filtering, a settling time of 30 ms to 40 ms is associated with this measurement.

The period measurement has a resolution of 3.90625 µs/LSB (256 kHz clock), which represents 0.0195% (50 Hz/256 kHz) when the line frequency is 50 Hz and 0.0234% (60 Hz/256 kHz) when the line frequency is 60 Hz. The value of the period register for 50 Hz networks is approximately 5120 (256 kHz/50 Hz) and for 60 Hz networks is approximately 4267 (256 kHz/60 Hz). The length of the register enables the measurement of line frequencies that are as low as 3.9 Hz (256 kHz/2^{16}). The period register is stable at ±1 LSB when the line is established, and the measurement does not change.

The following expressions can be used to compute the line period and frequency, using the period register:

$$T_L = \frac{PERIOD[15:0] + 1}{0\text{x}256\text{E}3}[\text{sec}] \quad (17)$$

$$f_L = \frac{0\text{x}256\text{E}3}{PERIOD[15:0] + 1}[\text{Hz}]$$

VOLTAGE SAG DETECTION

The ADE7816 includes a sag detection feature that warns the user when the absolute value of the line voltage falls below the programmable threshold for a programmable number of line cycles. This feature can provide an early warning signal that the line voltage is dropping out. The voltage sag feature is controlled by two registers: SAGCYC (Address 0xE704) and SAGLVL (Address 0xE509). These registers control the sag period and the sag voltage threshold, respectively.

Sag detection is disabled by default and can be enabled by writing a nonzero value to both the SAGCYC and SAGLVL registers. If either register is set to 0, the sag feature is disabled. If a voltage sag condition occurs, the sag bit (Bit 16) in the STATUS1 register (Address 0xE503) is set to 1.

SETTING THE SAGCYC REGISTER

The 8-bit, unsigned SAGCYC register contains the programmable sag period. The sag period is the number of half line cycles below which the voltage channel must remain before a sag condition occurs. Each LSB of the SAGCYC register corresponds to a half line cycle period. The SAGCYC register holds a maximum value of 255.

At 50 Hz, the maximum sag cycle time is 2.55 seconds.

$$\left(\frac{1}{50} \div 2\right) \times 255 = 2.55\text{ sec}$$

At 60 Hz, the maximum sag cycle time is 2.125 seconds.

$$\left(\frac{1}{60} \div 2\right) \times 255 = 2.125\text{ sec}$$

If the SAGCYC value is modified after the feature is enabled, the new SAGCYC period is effective immediately. Therefore, it is possible for a sag event to be caused by a combination of sag cycle periods. To prevent any overlap, the SAGLVL register should be reset to 0 to effectively disable the feature before the new cycle value is written to the SAGCYC register.

SETTING THE SAGLVL REGISTER

The content of the 24-bit SAGLVL register is compared to the absolute value of the output from the HPF. Writing 5,928,256 (0x5A7540) to the SAGLVL register sets the sag detection level at full scale. This results in the sag event triggering continuously. Writing 0x00 or 0x01 puts the sag detection level at 0; therefore, the sag event is never triggered.

VOLTAGE SAG INTERRUPT

The ADE7816 includes an interrupt that is associated with the voltage sag detection feature. If this interrupt is enabled, a voltage sag event causes the external $\overline{\text{IRQ1}}$ pin to go low. This interrupt is disabled by default and can be enabled by setting the sag bit (Bit 16) in the MASK1 register, Address 0xE50B (see the Interrupts section).

CHECKSUM

The ADE7816 has a 32-bit checksum register (Address 0xE51F) that ensures that certain important configuration registers maintain their desired value during normal operation.

The registers that are included in this feature are MASK0, MASK1, COMPMODE, gain, CONFIG, MMODE, ACCMODE, LCYCMODE, HSDC_CFG, plus four additional 16-bit reserved registers and six 8-bit reserved internal registers. All reserved registers always have default values. The ADE7816 computes the cyclic redundancy check (CRC) based on the IEEE802.3 standard. The registers are introduced, one by one, into a linear feedback shift register (LFSR) based generator, starting with the least significant bit (as shown in Figure 36). The 32-bit result is written in the checksum register. After power-up or a hardware/software reset, the CRC is computed on the default values of the registers. The default value of the checksum register is 0x33666787.

Figure 37 shows how the LFSR works. The MASK0, MASK1, COMPMODE, gain, CONFIG, MMODE, ACCMODE, LCYCMODE, and HSDC_CFG registers, along with the four 16-bit reserved registers and six 8-bit reserved internal registers, form the Bits[a_{255}, a_{254}, …, a_0] used by the LFSR. Bit a_0 is the least significant bit of the first internal register to enter the LFSR; Bit a_{255} is the most significant bit of the MASK0 register, the last register to enter the LFSR. The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where i = 0, 1, 2, …, 31, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{31} is the most significant bit.

g_i, where i = 0, 1, 2, …, 31 is the coefficient of the generating polynomial defined by the IEEE802.3 standard as follows:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (18)$$

$$g_0 = g_1 = g_2 = g_4 = g_5 = g_7 = 1$$
$$g_8 = g_{10} = g_{11} = g_{12} = g_{16} = g_{22} = g_{26} = g_{31} = 1 \quad (19)$$

All of the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{31}(j-1) \quad (20)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (21)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, ..., 31 \quad (22)$$

Equation 20, Equation 21, and Equation 22 must be repeated for j = 1, 2, …, 256. The value written into the checksum register contains Bit $b_i(256)$, i = 0, 1, …, 31. After the bits from the reserved internal register pass through the LFSR, the value of the CRC (which is obtained at Step j = 48) is 0x33660787.

Two different approaches can be followed in using the checksum register. One is to compute the CRC, based on Equation 18 to Equation 22, and then compare the value against the checksum register. Another is to periodically read the checksum register. If two consecutive readings differ, it can be assumed that one of the registers has changed value and that, therefore, the ADE7816 configuration has changed. The recommended response is to initiate a hardware/software reset that sets the values of all registers (including the reserved ones) to the default, and then reinitialize the configuration registers.

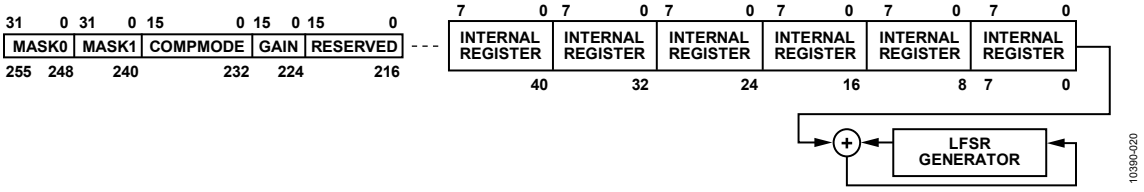


Figure 36. Checksum Register Calculation

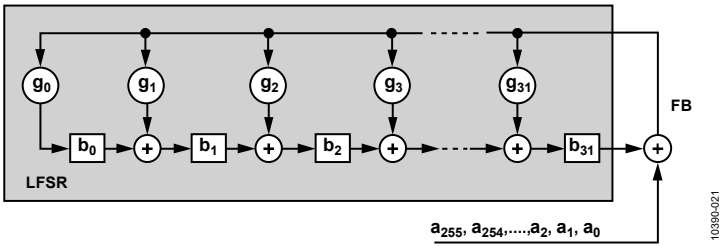


Figure 37. LFSR Generator Used in Checksum Register Calculation

LAYOUT GUIDELINES

Figure 38 shows a schematic of the ADE7816 with the following surrounding circuitry: decoupling capacitors at the VDD pin, the AVDD pin, the DVDD pin, the $REF_{IN/OUT}$ pin, the 16.384 MHz crystal, and the corresponding load capacitors. The rest of the pins are dependent on the application and are not shown in Figure 38.

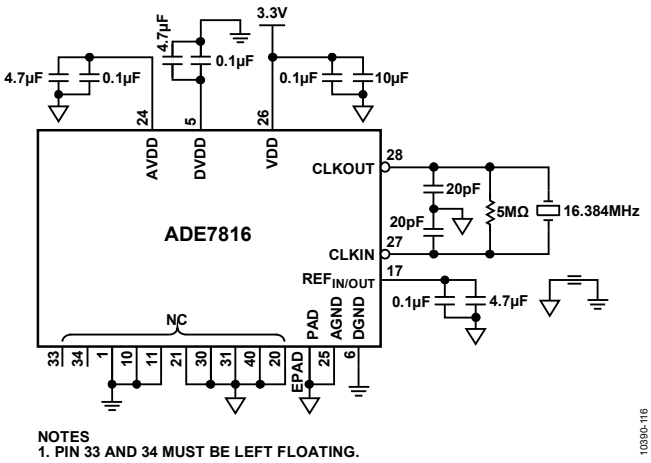


Figure 38. Crystal and Capacitors Connection

Figure 39 shows the recommended layout for optimal performance of a printed circuit board (PCB) with two layers of components placed on the top of the board. Following the layout guidelines shown in Figure 38 helps create a low noise design with higher resistance to EMC influences.

The VDD pin, AVDD pin, DVDD pin, and $REF_{IN/OUT}$ pin each have two decoupling ceramic capacitors. One capacitor is of the µF order and the other capacitor is of 220 nF or 100 nF order. Place these ceramic capacitors as close as possible to the ADE7816 to decouple high frequency noises and place the ceramic capacitor with the smaller value nearer to the pins of the ADE7816. The ceramic capacitor with the higher value must then be placed next to the capacitor with the lower value. This layout results in the 220 nF/100 nF capacitors being closer to the pins than the µF order capacitor.

For the crystal circuit, place the crystal load capacitors as close as possible to the CLKIN and CLKOUT pins.

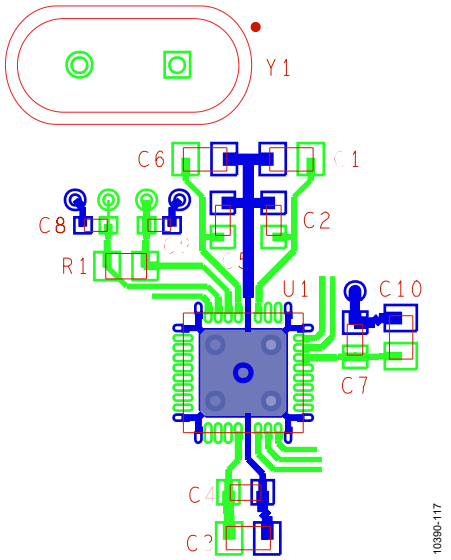


Figure 39. Recommended Decoupling Capacitors Layout

The exposed pad of the ADE7816 is soldered to an equivalent pad on the PCB. The AGND and DGND traces of the ADE7816 are then routed directly into the PCB pad. The bottom layer is mainly composed of a ground plane surrounding the crystal traces.

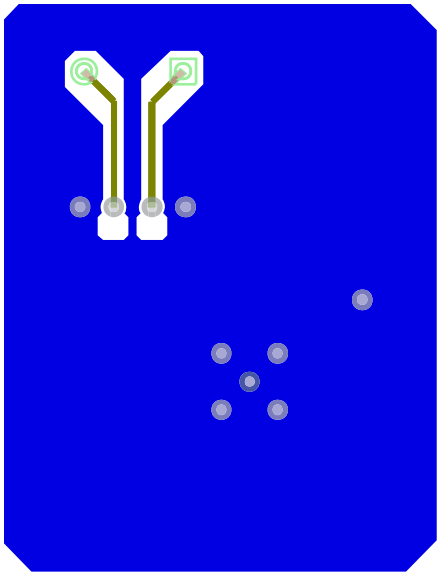


Figure 40. Bottom Layer Printed Circuit Board

CRYSTAL CIRCUIT

A 16.384 MHz digital clock signal can be provided to the CLKIN pin of the ADE7816. Alternatively, attach a crystal of the specified frequency (16.384 MHz) as shown in Figure 41. CL_1 and CL_2 denote the capacitances of the ceramic capacitors attached to the crystal pins, whereas CP_1 and CP_2 denote the parasitic capacitances on those crystal pins. The recommended, total capacitance value at each clock pin, CLKIN and CLKOUT, is 24 pF, which means that the following equation is true:

$$\text{Total Capacitance} = CP_1 + CL_1 = CP_2 + CL_2 = 24 \text{ pF}$$

Crystal manufacturer data sheets specify the crystal load capacitance value. A total capacitance of 24 pF is recommended per clock pin so select a crystal with a 12 pF load capacitance. In addition, when selecting the capacitance of the ceramic capacitors, CL_1 and CL_2, users must consider the parasitic capacitances, CP_1 and CP_2, on the crystal pins of the IC. As a result, the values of CL_1 and CL_2 must be based on the following equation:

$$CL_1 = CL_2 = 2 \times \text{Crystal Load Capacitance} - CP_1$$

where $CP_1 = CP_2$ and the crystal load capacitance is the value defined in the crystal manufacturer data sheets.

For example, if a 12 pF crystal is chosen and the parasitic capacitances on the clock pins are $CP_1 = CP_2 = 2$ pF, the capacitance of ceramic capacitors that are used in the crystal circuit are $CL_1 = CL_2 = 22$ pF.

A recommended crystal is VM6-1D11C12-TR-16.384MHZ with a maximum drive level 1 mW, a maximum effective series resistance (ESR) 20 Ω, and a load capacitance 12 pF. It is recommended to select this crystal or a crystal with similar specifications. Lower ESR and load capacitance values and higher drive level capability values of the crystal are preferable. It is also recommended to attach a 5 MΩ resistor in parallel to the crystal, as shown in Figure 41.

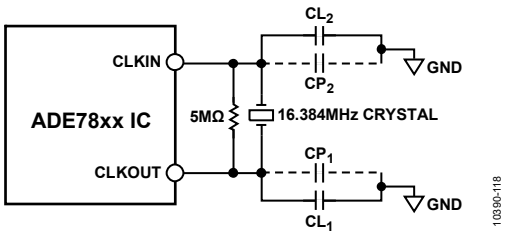


Figure 41. Crystal Circuit

OUTPUTS

This section describes the outputs from the ADE7816.

INTERRUPTS

The ADE7816 has two interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. Each pin is managed by a 32-bit interrupt mask register, MASK0 and MASK1 (Address 0xE50A and Address 0xE50B), respectively. To enable an interrupt, a bit in the MASKx register must be set to 1. To disable an interrupt, the bit must be cleared to 0. Two 32-bit status registers, STATUS0 and STATUS1 (Address 0xE502 and Address 0xE503, respectively), are associated with the interrupts. When an interrupt event occurs in the ADE7816, the corresponding flag in the interrupt status register is set to a Logic 1 (see Table 30 and Table 31). If the mask bit for this interrupt in the interrupt mask register is Logic 1, the $\overline{\text{IRQx}}$ logic output goes active low. The flag bits in the interrupt status register are set, irrespective of the state of the mask bits. To determine the source of the interrupt, the microcontroller must perform a read of the corresponding STATUSx register and identify which bit is set to 1. To erase the flag in the status register, write back to the STATUSx register with the flag set to 1. After an interrupt pin goes low, the status register is read and the source of the interrupt is identified. Then, the status register is written back, with no changes, to clear the status flag to 0. The $\overline{\text{IRQx}}$ pin remains low until the status flag is cancelled.

By default, all interrupts are disabled, with the exception of the RSTDONE interrupt. This interrupt can never be masked (disabled) and, therefore, Bit 15 (RSTDONE) in the MASK1 register does not have any functionality. The $\overline{\text{IRQ1}}$ pin always goes low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1 whenever a power-up or a hardware/software reset process ends. To cancel the RSTDONE status flag, the STATUS1 register nust be written with Bit 15 (RSTDONE) set to 1.

COMMUNICATION

Serial Interface Selection

After reset, the HSDC port is always disabled. Choose between the I²C and SPI ports by manipulating the $\overline{\text{SS}}$/HSA pin after power-up or after a hardware reset. If the $\overline{\text{SS}}$/HSA pin is held high, the ADE7816 uses the I²C port until a new hardware reset is executed. If the $\overline{\text{SS}}$/HSA pin is toggled high to low three times after power-up or after a hardware reset, the ADE7816 uses the SPI port until a new hardware reset is executed. This manipulation of the $\overline{\text{SS}}$/HSA pin can be accomplished in two ways. The first option is to use the $\overline{\text{SS}}$/HSA pin of the master device (that is, the microcontroller) as a regular I/O pin and toggle it three times. The second option is to execute three SPI write operations to a location in the address space that is not allocated to a specific ADE7816 register (such as Address 0xEBFF, where 8-bit writes can be executed).

These writes allow the $\overline{\text{SS}}$/HSA pin to toggle three times. See the SPI Write Operation section for details on the write protocol that is involved.

After the serial port choice is completed, it must be locked. If I²C is the active serial port, Bit 1 (I2C_LOCK) of the CONFIG2 register (Address 0xEC01) must be set to 1 to lock it in. From then on, the ADE7816 ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and an eventual switch to use of the SPI port is no longer possible. If the SPI is the active serial port, any write to the CONFIG2 register locks the port. From then on, a switch to the I²C port is no longer possible.

The functionality of the ADE7816 is accessible via several on-chip registers. The contents of these registers can be updated or read, using either the I²C or SPI interfaces. The HSDC port provides the instantaneous values of the voltages and current channels.

I²C-Compatible Interface

The ADE7816 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins, respectively, of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400 kHz.

The SDA and SCL pins are used for data transfer and are configured in a wire-AND'ed format that allows arbitration in a multimaster system.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

I²C Write Operation

The write operation, using the I²C interface of the ADE7816, initiated when the master generates a start condition, consists of one byte representing the address of the ADE7816, followed by the 16-bit address of the target register and by the value of the register.

The most significant seven bits of the address byte constitute the address of the ADE7816, which is 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a write operation, it must be cleared to 0; therefore, the first byte of the write operation is 0x70. After every byte is received, the ADE7816 generates an acknowledge. The register can be 8, 16, or 32 bits in length. After the last bit of the register is transmitted and the ADE7816 acknowledges the transfer, the master generates a stop condition. The addresses and the register content are sent with the most significant bit first. See Figure 43 for details of the I²C write operation.

I²C Read Operation

The read operation, using the I²C interface of the ADE7816, is accomplished in two stages. The first stage sets the pointer to the address of the register; the second stage reads the contents of the register (see Figure 44).

The first stage is initiated when the master generates a start condition. It consists of one byte, representing the address of the ADE7816, followed by the 16-bit address of the target register. The ADE7816 acknowledges every byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (see the I²C Write Operation section for details). After the last byte of the register address is sent and acknowledged by the ADE7816, the second stage begins with the master generating a new start condition, followed by an address byte. The most significant seven bits of this address byte constitute the address of the ADE7816, which is 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a read operation, it must be set to 1; therefore, the first byte of the read operation is 0x71. After this byte is received, the ADE7816 generates an acknowledge. Then the ADE7816 sends the value of the register, and, after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. Registers can be 8, 16, or 32 bits. After the last bit of the register is received, the master does not acknowledge the transfer but, instead, generates a stop condition.

SPI-Compatible Interface

The ADE7816 SPI is always a slave of the communication and consists of four pins (with dual functions): SCLK/SCL, MOSI/SDA, MISO/HSD, and $\overline{SS}$/HSA. The functions used in the SPI-compatible interface are SCLK, MOSI, MISO, and $\overline{SS}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt trigger input structure that allows the use of slow rising (and falling) clock edges. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7816 at the MOSI logic input on the falling edge of SCLK, and the ADE7816 samples it on the rising edge of SCLK. Data shifts out of the ADE7816 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum serial clock frequency that is supported by this interface is 2.5 MHz. MISO stays in high impedance when no data is transmitted from the ADE7816. Figure 42 shows details of the connection between the ADE7816 SPI and a master device containing a SPI interface.

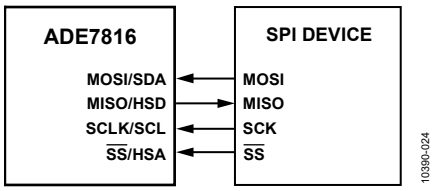


Figure 42. Connecting the ADE7816 SPI with a SPI Device

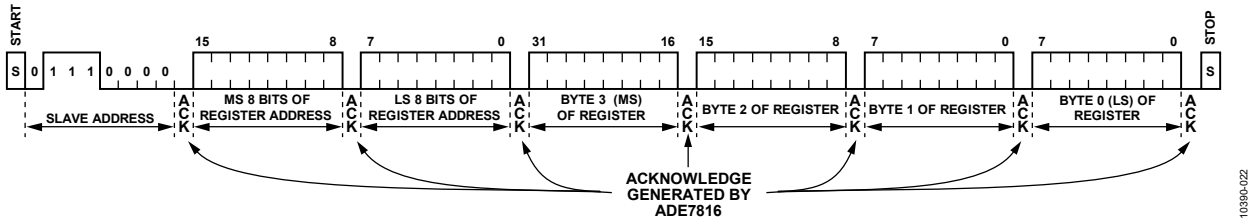


Figure 43. I²C Write Operation of a 32-Bit Register

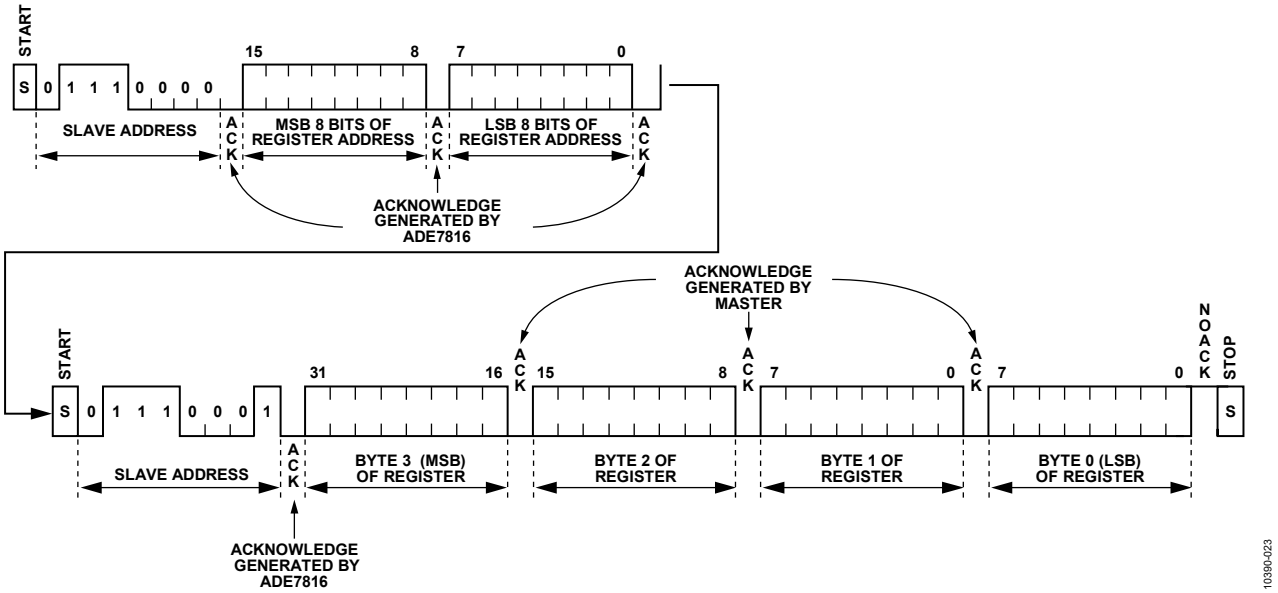


Figure 44. I²C Read Operation of a 32-Bit Register

The $\overline{SS}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. Drive the $\overline{SS}$ input low for the entire data transfer operation. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{SS}$ logic input to low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, the value of a register should be verified by reading it back each time it is written. The protocol is similar to the protocol used with the I²C interface.

SPI Read Operation

The read operation, using the SPI interface, initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7816, on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The ADE7816 SPI samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but, as good programming practice, they should be different from 0111000b, the seven bits used in the I²C protocol. Bit 0 (read/$\overline{write}$) of the address byte must be set to 1 for a read operation. Next, the master sends the 16-bit address of the register to be read. After the ADE7816 receives the last address bit of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit, it sets the $\overline{SS}$ and SCLK lines high, and the communication ends. The data lines, MOSI and MISO, go into a high impedance state (see Figure 45).

SPI Write Operation

The write operation, using the SPI interface, initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7816, on the MOSI line. The master sets data on the MOSI line, starting with the first high-to-low transition of SCLK. The SPI samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but, as a good programming practice, they should be different from 0111000b, the seven bits that are used in the I²C protocol. Bit 0 (read/$\overline{write}$) of the address byte must be 0 for a write operation. Next, the master sends the 16-bit address of the register that is written and the 32-, 16-, or 8-bit value of that register without losing any SCLK cycle. After the last bit is transmitted, the master sets the $\overline{SS}$ and SCLK lines high at the end of the SCLK cycle and the communication ends. The data lines, MOSI and MISO, go into a high impedance state (see Figure 46).

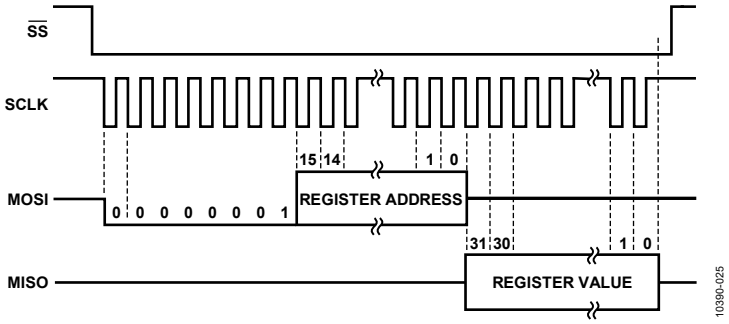


Figure 45. SPI Read Operation of a 32-Bit Register

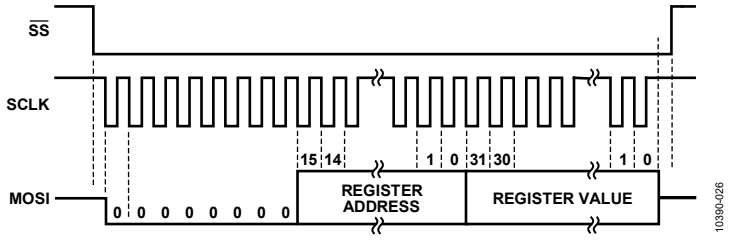


Figure 46. SPI Write Operation of a 32-Bit Register

HSDC Interface

The high speed data capture (HSDC) interface is disabled by default. It can be used only if the ADE7816 is configured with an I²C interface. The ADE7816 SPI interface cannot be used simultaneously with the HSDC port.

Bit 6 (HSDCEN) in the CONFIG register (Address 0xE618) activates HSDC when set to 1. If the HSDCEN bit is cleared to 0, the default value, the HSDC interface is disabled. Setting the HSDCEN bit to 1 when the SPI is in use does not have any effect. The HSDC port is an interface for sending up to four 32-bit words to an external device (usually a microprocessor or a DSP). The words represent the instantaneous values of the currents and voltage. The registers that are transmitted are IAWV/IDWV, IBWV/IEWV, ICWV/IFWV, and VWV. All are 24-bit registers that are sign extended to 32 bits.

The HSDC port can be interfaced with the SPI or similar interfaces. HSDC is always a master of the communication and consists of three pins: HSA, HSD, and HSCLK. HSA represents the select signal. It stays active low or high when a word is transmitted, and it is usually connected to the select pin of the slave. HSD sends data to the slave, and it is usually connected to the data input pin of the slave. HSCLK is the serial clock line that is generated by the ADE7816, and it is usually connected to the serial clock input of the slave. Figure 47 shows the connections between the ADE7816 HSDC and slave devices containing a SPI interface.

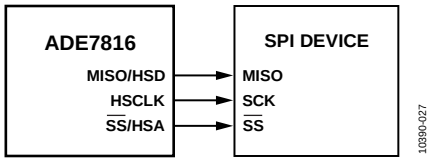


Figure 47. Connecting the ADE7816 HSDC with a SPI

The HSDC communication is managed by the HSDC_CFG register, Address 0xE706 (see Table 28). It is recommended that the HSDC_CFG register be set to the desired value before enabling the port, using Bit 6 (HSDCEN) in the CONFIG register. In this way, the state of various pins belonging to the HSDC port do not take levels that are inconsistent with the desired HSDC behavior. After a hardware reset or power-up, the MISO/HSD and $\overline{SS}$/HSA pins are set high.

Bit 0 (HCLK) in the HSDC_CFG register determines the serial clock frequency of the HSDC communication. When HCLK is 0 (the default value), the clock frequency is 8 MHz. When HCLK is 1, the clock frequency is 4 MHz. A bit of data is transmitted for every HSCLK high-to-low transition. The slave device that receives data from HSDC samples the HSD line on the low-to-high transition of HSCLK.

The words can be transmitted as 32-bit or 8-bit packages. When Bit 1 (HSIZE) in the HSDC_CFG register is 0 (the default value), the words are transmitted as 32-bit packages. When Bit HSIZE is 1, the registers are transmitted as 8-bit packages. The HSDC interface transmits the words MSB first.

When Bit 2 (HGAP) is set to 1, a gap of seven HSCLK cycles is introduced between packages. When the HGAP bit is cleared to 0 (the default value), no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication, and a data bit is placed on the HSD line with every HSCLK high-to-low transition.

For correct operation, Bits[4:3] (HXFER[1:0]) must be set to a value of 01b. The words representing the instantaneous values of currents and voltage are transmitted in the following order: IAWV/IDWV, VWV, IBWV/IEWV, VWV, ICVW/IFWV, and VWV, followed by one 32-bit word of all 0s. Note that the voltage waveform is sent three times. Bit 14 (CHANNEL_SEL) of the COMPMODE register (Address 0xE60E) can be used to select which group of current channels is transmitted (see the Selecting a Current Channel Group section).

Bit 5 (HSAPOL) of the HSDC_CFG register determines the HSA function polarity of the $\overline{SS}$/HSA pin during communication. When the HSAPOL bit is 0 (the default value), HSA is active low during the communication. This means that HSA stays high when no communication is in progress. When the communication starts, HSA goes low and stays low until the communication ends. Then it goes back to high. When HSAPOL is 1, the HSA function of the $\overline{SS}$/HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When the communication starts, HSA goes high and stays high until the communication ends; then it goes back to low.

Bits[7:6] of the HSDC_CFG register are reserved. Any value written into these bits has no consequence on HSDC behavior.

Figure 48 shows the HSDC transfer protocol for HGAP = 0, HXFER[1:0] = 01, and HSAPOL = 0. Note that the HSDC interface sets a data bit on the HSD line every HSCLK high-to-low transition, and the value of Bit HSIZE is irrelevant.

Figure 49 shows the HSDC transfer protocol for HSIZE = 0, HGAP = 1, HXFER[1:0] = 01, and HSAPOL = 0. Note that the HSDC interface introduces a gap of seven HSCLK cycles between every 32-bit word.

Figure 50 shows the HSDC transfer protocol for HSIZE = 1, HGAP = 1, HXFER[1:0] = 01, and HSAPOL = 0. Note that the HSDC interface introduces a gap of seven HSCLK cycles between every 8-bit word.

See Table 28 for the HSDC_CFG register and descriptions for the HCLK, HSIZE, HGAP, HXFER[1:0], and HSAPOL bits.

Table 11 lists the time that is required to execute an HSDC data transfer for all HSDC_CFG register settings.

Table 11. Communication Times for Various HSDC Settings

HXFER[1:0]	HGAP	HSIZE[1]	HCLK	Communication Time (µs)
01	0	N/A	0	28
01	0	N/A	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25

[1] N/A means not applicable.

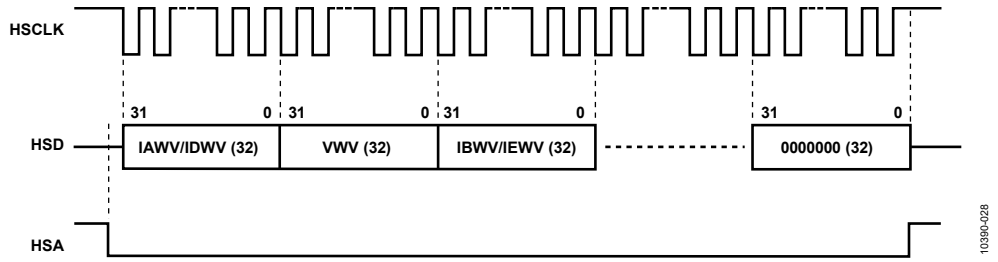


Figure 48. HSDC Communication for HGAP = 0, HXFER[1:0] = 01, and HSAPOL = 0; HSIZE Is Irrelevant

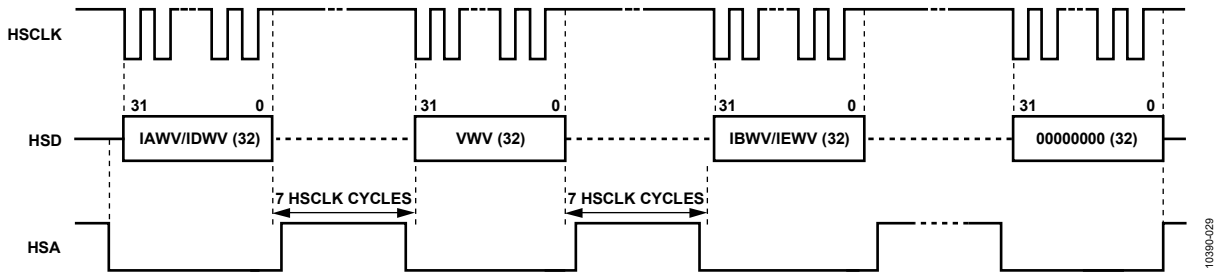


Figure 49. HSDC Communication for HSIZE = 0, HGAP = 1, HXFER[1:0] = 01, and HSAPOL = 0

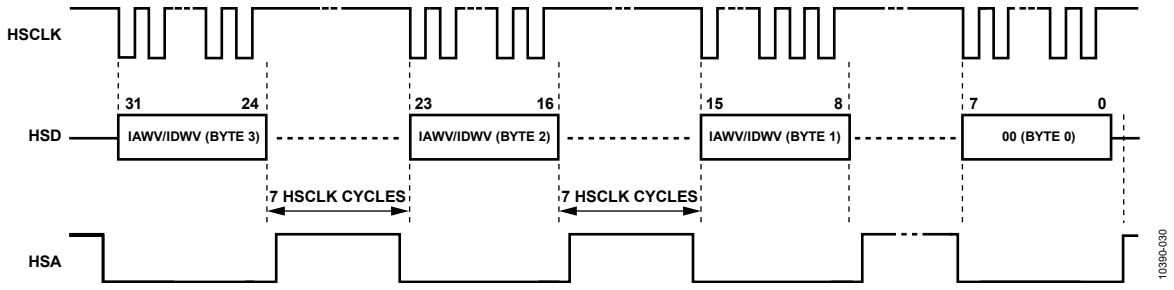


Figure 50. HSDC Communication for HSIZE = 1, HGAP = 1, HXFER[1:0] = 01, and HSAPOL = 0

REGISTERS

REGISTER PROTECTION

To protect the integrity of the data stored in the data memory (located at Address 0x4380 to Address 0x43BE), a write protection mechanism is available. By default, the protection is disabled, and registers that are located between Address 0x4380 and Address 0x43BE can be written without restriction. When the protection is enabled, no writes to these registers are allowed. Registers can always be read, without restriction, independent of the write protection state.

To enable the protection, write 0xAD to an internal 8-bit register that is located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.

It is recommended that the write protection be enabled before starting the DSP. If any register requires changing after this time, disable the protection, change the value, and then reenable the protection. There is no need to stop the DSP to change these registers.

To disable the protection, write 0xAD to an internal 8-bit register that is located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register that is located at Address 0xE7E3.

REGISTER FORMAT

The ADE7816 includes 8-, 16-, and 32-bit, signed and unsigned registers. All signed registers are in twos complement format. Some of the internal measurements are 24 bits long and have been extended to 32 bits prior to communication. This extension is accomplished in three different ways: sign extending (SE), zero padding (ZP), or zero padded and sign extended (ZPSE). When sign extending is used, the sign bit (Bit 23) of the twos complement signed number is duplicated in the uppermost byte prior to communication. Zero padding is achieved by writing 0s into the upper most byte prior to transmission. This format is used for unsigned numbers only. ZSPE formats are shown in Figure 51 and involve padding the most significant bits with 0s and sign extending Bits[27:24].

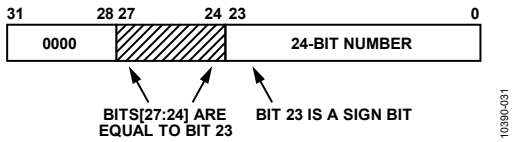


Figure 51. ZPSE Communication Format

The communication format of each register is specified in the Register Maps section (see Table 12 through Table 15).

REGISTER MAPS

Table 12. Calibration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	VGAIN	R/W	24	32 ZPSE	S	0x000000	Voltage gain adjustment.
0x4381	IAGAIN	R/W	24	32 ZPSE	S	0x000000	Current Channel A current gain adjustment.
0x4382	IBGAIN	R/W	24	32 ZPSE	S	0x000000	Current Channel B current gain adjustment.
0x4383	ICGAIN	R/W	24	32 ZPSE	S	0x000000	Current Channel C current gain adjustment.
0x4384	IDGAIN	R/W	24	32 ZPSE	S	0x000000	Current Channel D current gain adjustment.
0x4385	IEGAIN	R/W	24	32 ZPSE	S	0x000000	Current Channel E current gain adjustment.
0x4386	IFGAIN	R/W	24	32 ZPSE	S	0x000000	Current Channel F current gain adjustment.
0x4387	Reserved	R/W	24	32 ZPSE	S	0x000000	This register should be ignored.
0x4388	DICOEFF	R/W	24	32 ZPSE	S	0x000000	Register used in the digital integrator algorithm. When the integrator is enabled, this register should be set to 0xFFF8000.
0x4389	HPFDIS	R/W	24	32 ZPSE	S	0x000000	Disables the high-pass filter for all channels.
0x438A	VRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset.
0x438B	IARMSOS	R/W	24	32 ZPSE	S	0x000000	Current Channel A current rms offset.
0x438C	IBRMSOS	R/W	24	32 ZPSE	S	0x000000	Current Channel B current rms offset.
0x438D	ICRMSOS	R/W	24	32 ZPSE	S	0x000000	Current Channel C current rms offset.
0x438E	IDRMSOS	R/W	24	32 ZPSE	S	0x000000	Current Channel D current rms offset.
0x438F	IERMSOS	R/W	24	32 ZPSE	S	0x000000	Current Channel E current rms offset.
0x4390	IFRMSOS	R/W	24	32 ZPSE	S	0x000000	Current Channel F current rms offset.
0x4391	AWGAIN	R/W	24	32 ZPSE	S	0x000000	Channel A active power gain adjust.
0x4392	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Channel A active power offset adjust.
0x4393	BWGAIN	R/W	24	32 ZPSE	S	0x000000	Channel B active power gain adjust.
0x4394	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Channel B active power offset adjust.
0x4395	CWGAIN	R/W	24	32 ZPSE	S	0x000000	Channel C active power gain adjust.
0x4396	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Channel C active power offset adjust.
0x4397	DWGAIN	R/W	24	32 ZPSE	S	0x000000	Channel D active power gain adjust
0x4398	DWATTOS	R/W	24	32 ZPSE	S	0x000000	Channel D active power offset adjust.
0x4399	EWGAIN	R/W	24	32 ZPSE	S	0x000000	Channel E active power gain adjust.
0x439A	EWATTOS	R/W	24	32 ZPSE	S	0x000000	Channel E active power offset adjust.
0x439B	FWGAIN	R/W	24	32 ZPSE	S	0x000000	Channel F active power gain adjust.
0x439C	FWATTOS	R/W	24	32 ZPSE	S	0x000000	Channel F active power offset adjust.
0x439D	AVARGAIN	R/W	24	32 ZPSE	S	0x000000	Channel A reactive power gain adjust.
0x439E	AVAROS	R/W	24	32 ZPSE	S	0x000000	Channel A reactive power offset adjust.
0x439F	BVARGAIN	R/W	24	32 ZPSE	S	0x000000	Channel B reactive power gain adjust.
0x43A0	BVAROS	R/W	24	32 ZPSE	S	0x000000	Channel B reactive power offset adjust.
0x43A1	CVARGAIN	R/W	24	32 ZPSE	S	0x000000	Channel C reactive power gain adjust.
0x43A2	CVAROS	R/W	24	32 ZPSE	S	0x000000	Channel C reactive power offset adjust.
0x43A3	DVARGAIN	R/W	24	32 ZPSE	S	0x000000	Channel D reactive power gain adjust.
0x43A4	DVAROS	R/W	24	32 ZPSE	S	0x000000	Channel D reactive power offset adjust.
0x43A5	EVARGAIN	R/W	24	32 ZPSE	S	0x000000	Channel E reactive power gain adjust.
0x43A6	EVAROS	R/W	24	32 ZPSE	S	0x000000	Channel E reactive power offset adjust.
0x43A7	FVARGAIN	R/W	24	32 ZPSE	S	0x000000	Channel F reactive power gain adjust.
0x43A8	FVAROS	R/W	24	32 ZPSE	S	0x000000	Channel F reactive power offset adjust.
0x43A9	Reserved						This register should be ignored.
0x43AA	Reserved						This register should be ignored.
0x43AB	WTHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of the WTHR[47:0] threshold.
0x43AC	WTHR0	R/W	24	32 ZP	U	0x000000	Least significant 24 bits of the WTHR[47:0] threshold.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43AD	VARTHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of the VARTHR[47:0] threshold.
0x43AE	VARTHR0	R/W	24	32 ZP	U	0x000000	Least significant 24 bits of the VARTHR[47:0] threshold.
0x43AF	APNOLOAD	RW	24	32 ZP	U	0x000000	No load threshold in the active power datapath.
0x43B0	VARNOLOAD	R/W	24	32 ZPSE	S	0x000000	No load threshold in the reactive power datapath.
0x43B1	PCF_A_COEFF	R/W	24	32 ZPSE	U	0x000000	Phase calibration coefficient for Channel A. Set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.
0x43B2	PCF_B_COEFF	R/W	24	32 ZPSE	U	0x000000	Phase calibration coefficient for Channel B. Set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.
0x43B3	PCF_C_COEFF	R/W	24	32 ZPSE	U	0x000000	Phase calibration coefficient for Channel C. Set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.
0x43B4	PCF_D_COEFF	R/W	24	32 ZPSE	U	0x000000	Phase calibration coefficient for Channel D. Set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.
0x43B5	PCF_E_COEFF	R/W	24	32 ZPSE	U	0x000000	Phase calibration coefficient for Channel E. Set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.
0x43B6	PCF_F_COEFF	R/W	24	32 ZPSE	U	0x000000	Phase calibration coefficient for Channel F. Set to 0x400CA4 for a 50 Hz system and 0x401235 for a 60 Hz system.
0x43B7 to 0x43BF	Reserved	N/A	N/A	N/A	N/A	0x000000	These registers should be ignored.
0x43C0	VRMS	R	24	32 ZP	S	N/A	Voltage rms value.
0x43C1	IARMS	R	24	32 ZP	S	N/A	Current Channel A current rms value.
0x43C2	IBRMS	R	24	32 ZP	S	N/A	Current Channel B current rms value.
0x43C3	ICRMS	R	24	32 ZP	S	N/A	Current Channel C current rms value.
0x43C4	IDRMS	R	24	32 ZP	S	N/A	Current Channel D current rms value.
0x43C5	IERMS	R	24	32 ZP	S	N/A	Current Channel E current rms value.
0x43C6	IFRMS	R	24	32 ZP	S	N/A	Current Channel F current rms value.
0x43C7 to 0x43FF	Reserved						These registers should be ignored.

[1] R is read, and W is write.
[2] For more information, see the Register Format section.
[3] U indicates an unsigned register, and S indicates a signed register in twos complement format.

Table 13. Run Register

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE228	Run	R/W	16	16	U	0x0000	This register starts and stops the DSP.

[1] R is read, and W is write.
[2] U indicates an unsigned register.

Table 14. Billable Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Channel A active energy accumulation.
0xE401	BWATTHR	R	32	32	S	0x00000000	Channel B active energy accumulation.
0xE402	CWATTHR	R	32	32	S	0x00000000	Channel C active energy accumulation.
0xE403	DWATTHR	R	32	32	S	0x00000000	Channel D active energy accumulation.
0xE404	EWATTHR	R	32	32	S	0x00000000	Channel E active energy accumulation.
0xE405	FWATTHR	R	32	32	S	0x00000000	Channel F active energy accumulation.
0xE406	AVARHR	R	32	32	S	0x00000000	Channel A reactive energy accumulation.
0xE407	BVARHR	R	32	32	S	0x00000000	Channel B reactive energy accumulation.
0xE408	CVARHR	R	32	32	S	0x00000000	Channel C reactive energy accumulation.
0xE409	DVARHR	R	32	32	S	0x00000000	Channel D reactive energy accumulation.
0xE40A	EVARHR	R	32	32	S	0x00000000	Channel E reactive energy accumulation.
0xE40B	FVARHR	R	32	32	S	0x00000000	Channel F reactive energy accumulation.

[1] R is read, and W is write.
[2] S indicates a signed register in twos complement format.

Table 15. Configuration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE500	IPEAK	R	32	32	U	N/A	Current peak register.
0xE501	VPEAK	R	32	32	U	N/A	Voltage peak register.
0xE502	STATUS0	R/W	32	32	U	N/A	Interrupt Status Register 0.
0xE503	STATUS1	R/W	32	32	U	N/A	Interrupt Status Register 1.
0xE504	Reserved	R	20	32 ZP	U	N/A	This register should be ignored.
0xE505	Reserved	R	20	32 ZP	U	N/A	This register should be ignored.
0xE506	Reserved	R	20	32 ZP	U	N/A	This register should be ignored.
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage sag level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0.
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1.
0xE50C	IAWV/IDWV	R	24	32 SE	S	N/A	Instantaneous Current Channel A and Instantaneous Current Channel D.
0xE50D	IBWV/IEWV	R	24	32 SE	S	N/A	Instantaneous Current Channel B and Instantaneous Current Channel E.
0xE50E	ICWV/IFWV	R	24	32 SE	S	N/A	Instantaneous Current Channel C and Instantaneous Current Channel F.
0xE50F	Reserved	R	24	32 SE	S	N/A	This register should be ignored.
0xE510	VWV	R	24	32 SE	S	N/A	Instantaneous voltage.
0xE511 to 0xE51E	Reserved	R	24	32 SE	S	N/A	This register should be ignored.
0xE51F	Checksum	R	32	32	U	0x33666787	Checksum verification (see the Checksum section for details).
0xE520 to 0xE52E	Reserved						These registers should be ignored.
0xE600	CHSTATUS	R	16	16	U	N/A	Channel peak register.
0xE601	ANGLE0	R	16	16	U	N/A	Time Delay 0 (see the Angle Measurements section for details).
0xE602	ANGLE1	R	16	16	U	N/A	Time Delay 1 (see the Angle Measurements section for details).
0xE603	ANGLE2	R	16	16	U	N/A	Time Delay 2 (see the Angle Measurements section for details).
0xE604 to 0xE606	Reserved						These registers should be ignored.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE607	Period	R	16	16	U	N/A	Line period.
0xE608	CHNOLOAD	R	16	16	U	N/A	Channel no load register.
0xE609 to 0xE60B	Reserved						For proper operation, do not write to these addresses.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation mode register.
0xE60F	Gain	R/W	16	16	U	0x0000	PGA gains at ADC inputs (see Table 22).
0xE610 to 0xE616	Reserved						This register should be ignored.
0xE617	CHSIGN	R	16	16	U	N/A	Power sign register.
0xE618	CONFIG	R/W	16	16	U	0x0000	Configuration register.
0xE700	MMODE	R/W	8	8	U	0x1C	Measurement mode register.
0xE701	ACCMODE	R/W	8	8	U	0x00	Accumulation mode register.
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode.
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.
0xE704	SAGCYC	R/W	8	8	U	0x00	Sag detection half line cycles.
0xE705	Reserved						This register should be ignored.
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register.
0xE707	Version	R/W	8	8	U		Version of die.
0xE7E3	Reserved	R/W	8	8	U	0x00	Register protection (see the Register Protection section).
0xE7FE	Reserved						Register protection key (see the Register Protection section).
0xEBFF	Reserved		8	8			This address can be used in manipulating the $\overline{SS}$/HSA pin when SPI is chosen as the active port (see the Communication section for details).
0xEC00	Reserved						This register should be ignored.
0xEC01	CONFIG2	R/W	8	8	U	0x00	Configuration register (see Table 29).

[1] R is read, and W is write.
[2] 32 ZP is a 24- or 20-bit, signed or unsigned register that is transmitted as a 32-bit word with 8 or 12 MSBs, respectively, padded with 0s. 32 SE is a 24-bit, signed register that is transmitted as a 32-bit word that is sign extended to 32 bits.
[3] U indicates an unsigned register, and S indicates a signed register in twos complement format.
[4] N/A is not applicable.

REGISTER DESCRIPTIONS

Table 16. HPFDIS Register (Address 0x4389)

Bits	Default Value	Description
[23:0]	0x000000	When HPFDIS = 0x000000, all high-pass filters in voltage and current channels are enabled. When the register is set to any nonzero value, all high-pass filters are disabled.

Table 17. IPEAK Register (Address 0xE500)

Bits	Bit Name	Default Value	Description
[31:27]	Reserved	0x00000	These bits should be ignored.
26	IPCHANNEL2	0x0	The C or F current channel generated the IPEAKVAL[23:0] value.
25	IPCHANNEL1	0x0	The B or E current channel generated the IPEAKVAL[23:0] value.
24	IPCHANNEL0	0x0	The A or D current channel generated the IPEAKVAL[23:0] value.
[23:0]	IPEAKVAL[23:0]	0x0	Current channel peak value

Table 18. VPEAK Register (Address 0xE501)

Bits	Bit Name	Default Value	Description
[31:24]	Reserved	0x00000	These bits should be ignored.
[23:0]	VPEAKVAL[23:0]	0x0	Voltage channel peak value.

Note that Address 0xE502, Address 0xE503, Address 0xE50A, and Address 0xE50B are listed in Table 30 and Table 31.

Table 19. CHSTATUS Register (Address 0xE600)

Bits	Bit Name	Default Value	Description
[15:6]	Reserved	0x000	These bits should be ignored.
5	OICHANNEL2	0x0	The C or F current channel generated the overcurrent event.
4	OICHANNEL1	0x0	The B or E current channel generated the overcurrent event.
3	OICHANNEL0	0x0	The A or D current channel generated the overcurrent event.
[2:0]	Reserved	0x000	Reserved. These bits are always 0.

Table 20. CHNOLOAD Register (Address 0xE608)

Bits	Bit Name	Default Value	Description
[15:6]	Reserved	0x0000000	These bits should be ignored.
5	NOLOADF	0x0	0: Channel F is out of the no load condition. 1: Channel F is in the no load condition.
4	NOLOADE	0x0	0: Channel E is out of the no load condition. 1: Channel E is in the no load condition.
3	NOLOADD	0x0	0: Channel D is out of the no load condition. 1: Channel D is in the no load condition.
2	NOLOADC	0x0	0: Channel C is out of the no load condition. 1: Channel C is in the no load condition.
1	NOLOADB	0x0	0: Channel B is out of the no load condition. 1: Channel B is in the no load condition.
0	NOLOADA	0x0	0: Channel A is out of the no load condition. 1: Channel A is in the no load condition.

Table 21. COMPMODE Register (Address 0xE60E)

Bits	Bit Name	Default Value	Description
15	Reserved	0x0	This bit should be ignored.
14	CHANNEL_SEL	0x0	0: the A, B, and C current channels are used for the peak, overcurrent, zero crossing, angle, and waveform measurements. 1: the D, E, and F current channels are used for the peak, overcurrent, zero crossing, angle, and waveform measurements.
[13:11]	Reserved	0x0	These bits should be ignored.
[10:9]	ANGLESEL	0x00	00: the time delays between the voltage and currents are measured. 01: reserved. 10: the angles between current channels are measured. 11: no angles are measured.
[8:0]	Reserved	0x1FF	These bits should be ignored and not modified.

Table 22. Gain Register (Address 0xE60F)

Bits	Bit Name	Default Value	Description
[15:9]	Reserved	0x0000000	These bits should be ignored.
[8:6]	PGA3[2:0]	0x000	Gain selection for the D, E, and F current channels. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved.

Bits	Bit Name	Default Value	Description
[5:3]	PGA2[2:0]	0x000	Voltage channel gain selection. 000: gain = 1 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved.
[2:0]	PGA1[2:0]	0x000	Gain selection for the A, B, and C current channels. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved.

Table 23. CHSIGN Register (Address 0xE617)

Bits	Bit Name	Default Value	Description
[15:7]	Reserved	0x0000000	These bits should be ignored.
6	VAR3SIGN	0x0	0: the reactive power on the C or F channel is positive. 1: the reactive power on the C or F channel is negative.
5	VAR2SIGN	0x0	0: the reactive power on the B or E channel is positive. 1: the reactive power on the B or E channel is negative.
4	VAR1SIGN	0x0	0: the reactive power on the A or D channel is positive. 1: the reactive power on the A or D channel is negative.
3	Reserved	0x0	This bit should be ignored.
2	W3SIGN	0x0	0: the active power on the C or F channel is positive. 1: the active power on the C or F channel is negative.
1	W2SIGN	0x0	0: the active power on the B or E channel is positive. 1: the active power on the B or E channel is negative.
0	W1SIGN	0x0	0: the active power on the A or D channel is positive. 1: the active power on the A or D channel is negative.

Table 24. CONFIG Register (Address 0xE618)

Bits	Bit Name	Default Value	Description
[15:8]	Reserved	0x0	These bits should be ignored.
7	SWRST	0x0	Initiates a software reset.
6	HSDCEN	0x0	Enables the HSDC serial port.
[5:1]	Reserved	0x0	These bits should be ignored.
0	INTEN	0x0	Enables the digital integrator.

Table 25. MMODE Register (Address 0xE700)

Bits	Bit Name	Default Value	Description
[7:5]	Reserved	0x000	These bits should be ignored.
4	PEAKSEL2	0x1	The C or F current channel is selected for peak detection.
3	PEAKSEL1	0x1	The B or E current channel is selected for peak detection.
2	PEAKSEL0	0x1	The A or D current channel is selected for peak detection.
[1:0]	Reserved	0x00	These bits should be ignored.

Table 26. ACCMODE Register (Address 0xE701)

Bits	Bit Name	Default Value	Description
7	REVRPSEL	0x0	0: the sign of the reactive power is monitored on the A, B, and C channels. 1: the sign of the reactive power is monitored on the D, E, and F channels. Bit 14 (CHANNEL_SEL) of COMPMODE must be set to the same current channels.
6	REVAPSEL	0x0	0: the sign of the active power is monitored on the A, B, and C channels. 1: the sign of the active power is monitored on the D, E, and F channels. Bit 14 (CHANNEL_SEL) of COMPMODE must be set to the same current channels.
[5:4]	Reserved	0x00	These bits should be ignored and not modified.
[3:2]	VARACC[1:0]	0x00	00: signed accumulation for all reactive power measurements. 01: reserved. 10: reserved. 11: reserved.
[1:0]	WATTACC[1:0]	0x00	00: signed accumulation for all active power measurements. 01: reserved. 10: reserved. 11: reserved.

Table 27. LCYCMODE Register (Address 0xE702)

Bits	Bit Name	Default Value	Description
7	Reserved	0x0	Reserved. This bit does not control any functionality.
6	RSTREAD	0x1	Enables read-with-reset for all energy registers. Note that this bit has no function in line cycle accumulation mode and should be set to 0 when this mode is in use.
[5:4]	Reserved	0x0	These bits should be ignored.
3	ZX_SEL	0x0	Enables the voltage channel zero-crossing counter for line cycle accumulation mode.
2	Reserved	0x0	These bits should be ignored.
1	LVAR	0x0	Enables the reactive energy line cycle accumulation mode.
0	LWATT	0x0	Enables the active energy line cycle accumulation mode.

Table 28. HSDC_CFG Register (Address 0xE706)

Bits	Bit Name	Default Value	Description
[7:6]	Reserved	0x00	These bits should be ignored.
5	HSAPOL	0x0	0: $\overline{SS}$/HSA output pin is active low (default). 1: $\overline{SS}$/HSA output pin is active high.
[4:3]	HXFER[1:0]	0x00	00 = reserved. 01 = HSDC transmits current and voltage waveform data. 10 = reserved. 11 = reserved.
2	HGAP	0x0	0: no gap is introduced between packages (default). 1: a gap of seven HCLK cycles is introduced between packages.
1	HSIZE	0x0	0: HSDC transmits the 32-bit registers in 32-bit packages, most significant bit first (default). 1: HSDC transmits the 32-bit registers in 8-bit packages, most significant bit first.
0	HCLK	0x0	0: HSCLK = 8 MHz (default). 1: HSCLK = 4 MHz.

Table 29. CONFIG2 Register (Address 0xEC01)

Bits	Bit Name	Default Value	Description
[7:2]	Reserved	0x0	These bits should be ignored.
1	I2C_LOCK	0x0	Serial port lock.
0	EXTREFEN	0x0	Set to 1 to use with an external reference.

Interrupt Enable and Interrupt Status Registers

Table 30. STATUS0 Register (Address 0xE502) and MASK0 Register (Address 0xE50A)

Bits	Bit Name	Default Value	Description
[31:18]	Reserved	0 0000 0000 0000	These bits should be ignored.
17	DREADY	0x0	New waveform data is ready.
16	Reserved	0x0	This bit should be ignored.
15	Reserved	0x0	This bit should be ignored.
14	Reserved	0x0	This bit should be ignored.
13	Reserved	0x0	This bit should be ignored.
12	REVRP3	0x0	The sign of the reactive power has changed (C or F channel).
11	REVRP2	0x0	The sign of the reactive power has changed (B or E channel).
10	REVRP1	0x0	The sign of the reactive power has changed (A or D channel).
9	Reserved	0x0	This bit should be ignored.
8	REVAP3	0x0	The sign of the active power has changed (C or F channel).
7	REVAP2	0x0	The sign of the active power has changed (B or E channel).
6	REVAP1	0x0	The sign of the active power has changed (A or D channel).
5	LENERGY	0x0	The end of a line cycle accumulation period.
4	Reserved	0x0	This bit should be ignored.
3	REHF2	0x0	The active energy register is half full (D, E, or F channel).
2	REHF1	0x0	The reactive energy register is half full (A, B, or C channel).
1	AEHF2	0x0	The active energy register is half full (D, E, or F channel)
0	AEHF1	0x0	The active energy register is half full (A, B, or C channel).

Table 31. STATUS1 Register (Address 0xE503) and MASK1 Register (Address 0xE50B)

Bits	Bit Name	Default Value	Description
[31:25]	Reserved	0x0000000	These bits should be ignored.
24	PKV	0x0	The end of the voltage channel peak detection period.
23	PKI	0x0	The end of the current channel peak detection period.
22	Reserved	0x0	This bit should be ignored.
21	Reserved	0x1	This bit should be ignored.
20	Reserved	0x0	This bit should be ignored.
19	Reserved	0x0	This bit should be ignored.
18	OV	0x0	An overvoltage event has occurred.
17	OI	0x0	An overcurrent event has occurred.
16	Sag	0x0	A sag event has occurred.
15	RSTDONE	0x1	The end of a software or hardware reset.
14	ZXI3	0x0	C or F current channel zero crossing.
13	ZXI2	0x0	B or E current channel zero crossing.
12	ZXI1	0x0	A or D current channel zero crossing.
11	Reserved	0x0	This bit should be ignored.
10	Reserved	0x0	This bit should be ignored.
9	ZXV	0x0	Voltage channel zero crossing.
8	ZXTOI3	0x0	A zero crossing on the C or F current channel is missing.
7	ZXTOI2	0x0	A zero crossing on the B or E current channel is missing.
6	ZXTOI1	0x0	A zero crossing on the A or D current channel is missing.
5	Reserved	0x0	This bit should be ignored.
4	Reserved	0x0	This bit should be ignored.
3	ZXTOV	0x0	A zero crossing on the voltage channel is missing.
2	Reserved	0x0	This bit should be ignored.
1	NLOAD2	0x0	Active and reactive no load condition on the D, E, or F current channel.
0	NLOAD1	0x0	Active and reactive no load condition on the A, B, or C current channel.

OUTLINE DIMENSIONS

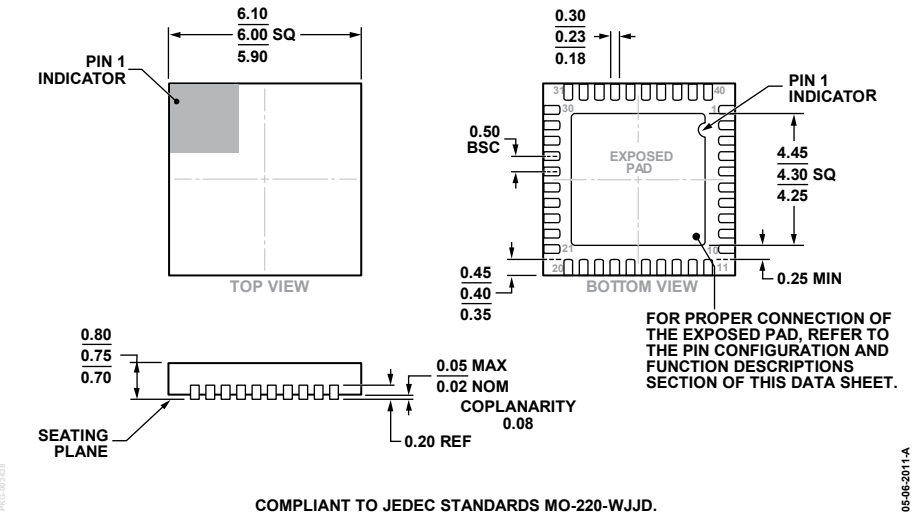


Figure 52. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE7816ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-10
ADE7816ACPZ-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-10
EVAL-ADE7816EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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