

NPIC6C596A

Power logic 8-bit shift register; open-drain outputs

Rev. 2 — 26 June 2020

Product data sheet

1. General description

The NPIC6C596A is an 8-bit serial-in/serial or parallel-out shift register with a storage register and open-drain outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset MR input. A LOW on MR resets both the shift register and storage register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. To provide additional hold time in cascaded applications, the serial output QS7 is clocked out on the falling edge of SHCP. Data in the storage register drives the gate of the output extended-drain NMOS (EDNMOS) transistor whenever the output enable input (\overline{OE}) is LOW. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the registers.

The open-drain outputs are 33 V/100 mA continuous current extended-drain NMOS transistors designed for use in systems that require moderate load power such as LEDs. Integrated voltage clamps in the outputs provide protection against inductive transients. These voltage clamps make the device suitable for power driver applications such as relays, solenoids and other low-current or medium-voltage loads.

2. Features and benefits

- Specified from -40 °C to +125 °C
- Wide supply range 2.3 V to 5.5 V
- Low R_{DSon}
- Eight Power EDNMOS transistor outputs of 100 mA continuous current
- 250 mA current limit capability
- Output clamping voltage 33 V
- 30 mJ avalanche energy capability
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption
- ESD protection:
 - HBM JDS-001 Class 2 exceeds 2500 V
 - CDM JESD22-C101E exceeds 1000 V

3. Applications

- LED sign
- Graphic status panel
- Fault status indicator

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|--------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| NPIC6C596AD | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| NPIC6C596APW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| NPIC6C596ABQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

5. Functional diagram

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aaa-002548

Fig. 1. Logic symbol

aaa-002550

Fig. 2. Functional diagram

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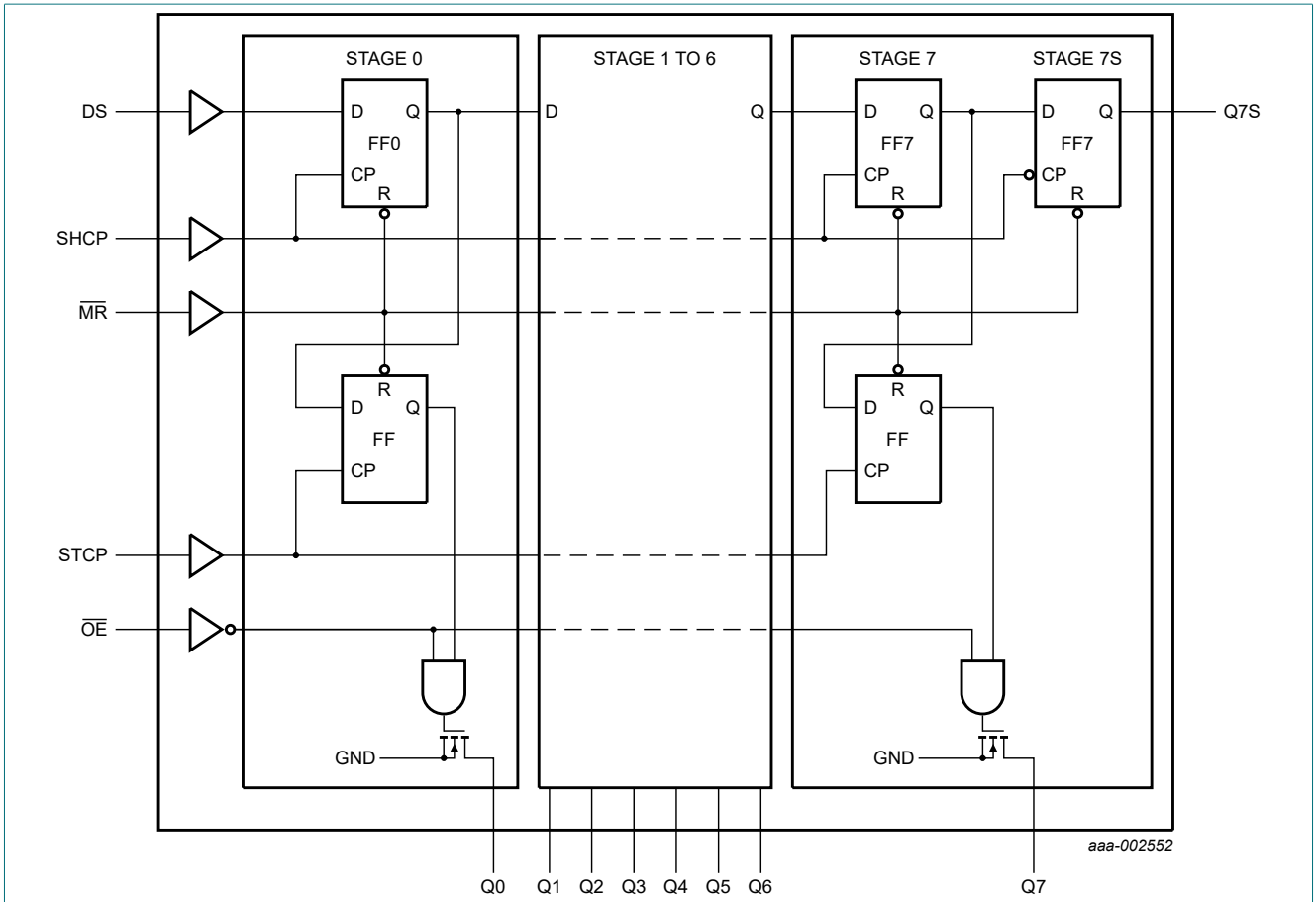


Fig. 5. Logic diagram

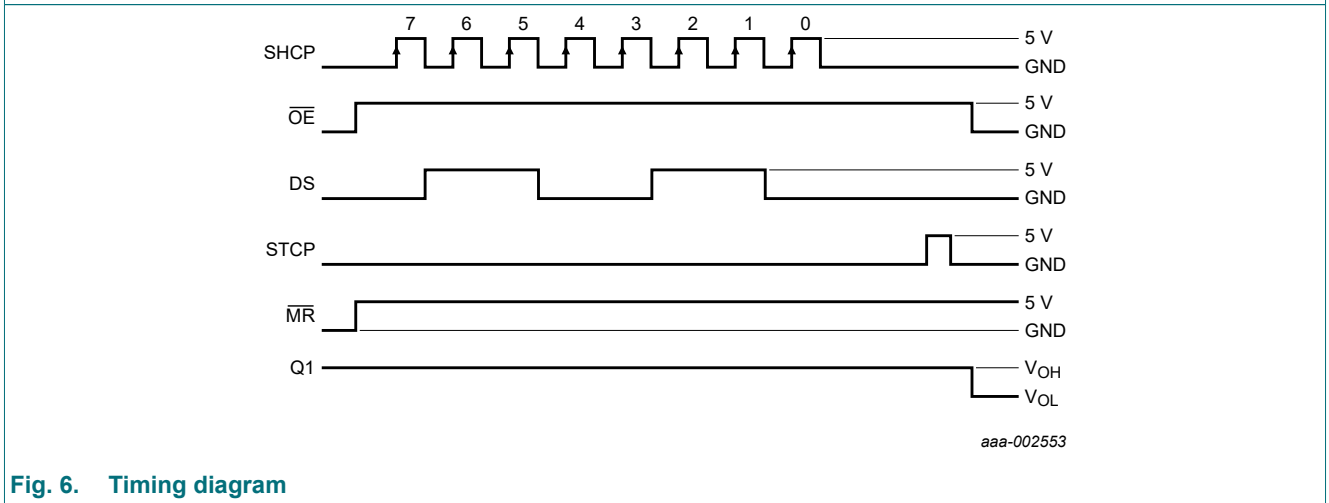
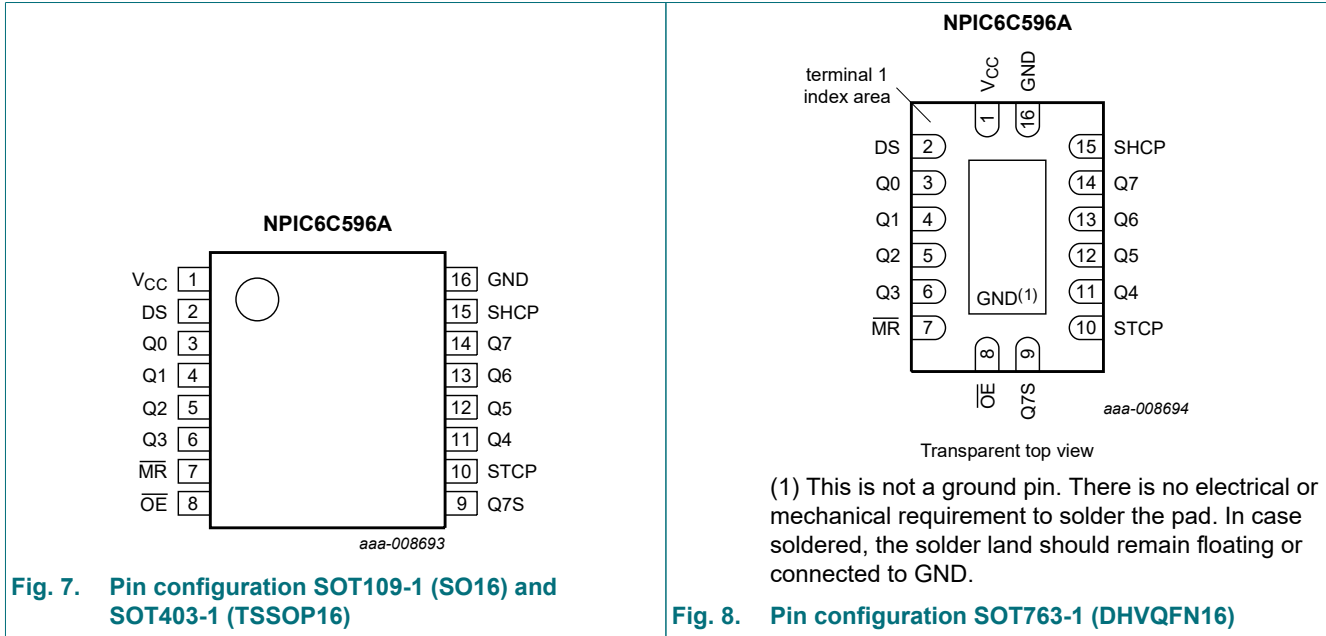


Fig. 6. Timing diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|----------------------------|-----------------------------------|
| V _{CC} | 1 | supply voltage |
| DS | 2 | serial data input |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 3, 4, 5, 6, 11, 12, 13, 14 | parallel data output (open-drain) |
| MR | 7 | master reset (active LOW) |
| OE | 8 | output enable input (active LOW) |
| Q7S | 9 | serial data output |
| STCP | 10 | storage register clock input |
| SHCP | 15 | shift register clock input |
| GND | 16 | ground (0 V) |

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------|---------------------------------|---|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.3 | +7.0 | V |
| V_{DS} | drain-source voltage | power EDNMOS drain-source voltage [1] | - | +33 | V |
| $I_{d(SD)}$ | source-drain diode current | continuous | - | 250 | mA |
| | | pulsed [2] | - | 500 | mA |
| I_D | drain current | $T_{amb} = 25\text{ °C}$ | | | |
| | | continuous; each output; all outputs on | - | 100 | mA |
| | | pulsed; each output; all outputs on [2] | - | 250 | mA |
| I_{DM} | peak drain current | single output; $T_{amb} = 25\text{ °C}$ [2] | - | 250 | mA |
| E_{AS} | non-repetitive avalanche energy | single pulse; see Fig. 9 [3] | - | 30 | mJ |
| I_{AL} | avalanche current | see Fig. 9 [3] | - | 200 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = 25\text{ °C}$ [4] | | | |
| | | SO16 | - | 800 | mW |
| | | TSSOP16 | - | 725 | mW |
| | | DHVQFN16 | - | 1825 | mW |
| | | $T_{amb} = 125\text{ °C}$ [4] | | | |
| | | SO16 | - | 160 | mW |
| | | TSSOP16 | - | 145 | mW |
| | | DHVQFN16 | - | 365 | mW |

[1] Each power EDNMOS source is internally connected to GND.

[2] Pulse duration $\leq 100\text{ }\mu\text{s}$ and duty cycle $\leq 2\%$.

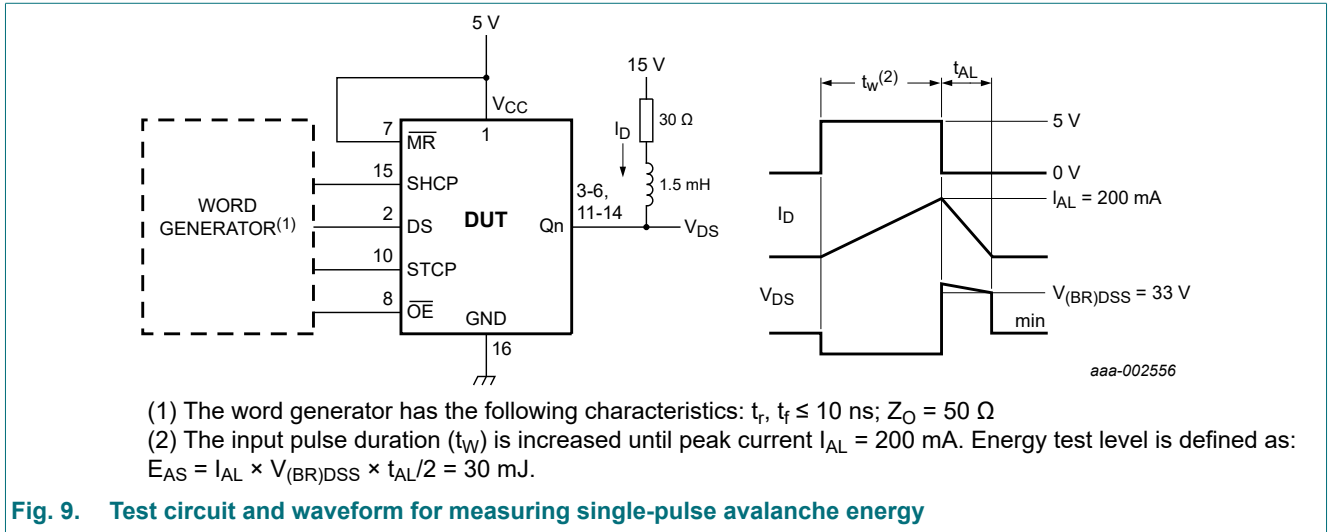
[3] $V_{DS} = 15\text{ V}$; starting junction temperature (T_J) = 25 °C ; $L = 1.5\text{ H}$; avalanche current (I_{AL}) = 200 mA .

[4] For SO16 packages: above 25 °C the value of P_{tot} derates linearly with 6.4 mW/°C .

For TSSOP16 packages: above 25 °C the value of P_{tot} derates linearly with 5.8 mW/°C .

For DHVQFN16 packages: above 25 °C the value of P_{tot} derates linearly with 14.6 mW/°C .

7.1. Test circuit and waveform



8. Recommended operating conditions

Table 4. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|---|-----|-----|------|------------------|
| V_{CC} | supply voltage | | 2.3 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| I_D | drain current | pulsed drain output current; $V_{CC} = 5 \text{ V}$; [1] [2] $T_{amb} = 25 \text{ }^\circ\text{C}$; all outputs on | - | - | 250 | mA |
| T_{amb} | ambient temperature | | -40 | - | +125 | $^\circ\text{C}$ |

- [1] Pulse duration $\leq 100 \mu\text{s}$ and duty cycle $\leq 2 \%$.
- [2] Technique should limit $T_j - T_{amb}$ to $10 \text{ }^\circ\text{C}$ maximum.

9. Static characteristics

Table 5. Static characteristics

At recommended operating conditions unless otherwise specified. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | $T_{amb} = 25 \text{ }^\circ\text{C}$ | | | Unit |
|----------|---------------------------|--|---------------------------------------|---------|--------------|---------------|
| | | | Min | Typ [1] | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$ | $0.85V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$ | - | - | $0.15V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | serial data output Q7S; $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = -20 \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$ | 2.64 | 4.49 | - | V |
| V_{OL} | LOW-level output voltage | serial data output Q7S; $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = 20 \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$ | - | 0.005 | 0.12 | V |
| I_I | input leakage current | $V_{CC} = 5.5 \text{ V}$; $V_I = V_{CC}$ | - | - | 1 | μA |
| | | $I_O = 4 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$ | - | 0.3 | 0.6 | V |

Power logic 8-bit shift register; open-drain outputs

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | Unit |
|----------------------|----------------------------------|--|--------------------------|---------|-----|------|
| | | | Min | Typ [1] | Max | |
| V _{(BR)DSS} | drain-source breakdown voltage | I _D = 1 mA | 33 | 37 | - | V |
| V _{SD} | source-drain voltage | diode forward voltage; I _F = 100 mA | - | 0.85 | 1.2 | V |
| I _{CC} | supply current | logic supply current; V _{CC} = 5.5 V; V _I = V _{CC} or GND | | | | |
| | | all outputs off | - | 0.004 | 200 | μA |
| | | all outputs on [2] | - | 0.006 | 500 | μA |
| | | all outputs off; SHCP = 5 MHz; C _L = 30 pF; see Fig. 14 and Fig. 16 | - | 0.75 | 5 | mA |
| I _{O(nom)} | nominal output current | V _{DS} = 0.5 V; T _{amb} = 85 °C; I _{out} = I _D [3] [4] [5] | - | 140 | - | mA |
| I _{DSX} | drain cut-off current | V _{CC} = 5.5 V; V _{DS} = 30 V | - | 0.002 | 0.2 | μA |
| | | V _{CC} = 5.5 V; V _{DS} = 30 V; T _{amb} = 125 °C | - | 0.15 | 0.3 | μA |
| R _{DSon} | drain-source on-state resistance | see Fig. 17 and Fig. 18 [3] [4] | | | | |
| | | V _{CC} = 3.0 V; I _D = 50 mA | - | 3.0 | 11 | Ω |
| | | V _{CC} = 3.0 V; I _D = 50 mA; T _{amb} = 125 °C | | 5.4 | 14 | Ω |
| | | V _{CC} = 3.0 V; I _D = 100 mA | - | 3.1 | 12 | Ω |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5.0 V.

[2] Output currents below 250 mA current limit.

[3] Technique should limit T_j - T_{amb} to 10 °C maximum.

[4] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

[5] Nominal output current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_{amb} = 85 °C.

10. Dynamic characteristics

Table 6. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit, see Figure 14.

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | Unit |
|------------------|------------------------------------|--|--------------------------|---------|-----|------|
| | | | Min | Typ [1] | Max | |
| t _{PLH} | LOW to HIGH propagation delay | \overline{OE} to Qn; I _D = 75 mA; see Fig. 10 and Fig. 19 | - | 97 | - | ns |
| t _{PHL} | HIGH to LOW propagation delay | \overline{OE} to Qn; I _D = 75 mA; see Fig. 10 and Fig. 19 | - | 9 | - | ns |
| t _r | rise time | \overline{OE} to Qn; I _D = 75 mA; see Fig. 10 and Fig. 19 | - | 60 | - | ns |
| t _f | fall time | \overline{OE} to Qn; I _D = 75 mA; see Fig. 10 and Fig. 19 | - | 18 | - | ns |
| t _{pd} | propagation delay | SHCP to Q7S; I _D = 75 mA; see Fig. 11 [2] | - | 5 | - | ns |
| f _{max} | maximum frequency | SHCP; I _D = 75 mA; see Fig. 11 [3] | - | - | 10 | MHz |
| t _{rr} | reverse recovery time | I _F = 100 mA; dI/dt = 10 A/μs; see Fig. 13 [4] [5] | - | 120 | - | ns |
| t _a | reverse recovery current rise time | I _F = 100 mA; dI/dt = 10 A/μs; see Fig. 13 [4] [5] | - | 100 | - | ns |
| t _{su} | set-up time | DS to SHCP; see Fig. 12 | 15 | - | - | ns |
| t _h | hold time | DS to SHCP; see Fig. 12 | 15 | - | - | ns |
| t _W | pulse width | | 40 | - | - | ns |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5.0 V.

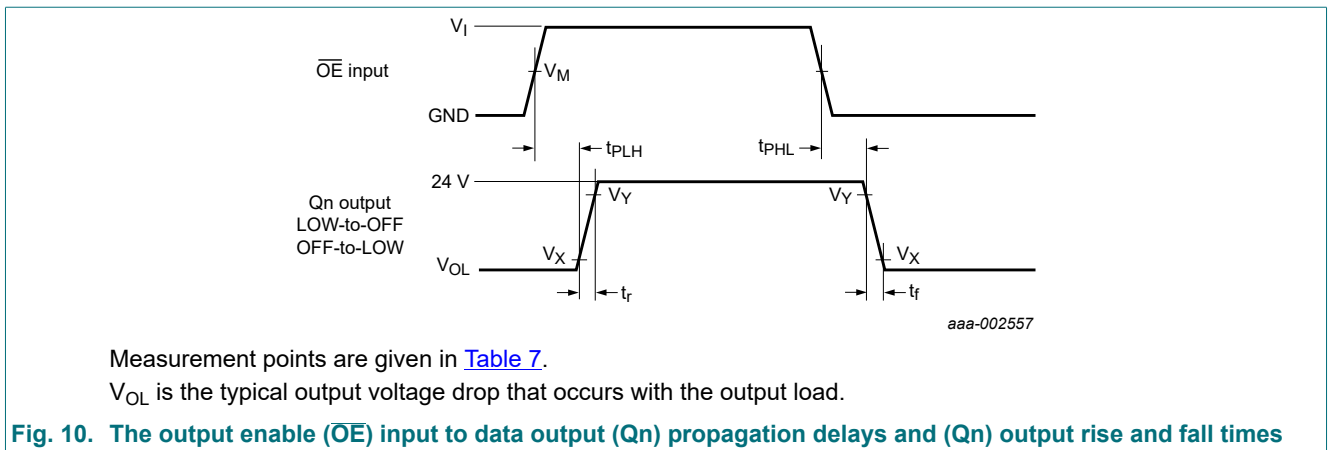
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

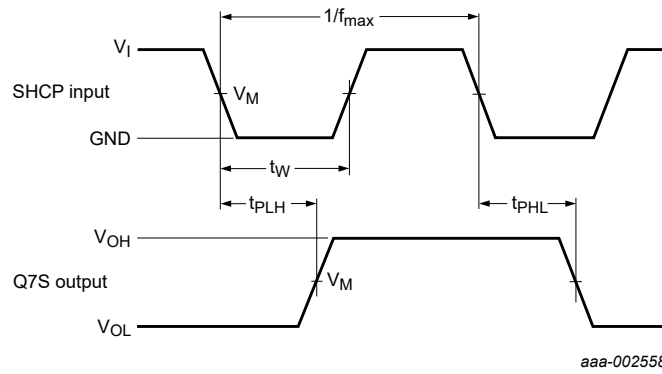
[3] This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SHCP → Q7S propagation delay and setup time plus some timing margin.

[4] Technique should limit T_J - T_{amb} to 10 °C maximum.

[5] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

10.1. Test circuits and waveforms





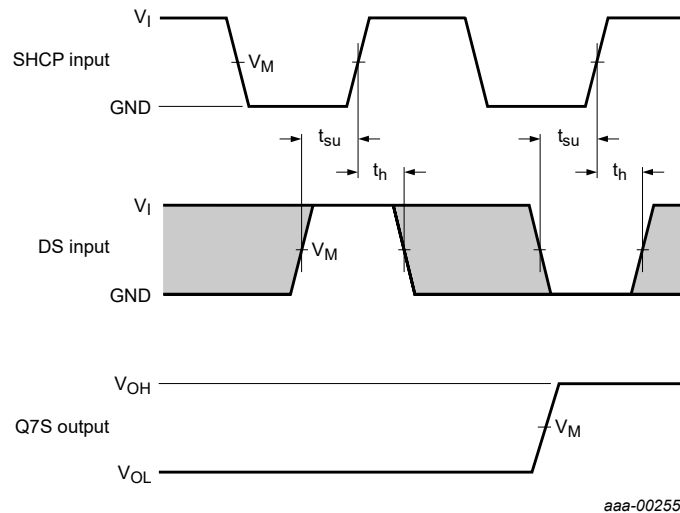
Measurement points are given in [Table 7](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 11. The shift clock (SHCP) to serial data output (Q7S) propagation delays with the minimum shift clock pulse width and maximum shift clock frequency

Table 7. Measurement points

| Supply voltage | Input | Output | | |
|----------------|-------------|-------------|-------------|-------------|
| V_{CC} | V_M | V_M | V_X | V_Y |
| 5 V | $0.5V_{CC}$ | $0.5V_{DS}$ | $0.1V_{DS}$ | $0.9V_{DS}$ |



Measurement points are given in [Table 8](#).

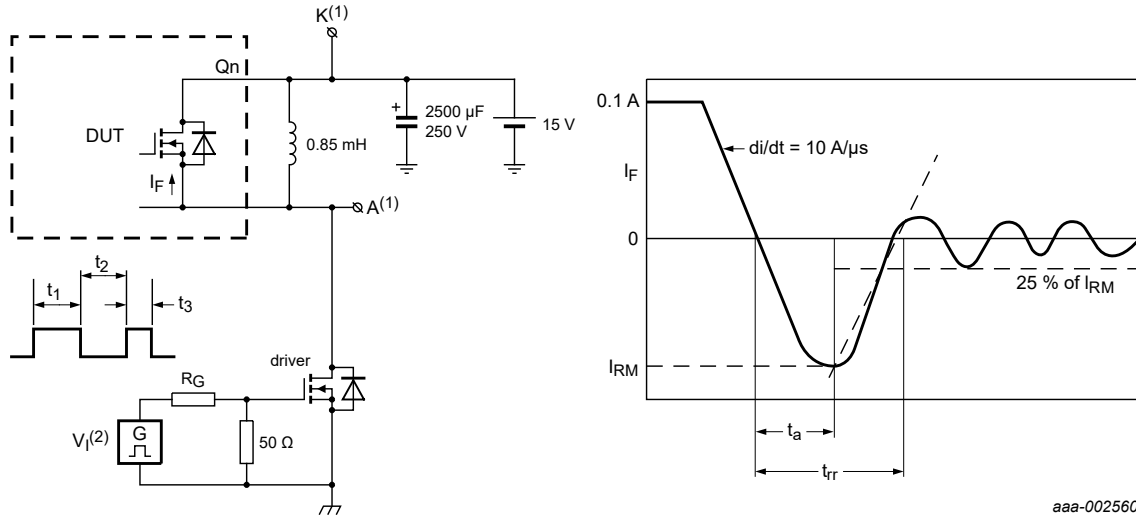
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 12. The data set-up and hold times for the serial data input (DS)

Table 8. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{CC} | V_M | V_M |
| 5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |



aaa-002560

(1) The open-drain Qn terminal under test is connected to testpoint K. All other terminals are connected together and connected to testpoint A.

(2) The V_1 amplitude and R_G are adjusted for $di/dt = 10 \text{ A}/\mu\text{s}$. A V_1 double-pulse train is used to set $I_F = 0.1 \text{ A}$, where $t_1 = 10 \mu\text{s}$, $t_2 = 7 \mu\text{s}$ and $t_3 = 3 \mu\text{s}$.

Fig. 13. Test circuit and waveform for measuring reverse recovery current

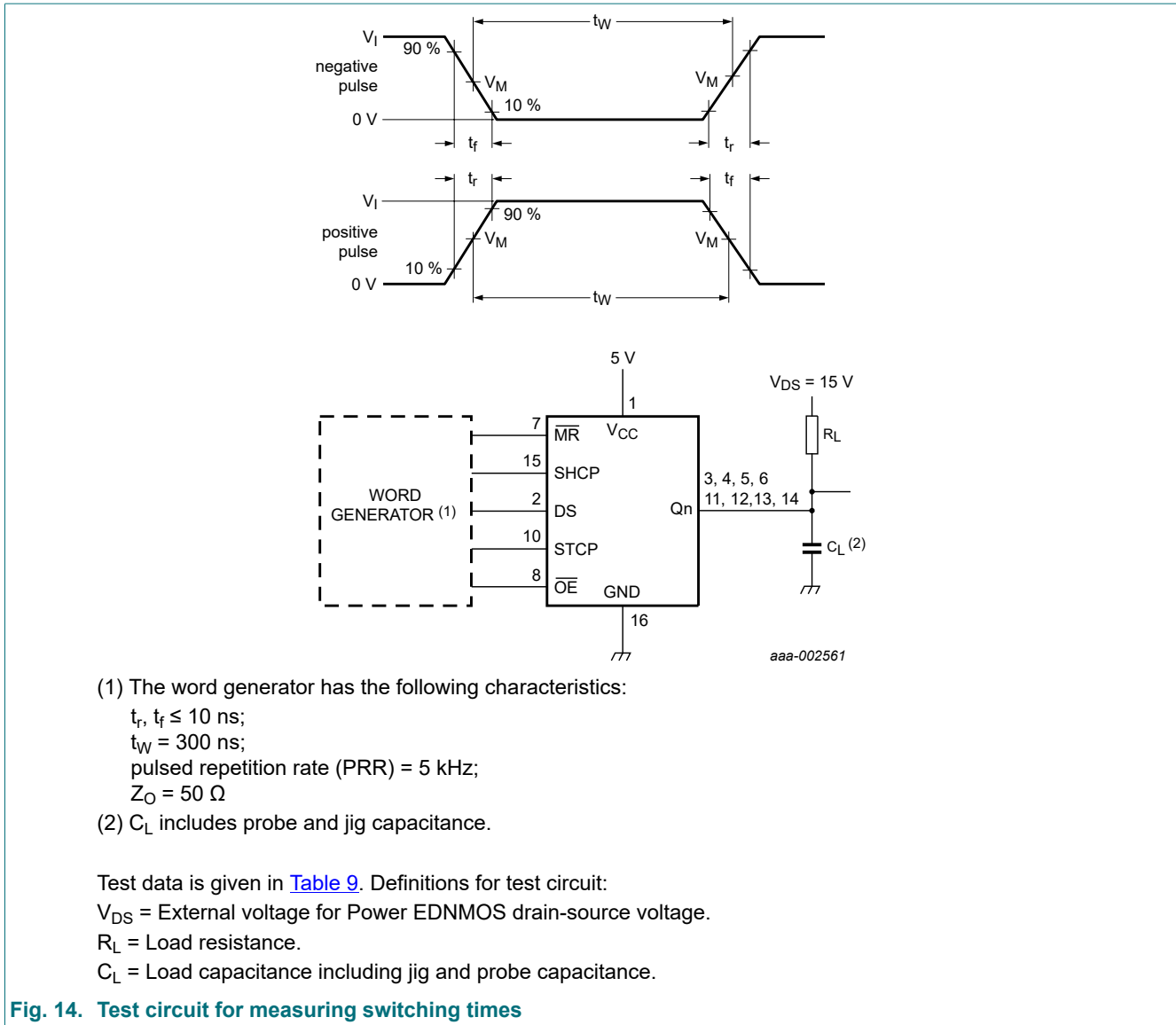


Fig. 14. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | | Load | |
|----------------|-------|----------------------|-------|-------|--------------|
| | V_I | t_r, t_f | V_M | C_L | R_L |
| 5 V | 5 V | $\leq 10 \text{ ns}$ | 50% | 30 pF | 200 Ω |

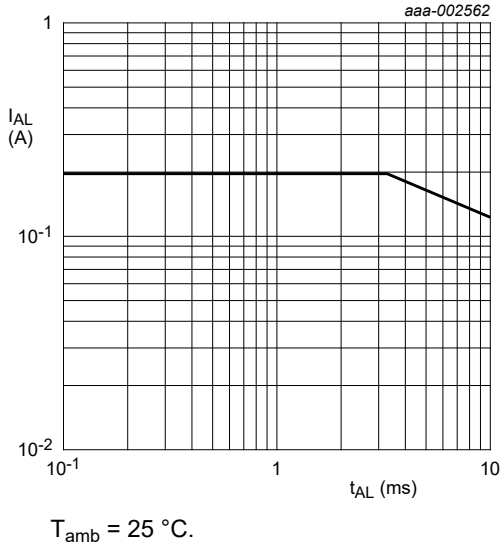


Fig. 15. Avalanche current (peak) versus time duration of avalanche

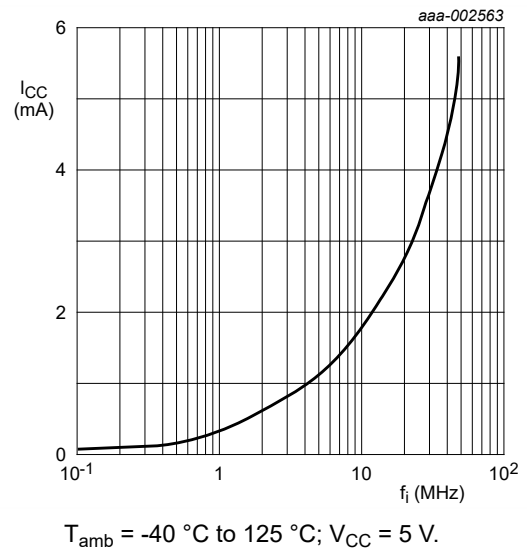


Fig. 16. Supply current versus frequency

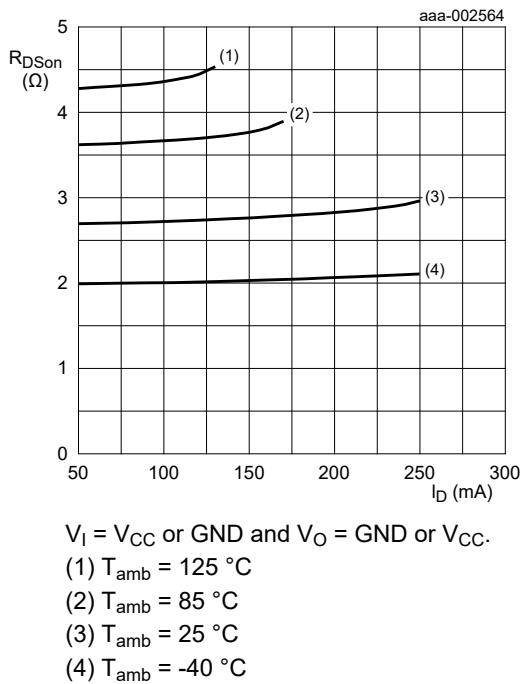


Fig. 17. Drain-source on-state resistance versus drain current

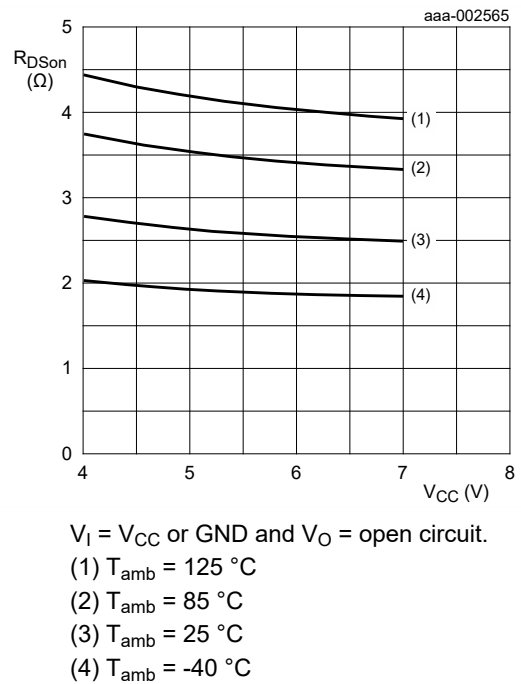
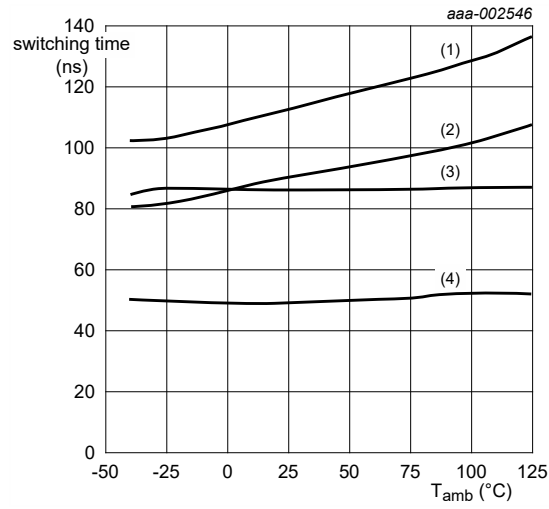


Fig. 18. Static drain-source on-state resistance versus supply voltage



Technique should limit T_J - T_C to 10 °C maximum.

- (1) t_{PLH}.
- (2) t_r.
- (3) t_f.
- (4) t_{PHL}.

Fig. 19. Switching time versus case temperature

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig. 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

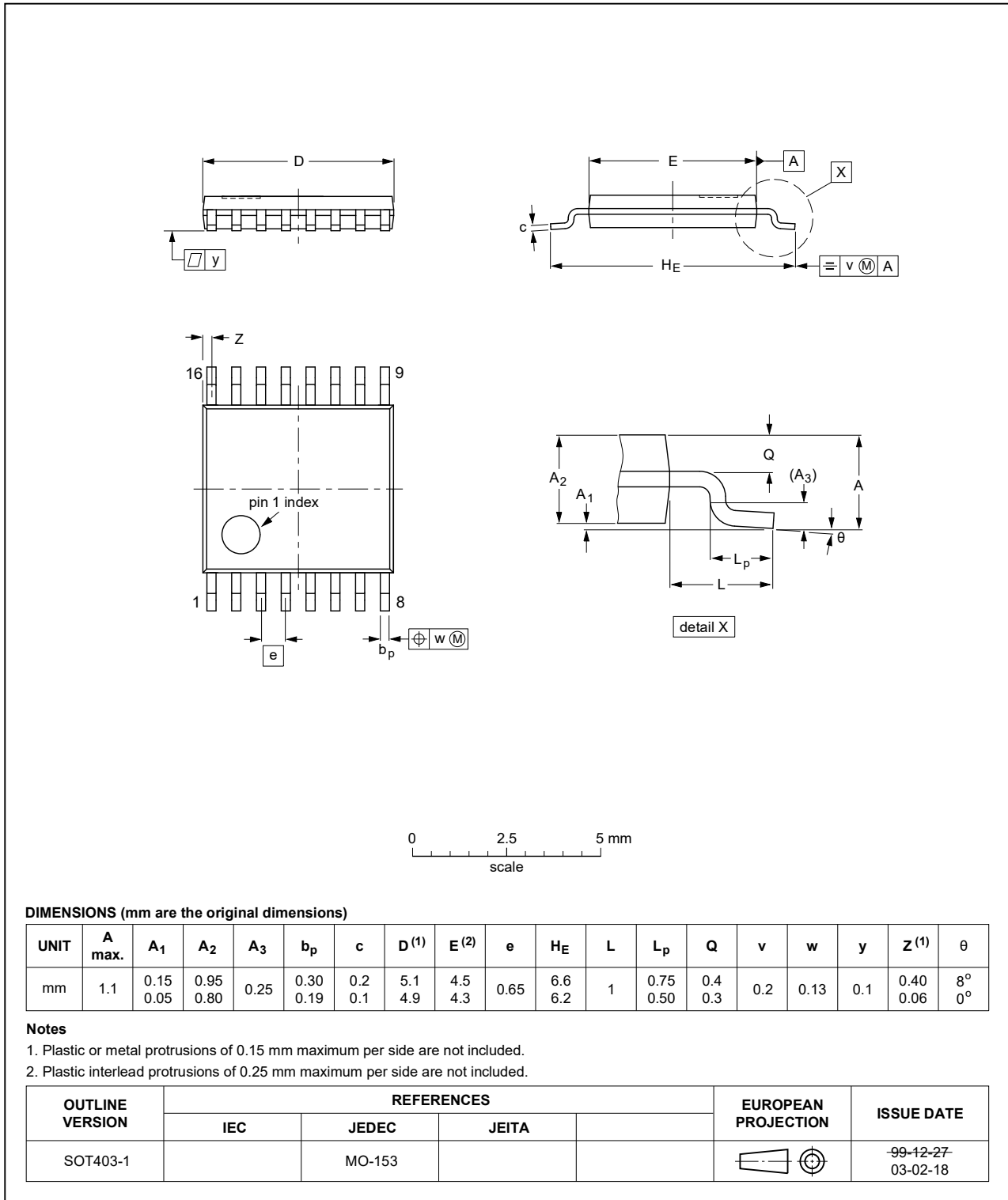


Fig. 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

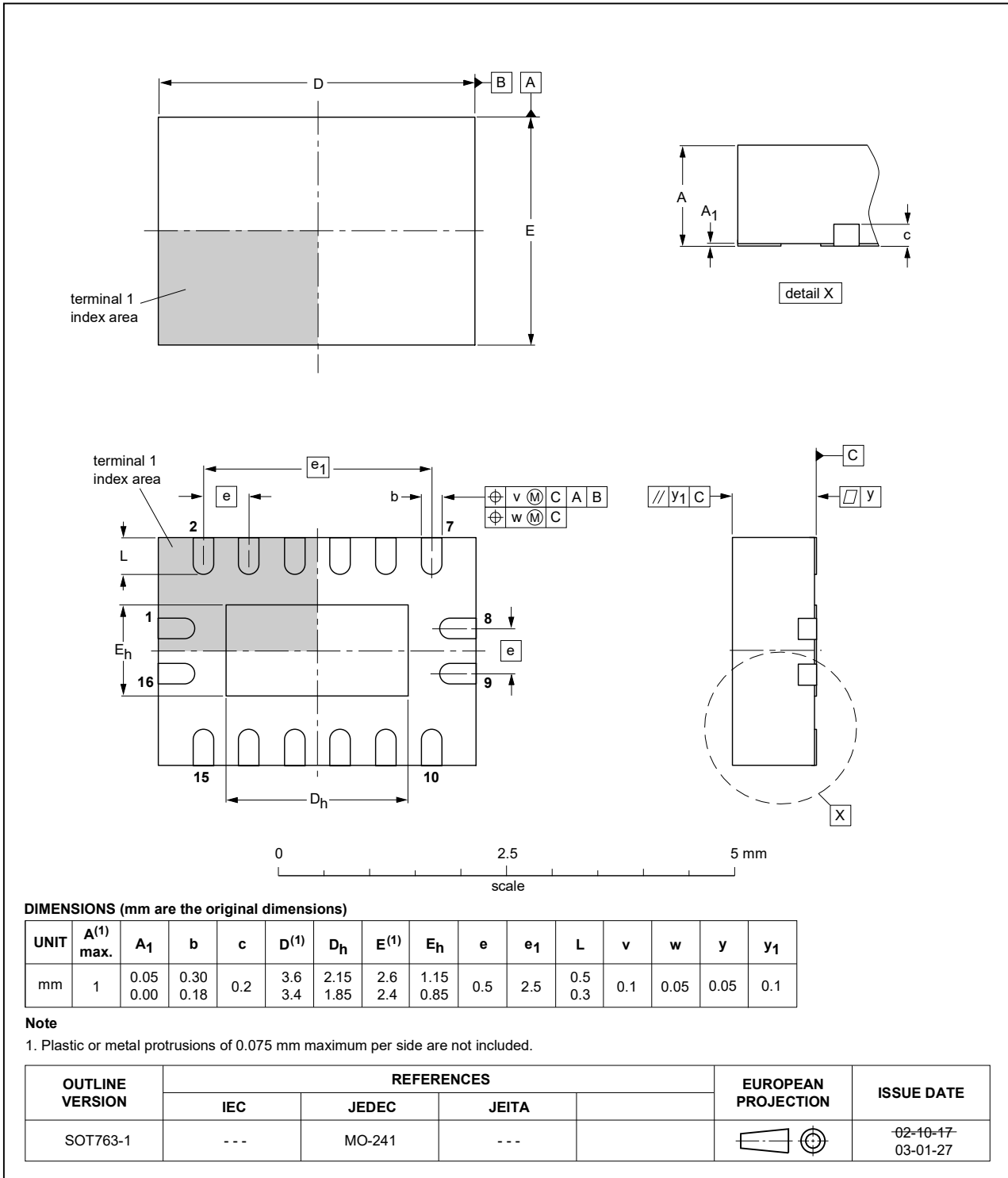


Fig. 22. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| EDNMOS | Extended Drain Negative Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|----------------|
| NPIC6C596A v.2 | 20200626 | Product data sheet | - | NPIC6C596A v.1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 8: Note in pin configuration drawing SOT763-1 (DHVQFN16) updated. | | | |
| NPIC6C596A v.1 | 20131023 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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