EVE2 TFT Module

Hardware Manual

Revision 1.3

Revision History

Revision	Date	Description	Author
1.3	March 6, 2018	Added Backlight circuitry and Parallel TFT information	Divino
1.2	October 23rd, 2017	Corrected bezel information in section 2.1. Added additional header information	Divino
1.1	October 10th, 2017	Added link to FTDI/Bridgetek Programmers Guide	Divino
1.0	August 3rd, 2017	Initial Release	Divino

Contents

1. Introduction

The Matrix Orbital EVE2 lineup utilizes FTDI/Bridgetek's second generation Embedded Video Engine to control, render, manage and display complex graphics on a full color TFT touch screen. By taking advantage of the 1 megabyte of graphics RAM, motion-JPEG encoded AVI videos can be played back in both portrait and landscape mode. Data can be displayed through a set of widgets such as gauges, spinners, sliders, and bar graphs.

Additional features include added touch control hardware, capable of recognizing and tracking touch movement and providing notification for up to 255 touch objects. Mono 8-bit linear audio wave playback at sampling frequencies from 8 kHz to 48 kHz is made possible by the built-in sound synthesizer and digital filter.

The EVE2 communicates using SPI protocol, and can be configured for quad SPI communication. Using SPI communication protocol makes the EVE2 compatible with many microcontrollers available on the market, including the FTDI/Bridgetek FT900, NXP 17XX, Arduino, and many more. With built-in graphics operations, and support for multiple widgets, development of high-quality Human Machine Interfaces (HMI) screens is simplified.

1.1. Key Features

- Advanced Embedded Video Engine(EVE) with high resolution graphics and video playback
- Support multiple widgets for simplified design development
- Support for Resistive and Capacitive Touch Screen Technology
- Support capacitive touch screen with up to 5 touches detection
- Support for LCD display with resolution up to SVGA (800x600) and formats with data enable (DE) mode or VSYNC/HSYNC mode
- Support landscape and portrait orientations
- Support playback of motion-JPEG encoded AVI videos
- -20°C to 70°C extended operating temperature range

1.2. Block Diagram

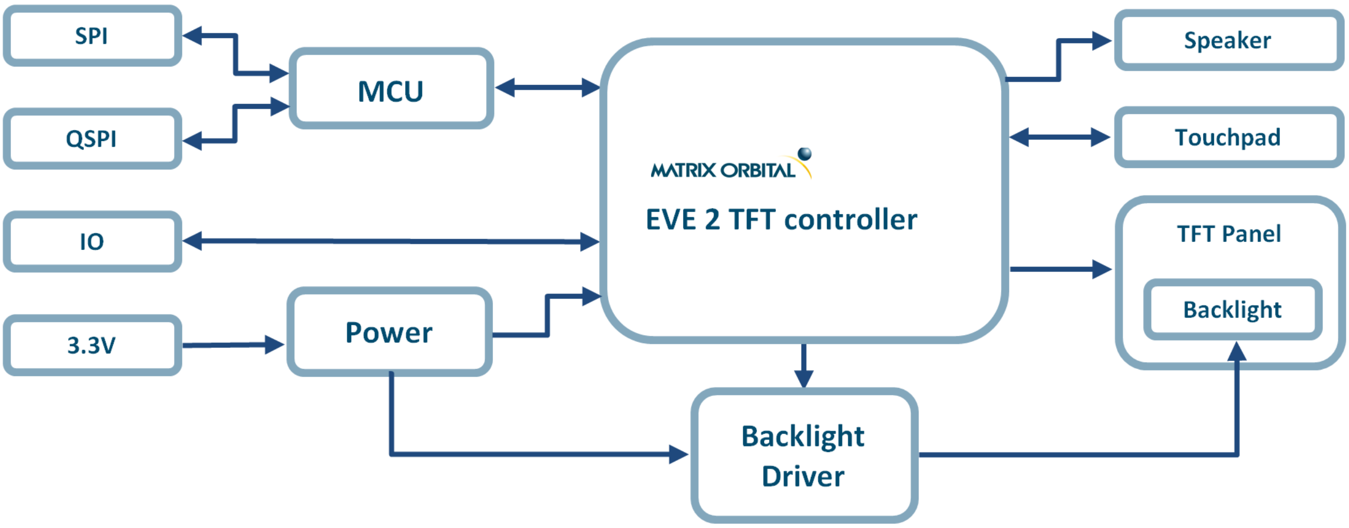

Figure 1: EVE2 TFT Module Block Diagram

2. FTDI/Bridgetek EVE Chip

FTDI/Bridgetek Chip develops innovative silicon solutions that enhance interaction with the latest in global technology. The major objective from the company is to ‘bridge technologies’ in order to support engineers with highly sophisticated, feature-rich, robust and simple-to-use product platforms. These platforms enable creation of electronic designs with high performance, low peripheral component requirements, low power budgets and minimal board real estate.

2.1. FTDI/Bridgetek EVE Graphics Engine

The FT81X series chips are graphics controllers with add-on features such as audio playback and touch capabilities. They consist of a rich set of graphics objects (primitive and widgets) that can be used for displaying various menus and screen shots for a range of products including home appliances, toys, industrial machinery, home automation, elevators, and many more.

EVE graphics controller ICs combine display, touch and audio functionality within a single chip and take an innovative object-oriented approach to HMI implementation that is proving highly effective. It leads to more streamlined solutions that are simpler to create, with significantly lower component counts, reduced board space requirements, curbed power consumption, etc. The second generation EVE devices at the heart of these new development modules have greater pixel resolution than the previous EVE ICs, resulting in sharper image rendering and greater colour depth. They also have accelerated data transfer and image/video loading capabilities, enhanced video playback, plus expanded memory resources.

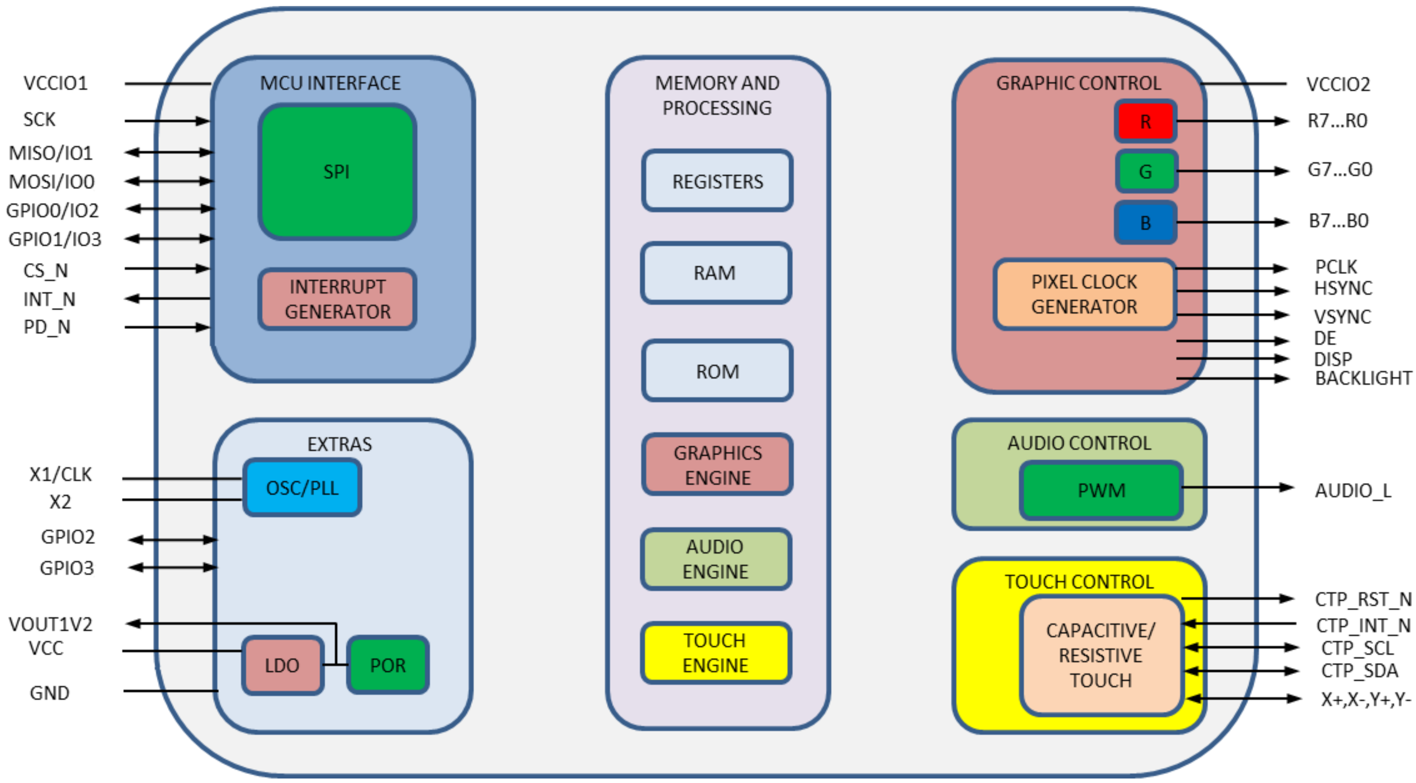

Figure 2: EVE2 Embedded Video Engine

More details regarding the EVE2 hardware specs can be found in the FTDI/Bridgetek FT81x Datasheet, available online. An FTDI/Bridgetek EVE2 programming guide, titled “FT81x Series Programming Guide”, is also available and can be downloaded at FTDI/Bridgetek’s website http://www.brtchip.com/ft81x

3. EVE2 Headers

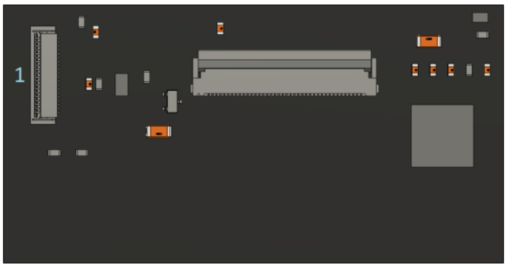

Figure 3: EVE2 Module Header Locations

Table 1: List of available Headers

#	Header	Standard Mate
1	SPI Communication and Power	FFC-20P

3.1. Communication Header Pinout

The 20 pin FFC header on the EVE2 TFT Module is used to interface with an SPI controller, and is compatible with a number of 20 pin ribbon cables. Any 20 pin FFC cable with a 0.5mm pitch and bottom contacts, such as the Wurth Electronics INC 687620050002 series ribbon cable will be compatible with the EVE2 module.

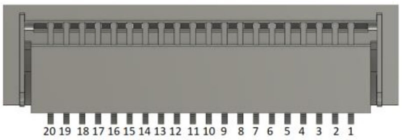

Figure 4: 20 pin FFC communication header

Table 2: 20 pin FFC communication header pinout

Pin	Symbol	Type	Function
1	VCC	Power	Logic Voltage (3.3V)
2	GND	Ground	Ground Connection
3	SCK	Input	SPI clock input
4	MISO	Input/output	SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1
5	MOSI	Input/output	SPI Single mode: SPI MISO input SPI Dual/Quad mode: SPI data line 0
6	CS	Input	SPI slave select input.*
7	$\overline{\text{INT}}$	Open Drain Output	Interrupt to host**
8	RST		FT81x Reset pin
9	N/C	No connection	No connection
10	AUDIO	Output	Audio PWM out
11	IO2	Input/output	SPI Single/Dual mode: General purpose IO 0 SPI Quad mode: SPI data line 2
12	IO3	Input/output	SPI Single/Dual mode: General purpose IO 1 SPI Quad mode: SPI data line 3
13	GPIO2	Input/output	General purpose IO 2
14	GPIO3	Input/output	General purpose IO 3
15	GND	Ground	Ground connection
16	VCC	Power	Logic Voltage (3.3V)
17	BLVDD	VDD	No Connect (Optional Backlight Voltage)
18	BLVDD	VDD	No Connect (Optional Backlight Voltage)
19	BLGND	Ground	Ground
20	BLGND	Ground	Ground

***Note:** The CS pin signifies when a SPI transaction occurs by going active low. When the pin goes inactive high, the write operation is considered complete.
****Note:** Open drain output (default) or push-pull output, active low

4. Communication Model

4.1. Programming Model

The FT81X appears to the host MCU as a memory-mapped SPI device. The host MCU sends commands and data over the serial protocol described in the data sheet.

4.2. General Software Architecture

The software architecture can be broadly classified into layers such as custom applications, graphics/GUI manager, video manger, audio manager, drivers etc. FT81X higher level graphics engine commands and co-processor engine widget commands are part of the graphics/GUI manager. Control & data paths of video and audio are part of video manager and audio manager. Communication between graphics/GUI manager and the hardware is via the SPI driver. Typically the display screen shot is constructed by the custom application based on the framework exposed by the graphics/GUI manager.

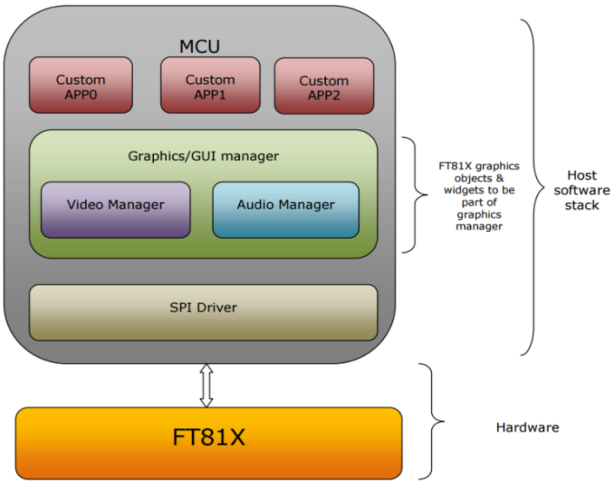

Figure 5: EVE2 Programmer model

5. Communication Interface

5.1. SPI Interface Timing Specification

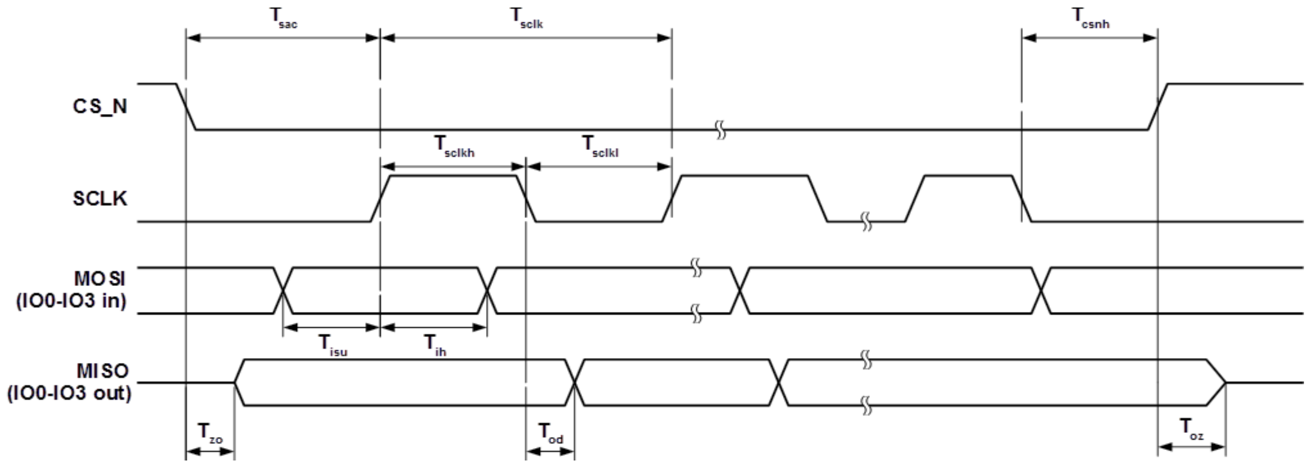

Figure 6: SPI Timing Diagram

Table 3: SPI Timing Signals

Parameter	Description	VCCIO = 3.3V		Units
		Min	Max	
Tsclk	SPI Clock Period (SINGLE/DUAL mode)	33.3		ns
Tslck	SPI clock Period (QUAD mode)	40		ns
Tsclkl	SPI clock low duration	13		ns
Tsclkh	SPI clock high duration	13		ns
Tsac	SPI access time	3		ns
Tisu	Input Setup	3		ns
Tih	Input hold	0		ns
Tzo	Output enable delay		11	ns
Toz	Output disable delay		10	ns
Tod	Output data delay		11	ns
Tcsnh	CSN hold time	0		ns

5.2. SPI and QSPI communication

The EVE2 TFT Module is capable of communicating to hosts and microcontrollers through a quad serial parallel interface (QSPI). Only SPI mode 0 is supported. The QSPI slave interface can operate up to 30MHZ, and can be configured in SINGLE, DUAL or QUAD channel modes.

The SPI slave defaults to SINGLE channel mode operation, using MISO as output to the master and MOSI as input from the master. The SPI slave can be configured to allow DUAL and QUAD channel modes by writing to register REG_SPI_WIDTH while in single channel mode.

Table 4: SPI/QSPI Communication Configuration

REG_SPI_WIDTH[1:0]	Channel Mode	Data pins	Max bus speed
00	SINGLE - default mode	MISO, MOSI	30 MHz
01	DUAL	IO0, IO1	30 MHz
10	QUAD	IO0, IO1, IO2, IO3	25 MHz
11	Reserved	-	-

When DUAL/QUAD channel modes are enabled, the SPI data ports become unidirectional. SPI transactions will be signified by CS going active low when DUAL/QUAD modes are active, and data ports are set as inputs.

Hence, for writing to the FT81x, the protocol is “WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ …” The write operation is considered complete when CS goes inactive high.

For reading from the FT81x, the protocol is “RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ”. However as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the FT81x. Therefore it is important that the firmware controlling the SPI master changes the SPI master data port direction to “input” after transmitting Addr0. The FT81x will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the FT81x will reset all its data ports’ direction to input once CS goes inactive high (i.e. at the end of the current SPI master transaction).

The below diagram depicts the behaviour of both the SPI master and slave in the master read case.

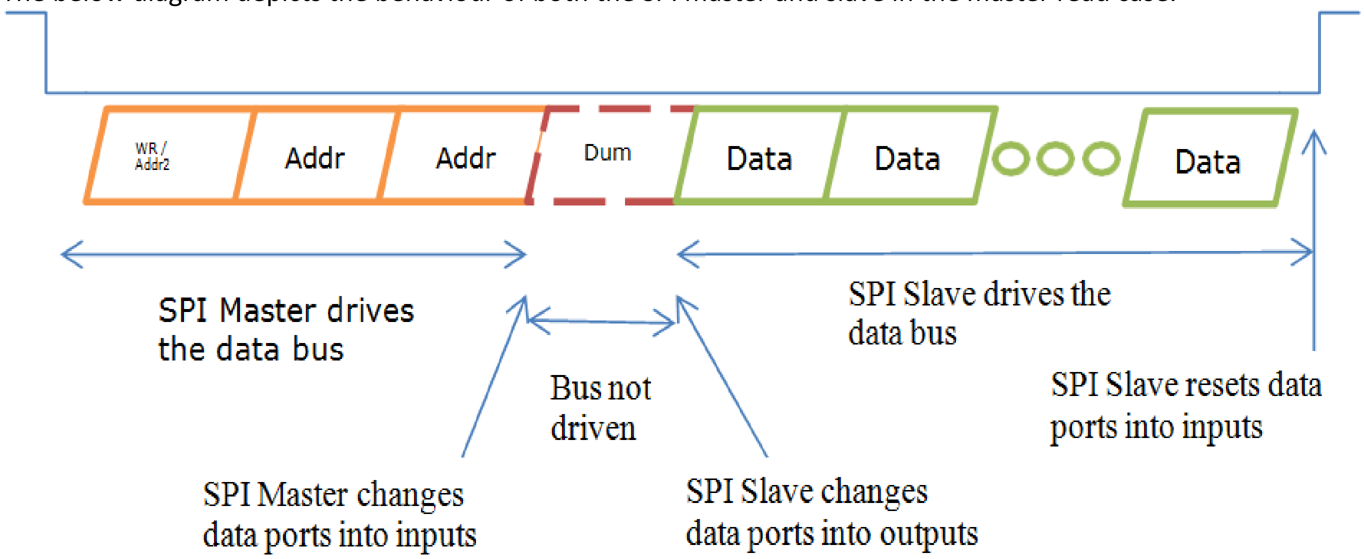

Figure 7: SPI Master and Slave bus behaviour

For DUAL channel operation, MISO(MSB) and MOSI are used. In Quad channel operation, IO3(MSB), IO2, MISO, and MOSI are used.

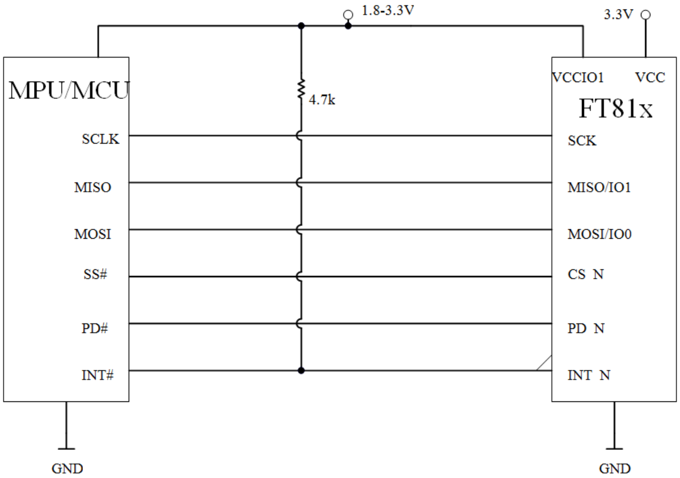

Figure 8: Single/Dual Channel SPI Interface connection

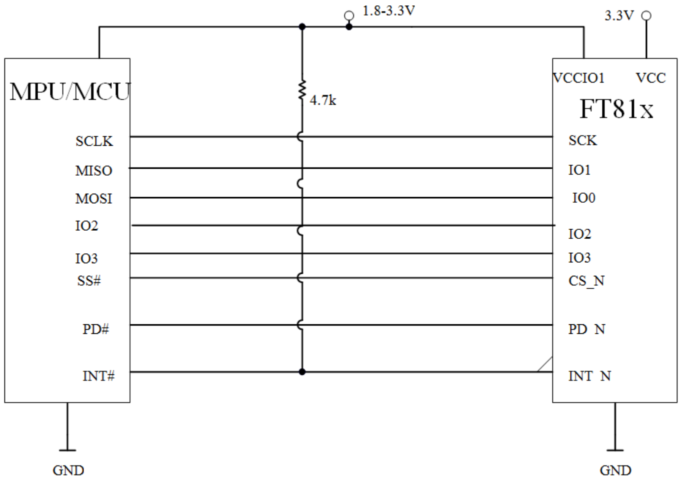

Figure 9: Quad channel SPI Interface connection

5.3. Serial Data Protocol

When interfaced with a host, the FT81x will appear as a memory-mapped SPI device. Communication between the host and the FT81x is accomplished through a series of reads and writes to a large (4 megabyte) address space. Within this address space are dedicated areas for graphics, audio and touch control.

The FT81x address space is read and written to using SPI transactions. Memory read, memory write and command write transactions are sent by the most significant bit first.

Each transaction starts with CS going low, and ends when CS going high. Data transactions have no limit regarding data length, so long as the memory address is continuous.

When initiating an SPI memory read transaction, the host will send two zero bits, followed by the 22-bit address. A dummy byte follows the address, and the FT81x will respond to each host byte with read data bytes.

Table 5: SPI Memory read transaction

7	6	5	4	3	2	1	0	
0	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Address
Byte n								

For SPI memory write transactions, a '1' bit and '0' bit is sent by the host, followed by the 22-bit address. The write data follows.

Table 6: SPI Memory write transaction

7	6	5	4	3	2	1	0	
1	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Address
Byte n								

6. Peripherals

6.1. Audio Engine

FT81x provides mono audio output through a PWM output pin, AUDIO_L. It outputs two audio sources, the sound synthesizer and audio file playback.

6.2. Sound Synthesizer

A sound processor, AUDIO ENGINE, generates the sound effects from a small ROM library of waves table. To play a sound effect listed in Table 4.3, load the REG_SOUND register with a code value and write 1 to the REG_PLAY register. The REG_PLAY register reads 1 while the effect is playing and returns a '0' when the effect ends. Some sound effects play continuously until interrupted or instructed to play the next sound effect. To interrupt an effect, write a new value to REG_SOUND and REG_PLAY registers; e.g. write 0 (Silence) to REG_SOUND and 1 to PEG_PLAY to stop the sound effect.

The sound volume is controlled by register REG_VOL_SOUND. The 16-bit REG_SOUND register takes an 8-bit sound in the low byte. For some sounds, marked "pitch adjust" in the table below, the high 8 bits contain a MIDI note value. For these sounds, a note value of zero indicates middle C. For other sounds the high byte of REG_SOUND is ignored.

Figure 10: Sound Effect

Value	Effect	Continuous	Pitch Adjust
00h	Silence	Y	N
01h	Square Wave	Y	Y
02h	Sine Wave	Y	Y
03h	Sawtooth Wave	Y	Y
04h	Triangle Wave	Y	Y
05h	Beeping	Y	Y
06h	Alarm	Y	Y
07h	Warble	Y	Y
08h	Carousel	Y	Y
10h	1 short pip	N	Y
11h	2 short pips	N	Y
12h	3 short pips	N	Y
13h	4 short pips	N	Y
14h	5 short pips	N	Y
15h	6 short pips	N	Y
16h	7 short pips	N	Y
17h	8 short pips	N	Y
18h	9 short pips	N	Y
19h	10 short pips	N	Y
1Ah	11 short pips	N	Y
1Bh	12 short pips	N	Y
1Ch	13 short pips	N	Y
1Dh	14 short pips	N	Y
1Eh	15 short pips	N	Y
1Fh	16 short pips	N	Y
23h	DTMF #	Y	N
2Ch	DTMF *	Y	N
30h	DTMF 0	Y	N
31h	DTMF 1	Y	N

Value	Effect	Continuous	Pitch Adjust
32h	DTMF 2	Y	N
33h	DTMF 3	Y	N
34h	DTMF 4	Y	N
35h	DTMF 5	Y	N
36h	DTMF 6	Y	N
37h	DTMF 7	Y	N
38h	DTMF 8	Y	N
39h	DTMF 9	Y	N
40h	Harp	N	Y
41h	Xylophone	N	Y
42h	Tuba	N	Y
43h	Glockenspiel	N	Y
44h	Organ	N	Y
45h	Trumpet	N	Y
46h	Piano	N	Y
47h	Chimes	N	Y
48h	Music Box	N	Y
49h	Bell	N	Y
50h	Click	N	N
51h	Switch	N	N
52h	Cowbell	N	N
53h	Notch	N	N
54h	Hihat	N	N
55h	Kickdrum	N	N
56h	Pop	N	N
57h	Clack	N	N
58h	Chack	N	N
60h	Mute	N	N
61h	Unmute	N	N

Figure 11: MIDI Note Effect

MIDI note	ANSI note	Freq (Hz)	MIDI note	ANSI note	Freq (Hz)	MIDI note	ANSI note	Freq (Hz)	MIDI note	ANSI note	Freq (Hz)
21	A0	27.5	43	G2	98.0	65	F4	349.2	87	D#6	1244.5
22	A#0	29.1	44	G#2	103.8	66	F#4	370.0	88	E6	1318.5
23	B0	30.9	45	A2	110.0	67	G4	392.0	89	F6	1396.9
24	C1	32.7	46	A#2	116.5	68	G#4	415.3	90	F#6	1480.0
25	C#1	34.6	47	B2	123.5	69	A4	440.0	91	G6	1568.0
26	D1	36.7	48	C3	130.8	70	A#4	466.2	92	G#6	1661.2
27	D#1	38.9	49	C#3	138.6	71	B4	493.9	93	A6	1760.0
28	E1	41.2	50	D3	146.8	72	C5	523.3	94	A#6	1864.7
29	F1	43.7	51	D#3	155.6	73	C#5	554.4	95	B6	1975.5
30	F#1	46.2	52	E3	164.8	74	D5	587.3	96	C7	2093.0
31	G1	49.0	53	F3	174.6	75	D#5	622.3	97	C#7	2217.5
32	G#1	51.9	54	F#3	185.0	76	E5	659.3	98	D7	2349.3
33	A1	55.0	55	G3	196.0	77	F5	698.5	99	D#7	2489.0
34	A#1	58.3	56	G#3	207.7	78	F#5	740.0	100	E7	2637.0
35	B1	61.7	57	A3	220.0	79	G5	784.0	101	F7	2793.8
36	C2	65.4	58	A#3	233.1	80	G#5	830.6	102	F#7	2960.0
37	C#2	69.3	59	B3	246.9	81	A5	880.0	103	G7	3136.0
38	D2	73.4	60	C4	261.6	82	A#5	932.3	104	G#7	3322.4
39	D#2	77.8	61	C#4	277.2	83	B5	987.8	105	A7	3520.0
40	E2	82.4	62	D4	293.7	84	C6	1046.5	106	A#7	3729.3
41	F2	87.3	63	D#4	311.1	85	C#6	1108.7	107	B7	3951.1
42	F#2	92.5	64	E4	329.6	86	D6	1174.7	108	C8	4186.0

6.3. Audio Playback

The FT81x can play back recorded sound through its audio output. To do this, load the original sound data into the FT81x's RAM, and set registers to start the playback.

The registers controlling audio playback are:

REG_PLAYBACK_START: the start address of the audio data

REG_PLAYBACK_LENGTH: the length of the audio data, in bytes

REG_PLAYBACK_FREQ: the playback sampling frequency, in Hz

REG_PLAYBACK_FORMAT: the playback format, one of LINEAR SAMPLES, uLAW SAMPLES, or ADPCM SAMPLES

REG_PLAYBACK_LOOP: if zero, the sample is played once. If one, the sample is repeated indefinitely

REG_PLAYBACK_PLAY: a write to this location triggers the start of audio playback, regardless of writing '0' or '1'. Read back '1' when playback is ongoing, and '0' when playback finishes

REG_VOL_PB: playback volume, 0-255

The mono audio formats supported are 8-bits PCM, 8-bits uLAW and 4-bits IMA-ADPCM. For ADPCM_SAMPLES, each sample is 4 bits, so two samples are packed per byte, the first sample is in bits 0-3 and the second is in bits 4-7.

The current audio playback read pointer can be queried by reading the REG_PLAYBACK_READPTR. Using a large sample buffer, looping, and this read pointer, the host MPU/MCU can supply a continuous stream of audio.

6.4. General Purpose Input Output

Depending on the package, the FT81x can be configured to use up to 4 GPIO pins. These GPIO pins are controlled by the REG_GPIOX_DIR and REG_GPIOX registers. Alternatively the GPIO0 and GPIO1 pins can also be controlled by REG_GPIO_DIR and REG_GPIO to maintain backward compatibility with the FT800/FT801.

When the QSPI is enabled in Quad mode, GPIO0/IO2 and GPIO1/IO3 pins are used as data lines of the QSPI.

7. Backlight

7.1. Backlight Driver

The EVE2 Module comes equipped with its own backlight driver and integrated backlight control circuit, but if you are running a high brightness or 7" inch display variant, more power may need to be supplied to the display. The EVE2 Module can be configured to provide additional current through pins 17, 18, 19, and 20 by populating the R1 and R2 resistor pads with 0 Ohm resistors. With R1 and R2 populated, additional 3.3V power can be supplied to pins 17 and 18, doubling the amount of current that can be fed to the display.

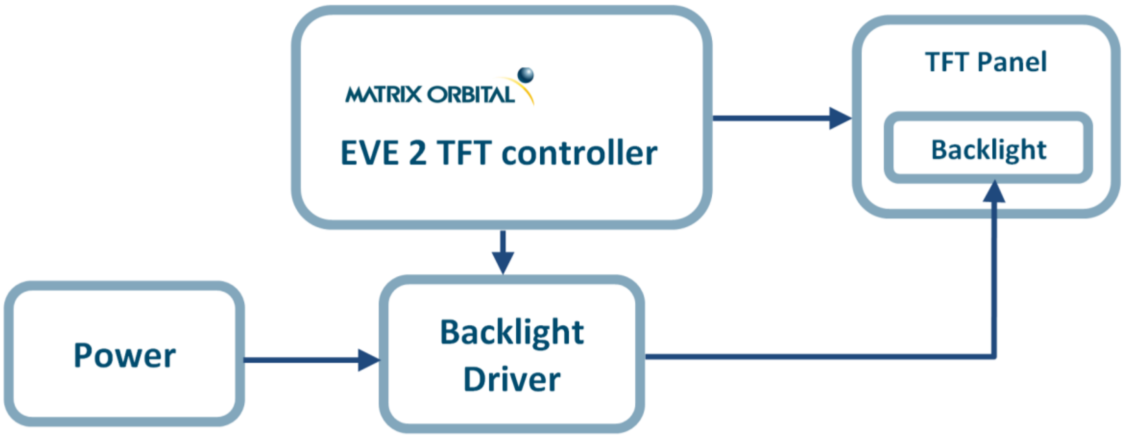

Figure 12: Backlight Driver Block Diagram

8. TFT Display

8.1. EVE2 Module Displays

The EVE2 Module is paired with a Matrix Orbital Parallel TFT display. Information about Matrix Orbital's Parallel TFT lineup, including drawings, dimensions, and tolerances can be found online at:

https://www.matrixorbital.ca/manuals/parallel-display/mop-tft-manual

Table 7: EVE2 Parallel Display Datasheet

EVE2 Display	Parallel TFT Datasheet
EVE2-29A	MOP-TFT320102-29A
EVE2-35A	MOP-TFT320240-35A
EVE2-38A	MOP-TFT480116-38A
EVE2-43A	MOP-TFT480272-43A
EVE2-50A	MOP-TFT800480-50A
EVE2-70A	MOP-TFT800480-70A

8.2. EVE2 TFT Display Timings

Table 8: EVE2 TFT Display Timings

EVE Timings	Display					
	EVE2-29	EVE2-35	EVE2-38	EVE2-43	EVE2-50	EVE2-70
REG_HSIZE	320	320	480	480	800	800
REG_VSIZE	102	240	272	272	480	480
REG_HCYCLE	408	408	524	548	928	928
REG_HOFFSET	70	68	43	43	88	88
REG_HSYNC0	0	0	0	0	0	0
REG_HSYNC1	10	10	41	41	48	48
REG_VCYCLE	262	262	288	292	525	525
REG_VOFFSET	156	18	12	12	32	32
REG_VSYNC0	0	0	156	0	0	0
REG_VSYNC1	2	2	10	10	3	3
REG_ PCLK	8	8	5	5	2	2
REG_SWIZZLE	0	0	0	0	0	0
REG_PCLK_POL	0	0	1	1	1	1
REG_CSPREAD	1	1	1	1	0	0
REG_DITHER	1	1	1	1	1	1

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Table 9: EVE2 Module Limiting Values

Item	Value	Unit
Storage Temperature	-30 to 80	°C
Ambient Temperature (Power Applied)	-20 to +70	°C
VCC Supply Voltage	0 to +4	V
DC Input Voltage	-0.5 to + (VCCIO + 0.3)	V

9.2. EVE2 DC Characteristics

Table 10: EVE2 DC characteristics

Item	Description	Min.	Typ.	Max.	Unit	Conditions
VCC	VCC operating supply voltage	2.97	3.30	3.63	V	Normal Operation
Icc1	Power Down Current	-	0.17	-	mA	Power down mode
Icc2	Sleep Current	-	0.76	-	mA	Sleep Mode
Icc3	Standby Current	-	1.8	-	mA	Standby Mode
Icc4	Operating Current	-	22	-	mA	Normal Operations

9.3. EVE2 Digital I/O Pin Characteristics

Table 11: Digital I/O Specifications

Parameter	Description	Min	Typ.	Max	Units	Conditions
Voh	Output Voltage High	VCCIO- 0.4	3.3V-	-	V	Ioh=5mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=5mA
Vih	Input High Voltage	2.0	-	-	V	
Vil	Input Low Voltage	-	-	0.8	V	
Vth	Schmitt Hysteresis Voltage	0.22	-	0.3	V	
Iin	Input leakage current	-10	-	10	uA	Vin = VCCIO or 0
Ioz	Tri-state output leakage current	-10	-	10	uA	Vin = VCCIO or 0
Rpu	Pull-up resistor	-	42	-	kΩ	
Rpd	Pull-down resistor	-	44	-	kΩ	

9.4. Power Specifications

Parameter		EVE2-29A	EVE2-35A	EVE2-38A	EVE2-43A	EVE2-50A	EVE2-70A	Units
EVE2 Logic		35	35	35	35	35	35	mA
TFT Power Supply (max)		40	20	30	24	199.2	140	mA
TFT Backlight	Min	0	0	0	0	0	0	mA
	Typ	120	124	240	206	240	465	mA
	Max	144	149	288	247	288	558	mA

9.5. Touch Sense Characteristics

Table 12: Touch Panel characteristics

Parameter	Description	Min	Typ.	Max	Units	Conditions
Rsw-on	X-,X+,Y- and Y+ Drive On resistance	-	6	10	Ω	VCCIO=3.3V
Rsw-off	X-,X+,Y- and Y+ Drive Off resistance	10	-	-	MΩ	
Rpu	Touch sense pull up resistance	78	100	125	kΩ	
Vth+	Touch Detection rising-edge threshold on XP pin	1.59	-	2.04	V	VCCIO=3.3V
Vth-	Touch Detection falling-edge threshold on XP pin	1.23	-	1.55	V	VCCIO=3.3V
Rl	X-axis and Y-axis drive load resistance	200	-	-	Ω	

10. Mounting

10.1. Extended Capacitive Touch

Extended capacitive touch EVE2 units will come with a double sided adhesive already applied on the exposed back side of the bezel. A 3M 93010LE tape with 300LSE adhesive is used, allowing the display to be easily mounted on flat surfaces. In addition, the tape can maintain its bond in environments of 100% relative humidity at 38°C, and can withstand temperatures up to 149°C.

11. Ordering Options

11.1. Matrix Orbital EVE2 series displays

The EVE2 TFT Module has multiple size and touch variants, to ensure that there is an option for every application. Resistive touch panels are also available, allowing interactive touch functionality for all applications.

Table 13: EVE2 Displays, and GTT counterpart

Size	Touch Screen Type	Matrix Orbital Part Number	Intelligent Series Upgrade
2.9”	None	EVE2-29A- TPN	GTT29A-TPN-BLM-B0-H1
3.5”	None	EVE2-38A- TPN	GTT35A-TPN-BLM-B0-H1
	Resistive	EVE2-35A- TPR	GTT35A-TPR-BLM-B0-H1
	Capacitive	EVE2-35G-TPC	GTT35A-TPC-BLM-B0-H1
3.8”	None	EVE2-38A-TPN	GTT38A-TPN-BLH-B0-H1
	Resistive	EVE2-38A-TPR	GTT38A-TPR-BLH-B0-H1
	Capacitive	EVE2-38G-TPC	GTT38A-TPC-BLH-B0-H1
4.3”	None	EVE2-43A-TPN	GTT43A TPN-BLM-B0-H1
	Resistive	EVE2-43A-TPR	GTT43A TPR-BLM-B0-H1
	Capacitive	EVE2-43G-TPC	GTT43A TPC-BLM-B0-H1
5.0”	None	EVE2-50A-TPN	GTT50A-TPN-BLM-B0-H1
	Resistive	EVE2-50A-TPR	GTT50A-TPR-BLM-B0-H1
	Capacitive	EVE2-50G-TPC	GTT50A-TPC-BLM-B0-H1
7.0”	None	EVE2-70A-TPN	GTT70A-TPN-BLM-B0-H1
	Resistive	EVE2-70A-TPR	GTT70A-TPR-BLM-B0-H1
	Capacitive	EVE2-70G-TPC	GTT70A-TPC-BLM-B0-H1

11.2. Matrix Orbital Product Line Comparison

Table 14: Product comparison chart

Features		Display Series		
		Parallel	EVE2	GTT
Memory	Storage			2GB
	RAM		1MB	32/64MB
Interface	RS232			✓
	TTL			✓
	I2C			✓
	RS422			✓
	USB			✓
	Parallel	✓		
	SPI		✓	
Touch	None	✓	✓	✓
	Resistive	✓	✓	✓
	PCAP	✓	✓	✓
	Keyboard			✓
Features	Piezo			✓
	Vibration feedback			✓
	Audio playback		✓	
	GPO		4	10
Voltage	3.3V		✓	
	5V	✓		✓
	9-35V			✓
Development Time		•••••	•••	•
Cost		$	$$	$$$$

11.3. Software Support

Table 15: EVE Screen Editor and GTT Designer Suite comparison

Features	FTDI/Bridgetek EVE Screen Editor	GTT Designer Suite
Drag and drop functionality	✓	✓
Send commands directly to display	✓	✓
Command list generation	✓	✓
Intuitive design format	✓	✓
Deploy screens to the display	-	✓
Multiple screen generation	-	✓
Device Inspector	✓	-

12. Dimensional Drawing

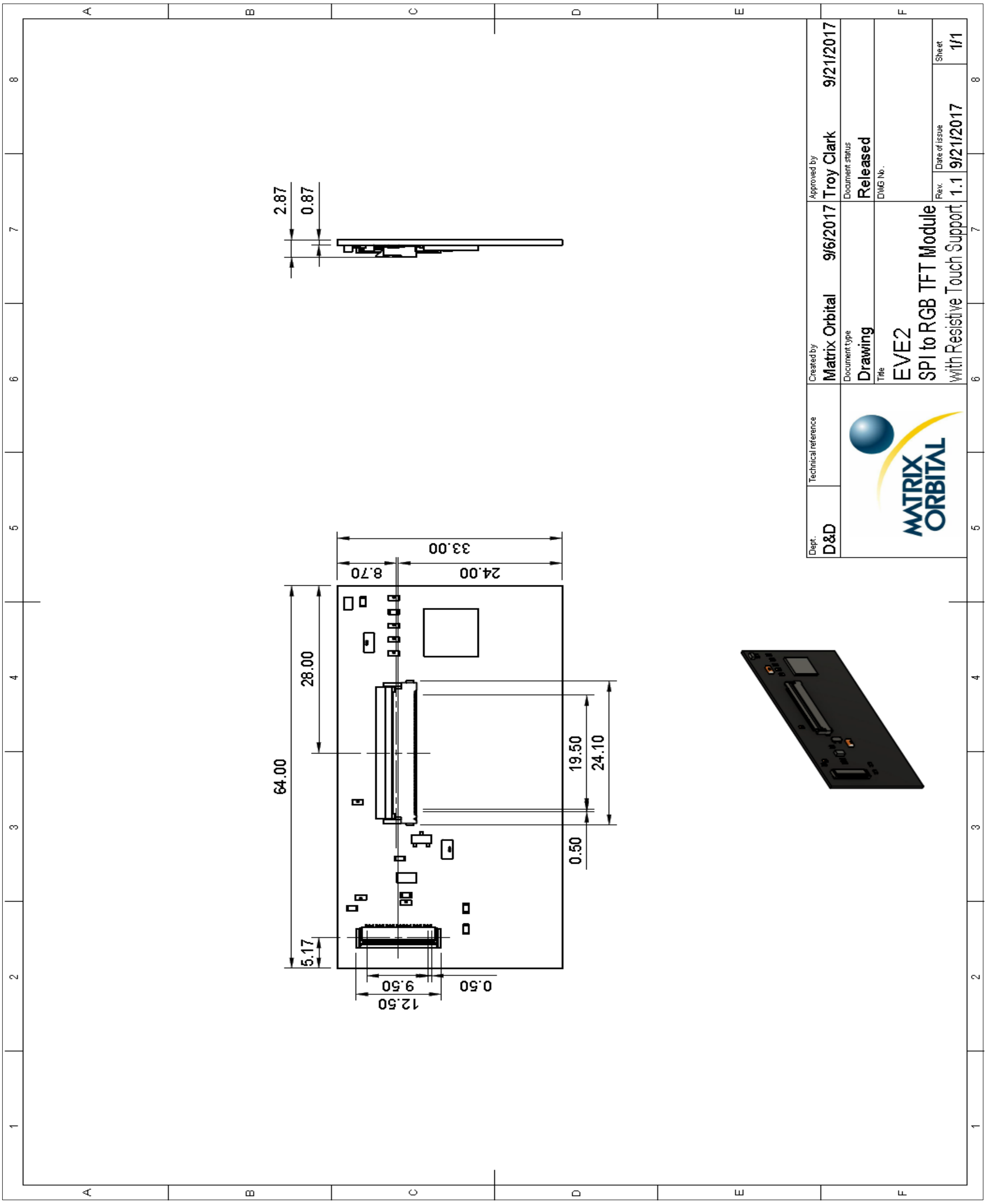

Figure 13: EVE2 TFT Module Technical Drawing

13. EVE2 TFT Module Schematic

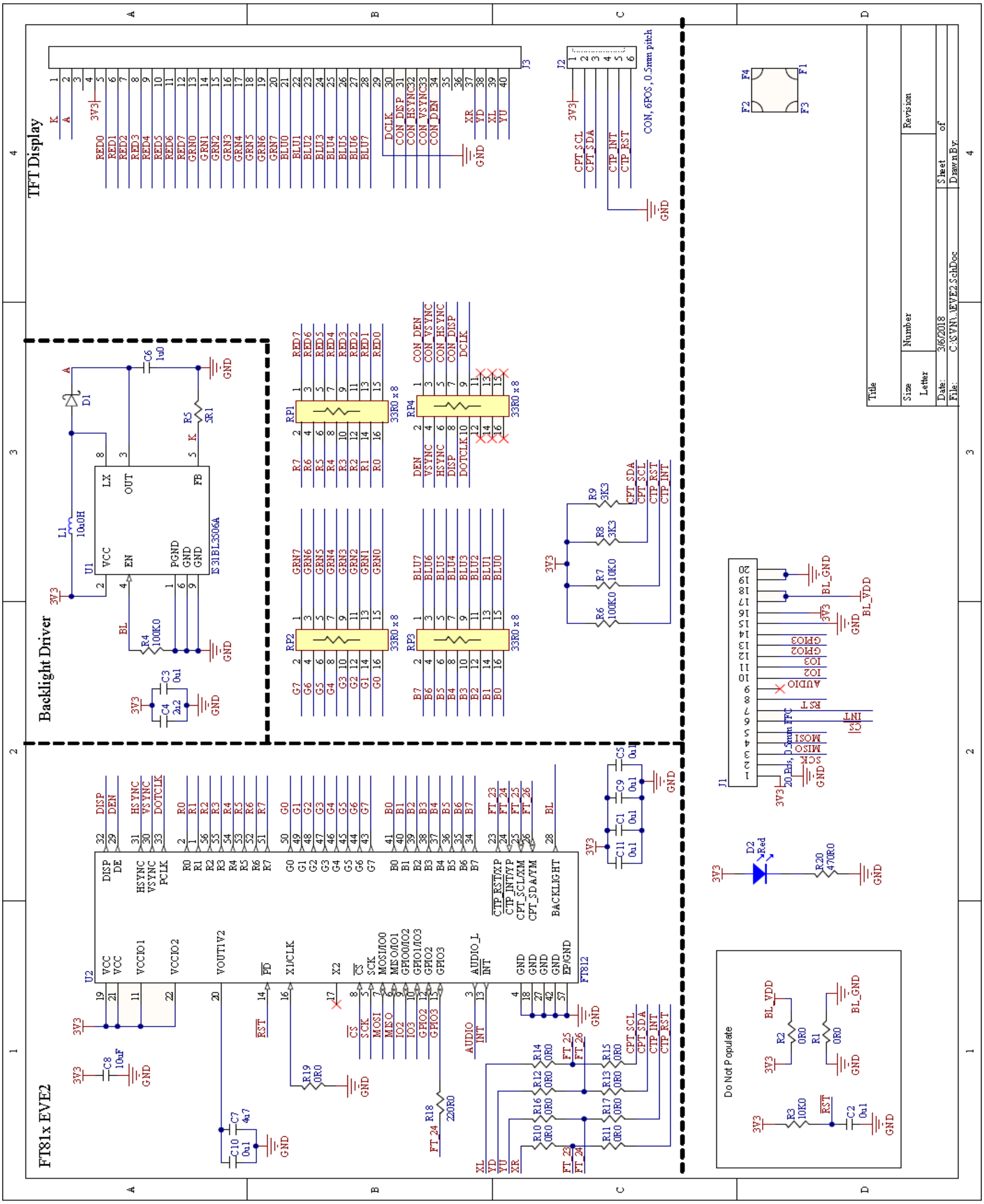

Figure 14: EVE2 TFT Module Schematic

14. Contact

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