Freescale Semiconductor
Technical Data

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# MPC8280 PowerQUICC II Family Hardware Specifications

This document contains detailed information about power considerations, DC/AC electrical characteristics, and AC timing specifications for .13µm (HiP7) members of the PowerQUICC II family of integrated communications processors—the MPC8280, the MPC8275, and the MPC8270 (collectively called the MPC8280 throughout this document).

**Contents**

1. Overview . . . . . 2
2. Operating Conditions . . . . . 7
3. DC Electrical Characteristics . . . . . 9
4. Thermal Characteristics . . . . . 12
5. Power Dissipation . . . . . 15
6. AC Electrical Characteristics . . . . . 16
7. Clock Configuration Modes . . . . . 26
8. Pinout . . . . . 45
9. Package Description . . . . . 75
10. Ordering Information . . . . . 79
11. Document Revision History . . . . . 79

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# 1 Overview

This table shows the functionality supported by each SoC in the MPC8280 family.

**Table 1. MPC8280 PowerQUICC II Family Functionality**

| Functionality | SoCs | | | |
|---|---|---|---|---|
| | MPC8270 | | MPC8275 | MPC8280 |
| Package[1] | 480 TBGA | 516 PBGA | 516 PBGA | 480 TBGA |
| Serial communications controllers (SCCs) | 4 | 4 | 4 | 4 |
| QUICC multi-channel controller (QMC) | — | — | — | — |
| Fast communication controllers (FCCs) | 3 | 3 | 3 | 3 |
| I-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| D-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| Ethernet (10/100) | 3 | 3 | 3 | 3 |
| UTOPIA II Ports | 0 | 0 | 2 | 2 |
| Multi-channel controllers (MCCs) | 1 | 1 | 1 | 2 |
| PCI bridge | Yes | Yes | Yes | Yes |
| Transmission convergence (TC) layer | — | — | — | Yes |
| Inverse multiplexing for ATM (IMA) | — | — | — | Yes |
| Universal serial bus (USB) 2.0 full/low rate | 1 | 1 | 1 | 1 |
| Security engine (SEC) | — | — | — | — |

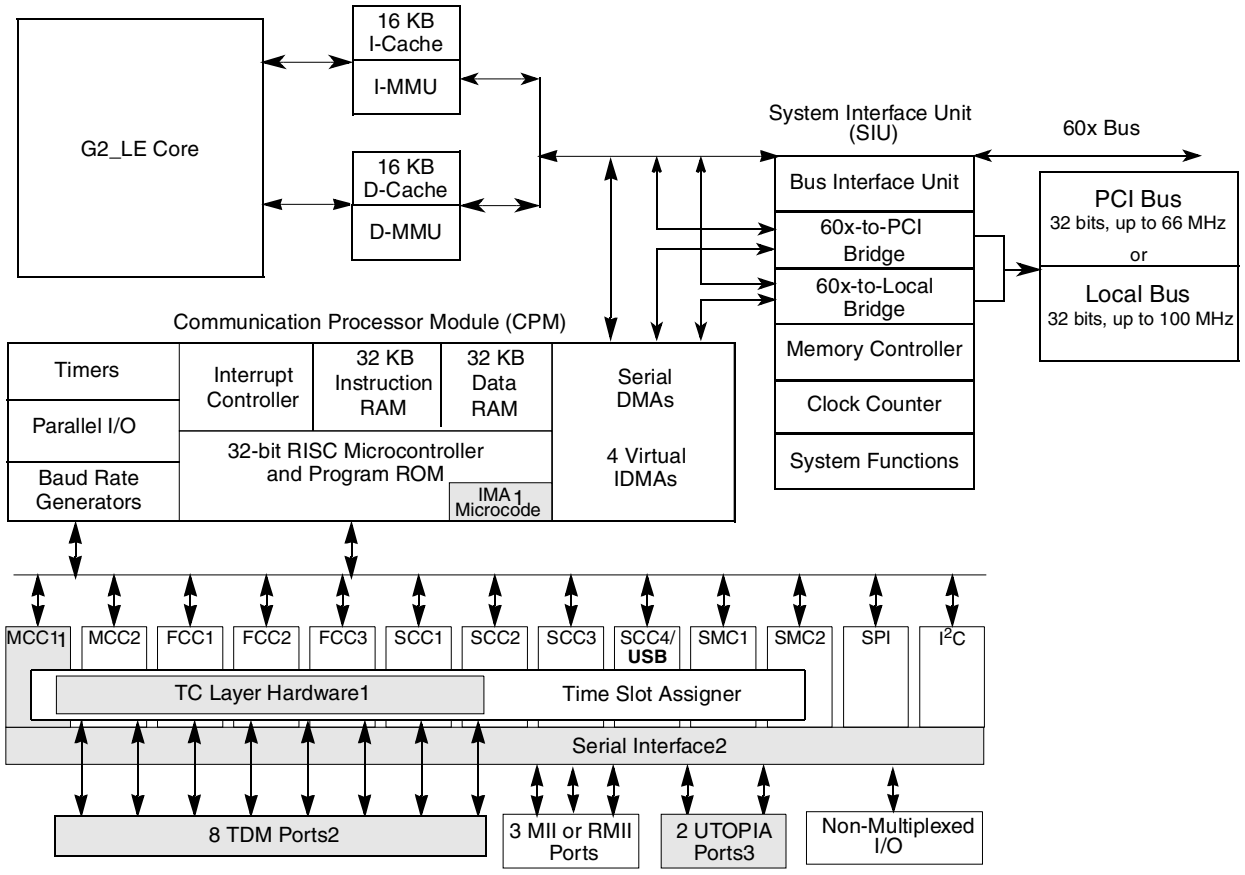
[1] See Table 2.

Devices in the MPC8280 family are available in four packages—the standard ZU and VV packages and the alternate VR or ZQ packages—as shown in Table 2. Note that throughout this document, references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Freescale sales office. For package ordering information, see Section 10, “Ordering Information.”

**Table 2. HiP7 PowerQUICC II Device Packages**

| Code (Package) | ZU (480 TBGA—Leaded) | VV (480 TBGA—Lead Free) | VR (516 PBGA—Lead free) | ZQ (516 PBGA—Lead spheres) |
|---|---|---|---|---|
| Device | MPC8280 | MPC8280 | MPC8275VR | MPC8275ZQ |
| | MPC8270 | MPC8270 | MPC8270VR | MPC8270ZQ |

This figure shows the block diagram of the SoC. Shaded portions are SoC-specific; see the notes below the figure.




**Notes:**
[1] MPC8280 only (**not on MPC8270,** the VR package, nor the ZQ package)
[2] MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).
[3] MPC8280, MPC8275VR, MPC8275ZQ only (**not on MPC8270,** MPC8270VR, nor MPC8270ZQ)

**Figure 1. SoC Block Diagram**

## 1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)

  - Common on-chip processor (COP) test interface
  - High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
  - Supports bus snooping
  - Support for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
  - PCI host bridge or peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI

  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
  - Supports the $I_2O$ standard
  - Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66.67/83.33/100 MHz, 3.3 V specification
  - 60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port
  - Uses the local bus signals, removing need for additional pins
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- 12-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x) and byte selects for 32-bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2_LE core through an on-chip 32 KB dual-port data RAM, an on-chip 32 KB dual-port instruction RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)

- ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64 K external connections (no ATM support for the MPC8270)
- Transparent
- HDLC—Up to T3 rates (clear channel)
- FCC2 can also be connected to the TC layer (MPC8280 only)

— Two multichannel controllers (MCCs) (one MCC on the MPC8270)

- Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
- Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC

— Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:

- Ethernet/IEEE 802.3 CDMA/CS
- HDLC/SDLC and HDLC bus
- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Binary synchronous (BISYNC) communications
- Transparent

• Universal serial bus (USB) controller

— Supports USB 2.0 full/low rate compatible

— USB host mode

- Supports control, bulk, interrupt, and isochronous data transfers
- CRC16 generation and checking
- NRZI encoding/decoding with bit stuffing
- Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
- Flexible data buffers with multiple buffers per frame
- Supports local loopback mode for diagnostics (12 Mbps only)

— Supports USB slave mode

- Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
- CRC16 generation and checking
- CRC5 checking
- NRZI encoding/decoding with bit stuffing
- 12- or 1.5-Mbps data rate
- Flexible data buffers with multiple buffers per frame
- Automatic retransmission upon transmit error

— Two serial management controllers (SMCs), identical to those of the MPC860

  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One $I^2C$ controller (identical to the MPC860 $I^2C$ controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
  - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

# 2 Operating Conditions

This table shows the maximum electrical ratings.

**Table 3. Absolute Maximum Ratings[1]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage[2] | VDD | –0.3 – 2.25 | V |
| PLL supply voltage[2] | VCCSYN | –0.3 – 2.25 | V |
| I/O supply voltage[3] | VDDH | –0.3 – 4.0 | V |
| Input voltage[4] | VIN | GND(–0.3) – 3.6 | V |
| Junction temperature | $T_j$ | 120 | °C |
| Storage temperature range | $T_{STG}$ | (–55) – (+150) | °C |

[1] Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

This table lists recommended operational voltage conditions.

**Table 4. Recommended Operating Conditions[1]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage | VDD | 1.45 – 1.60 | V |
| PLL supply voltage | VCCSYN | 1.45 – 1.60 | V |
| I/O supply voltage | VDDH | 3.135 – 3.465 | V |
| Input voltage | VIN | GND (–0.3) – 3.465 | V |
| Junction temperature (maximum) | $T_j$ | 105[2] | °C |
| Ambient temperature | $T_A$ | 0–70[2] | °C |

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A} – 105_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or $V_{CC}$).

This figure shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

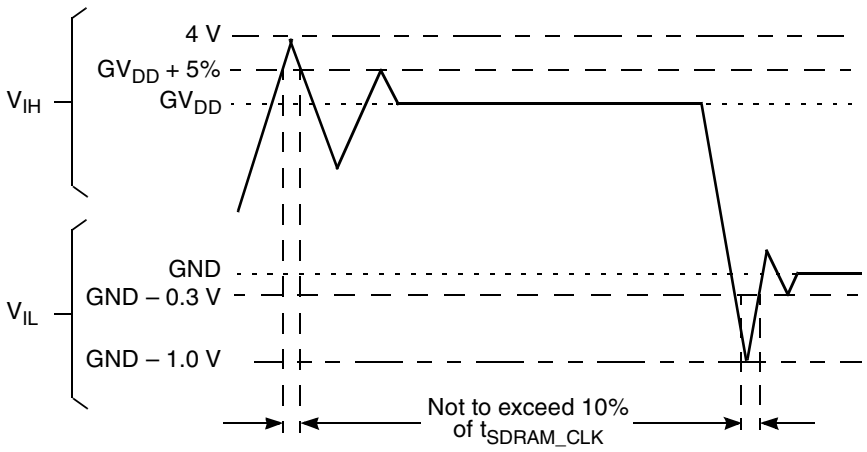



**Figure 2. Overshoot/Undershoot Voltage**

# 3 DC Electrical Characteristics

This table shows DC electrical characteristics.

**Table 5. DC Electrical Characteristics[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[3] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[3] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V[4] | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[5] (UTOPIA pins only): $I_{OH}$ = -8.0mA<br>PA[0-31]<br>PB[4-31]<br>PC[0-31]<br>PD[4-31] | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[5] (UTOPIA pins only): $I_{OL}$ = 8.0mA<br>PA[0-31]<br>PB[4-31]<br>PC[0-31]<br>PD[4-31] | $V_{OL}$ | — | 0.5 | V |

**Table 5. DC Electrical Characteristics[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 6.0mA<br>BR<br>BG<br>ABB/IRQ2<br>TS<br>A[0-31]<br>TT[0-4]<br>TBST<br>TSIZE[0–3]<br>AACK<br>ARTRY<br>DBG<br>DBB/IRQ3<br>D[0-63]<br>DP(0)/RSRV/EXT_BR2<br>DP(1)/IRQ1/EXT_BG2<br>DP(2)/TLBISYNC/IRQ2/EXT_DBG2<br>DP(3)/IRQ3/EXT_BR3/CKSTP_OUT<br>DP(4)/IRQ4/EXT_BG3/CORE_SREST<br>DP(5)/TBEN/EXT_DBG3/IRQ5/CINT<br>DP(6)/CSE(0)/IRQ6<br>DP(7)/CSE(1)/IRQ7<br>PSDVAL<br>TA<br>TEA<br>GBL/IRQ1<br>CI/BADDR29/IRQ2<br>WT/BADDR30/IRQ3<br>L2_HIT/IRQ4<br>CPU_BG/BADDR31/IRQ5/CINT<br>CPU_DBG<br>CPU_BR<br>IRQ0/NMI_OUT<br>IRQ7/PCI_RSTINT_OUT/APE<br>PORESET<br>HRESET<br>SRESET<br>RSTCONF | $V_{OL}$ | — | 0.4 | V |

**Table 5. DC Electrical Characteristics[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 5.3mA<br>CS[0-9]<br>CS(10)/BCTL1<br>CS(11)/AP(0)<br>BADDR[27–28]<br>ALE<br>BCTL0<br>PWE[0–7]/PSDDQM[0–7]/PBS[0–7]<br>PSDA10/PGPL0<br>PSDWE/PGPL1<br>POE/PSDRAS/PGPL2<br>PSDCAS/PGPL3<br>PGTA/PUPMWAIT/PGPL4/PPBS<br>PSDAMUX/PGPL5<br>LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3]<br>LSDA10/LGPL0/PCI_MODCKH0<br>LSDWE/LGPL1/PCI_MODCKH1<br>LOE/LSDRAS/LGPL2/PCI_MODCKH2<br>LSDCAS/LGPL3/PCI_MODCKH3<br>LGTA/LUPMWAIT/LGPL4/LPBS<br>LSDAMUX/LGPL5/PCI_MODCK<br>LWR<br>MODCK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2] | $V_{OL}$ | — | 0.4 | V |
| $I_{OL}$ = 3.2mA<br>L_A14/PAR<br>L_A15/FRAME/SMI<br>L_A16/TRDY<br>L_A17/IRDY/CKSTP_OUT<br>L_A18/STOP<br>L_A19/DEVSEL<br>L_A20/IDSEL<br>L_A21/PERR<br>L_A22/SERR<br>L_A23/REQ0<br>L_A24/REQ1/HSEJSW<br>L_A25/GNT0<br>L_A26/GNT1/HSLED<br>L_A27/GNT2/HSENUM<br>L_A28/RST/CORE_SRESET<br>L_A29/INTAL_A30/REQ2<br>L_A31<br>LCL_D[0-31)]/AD[0-31]<br>LCL_DP[03]/C/BE[0-3]<br>PA[0–31]<br>PB[4–31]<br>PC[0–31]<br>PD[4–31]<br>TDO<br>QREQ | | | | |

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, either pull unused pins to GND or VDDH or configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

4 $V_{IL}$ for IIC interface does not match IIC standard, but does meet IIC standard for $V_{OL}$ and should not cause any compatibility issue.
5 MPC8280, MPC8275VR, MPC8275ZQ only.

# 4 Thermal Characteristics

This table describes thermal characteristics for both the packages. See Table 2 for information on a given SoC's package. Discussions of each characteristic are provided in Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance," and Section 4.5, "Experimental Determination." For the these discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

**Table 6. Thermal Characteristics**

| Characteristic | Symbol | Value | | Unit | Air Flow |
|---|---|---|---|---|---|
| | | 480 TBGA | 516 PBGA | | |
| Junction to ambient—single-layer board[1] | $R_{\theta JA}$ | 16 | 27 | °C/W | Natural convection |
| | | 11 | 21 | | 1 m/s |
| Junction to ambient—four-layer board | $R_{\theta JA}$ | 12 | 19 | °C/W | Natural convection |
| | | 9 | 16 | | 1 m/s |
| Junction to board[2] | $R_{\theta JB}$ | 6 | 11 | °C/W | — |
| Junction to case[3] | $R_{\theta JC}$ | 2 | 8 | °C/W | — |
| Junction-to-package top[4] | $\Psi_{JT}$ | 2 | 2 | °C/W | — |

1 Assumes no thermal vias
2 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (°C)
$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)
$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

## 4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

## 4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

**Table 7. Estimated Power Dissipation for Various Configurations[1]**

| Bus (MHz) | CPM Multiplication Factor | CPM (MHz) | CPU Multiplication Factor | CPU (MHz) | $P_{INT}$(W)[2,3] | |
|---|---|---|---|---|---|---|
| | | | | | Vddl 1.5 Volts | |
| | | | | | Nominal | Maximum |
| 66.67 | 2.5 | 166 | 3.5 | 233 | 0.95 | 1.0 |
| 66.67 | 2.5 | 166 | 4 | 266 | 1.0 | 1.05 |
| 66.67 | 3 | 200 | 4 | 266 | 1.05 | 1.1 |
| 66.67 | 3.5 | 233 | 4.5 | 300 | 1.05 | 1.15 |
| 83.33 | 3 | 250 | 4 | 333 | 1.25 | 1.35 |
| 83.33 | 3 | 250 | 4.5 | 375 | 1.3 | 1.4 |
| 83.33 | 3.5 | 292 | 5 | 417 | 1.45 | 1.55 |
| 100 | 3 | 300 | 4 | 400 | 1.5 | 1.6 |
| 100 | 3 | 300 | 4.5 | 450 | 1.55 | 1.65 |

1 Test temperature = 105° C

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

3 Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.45 W (nominal), 0.5 W (maximum)
83.3 MHz = 0.5W (nominal), 0.6 W (maximum)
100 MHz = 0.6 W (nominal), 0.7 W (maximum)

# 6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

**Table 8. Output Buffer Impedances[1]**

| Output Buffers | Typical Impedance (Ω) |
|---|---|
| 60x bus | 45 or 27[2] |
| Local bus | 45 |
| Memory controller | 45 or 27[2] |
| Parallel I/O | 45 |
| PCI | 27 |

1 These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.

2 On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45 Ω.
On all other revisions, impedance value is selected through the SIUMCR[20,21]. See the SoC reference manual.

## 6.1 CPM AC Characteristics

This table lists CPM output characteristics.

**Table 9. AC Characteristics for CPM Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | Minimum Delay | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 66 MHz | 83 MHz | 100 MHz |
| sp36a | sp37a | FCC outputs—internal clock (NMSI) | 6 | 5.5 | 5.5 | 0.5 | 0.5 | 0.5 |
| sp36b | sp37b | FCC outputs—external clock (NMSI) | 8 | 8 | 8 | 2 | 2 | 2 |
| sp38a | sp39a | SCC/SMC/SPI/I2C outputs—internal clock (NMSI) | 10 | 10 | 10 | 0 | 0 | 0 |
| sp38b | sp39b | SCC/SMC/SPI/I2C outputs—external clock (NMSI) | 8 | 8 | 8 | 2 | 2 | 2 |
| sp40 | sp41 | TDM outputs/SI | 11 | 11 | 11 | 2.5 | 2.5 | 2.5 |
| sp42 | sp43 | TIMER/IDMA outputs | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 |
| sp42a | sp43a | PIO outputs | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 |

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 10. AC Characteristics for CPM Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | |
|---|---|---|---|---|---|---|---|---|
| Setup | Hold | | Setup | | | Hold | | |
| | | | 66 MHz | 83 MHz | 100 MHz | 66 MHz | 83 MHz | 100 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 6 | 6 | 6 | 0 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 2.5 | 2.5 | 2.5 | 2 | 2 | 2 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 6 | 6 | 6 | 0 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 4 | 4 | 4 | 2 | 2 | 2 |
| sp20 | sp21 | TDM inputs/SI | 5 | 5 | 5 | 2.5 | 2.5 | 2.5 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 8 | 8 | 8 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

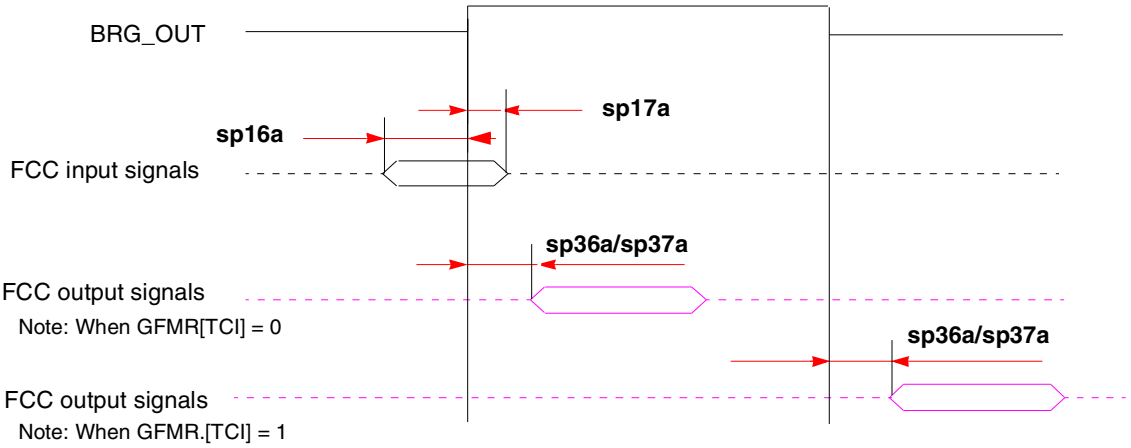



**Figure 3. FCC Internal Clock Diagram**

This figure shows the FCC external clock.

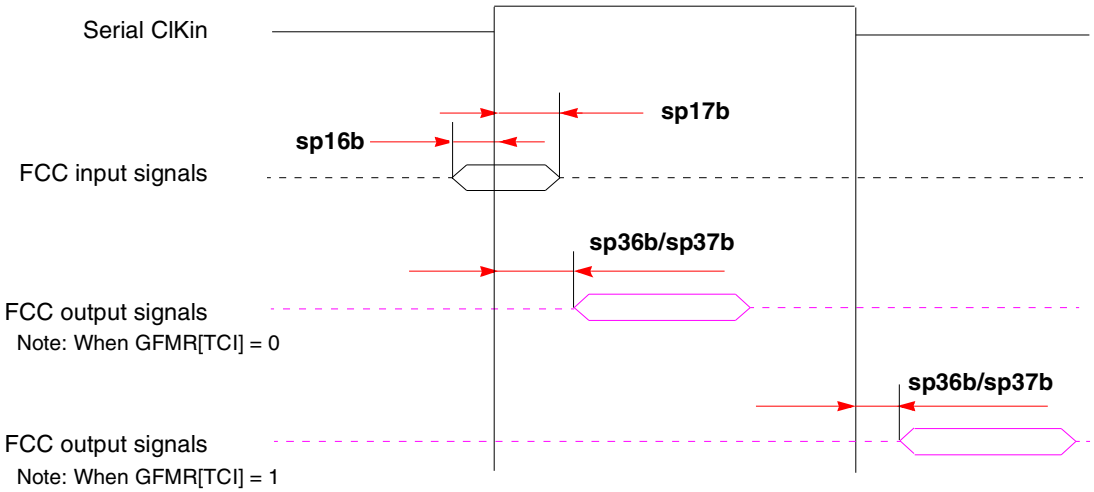
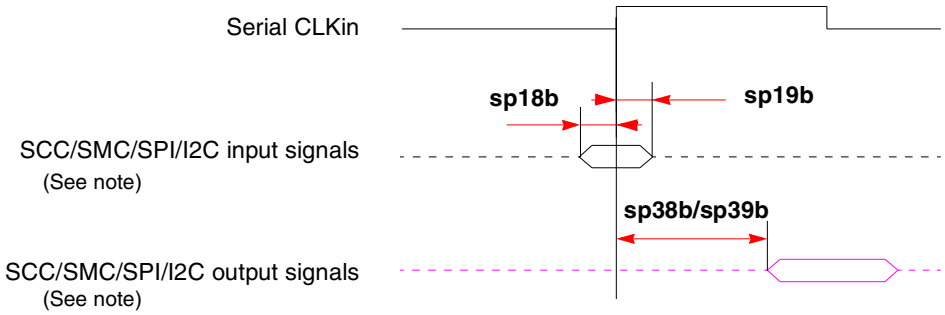



**Figure 4. FCC External Clock Diagram**

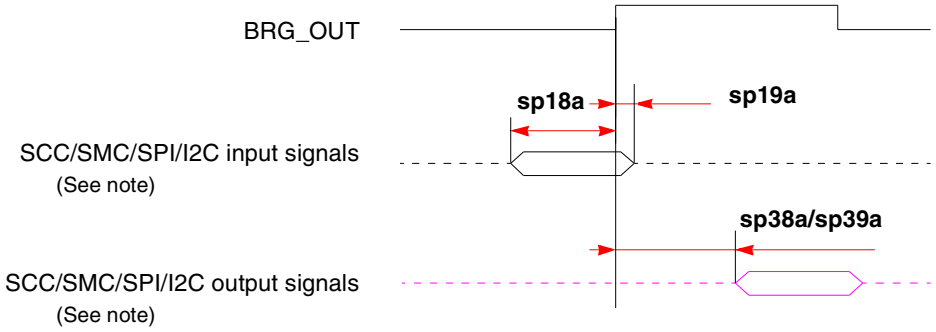
This figure shows the SCC/SMC/SPI/$I^2C$ external clock.




Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/$I^2C$ External Clock Diagram**

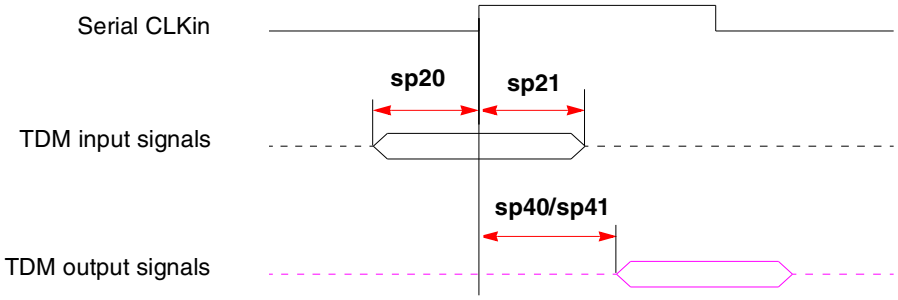
This figure shows the SCC/SMC/SPI/I$^2$C internal clock.




**Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I$^2$C Internal Clock Diagram**

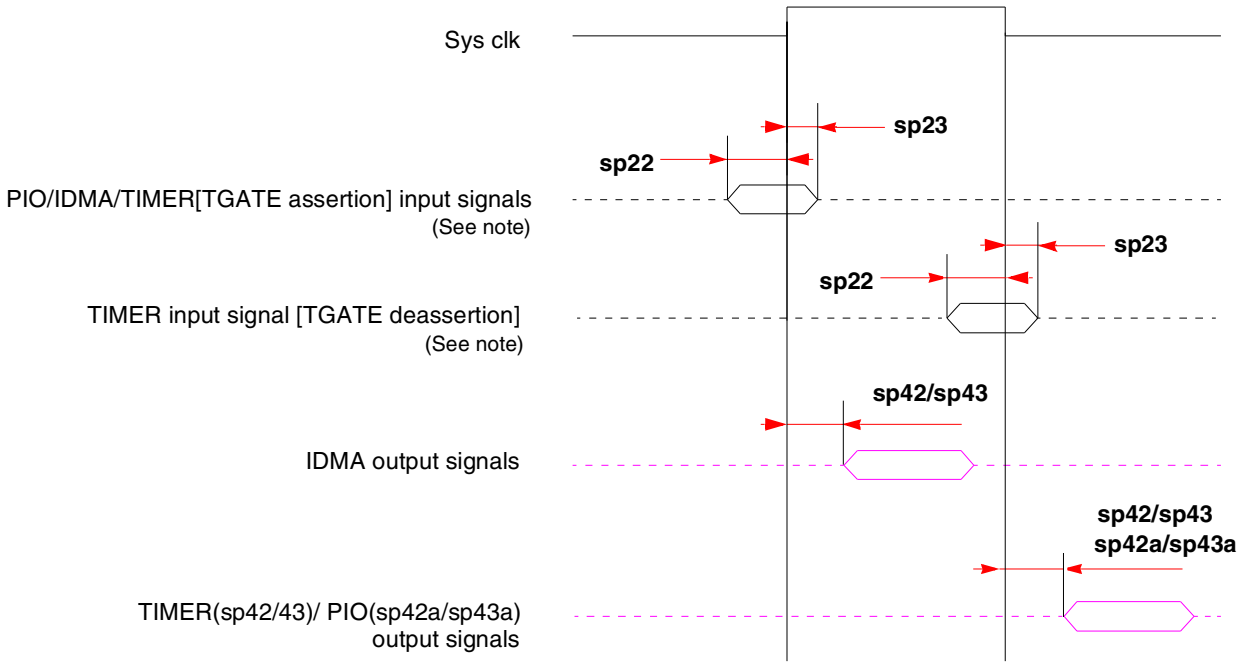
This figure shows TDM input and output signals.




**Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

This figure shows PIO and timer signals.




**Note:** TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

**Figure 8. PIO and Timer Signal Diagram**

## 6.2 SIU AC Characteristics

This table lists SIU input characteristics.

### NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/file time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.

### NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

### NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

### NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

**Table 11. AC Characteristics for SIU Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp11 | sp10 | $\overline{\text{AACK}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{ARTRY}}/\overline{\text{TEA}}$ | 6 | 5 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |
| sp12 | sp10 | Data bus in normal mode | 5 | 4 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |
| sp13 | sp10 | Data bus in pipeline mode (without ECC and PARITY) | N/A | 4 | 2.5 | 1.5 | N/A | 0.5 | 0.5 | 0.5 |
| sp15 | sp10 | All other pins | 5 | 4 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

**Table 12. AC Characteristics for SIU Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | | Minimum Delay | | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp31 | sp30 | $\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ | 7 | 6 | 5.5 | N/A | 1 | 1 | 1 | N/A |
| sp32 | sp30 | ADD/ADD_atr./BADDR/CI/GBL/WT | 8 | 6.5 | 5.5 | 4.5[2] | 1 | 1 | 1 | 1 [2] |
| sp33 | sp30 | Data bus[3] | 6.5 | 6.5 | 5.5 | 4.5 | 0.8 | 0.8 | 0.8 | 1 |
| sp34 | sp30 | Memory controller signals/ALE | 6 | 5.5 | 5.5 | 4.5 | 1 | 1 | 1 | 1 |
| sp35 | sp30 | All other signals | 6 | 5.5 | 5.5 | N/A | 1 | 1 | 1 | N/A |

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2 Value is for ADD only; other sp32/sp30 signals are not applicable.
3 To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.

**NOTE**

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing.

This table lists SIU input characteristics.

**Table 13. AC Characteristics for SIU Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | |
|---|---|---|---|---|---|---|---|---|
| Setup | Hold | | Setup | | | Hold | | |
| | | | 66 MHz | 83 MHz | 100 MHz | 66 MHz | 83 MHz | 100 MHz |
| sp11 | sp10 | $\overline{\text{AACK}}$/$\overline{\text{TA}}$/$\overline{\text{TS}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{ARTRY}}$/ $\overline{\text{TEA}}$ | 6 | 5 | 3.5 | 0.5 | 0.5 | 0.5 |
| sp12 | sp10 | Data bus in normal mode | 5 | 4 | 3.5 | 0.5 | 0.5 | 0.5 |
| sp13 | sp10 | Data bus in ECC and PARITY modes | 7 | 5 | 3.5 | 0.5 | 0.5 | 0.5 |
| sp13a | sp10 | Pipeline mode—Data bus (with or without ECC/PARITY) | 5 | 4 | 2.5 | 0.5 | 0.5 | 0.5 |
| sp14 | sp10 | DP pins | 7 | 5 | 3.5 | 0.5 | 0.5 | 0.5 |
| sp14a | sp10 | Pipeline mode—DP pins | — | 4 | 2.5 | — | 0.5 | 0.5 |
| sp15 | sp10 | All other pins | 5 | 4 | 3.5 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

**Table 14. AC Characteristics for SIU Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | |
|---|---|---|---|---|---|---|---|---|
| Max | Min | | Maximum Delay | | | Minimum Delay | | |
| | | | 66 MHz | 83 MHz | 100 MHz | 66 MHz | 83 MHz | 100 MHz |
| sp31 | sp30 | $\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ | 7 | 6 | 5.5 | 1 | 1 | 1 |
| sp32 | sp30 | ADD/ADD_atr./BADDR/CI/GBL/WT | 8 | 6.5 | 5.5 | 1 | 1 | 1 |
| sp33a | sp30 | Data bus[2] | 6.5 | 6.5 | 5.5 | 0.7 | 0.7 | 0.7 |
| sp33b | sp30 | DP | 6 | 5.5 | 5.5 | 1 | 1 | 1 |
| sp34 | sp30 | Memory controller signals/ALE | 6 | 5.5 | 5.5 | 1 | 1 | 1 |
| sp35 | sp30 | All other signals | 6 | 5.5 | 5.5 | 1 | 1 | 1 |
| sp35a | sp30 | AP | 7 | 7 | 7 | 1 | 1 | 1 |

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2 To achieve 1 ns of hold time at 66, 83, or 100 MHz, a minimum loading of 20 pF is required.

This figure shows the interaction of several bus signals.

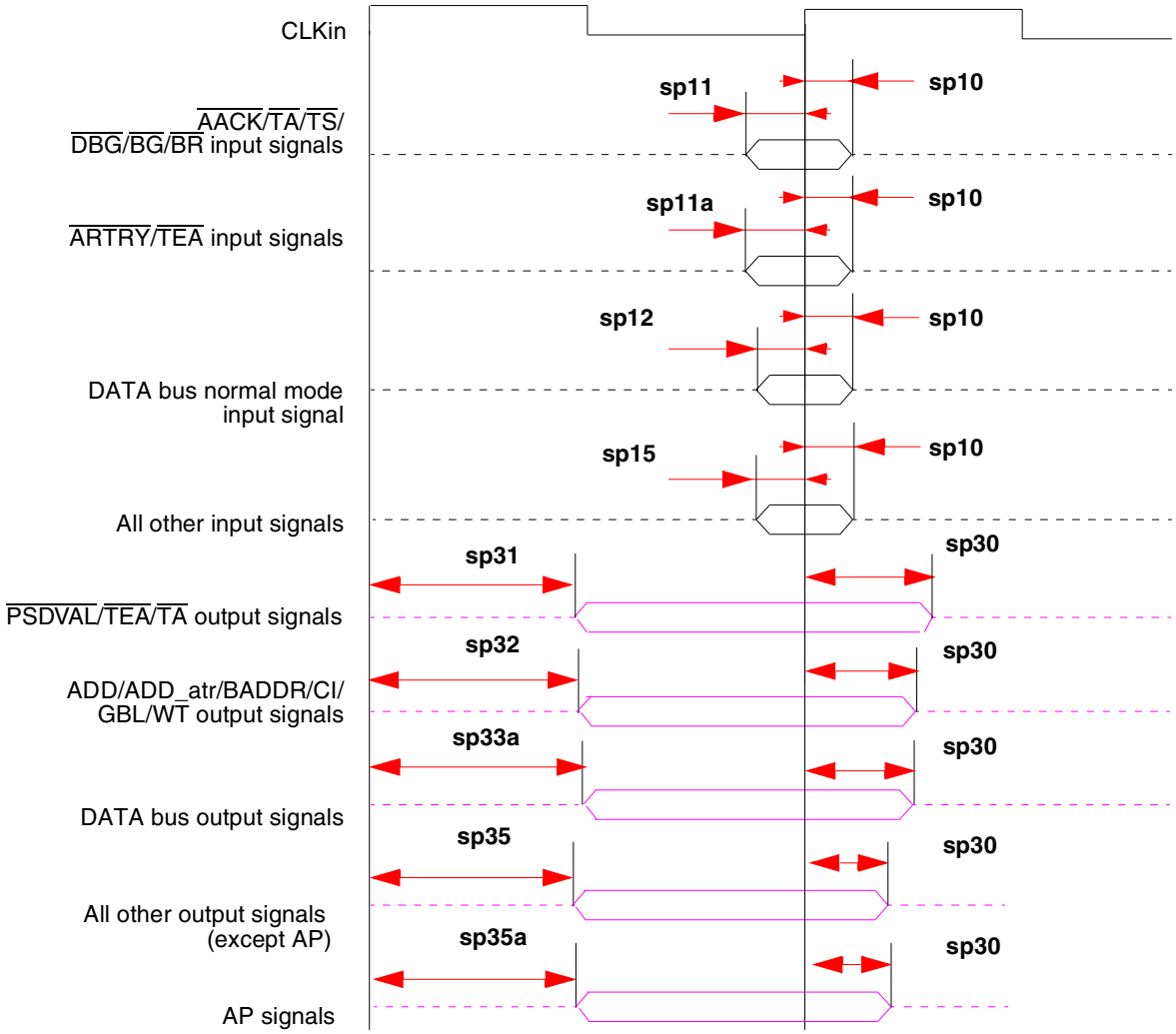



**Figure 9. Bus Signals**

This figure shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

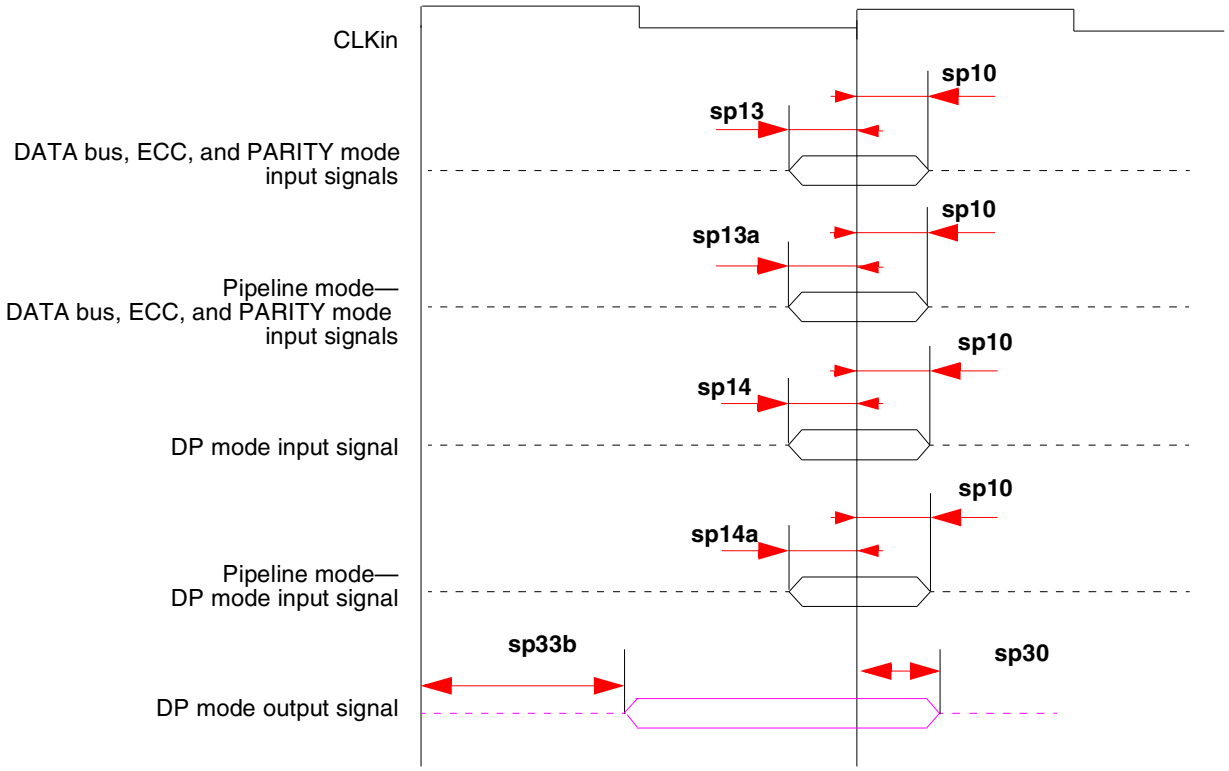



**Figure 10. Parity Mode Diagram**

This figure shows signal behavior in MEMC mode.

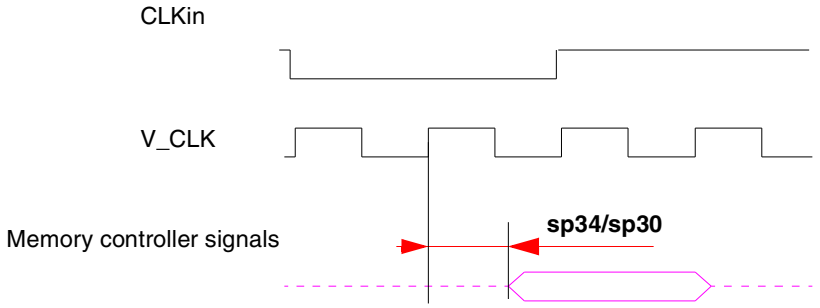



**Figure 11. MEMC Mode Diagram**

**NOTE**

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 15.

**Table 15. Tick Spacing for Memory Controller Signals**

| PLL Clock Ratio | Tick Spacing (T1 Occurs at the Rising Edge of CLKin) | | |
|---|---|---|---|
| | T2 | T3 | T4 |
| 1:2, 1:3, 1:4, 1:5, 1:6 | 1/4 CLKin | 1/2 CLKin | 3/4 CLKin |
| 1:2.5 | 3/10 CLKin | 1/2 CLKin | 8/10 CLKin |
| 1:3.5 | 4/14 CLKin | 1/2 CLKin | 11/14 CLKin |

This table is a representation of the information in Table 15.

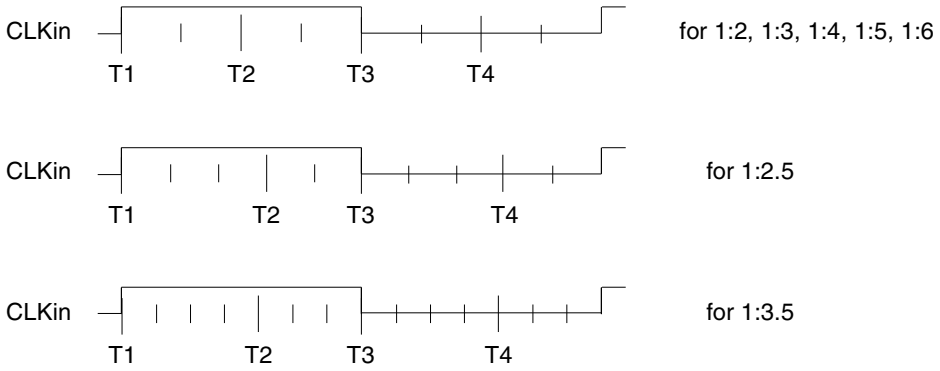



**Figure 12. Internal Tick Spacing for Memory Controller Signals**

**NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

## 6.3 JTAG Timings

This table lists the JTAG timings.

**Table 16. JTAG Timings[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ and $t_{JTGF}$ | 0 | 5 | ns | 6 |
| TRST assert time | $t_{TRST}$ | 25 | — | ns | 3, 6 |
| Input setup times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |

**Table 16. JTAG Timings[1] (continued)**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input hold times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Output valid times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>—<br>— | <br>10<br>10 | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| Output hold times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>1<br>1 | <br>—<br>— | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| JTAG external clock to output high impedance<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>1<br>1 | <br>10<br>10 | <br>ns<br>ns | <br>5, 6<br>5, 6 |

1 All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to $t_{TCLK}$.

5 Non-JTAG signal output timing with respect to $t_{TCLK}$.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

# 7 Clock Configuration Modes

This SoC includes the following clocking modes:

- Local
- PCI host
- PCI agent

The clocking mode is set according to the following input pins as shown in the following table:

- PCI_MODE
- PCI_CFG[0]
- PCI_MODCK

**Table 17. SoC Clocking Modes**

| Pins | | | Clocking Mode | PCI Clock Frequency Range (MHZ) | Reference |
|---|---|---|---|---|---|
| PCI_MODE | PCI_CFG[0] | PCI_MODCK[1] | | | |
| 1 | — | — | Local bus | — | Table 18 |
| 0 | 0 | 0 | PCI host | 50–66 | Table 19 |
| 0 | 0 | 1 | | 25–50 | Table 20 |
| 0 | 1 | 0 | PCI agent | 50–66 | Table 21 |
| 0 | 1 | 1 | | 25–50 | Table 22 |

1 Determines PCI clock frequency range. See Section 7.2, "PCI Host Mode," and Section 7.3, "PCI Agent Mode."

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

## 7.1 Local Bus Mode

This table lists clock configurations for the SoC in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

**NOTE**

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

**Table 18. Clock Configurations for Local Bus Mode[1]**

| Mode[2] | Bus Clock[3] (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1:3] | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H= 0000)** | | | | | | | | |
| 0000_000 | 37.5 | 133.3 | 3 | 112.5 | 400.0 | 4 | 150.0 | 533.3 |
| 0000_001 | 33.3 | 133.3 | 3 | 100.0 | 400.0 | 5 | 166.7 | 666.7 |
| 0000_010 | 37.5 | 100.0 | 4 | 150.0 | 400.0 | 4 | 150.0 | 400.0 |
| 0000_011 | 30.0 | 100.0 | 4 | 120.0 | 400.0 | 5 | 150.0 | 500.0 |
| 0000_100 | 60.0 | 167.0 | 2 | 120.0 | 334.0 | 2.5 | 150.0 | 417.5 |
| 0000_101 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 3 | 150.0 | 501.0 |
| 0000_110 | 60.0 | 160.0 | 2.5 | 150.0 | 400.0 | 2.5 | 150.0 | 400.0 |
| 0000_111 | 50.0 | 160.0 | 2.5 | 125.0 | 400.0 | 3 | 150.0 | 480.0 |
| **Full Configuration Modes** | | | | | | | | |
| 0001_000 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 4 | 200.0 | 668.0 |

**Table 18. Clock Configurations for Local Bus Mode[1] (continued)**

| Mode[2] | Bus Clock[3] (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1:3] | Low | High | | Low | High | | Low | High |
| 0001_001 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 5 | 250.0 | 835.0 |
| 0001_010 | 50.0 | 145.8 | 2 | 100.0 | 291.7 | 6 | 300.0 | 875.0 |
| 0001_011 | Reserved | | | | | | | |
| 0001_100 | Reserved | | | | | | | |
| | | | | | | | | |
| 0001_101 | 37.5 | 133.3 | 3 | 112.5 | 400.0 | 4 | 150.0 | 533.3 |
| 0001_110 | 33.3 | 133.3 | 3 | 100.0 | 400.0 | 5 | 166.7 | 666.7 |
| 1000_111 | 33.3 | 133.3 | 3 | 100.0 | 400.0 | 5.5 | 183.3 | 733.3 |
| 0001_111 | 33.3 | 133.3 | 3 | 100.0 | 400.0 | 6 | 200.0 | 800.0 |
| 0010_000 | Reserved | | | | | | | |
| 0010_001 | Reserved | | | | | | | |
| | | | | | | | | |
| 0010_010 | 37.5 | 100.0 | 4 | 150.0 | 400.0 | 4 | 150.0 | 400.0 |
| 0010_011 | 30.0 | 100.0 | 4 | 120.0 | 400.0 | 5 | 150.0 | 500.0 |
| 0010_100 | 25.0 | 100.0 | 4 | 100.0 | 400.0 | 6 | 150.0 | 600.0 |
| 0010_101 | 25.0 | 100.0 | 4 | 100.0 | 400.0 | 7 | 175.0 | 700.0 |
| 0010_110 | 25.0 | 100.0 | 4 | 100.0 | 400.0 | 8 | 200.0 | 800.0 |
| | | | | | | | | |
| 0010_111 | Reserved | | | | | | | |
| 0011_000 | 30.0 | 80.0 | 5 | 150.0 | 400.0 | 5 | 150.0 | 400.0 |
| 0011_001 | 25.0 | 80.0 | 5 | 125.0 | 400.0 | 6 | 150.0 | 480.0 |
| 0011_010 | 25.0 | 80.0 | 5 | 125.0 | 400.0 | 7 | 175.0 | 560.0 |
| 0011_011 | 25.0 | 80.0 | 5 | 125.0 | 400.0 | 8 | 200.0 | 640.0 |
| | | | | | | | | |
| 0011_100 | Reserved | | | | | | | |
| 0011_101 | Reserved | | | | | | | |
| 0011_110 | 25.0 | 66.7 | 6 | 150.0 | 400.0 | 6 | 150.0 | 400.0 |
| 0011_111 | 25.0 | 66.7 | 6 | 150.0 | 400.0 | 7 | 175.0 | 466.7 |
| 0100_000 | 25.0 | 66.7 | 6 | 150.0 | 400.0 | 8 | 200.0 | 533.3 |
| | | | | | | | | |
| 0101_101 | 75.0 | 167.0 | 2 | 150.0 | 334.0 | 2 | 166.7 | 334.0 |
| 0101_110 | 60.0 | 167.0 | 2 | 120.0 | 334.0 | 2.5 | 166.7 | 417.5 |
| 0101_111 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 3 | 200.0 | 501.0 |

**Table 18. Clock Configurations for Local Bus Mode[1] (continued)**

| Mode[2] | Bus Clock[3] (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1:3] | Low | High | | Low | High | | Low | High |
| 0110_000 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 3.5 | 250.0 | 584.5 |
| 0110_001 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 4 | 250.0 | 668.0 |
| 0110_010 | 50.0 | 167.0 | 2 | 100.0 | 334.0 | 4.5 | 250.0 | 751.5 |
| | | | | | | | | |
| 0110_011 | Reserved | | | | | | | |
| 0110_100 | 60.0 | 160.0 | 2.5 | 150.0 | 400.0 | 2.5 | 150.0 | 400.0 |
| 0110_101 | 50.0 | 160.0 | 2.5 | 125.0 | 400.0 | 3 | 150.0 | 480.0 |
| 0110_110 | 42.9 | 160.0 | 2.5 | 107.1 | 400.0 | 3.5 | 150.0 | 560.0 |
| 0110_111 | 40.0 | 160.0 | 2.5 | 100.0 | 400.0 | 4 | 160.0 | 640.0 |
| 0111_000 | 40.0 | 160.0 | 2.5 | 100.0 | 400.0 | 4.5 | 180.0 | 720.0 |
| | | | | | | | | |
| 0111_001 | Reserved | | | | | | | |
| 0111_010 | Reserved | | | | | | | |
| 0111_011 | 50.0 | 133.3 | 3 | 150.0 | 400.0 | 3 | 150.0 | 400.0 |
| 0111_100 | 42.9 | 133.3 | 3 | 128.6 | 400.0 | 3.5 | 150.0 | 466.7 |
| 0111_101 | 37.5 | 133.3 | 3 | 112.5 | 400.0 | 4 | 150.0 | 533.3 |
| 0111_110 | 33.3 | 133.3 | 3 | 100.0 | 400.0 | 4.5 | 150.0 | 600.0 |
| 0111_111 | Reserved | | | | | | | |
| | | | | | | | | |
| 1000_000 | Reserved | | | | | | | |
| 1000_001 | Reserved | | | | | | | |
| 1000_010 | 42.9 | 114.3 | 3.5 | 150.0 | 400.0 | 3.5 | 150.0 | 400.0 |
| 1000_011 | 37.5 | 114.3 | 3.5 | 131.3 | 400.0 | 4 | 150.0 | 457.1 |
| 1000_100 | 33.3 | 114.3 | 3.5 | 116.7 | 400.0 | 4.5 | 150.0 | 514.3 |
| 1000_101 | 30.0 | 114.3 | 3.5 | 105.0 | 400.0 | 5 | 150.0 | 571.4 |
| 1000_110 | 28.6 | 114.3 | 3.5 | 100.0 | 400.0 | 5.5 | 150.0 | 628.6 |
| | | | | | | | | |
| 1100_000 | Reserved | | | | | | | |
| 1100_001 | Reserved | | | | | | | |
| 1100_010 | Reserved | | | | | | | |
| | | | | | | | | |
| 1101_000 | Reserved | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

3 60x and local bus frequency. Identical to CLKIN.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

## 7.2 PCI Host Mode

These tables show clock configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI host mode the input clock is the following:

**NOTE: PCI_MODCK**

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

**NOTE: Tval (Output Hold)**

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

**Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |
| 0000_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_110 | 50.0 | 66.7 | 3.5 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0000_111 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_000 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 5 | 250.0 | 333.3 | 3 | 50.0 | 66.7 |

**Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0001_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 6 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0001_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 7 | 350.0 | 466.6 | 3 | 50.0 | 66.7 |
| 0001_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 8 | 400.0 | 533.3 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0010_000 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 5 | 250.0 | 333.3 | 4 | 50.0 | 66.7 |
| 0010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 6 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 0010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 7 | 350.0 | 466.6 | 4 | 50.0 | 66.7 |
| 0010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 8 | 400.0 | 533.3 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0010_100 | 75.0 | 100.0 | 4 | 300.0 | 400.0 | 5 | 375.0 | 500.0 | 6 | 50.0 | 66.7 |
| 0010_101 | 75.0 | 100.0 | 4 | 300.0 | 400.0 | 5.5 | 412.5 | 549.9 | 6 | 50.0 | 66.7 |
| 0010_110 | 75.0 | 100.0 | 4 | 300.0 | 400.0 | 6 | 450.0 | 599.9 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0011_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 250.0 | 333.3 | 5 | 50.0 | 66.7 |
| 0011_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 6 | 300.0 | 400.0 | 5 | 50.0 | 66.7 |
| 0011_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 7 | 350.0 | 466.6 | 5 | 50.0 | 66.7 |
| 0011_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 8 | 400.0 | 533.3 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 6 | 300.0 | 400.0 | 6 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 7 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 8 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0101_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0101_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3.5 | 175.0 | 233.3 | 2 | 50.0 | 66.7 |
| 0101_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4 | 200.0 | 266.6 | 2 | 50.0 | 66.7 |
| 0101_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4.5 | 225.0 | 300.0 | 2 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 2.5 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0110_001 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0110_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |

**Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0110_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0110_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 3 | 50.0 | 66.7 |
| 0110_101 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 5 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0110_110 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 6 | 360.0 | 480.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0111_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1000_010 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 4 | 50.0 | 66.7 |
| 1000_011 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 4 | 50.0 | 66.7 |
| 1000_100 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 1000_101 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 6 | 400.0 | 533.3 | 4 | 50.0 | 66.7 |
| 1000_110 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 6.5 | 433.3 | 577.7 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 3.5 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_011 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 4 | 228.6 | 304.7 | 4 | 50.0 | 66.7 |
| 1001_100 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 4.5 | 257.1 | 342.8 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1001_101 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 5 | 428.6 | 571.4 | 6 | 50.0 | 66.7 |
| 1001_110 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 5.5 | 471.4 | 628.5 | 6 | 50.0 | 66.7 |
| 1001_111 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 6 | 514.3 | 685.6 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 1010_001 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 3 | 50.0 | 66.7 |
| 1010_010 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |

**Table 19. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1010_011 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 3 | 50.0 | 66.7 |
| 1010_100 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 4 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1011_010 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 4 | 50.0 | 66.7 |
| 1011_011 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 4 | 50.0 | 66.7 |
| 1011_100 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 4 | 50.0 | 66.7 |
| 1011_101 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 4.5 | 360.0 | 480.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1101_000 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 5 | 50.0 | 66.7 |
| 1101_001 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 5 | 50.0 | 66.7 |
| 1101_010 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 5 | 50.0 | 66.7 |
| 1101_011 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 5 | 50.0 | 66.7 |
| 1101_100 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1101_101 | 125.0 | 166.7 | 2 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| 1101_110 | 125.0 | 166.7 | 2 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1110_000 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 3.5 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 1110_001 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| 1110_010 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 6 | 50.0 | 66.7 |
| 1110_011 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 6 | 50.0 | 66.7 |
| 1110_100 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As Table 17 shows, PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower configurations.

3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

4 60x and local bus frequency. Identical to CLKIN.

5 CPM multiplication factor = CPM clock/bus clock

6 CPU multiplication factor = Core PLL multiplication factor

**Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0000_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0000_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0000_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0000_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0000_101 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0000_110 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0000_111 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 0001_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 6 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0001_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 7 | 350.0 | 700.0 | 6 | 25.0 | 50.0 |
| 0001_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 8 | 400.0 | 800.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_000 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 0010_001 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 6 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 0010_010 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 7 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| 0010_011 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 8 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_100 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 0010_101 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5.5 | 206.3 | 412.5 | 6 | 25.0 | 50.0 |

**Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0010_110 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 6 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0011_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 5 | 150.0 | 250.0 | 5 | 30.0 | 50.0 |
| 0011_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 6 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 0011_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 7 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 0011_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 8 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 6 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 7 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 8 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0101_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0101_010 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3.5 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0101_011 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 4 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| 0101_100 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 4.5 | 225.0 | 450.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0110_001 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0110_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0110_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0110_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 6 | 25.0 | 50.0 |
| 0110_101 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 5 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0110_110 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 6 | 360.0 | 720.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0111_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0111_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 0111_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |

**Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |
| 1011_101 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4.5 | 360.0 | 720.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_000 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |

**Table 20. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock[4] (MHz) | | CPM Multiplication Factor[5] | CPM Clock (MHz) | | CPU Multiplication Factor[6] | CPU Clock (MHz) | | PCI Division Factor | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1101_001 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 1101_010 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| 1101_011 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 5 | 25.0 | 50.0 |
| 1101_100 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_101 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 5 | 25.0 | 50.0 |
| 1101_110 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 1110_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 1110_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1110_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 1110_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As Table 17 shows, PCI_MODCK determines the PCI clock frequency range. See Table 20 for higher configurations.

3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

4 60x and local bus frequency. Identical to CLKIN.

5 CPM multiplication factor = CPM clock/bus clock

6 CPU multiplication factor = Core PLL multiplication factor

## 7.3 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI agent mode the following:

### NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

### NOTE: Tval (Output Hold)

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

**Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0000_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0000_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 5 | 150.0 | 166.7 | 4 | 30.0 | 33.3 |
| 0001_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 6 | 150.0 | 200.0 | 4 | 25.0 | 33.3 |
| 0001_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 7 | 175.0 | 233.3 | 4 | 25.0 | 33.3 |
| 0001_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 8 | 200.0 | 266.6 | 4 | 25.0 | 33.3 |
| | | | | | | | | | | | |
| 0010_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0010_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0010_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 0010_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | Reserved | | | | | | | | | | |
| 0011_010 | Reserved | | | | | | | | | | |
| 0011_011 | Reserved | | | | | | | | | | |
| 0011_100 | Reserved | | | | | | | | | | |

**Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0100_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 250.0 | 333.3 | 2.5 | 100.0 | 133.3 |
| 0101_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 2.5 | 100.0 | 133.3 |
| 0101_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 2.5 | 100.0 | 133.3 |
| 0101_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 2.5 | 100.0 | 133.3 |
| 0101_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 2.5 | 100.0 | 133.3 |
| 0101_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 2.5 | 100.0 | 133.3 |
| 0101_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 550.0 | 733.3 | 2.5 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 0110_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0110_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 0110_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 0111_000 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 2 | 75.0 | 100.0 |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 2 | 75.0 | 100.0 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 2 | 75.0 | 100.0 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 2 | 75.0 | 100.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 150.0 | 166.7 | 2.5 | 60.0 | 80.0 |
| 1000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 1000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 1000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 1000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |

**Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 225.0 | 300.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 1010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 1010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 1010_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 2.5 | 80.0 | 106.7 |
| 1011_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| 1011_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 2.5 | 80.0 | 106.7 |
| 1011_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 2.5 | 80.0 | 106.7 |
| | | | | | | | | | | | |
| 1100_101 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 3 | 100.0 | 133.3 |
| 1100_110 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 3 | 100.0 | 133.3 |
| 1100_111 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 3 | 100.0 | 133.3 |
| 1101_000 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 3 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 1101_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 3.5 | 420.0 | 559.9 | 2.5 | 120.0 | 160.0 |
| 1101_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 480.0 | 639.9 | 2.5 | 120.0 | 160.0 |
| 1101_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 540.0 | 719.9 | 2.5 | 120.0 | 160.0 |
| 1101_100 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 600.0 | 799.9 | 2.5 | 120.0 | 160.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 312.5 | 416.6 | 2 | 125.0 | 166.7 |
| 1110_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 2 | 125.0 | 166.7 |
| 1110_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 437.5 | 583.3 | 2 | 125.0 | 166.7 |

**Table 21. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1110_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 2 | 125.0 | 166.7 |
| | | | | | | | | | | | |
| 1110_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 3 | 83.3 | 111.1 |
| 1110_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 3 | 83.3 | 111.1 |
| 1110_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 416.7 | 555.5 | 3 | 83.3 | 111.1 |
| 1110_111 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 458.3 | 611.1 | 3 | 83.3 | 111.1 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev 0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As shown in Table 17, PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower configurations.

3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/PCI clock

5 CPU multiplication factor = Core PLL multiplication factor

**Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 2 | 60.0 | 100.0 |
| 0000_001 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 2 | 50.0 | 100.0 |
| 0000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 0000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0000_110 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |

**Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0000_111 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0001_010 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 6 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0001_011 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 7 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0001_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 8 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0010_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0010_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 0010_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | 37.5 | 50.0 | 4 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0011_010 | 32.1 | 50.0 | 4 | 128.6 | 200.0 | 3.5 | 150.0 | 233.3 | 3 | 42.9 | 66.7 |
| 0011_011 | 28.1 | 50.0 | 4 | 112.5 | 200.0 | 4 | 150.0 | 266.7 | 3 | 37.5 | 66.7 |
| 0011_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 4.5 | 150.0 | 300.0 | 3 | 33.3 | 66.7 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 3 | 50.0 | 100.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 0100_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0101_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 2.5 | 150.0 | 250.0 | 2.5 | 60.0 | 100.0 |
| 0101_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 2.5 | 50.0 | 100.0 |
| 0101_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 2.5 | 50.0 | 100.0 |
| 0101_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 2.5 | 50.0 | 100.0 |
| 0101_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 2.5 | 50.0 | 100.0 |
| 0101_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 2.5 | 50.0 | 100.0 |
| 0101_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 275.0 | 550.0 | 2.5 | 50.0 | 100.0 |
| | | | | | | | | | | | |

**Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 0110_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0110_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 0110_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 0111_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 2 | 75.0 | 150.0 |
| 0111_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 2 | 75.0 | 150.0 |
| 0111_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 2 | 75.0 | 150.0 |
| 0111_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 2 | 75.0 | 150.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 2.5 | 60.0 | 120.0 |
| 1000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 1000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 200.0 | 400.0 | 4 | 50.0 | 100.0 |
| 1001_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 225.0 | 450.0 | 4 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 1010_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 1010_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 1010_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 2.5 | 80.0 | 160.0 |

**Table 22. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1011_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| 1011_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 2.5 | 80.0 | 160.0 |
| 1011_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 2.5 | 80.0 | 160.0 |
| | | | | | | | | | | | |
| 1100_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 1100_110 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| 1100_111 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 3 | 50.0 | 100.0 |
| 1101_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 1101_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1101_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1101_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| 1101_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5 | 300.0 | 600.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 1110_000 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 2.5 | 156.3 | 312.5 | 2 | 62.5 | 125.0 |
| 1110_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 2 | 62.5 | 125.0 |
| 1110_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3.5 | 218.8 | 437.5 | 2 | 62.5 | 125.0 |
| 1110_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 2 | 62.5 | 125.0 |
| | | | | | | | | | | | |
| 1110_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 166.7 | 333.3 | 3 | 41.7 | 83.3 |
| 1110_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 187.5 | 375.0 | 3 | 41.7 | 83.3 |
| 1110_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 208.3 | 416.7 | 3 | 41.7 | 83.3 |
| 1110_111 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 229.2 | 458.3 | 3 | 41.7 | 83.3 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor <= 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor >= 3.5: for Rev 0.1 the minimum CPU frequency is 250 MHz; for Rev A or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2 As shown in Table 17, PCI_MODCK determines the PCI clock range. See Table 20 for higher range configurations.
3 MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
4 CPM multiplication factor = CPM clock/PCI clock
5 CPU multiplication factor = Core PLL multiplication factor

# 8 Pinout

This section provides the pin assignments and pinout lists for both HiP7 PowerQUICC II packages.

## 8.1 ZU and VV Packages—MPC8280 and MPC8270

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, see Section 8.2, “VR and ZQ Packages—MPC8275 and MPC8270.”

This figure shows the pinout of the ZU and VV packages as viewed from the top surface.

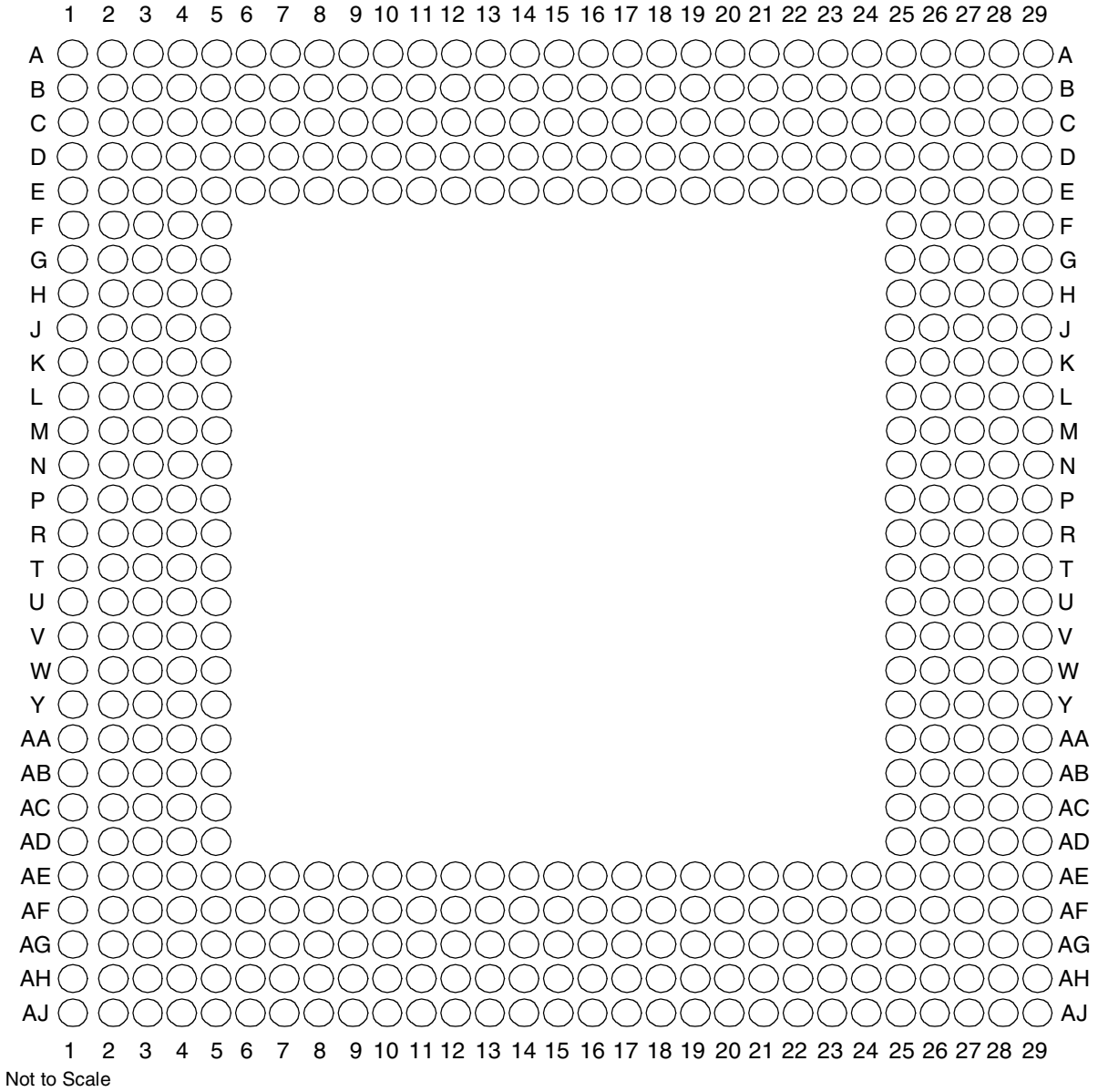



**Figure 13. Pinout of the 480 TBGA Package (View from Top)**

This table lists the pins of the MPC8280 and MPC8270, and Table 24 defines conventions and acronyms used in this table.

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| $\overline{BR}$ | | W5 |
| $\overline{BG}$ | | F4 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| $\overline{ABB}$/$\overline{IRQ2}$ | | E2 |
| $\overline{TS}$ | | E3 |
| A0 | | G1 |
| A1 | | H5 |
| A2 | | H2 |
| A3 | | H1 |
| A4 | | J5 |
| A5 | | J4 |
| A6 | | J3 |
| A7 | | J2 |
| A8 | | J1 |
| A9 | | K4 |
| A10 | | K3 |
| A11 | | K2 |
| A12 | | K1 |
| A13 | | L5 |
| A14 | | L4 |
| A15 | | L3 |
| A16 | | L2 |
| A17 | | L1 |
| A18 | | M5 |
| A19 | | N5 |
| A20 | | N4 |
| A21 | | N3 |
| A22 | | N2 |
| A23 | | N1 |
| A24 | | P4 |
| A25 | | P3 |
| A26 | | P2 |
| A27 | | P1 |
| A28 | | R1 |
| A29 | | R3 |
| A30 | | R5 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| A31 | | R4 |
| TT0 | | F1 |
| TT1 | | G4 |
| TT2 | | G3 |
| TT3 | | G2 |
| TT4 | | F2 |
| $\overline{\text{TBST}}$ | | D3 |
| TSIZ0 | | C1 |
| TSIZ1 | | E4 |
| TSIZ2 | | D2 |
| TSIZ3 | | F5 |
| $\overline{\text{AACK}}$ | | F3 |
| $\overline{\text{ARTRY}}$ | | E1 |
| $\overline{\text{DBG}}$ | | V1 |
| $\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$ | | V2 |
| D0 | | B20 |
| D1 | | A18 |
| D2 | | A16 |
| D3 | | A13 |
| D4 | | E12 |
| D5 | | D9 |
| D6 | | A6 |
| D7 | | B5 |
| D8 | | A20 |
| D9 | | E17 |
| D10 | | B15 |
| D11 | | B13 |
| D12 | | A11 |
| D13 | | E9 |
| D14 | | B7 |
| D15 | | B4 |
| D16 | | D19 |
| D17 | | D17 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| D18 | | D15 |
| D19 | | C13 |
| D20 | | B11 |
| D21 | | A8 |
| D22 | | A5 |
| D23 | | C5 |
| D24 | | C19 |
| D25 | | C17 |
| D26 | | C15 |
| D27 | | D13 |
| D28 | | C11 |
| D29 | | B8 |
| D30 | | A4 |
| D31 | | E6 |
| D32 | | E18 |
| D33 | | B17 |
| D34 | | A15 |
| D35 | | A12 |
| D36 | | D11 |
| D37 | | C8 |
| D38 | | E7 |
| D39 | | A3 |
| D40 | | D18 |
| D41 | | A17 |
| D42 | | A14 |
| D43 | | B12 |
| D44 | | A10 |
| D45 | | D8 |
| D46 | | B6 |
| D47 | | C4 |
| D48 | | C18 |
| D49 | | E16 |
| D50 | | B14 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| D51 | | C12 |
| D52 | | B10 |
| D53 | | A7 |
| D54 | | C6 |
| D55 | | D5 |
| D56 | | B18 |
| D57 | | B16 |
| D58 | | E14 |
| D59 | | D12 |
| D60 | | C10 |
| D61 | | E8 |
| D62 | | D6 |
| D63 | | C2 |
| DP0/RSRV/EXT_BR2 | | B22 |
| IRQ1/DP1/EXT_BG2 | | A22 |
| IRQ2/DP2/TLBISYNC/EXT_DBG2 | | E21 |
| IRQ3/DP3/CKSTP_OUT/EXT_BR3 | | D21 |
| IRQ4/DP4/CORE_SRESET/EXT_BG3 | | C21 |
| IRQ5/CINT/DP5/TBEN/EXT_DBG3 | | B21 |
| IRQ6/DP6/CSE0 | | A21 |
| IRQ7/DP7/CSE1 | | E20 |
| PSDVAL | | V3 |
| TA | | C22 |
| TEA | | V5 |
| GBL/IRQ1 | | W1 |
| CI/BADDR29/IRQ2 | | U2 |
| WT/BADDR30/IRQ3 | | U3 |
| L2_HIT/IRQ4 | | Y4 |
| CPU_BG/BADDR31/IRQ5/CINT | | U4 |
| CPU_DBG | | R2 |
| CPU_BR | | Y3 |
| CS0 | | F25 |
| CS1 | | C29 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| $\overline{CS2}$ | | E27 |
| $\overline{CS3}$ | | E28 |
| $\overline{CS4}$ | | F26 |
| $\overline{CS5}$ | | F27 |
| $\overline{CS6}$ | | F28 |
| $\overline{CS7}$ | | G25 |
| $\overline{CS8}$ | | D29 |
| $\overline{CS9}$ | | E29 |
| $\overline{CS10}$/$\overline{BCTL1}$ | | F29 |
| $\overline{CS11}$/AP0 | | G28 |
| BADDR27 | | T5 |
| BADDR28 | | U1 |
| ALE | | T2 |
| $\overline{BCTL0}$ | | A27 |
| $\overline{PWE0}$/$\overline{PSDDQM0}$/$\overline{PBS0}$ | | C25 |
| $\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$ | | E24 |
| $\overline{PWE2}$/$\overline{PSDDQM2}$/$\overline{PBS2}$ | | D24 |
| $\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$ | | C24 |
| $\overline{PWE4}$/$\overline{PSDDQM4}$/$\overline{PBS4}$ | | B26 |
| $\overline{PWE5}$/$\overline{PSDDQM5}$/$\overline{PBS5}$ | | A26 |
| $\overline{PWE6}$/$\overline{PSDDQM6}$/$\overline{PBS6}$ | | B25 |
| $\overline{PWE7}$/$\overline{PSDDQM7}$/$\overline{PBS7}$ | | A25 |
| PSDA10/PGPL0 | | E23 |
| $\overline{PSDWE}$/PGPL1 | | B24 |
| $\overline{POE}$/$\overline{PSDRAS}$/PGPL2 | | A24 |
| $\overline{PSDCAS}$/PGPL3 | | B23 |
| $\overline{PGTA}$/PUPMWAIT/PGPL4/$\overline{PPBS}$ | | A23 |
| PSDAMUX/PGPL5 | | D22 |
| $\overline{LWE0}$/$\overline{LSDDQM0}$/$\overline{LBS0}$/PCI_CFG0 | | H28 |
| $\overline{LWE1}$/$\overline{LSDDQM1}$/$\overline{LBS1}$/PCI_CFG1 | | H27 |
| $\overline{LWE2}$/$\overline{LSDDQM2}$/$\overline{LBS2}$/PCI_CFG2 | | H26 |
| $\overline{LWE3}$/$\overline{LSDDQM3}$/$\overline{LBS3}$/PCI_CFG3 | | G29 |
| LSDA10/LGPL0/PCI_MODCKH0 | | D27 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| LSDWE/LGPL1/PCI_MODCKH1 | | C28 |
| LOE/LSDRAS/LGPL2/PCI_MODCKH2 | | E26 |
| LSDCAS/LGPL3/PCI_MODCKH3 | | D25 |
| LGTA/LUPMWAIT/LGPL4/LPBS | | C26 |
| LGPL5/LSDAMUX/PCI_MODCK | | B27 |
| LWR | | D28 |
| L_A14/PAR | | N27 |
| L_A15/FRAME/SMI | | T29 |
| L_A16/TRDY | | R27 |
| L_A17/IRDY/CKSTP_OUT | | R26 |
| L_A18/STOP | | R29 |
| L_A19/DEVSEL | | R28 |
| L_A20/IDSEL | | W29 |
| L_A21/PERR | | P28 |
| L_A22/SERR | | N26 |
| L_A23/REQ0 | | AA27 |
| L_A24/REQ1/HSEJSW | | P29 |
| L_A25/GNT0 | | AA26 |
| L_A26/GNT1/HSLED | | N25 |
| L_A27/GNT2/HSENUM | | AA25 |
| L_A28/RST/CORE_SRESET | | AB29 |
| L_A29/INTA | | AB28 |
| L_A30/REQ2 | | P25 |
| L_A31/DLLOUT | | AB27 |
| LCL_D0/AD0 | | H29 |
| LCL_D1/AD1 | | J29 |
| LCL_D2/AD2 | | J28 |
| LCL_D3/AD3 | | J27 |
| LCL_D4/AD4 | | J26 |
| LCL_D5/AD5 | | J25 |
| LCL_D6/AD6 | | K25 |
| LCL_D7/AD7 | | L29 |
| LCL_D8/AD8 | | L27 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| LCL_D9/AD9 | | L26 |
| LCL_D10/AD10 | | L25 |
| LCL_D11/AD11 | | M29 |
| LCL_D12/AD12 | | M28 |
| LCL_D13/AD13 | | M27 |
| LCL_D14/AD14 | | M26 |
| LCL_D15/AD15 | | N29 |
| LCL_D16/AD16 | | T25 |
| LCL_D17/AD17 | | U27 |
| LCL_D18/AD18 | | U26 |
| LCL_D19/AD19 | | U25 |
| LCL_D20/AD20 | | V29 |
| LCL_D21/AD21 | | V28 |
| LCL_D22/AD22 | | V27 |
| LCL_D23/AD23 | | V26 |
| LCL_D24/AD24 | | W27 |
| LCL_D25/AD25 | | W26 |
| LCL_D26/AD26 | | W25 |
| LCL_D27/AD27 | | Y29 |
| LCL_D28/AD28 | | Y28 |
| LCL_D29/AD29 | | Y25 |
| LCL_D30/AD30 | | AA29 |
| LCL_D31/AD31 | | AA28 |
| LCL_DP0/C0/$\overline{\text{BE0}}$ | | L28 |
| LCL_DP1/C1/$\overline{\text{BE1}}$ | | N28 |
| LCL_DP2/C2/$\overline{\text{BE2}}$ | | T28 |
| LCL_DP3/C3/$\overline{\text{BE3}}$ | | W28 |
| $\overline{\text{IRQ0}}$/$\overline{\text{NMI_OUT}}$ | | T1 |
| $\overline{\text{IRQ7}}$/$\overline{\text{INT_OUT}}$/$\overline{\text{APE}}$ | | D1 |
| $\overline{\text{TRST}}$[1] | | AH3 |
| TCK | | AG5 |
| TMS | | AJ3 |
| TDI | | AE6 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| TDO | | AF5 |
| TRIS | | AB4 |
| $\overline{\text{PORESET}}$[1] | | AG6 |
| $\overline{\text{HRESET}}$ | | AH5 |
| $\overline{\text{SRESET}}$ | | AF6 |
| $\overline{\text{QREQ}}$ | | AA3 |
| $\overline{\text{RSTCONF}}$ | | AJ4 |
| MODCK1/AP1/TC0/BNKSEL0 | | W2 |
| MODCK2/AP2/TC1/BNKSEL1 | | W3 |
| MODCK3/AP3/TC2/BNKSEL2 | | W4 |
| CLKIN1 | | AH4 |
| PA0/$\overline{\text{RESTART1}}$/DREQ3 | FCC2_UTM_TXADDR2 | AC29[2] |
| PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$ | FCC2_UTM_TXADDR1 | AC25[2] |
| PA2/CLK20/$\overline{\text{DACK3}}$ | FCC2_UTM_TXADDR0 | AE28[2] |
| PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2 | FCC2_UTM_RXADDR0 | AG29[2] |
| PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$ | FCC2_UTM_RXADDR1 | AG28[2] |
| PA5/$\overline{\text{RESTART2}}$/DREQ4 | FCC2_UTM_RXADDR2/FCC1_UT_RXPRTY | AG26[2] |
| PA6/FCC2_RXADDR3 | L1RSYNCA1 | AE24[2] |
| PA7/SMSYN2/FCC2_TXADDR3 | L1TSYNCA1/L1GNTA1 | AH25[2] |
| PA8/SMRXD2/FCC2_TXADDR4 | L1RXD0A1/L1RXDA1 | AF23[2] |
| PA9/SMTXD2 | L1TXD0A1 | AH23[2] |
| PA10/MSNUM5 | FCC1_UT8_RXD0/FCC1_UT16_RXD8 | AE22[2] |
| PA11/MSNUM4 | FCC1_UT8_RXD1/FCC1_UT16_RXD9 | AH22[2] |
| PA12/MSNUM3 | FCC1_UT8_RXD2/ FCC1_UT16_RXD10 | AJ21[2] |
| PA13/MSNUM2 | FCC1_UT8_RXD3/ FCC1_UT16_RXD11 | AH20[2] |
| PA14/FCC1_MII_HDLC_RXD3 | FCC1_UT8_RXD4/ FCC1_UT16_RXD12 | AG19[2] |
| PA15/FCC1_MII_HDLC_RXD2 | FCC1_UT8_RXD5/ FCC1_UT16_RXD13 | AF18[2] |
| PA16/FCC1_MII_HDLC_RXD1/ FCCI_RMII_RXD1 | FCC1_UT8_RXD6/ FCC1_UT16_RXD14 | AF17[2] |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCCI_RMII_RXD0 | FCC1_UT8_RXD7/ FCC1_UT16_RXD15 | AE16[2] |
| PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0 | FCC1_UT8_TXD7/FCC1_UT16_TXD15 | AJ16[2] |
| PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1 | FCC1_UT8_TXD6/FCC1_UT16_TXD14 | AG15[2] |
| PA20/FCC1_MII_HDLC_TXD2 | FCC1_UT8_TXD5/FCC1_UT16_TXD13 | AJ13[2] |
| PA21/FCC1_MII_HDLC_TXD3 | FCC1_UT8_TXD4/FCC1_UT16_TXD12 | AE13[2] |
| PA22 | FCC1_UT8_TXD3/FCC1_UT16_TXD11 | AF12[2] |
| PA23 | FCC1_UT8_TXD2/FCC1_UT16_TXD10 | AG11[2] |
| PA24/MSNUM1 | FCC1_UT8_TXD1/FCC1_UT16_TXD9 | AH9[2] |
| PA25/MSNUM0 | FCC1_UT8_TXD0/FCC1_UT16_TXD8 | AJ8[2] |
| PA26/FCC1_RMII_RX_ER | FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV | AH7[2] |
| PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV | FCC1_UT_RXSOC | AF7[2] |
| PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN | $\overline{\text{FCC1_UTM_RXENB}}$/ $\overline{\text{FCC1_UTS_RXENB}}$ | AD5[2] |
| PA29/FCC1_MII_TX_ER | FCC1_UT_TXSOC | AF1[2] |
| PA30/FCC1_MII_CRS/$\overline{\text{FCC1_RTS}}$ | FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV | AD3[2] |
| PA31/FCC1_MII_COL | $\overline{\text{FCC1_UTM_TXENB}}$/ $\overline{\text{FCC1_UTS_TXENB}}$ | AB5[2] |
| PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3_RTS}}$ | FCC2_UT8_RXD0 | AD28[2] |
| PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2 | FCC2_UT8_RXD1 | AD26[2] |
| PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2 | FCC2_UT8_RXD2 | AD25[2] |
| PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2 | FCC2_UT8_RXD3 | AE26[2] |
| PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3 | FCC2_UT8_TXD3/L1RSYNCD1 | AH27[2] |
| PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2 | FCC2_UT8_TXD2/L1TSYNCD1/ L1GNTD1 | AG24[2] |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| PB10/FCC3_MII_HDLC_RXD2 | FCC2_UT8_TXD1/L1RXDD1 | AH24[2] |
| PB11/FCC3_MII_HDLC_RXD3 | FCC2_UT8_TXD0/L1TXDD1 | AJ24[2] |
| PB12/FCC3_MII_CRS/TXD2 | L1CLKOB1/L1RSYNCC1 | AG22[2] |
| PB13/FCC3_MII_COL/L1TXD1A2 | $\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1 | AH21[2] |
| PB14/FCC3_MII_RMII_TX_EN//RXD3 | L1RXDC1 | AG20[2] |
| PB15/FCC3_MII_TX_ER/RXD2 | L1TXDC1 | AF19[2] |
| PB16/FCC3_MII_RMII_RX_ER/CLK18 | L1CLKOA1 | AJ18[2] |
| PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV | L1RQA1 | AJ17[2] |
| PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2 | FCC2_UT8_RXD4 | AE14[2] |
| PB19FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2 | FCC2_UT8_RXD5 | AF13[2] |
| PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2 | FCC2_UT8_RXD6/L1TXD1A1 | AG12[2] |
| PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2 | FCC2_UT8_RXD7/L1TXD2A1 | AH11[2] |
| PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2 | FCC2_UT8_TXD7/L1RXD1A1 | AH16[2] |
| PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1 | FCC2_UT8_TXD6/L1RXD2A1 | AE15[2] |
| PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2 | FCC2_UT8_TXD5/L1RXD3A1 | AJ9[2] |
| PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2 | FCC2_UT8_TXD4/L1TXD3A1 | AE9[2] |
| PB26/FCC2_MII_CRS/L1RXDC2 | FCC2_UT8_TXD1 | AJ7[2] |
| PB27/FCC2_MII_COL/L1TXDC2 | FCC2_UT8_TXD0 | AH6[2] |
| PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/$\overline{\text{FCC2_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1 | | AE3[2] |
| PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN | FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV | AE2[2] |
| PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2 | FCC2_UT_TXSOC | AC5[2] |
| PB31/FCC2_MII_TX_ER/L1TXDB2 | FCC2_UT_RXSOC | AC4[2] |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2 | | AB26[2] |
| PC1/DREQ2/BRGO6/L1RQA2/ SPISEL | | AD29[2] |
| PC2/FCC3_CD/DONE2 | FCC2_UT8_TXD3 | AE29[2] |
| PC3/FCC3_CTS/DACK2/CTS4/ USB_RP | FCC2_UT8_TXD2 | AE27[2] |
| PC4/SI2_L1ST4/FCC2_CD | FCC2_UTM_RXENB/ FCC2_UTS_RXENB | AF27[2] |
| PC5/SI2_L1ST3/FCC2_CTS | FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV | AF24[2] |
| PC6/FCC1_CD | L1CLKOC1/FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1 | AJ26[2] |
| PC7/FCC1_CTS | L1RQC1/FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1 | AJ25[2] |
| PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USBRN | FCC1_UT16_TXD0 | AF22[2] |
| PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP | FCC1_UT16_TXD1 | AE21[2] |
| PC10/CD3/RENA3 | FCC1_UT16_TXD2/SI1_L1ST4/ FCC2_UT8_RXD3 | AF20[2] |
| PC11/CTS3/CLSN3/L1TXD3A2 | L1CLKOD1/FCC2_UT8_RXD2 | AE19[2] |
| PC12/CD2/RENA2 | SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1 | AE18[2] |
| PC13/CTS2/CLSN2 | L1RQD1/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1 | AH18[2] |
| PC14/CD1/RENA1 | FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0 | AH17[2] |
| PC15/CTS1/CLSN1/SMTXD2 | FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0 | AG16[2] |
| PC16/CLK16/TIN4 | | AF15[2] |
| PC17/CLK15/TIN3/BRGO8 | | AJ15[2] |
| PC18/CLK14/TGATE2 | | AH14[2] |
| PC19/CLK13/BRGO7/SPICLK | | AG13[2] |
| PC20/CLK12/TGATE1/USB_OE | | AH12[2] |
| PC21/CLK11/BRGO6 | | AJ11[2] |
| PC22/CLK10/DONE1/FCC1_UT_TXPRTY | | AG10[2] |
| PC23/CLK9/BRGO5/DACK1 | | AE10[2] |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| PC24/CLK8/$\overline{\text{TOUT4}}$ | FCC2_UT8_TXD3 | AF9[2] |
| PC25/CLK7/BRGO4 | FCC2_UT8_TXD2 | AE8[2] |
| PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK | | AJ6[2] |
| PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3 | | AG2[2] |
| PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2/ FCC2_RXADDR4 | | AF3[2] |
| PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1 | | AF2[2] |
| PC30/CLK2/$\overline{\text{TOUT1}}$ | FCC2_UT8_TXD3 | AE1[2] |
| PC31/CLK1/BRGO1 | | AD1[2] |
| PD4/BRGO8/$\overline{\text{FCC3_RTS}}$/SMRXD2 | L1TSYNCD1/L1GNTD1 | AC28[2] |
| PD5/$\overline{\text{DONE1}}$ | FCC1_UT16_TXD3 | AD27[2] |
| PD6/$\overline{\text{DACK1}}$ | FCC1_UT16_TXD4 | AF29[2] |
| PD7/SMSYN1/FCC1_TXCLAV2 | FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1 | AF28[2] |
| PD8/SMRXD1/BRGO5 | FCC2_UT_TXPRTY | AG25[2] |
| PD9/SMTXD1/BRGO3 | FCC2_UT_RXPRTY | AH26[2] |
| PD10/L1CLKOB2/BRGO4 | FCC2_UT8_RXD1/L1RSYNCB1 | AJ27[2] |
| PD11/$\overline{\text{L1RQB2}}$ | FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1 | AJ23[2] |
| PD12 | SI1_L1ST2/L1RXDB1 | AG23[2] |
| PD13 | SI1_L1ST1/L1TXDB1 | AJ22[2] |
| PD14/L1CLKOC2/I2CSCL | FCC1_UT16_RXD0 | AE20[2] |
| PD15/$\overline{\text{L1RQC2}}$/I2CSDA | FCC1_UT16_RXD1 | AJ20[2] |
| PD16/SPIMISO | FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1 | AG18[2] |
| PD17/BRGO2/SPIMOSI | FCC1_UT_RXPRTY | AG17[2] |
| PD18/SPICLK | FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0 | AF16[2] |
| PD19/SPISEL/BRGO1 | FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0 | AH15[2] |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8280/MPC8270** | **MPC8280 only** | |
| PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP | FCC1_UT16_RXD2 | AJ14[2] |
| PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN | FCC1_UT16_RXD3 | AH13[2] |
| PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD | FCC1_UT16_TXD5 | AJ12[2] |
| PD23/RTS3/TENA3 | FCC1_UT16_RXD4/L1RSYNCD1 | AE12[2] |
| PD24/TXD3 | FCC1_UT16_RXD5/L1RXDD1 | AF10[2] |
| PD25/RXD3 | FCC1_UT16_TXD6/L1TXDD1 | AG9[2] |
| PD26/RTS2/TENA2 | FCC1_UT16_RXD6/L1RSYNCC1 | AH8[2] |
| PD27/TXD2 | FCC1_UT16_RXD7/L1RXDC1 | AG7[2] |
| PD28/RXD2 | FCC1_UT16_TXD7/L1TXDC1 | AE4[2] |
| PD29/RTS1/TENA1 | FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1 | AG1[2] |
| PD30/TXD1 | FCC2_UTM_TXENB/ FCC2_UTS_TXENB | AD4[2] |
| PD31/RXD1 | | AD2[2] |
| VCCSYN | | AB3 |
| VCCSYN1 | | B9 |
| CLKIN2 | | AE11 |
| SPARE4[3] | | U5 |
| PCI_MODE[4] | | AF25 |
| SPARE6[3] | | V4 |
| No connect[5] | | AA1, AG4 |
| I/O power | | AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5 |

**Table 23. MPC8280 and MPC8270 (ZU and VV Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8280/MPC8270 | MPC8280 only | |
| Core power | | U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5 |
| Ground | | AA5, AB1[6], AB2[7], AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3 |

1 Should be tied to VDDH via a 2K Ω external pull-up resistor.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

3 Must be pulled down or left floating.

4 If PCI is not desired, must be pulled up or left floating.

5 Sphere is not connected to die.

6 GNDSYN (AB1): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the SoC. New designs must connect AB1 to GND and follow the suggestions in Section 4.6, “Layout Practices.” Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.

7 XFC (AB2) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8280 because there is no need for external capacitor to operate the PLL. New designs should connect AB2 (XFC) pin to GND. Old designs in which the SoC is used as a drop-in replacement can leave the pin connected to the current capacitor.

This table describes symbols used in Table 23.

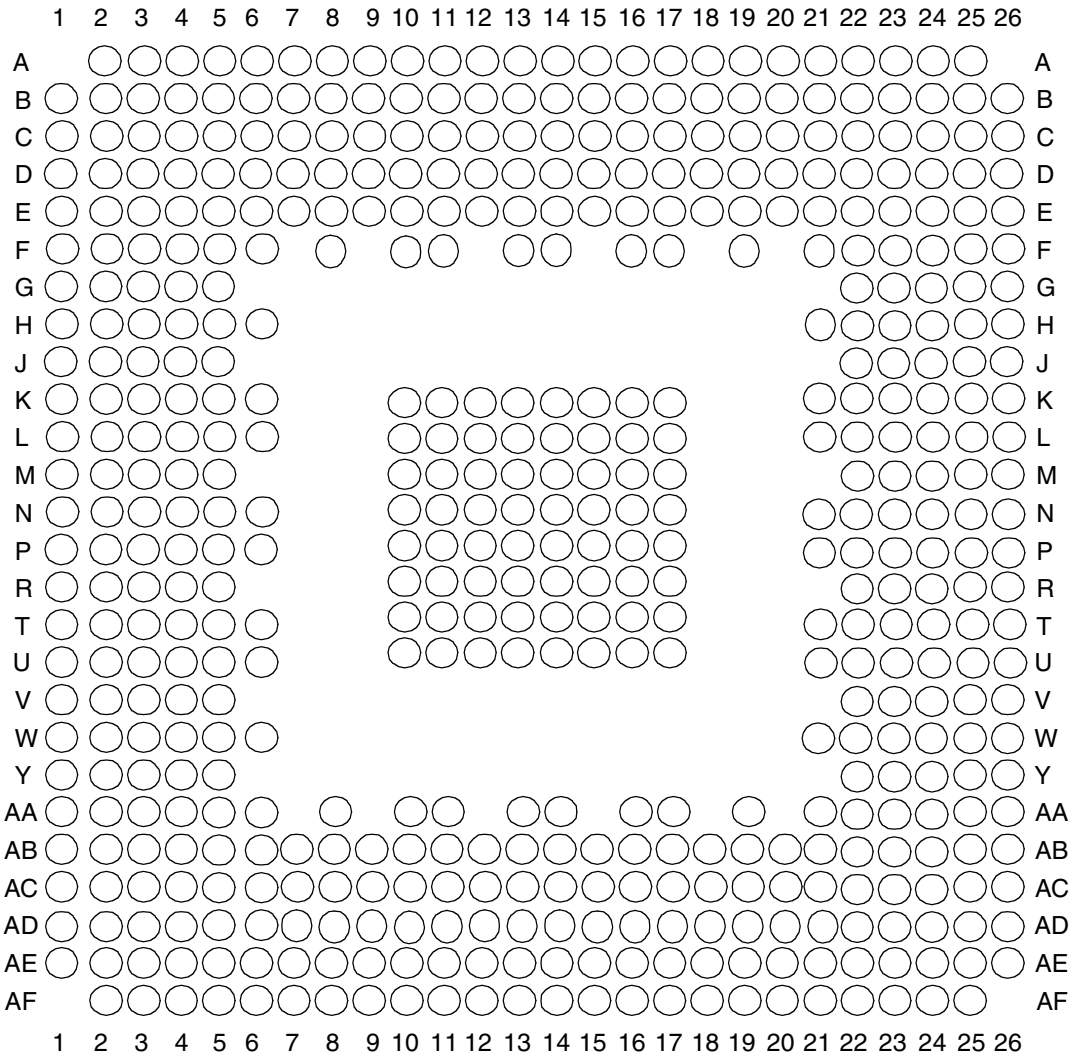
**Table 24. Symbol Legend**

| Symbol | Meaning |
|---|---|
| $\overline{\text{OVERBAR}}$ | Signals with overbars, such as $\overline{\text{TA}}$, are active low. |
| UTM | Indicates that a signal is part of the UTOPIA master interface. |
| UTS | Indicates that a signal is part of the UTOPIA slave interface. |
| UT8 | Indicates that a signal is part of the 8-bit UTOPIA interface. |
| UT16 | Indicates that a signal is part of the 16-bit UTOPIA interface. |
| MII | Indicates that a signal is part of the media independent interface. |
| RMII | Indicates that a signal is part of the reduced media independent interface. |

## 8.2 VR and ZQ Packages—MPC8275 and MPC8270

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8280 and the MPC8270, see Section 8.1, “ZU and VV Packages—MPC8280 and MPC8270.

This figure shows the pinout of the VR and ZQ packages as viewed from the top surface.




Not to Scale

**Figure 14. Pinout of the 516 PBGA Package (View from Top)**

This table shows the pinout list of the MPC8275 and MPC8270. Table 24 defines conventions and acronyms used in Table 25.

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| $\overline{\text{BR}}$ | | C16 |
| $\overline{\text{BG}}$ | | D2 |
| $\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$ | | C1 |
| $\overline{\text{TS}}$ | | D1 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| A0 | | D5 |
| A1 | | E8 |
| A2 | | C4 |
| A3 | | B4 |
| A4 | | A4 |
| A5 | | D7 |
| A6 | | D8 |
| A7 | | C6 |
| A8 | | B5 |
| A9 | | B6 |
| A10 | | C7 |
| A11 | | C8 |
| A12 | | A6 |
| A13 | | D9 |
| A14 | | F11 |
| A15 | | B7 |
| A16 | | B8 |
| A17 | | C9 |
| A18 | | A7 |
| A19 | | B9 |
| A20 | | E11 |
| A21 | | A8 |
| A22 | | D11 |
| A23 | | B10 |
| A24 | | C11 |
| A25 | | A9 |
| A26 | | B11 |
| A27 | | C12 |
| A28 | | D12 |
| A29 | | A10 |
| A30 | | B12 |
| A31 | | B13 |
| TT0 | | E7 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| TT1 | | B3 |
| TT2 | | F8 |
| TT3 | | A3 |
| TT4 | | C3 |
| $\overline{\text{TBST}}$ | | F5 |
| TSIZ0 | | E3 |
| TSIZ1 | | E2 |
| TSIZ2 | | E1 |
| TSIZ3 | | E4 |
| $\overline{\text{AACK}}$ | | D3 |
| $\overline{\text{ARTRY}}$ | | C2 |
| $\overline{\text{DBG}}$ | | A14 |
| $\overline{\text{DBB}}$/IRQ3 | | C15 |
| D0 | | W4 |
| D1 | | Y1 |
| D2 | | V1 |
| D3 | | P4 |
| D4 | | N3 |
| D5 | | K5 |
| D6 | | J4 |
| D7 | | G1 |
| D8 | | AB1 |
| D9 | | U4 |
| D10 | | U2 |
| D11 | | N6 |
| D12 | | N1 |
| D13 | | L1 |
| D14 | | J5 |
| D15 | | G3 |
| D16 | | AA2 |
| D17 | | W1 |
| D18 | | T3 |
| D19 | | T1 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| D20 | | M2 |
| D21 | | K2 |
| D22 | | J1 |
| D23 | | G4 |
| D24 | | U5 |
| D25 | | T5 |
| D26 | | P5 |
| D27 | | P3 |
| D28 | | M3 |
| D29 | | K3 |
| D30 | | H2 |
| D31 | | G5 |
| D32 | | AA1 |
| D33 | | V2 |
| D34 | | U1 |
| D35 | | P2 |
| D36 | | M4 |
| D37 | | K4 |
| D38 | | H3 |
| D39 | | F2 |
| D40 | | Y2 |
| D41 | | U3 |
| D42 | | T2 |
| D43 | | N2 |
| D44 | | M5 |
| D45 | | K1 |
| D46 | | H4 |
| D47 | | F1 |
| D48 | | W2 |
| D49 | | T4 |
| D50 | | R3 |
| D51 | | N4 |
| D52 | | M1 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| D53 | | J2 |
| D54 | | H5 |
| D55 | | F3 |
| D56 | | V3 |
| D57 | | R5 |
| D58 | | R2 |
| D59 | | N5 |
| D60 | | L2 |
| D61 | | J3 |
| D62 | | H1 |
| D63 | | F4 |
| DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT_BR2}}$ | | AB3 |
| $\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT_BG2}}$ | | W5 |
| $\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT_DBG2}}$ | | AC2 |
| $\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP_OUT}}$/$\overline{\text{EXT_BR3}}$ | | AA3 |
| $\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE_SRESET}}$/$\overline{\text{EXT_BG3}}$ | | AD1 |
| $\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT_DBG3}}$ | | AC1 |
| $\overline{\text{IRQ6}}$/DP6/CSE0 | | AB2 |
| $\overline{\text{IRQ7}}$/DP7/CSE1 | | Y3 |
| $\overline{\text{PSDVAL}}$ | | D15 |
| $\overline{\text{TA}}$ | | Y4 |
| $\overline{\text{TEA}}$ | | D16 |
| $\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$ | | E15 |
| $\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$ | | D14 |
| $\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$ | | E14 |
| $\overline{\text{L2_HIT}}$/$\overline{\text{IRQ4}}$ | | A17 |
| $\overline{\text{CPU_BG}}$/BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$ | | B14 |
| $\overline{\text{CPU_DBG}}$ | | F13 |
| $\overline{\text{CPU_BR}}$ | | B17 |
| $\overline{\text{CS0}}$ | | AC6 |
| $\overline{\text{CS1}}$ | | AD6 |
| $\overline{\text{CS2}}$ | | AE6 |
| $\overline{\text{CS3}}$ | | AB7 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| CS4 | | AF7 |
| CS5 | | AC7 |
| CS6 | | AD7 |
| CS7 | | AF8 |
| CS8 | | AE8 |
| CS9 | | AD8 |
| CS10/BCTL1 | | AC8 |
| CS11/AP0 | | AB8 |
| BADDR27 | | C13 |
| BADDR28 | | A12 |
| ALE | | D13 |
| BCTL0 | | AF4 |
| PWE0/PSDDQM0/PBS0 | | AA5 |
| PWE1/PSDDQM1/PBS1 | | AE4 |
| PWE2/PSDDQM2/PBS2 | | AD4 |
| PWE3/PSDDQM3/PBS3 | | AF3 |
| PWE4/PSDDQM4/PBS4 | | AB4 |
| PWE5/PSDDQM5/PBS5 | | AE3 |
| PWE6/PSDDQM6/PBS6 | | AF2 |
| PWE7/PSDDQM7/PBS7 | | AD3 |
| PSDA10/PGPL0 | | AE2 |
| PSDWE/PGPL1 | | AD2 |
| POE/PSDRAS/PGPL2 | | AE1 |
| PSDCAS/PGPL3 | | AC3 |
| PGTA/PUPMWAIT/PGPL4/PPBS | | W6 |
| PSDAMUX/PGPL5 | | AA4 |
| LWE0/LSDDQM0/LBS0/PCI_CFG0 | | AC9 |
| LWE1/LSDDQM1/LBS1/PCI_CFG1 | | AD9 |
| LWE2/LSDDQM2/LBS2/PCI_CFG2 | | AE9 |
| LWE3/LSDDQM3/LBS3/PCI_CFG3 | | AF9 |
| LSDA10/LGPL0/PCI_MODCKH0 | | AB6 |
| LSDWE/LGPL1/PCI_MODCKH1 | | AF5 |
| LOE/LSDRAS/LGPL2/PCI_MODCKH2 | | AE5 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| LSDCAS/LGPL3/PCI_MODCKH3 | | AD5 |
| LGTA/LUPMWAIT/LGPL4/LPBS | | AC5 |
| LGPL5/LSDAMUX/PCI_MODCK | | AB5 |
| LWR | | AF6 |
| L_A14/PAR | | AE13 |
| L_A15/FRAME/SMI | | AD15 |
| L_A16/TRDY | | AF16 |
| L_A17/IRDY/CKSTP_OUT | | AF15 |
| L_A18/STOP | | AE15 |
| L_A19/DEVSEL | | AE14 |
| L_A20/IDSEL | | AC17 |
| L_A21/PERR | | AD14 |
| L_A22/SERR | | AF13 |
| L_A23/REQ0 | | AE20 |
| L_A24/REQ1/HSEJSW | | AC14 |
| L_A25/GNT0 | | AC19 |
| L_A26/GNT1/HSLED | | AD13 |
| L_A27/GNT2/HSENUM | | AF21 |
| L_A28/RST/CORE_SRESET | | AF22 |
| L_A29/INTA | | AE21 |
| L_A30/REQ2 | | AB14 |
| L_A31/DLLOUT | | AD20 |
| LCL_D0/AD0 | | AB9 |
| LCL_D1/AD1 | | AB10 |
| LCL_D2/AD2 | | AC10 |
| LCL_D3/AD3 | | AD10 |
| LCL_D4/AD4 | | AE10 |
| LCL_D5/AD5 | | AF10 |
| LCL_D6/AD6 | | AF11 |
| LCL_D7/AD7 | | AB12 |
| LCL_D8/AD8 | | AB11 |
| LCL_D9/AD9 | | AF12 |
| LCL_D10/AD10 | | AE11 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| LCL_D11/AD11 | | AC13 |
| LCL_D12/AD12 | | AC12 |
| LCL_D13/AD13 | | AB13 |
| LCL_D14/AD14 | | AD12 |
| LCL_D15/AD15 | | AF14 |
| LCL_D16/AD16 | | AF17 |
| LCL_D17/AD17 | | AE16 |
| LCL_D18/AD18 | | AD16 |
| LCL_D19/AD19 | | AC16 |
| LCL_D20/AD20 | | AB16 |
| LCL_D21/AD21 | | AF18 |
| LCL_D22/AD22 | | AE17 |
| LCL_D23/AD23 | | AD17 |
| LCL_D24/AD24 | | AB17 |
| LCL_D25/AD25 | | AE18 |
| LCL_D26/AD26 | | AD18 |
| LCL_D27/AD27 | | AC18 |
| LCL_D28/AD28 | | AE19 |
| LCL_D29/AD29 | | AF20 |
| LCL_D30/AD30 | | AD19 |
| LCL_D31/AD31 | | AB18 |
| LCL_DP0/C0/$\overline{\text{BE0}}$ | | AE12 |
| LCL_DP1/C1/$\overline{\text{BE1}}$ | | AA13 |
| LCL_DP2/C2/$\overline{\text{BE2}}$ | | AC15 |
| LCL_DP3/C3/$\overline{\text{BE3}}$ | | AF19 |
| $\overline{\text{IRQ0}}$/$\overline{\text{NMI_OUT}}$ | | A11 |
| $\overline{\text{IRQ7}}$/$\overline{\text{INT_OUT}}$/$\overline{\text{APE}}$ | | E5 |
| $\overline{\text{TRST}}$[1] | | F22 |
| TCK | | A24 |
| TMS | | C24 |
| TDI | | A25 |
| TDO | | B24 |
| $\overline{\text{TRIS}}$ | | C19 |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PORESET[2] | | B25 |
| HRESET | | D24 |
| SRESET | | E23 |
| QREQ | | D18 |
| RSTCONF | | E24 |
| MODCK1/AP1/TC0/BNKSEL0 | | B16 |
| MODCK2/AP2/TC1/BNKSEL1 | | F16 |
| MODCK3/AP3/TC2/BNKSEL2 | | A15 |
| CLKIN1 | | G22 |
| PA0/RESTART1/DREQ3 | FCC2_UTM_TXADDR2 | AC20[2] |
| PA1/REJECT1/DONE3 | FCC2_UTM_TXADDR1 | AC21[2] |
| PA2/CLK20/DACK3 | FCC2_UTM_TXADDR0 | AF25[2] |
| PA3/CLK19/DACK4/L1RXD1A2 | FCC2_UTM_RXADDR0 | AE24[2] |
| PA4/REJECT2/DONE4 | FCC2_UTM_RXADDR1 | AA21[2] |
| PA5/RESTART2/DREQ4 | FCC2_UTM_RXADDR2 | AD25[2] |
| PA6 | FCC2_UT_RXADDR3 | AC24[2] |
| PA7/SMSYN2 | FCC2_UT_TXADDR3 | AA22[2] |
| PA8/SMRXD2 | FCC2_UT_TXADDR4 | AA23[2] |
| PA9/SMTXD2 | | Y26[2] |
| PA10/MSNUM5 | FCC1_UT8_RXD0/FCC1_UT16_RXD8 | W22[2] |
| PA11/MSNUM4 | FCC1_UT8_RXD1/FCC1_UT16_RXD9 | W23[2] |
| PA12/MSNUM3 | FCC1_UT8_RXD2/<br>FCC1_UT16_RXD10 | V26[2] |
| PA13/MSNUM2 | FCC1_UT8_RXD3/<br>FCC1_UT16_RXD11 | V25[2] |
| PA14/FCC1_MII_HDLC_RXD3 | FCC1_UT8_RXD4/<br>FCC1_UT16_RXD12 | T22[2] |
| PA15/FCC1_MII_HDLC_RXD2 | /FCC1_UT8_RXD5/<br>FCC1_UT16_RXD13 | T25[2] |
| PA16/FCC1_MII_HDLC_RXD1/<br>FCC1_RMII_RXD1 | FCC1_UT8_RXD6/<br>FCC1_UT16_RXD14 | R24[2] |
| PA17/FCC_MII_HDLC_RXD0/<br>FCC1_MII_TRAN_RXD/<br>FCCI_RMII_RXD0 | FCC1_UT8_RXD7/<br>FCC1_UT16_RXD15 | P22[2] |
| PA18/FCC1_MII_HDLC_TXD0/<br>FCC1_MII_TRAN_TXD/<br>FCC1_RMII_TXD0 | FCC1_UT8_TXD7/FCC1_UT16_TXD15 | N26[2] |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1 | FCC1_UT8_TXD6/FCC1_UT16_TXD14 | N23[2] |
| PA20/FCC1_MII_HDLC_TXD2 | FCC1_UT8_TXD5/FCC1_UT16_TXD13 | K26[2] |
| PA21/FCC1_MII_HDLC_TXD3 | FCC1_UT8_TXD4/FCC1_UT16_TXD12 | L23[2] |
| PA22 | FCC1_UT8_TXD3/FCC1_UT16_TXD11 | K23[2] |
| PA23 | FCC1_UT8_TXD2/FCC1_UT16_TXD10 | H26[2] |
| PA24/MSNUM1 | FCC1_UT8_TXD1/FCC1_UT16_TXD9 | F25[2] |
| PA25/MSNUM0 | FCC1_UT8_TXD0/FCC1_UT16_TXD8 | D26[2] |
| PA26/FCC1_MII_RMII_RX_ER/ | FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV | D25[2] |
| PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV | FCC1_UT_RXSOC | C25[2] |
| PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN | $\overline{\text{FCC1_UTM_RXENB}}$/ $\overline{\text{FCC1_UTS_RXENB}}$ | C22[2] |
| PA29/FCC1_MII_TX_ER | FCC1_UT_TXSOC | B21[2] |
| PA30/FCC1_MII_CRS/$\overline{\text{FCC1_RTS}}$ | FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV | A20[2] |
| PA31/FCC1_MII_COL | $\overline{\text{FCC1_UTM_TXENB}}$/ $\overline{\text{FCC1_UTS_TXENB}}$ | A19[2] |
| PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3_RTS}}$ | FCC2_UT8_RXD0 | AD21[2] |
| PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2 | FCC2_UT8_RXD1 | AD22[2] |
| PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2 | FCC2_UT8_RXD2 | AC22[2] |
| PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2 | FCC2_UT8_RXD3 | AE26[2] |
| PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3 | FCC2_UT8_TXD3 | AB23[2] |
| PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2 | FCC2_UT8_TXD2 | AC26[2] |
| PB10/FCC3_MII_HDLC_RXD2 | FCC2_UT8_TXD1 | AB26[2] |
| PB11/FCC3_MII_HDLC_RXD3 | FCC2_UT8_TXD0 | AA25[2] |
| PB12/FCC3_MII_CRS/TXD2 | | W26[2] |
| PB13/FCC3_MII_COL/L1TXD1A2 | | W25[2] |
| PB14/FCC3_MII_RMII_TX_EN/RXD3 | | V24[2] |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PB15/FCC3_MII_TX_ER/RXD2 | | U24[2] |
| PB16/FCC3_MII_RMII_RX_ER/CLK18 | | R22[2] |
| PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV | | R23[2] |
| PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2 | FCC2_UT8_RXD4 | M23[2] |
| PB19FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2 | FCC2_UT8_RXD5 | L24[2] |
| PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2 | FCC2_UT8_RXD6 | K24[2] |
| PB21//FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2 | FCC2_UT8_RXD7 | L21[2] |
| PB22/FCC2_MII_HDLC_RMII_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2 | FCC2_UT8_TXD7 | P25[2] |
| PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1 | FCC2_UT8_TXD6 | N25[2] |
| PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2 | FCC2_UT8_TXD5 | E26[2] |
| PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2 | FCC2_UT8_TXD4 | H23[2] |
| PB26/FCC2_MII_CRS/L1RXDC2 | FCC2_UT8_TXD1 | C26[2] |
| PB27/FCC2_MII_COL/L1TXDC2 | FCC2_UT8_TXD0 | B26[2] |
| PB28/FCC2_MII_RX_ER/FCC2_RMII_RX_ER/ $\overline{\text{FCC2_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1 | | A22[2] |
| PB29/L1RSYNCB2/ FCC2_MII_TX_EN/FCC2_RMII_TX_EN | FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV | A21[2] |
| PB30/FCC2_MII_RX_DV/L1RXDB2/ FCC2_RMII_CRS_DV | FCC2_UT_TXSOC | E20[2] |
| PB31/FCC2_MII_TX_ER/L1TXDB2 | FCC2_UT_RXSOC | C20[2] |
| PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/ L1CLKOA2 | | AE22[2] |
| PC1/DREQ2/$\overline{\text{SPISEL}}$/BRGO6/$\overline{\text{L1RQA2}}$ | | AA19[2] |
| PC2/$\overline{\text{FCC3_CD}}$/$\overline{\text{DONE2}}$ | FCC2_UT8_TXD3 | AF24[2] |
| PC3/$\overline{\text{FCC3_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$/ USB_RP | FCC2_UT8_TXD2 | AE25[2] |
| PC4/SI2_L1ST4/$\overline{\text{FCC2_CD}}$ | $\overline{\text{FCC2_UTM_RXENB}}$/ $\overline{\text{FCC2_UTS_RXENB}}$ | AB22[2] |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PC5/SI2_L1ST3/FCC2_CTS | FCC2_UTM_TXCLAV/<br>FCC2_UTS_TXCLAV | AC25[2] |
| PC6/FCC1_CD | FCC1_UTM_RXADDR2/<br>FCC1_UTS_RXADDR2/<br>FCC1_UTM_RXCLAV1 | AB25[2] |
| PC7/FCC1_CTS | FCC1_UTM_TXADDR2/<br>FCC1_UTS_TXADDR2/<br>FCC1_UTM_TXCLAV1 | AA24[2] |
| PC8/CD4/RENA4/SI2_L1ST2/CTS3/<br>USB_RN | FCC1_UT16_TXD0 | Y24[2] |
| PC9/CTS4/CLSN4/SI2_L1ST1/<br>L1TSYNCA2/L1GNTA2/USB_RP | FCC1_UT16_TXD1 | U22[2] |
| PC10/CD3/RENA3 | FCC1_UT16_TXD2/FCC2_UT8_RXD3 | V23[2] |
| PC11/CTS3/CLSN3/L1TXD3A2 | FCC2_UT8_RXD2 | U23[2] |
| PC12/CD2/RENA2 | FCC1_UTM_RXADDR1/<br>FCC1_UTS_RXADDR1 | T26[2] |
| PC13/CTS2/CLSN2 | FCC1_UTM_TXADDR1/<br>FCC1_UTS_TXADDR1 | R26[2] |
| PC14/CD1/RENA1 | FCC1_UTM_RXADDR0/<br>FCC1_UTS_RXADDR0 | P26[2] |
| PC15/CTS1/CLSN1/SMTXD2 | FCC1_UTM_TXADDR0/<br>FCC1_UTS_TXADDR0 | P24[2] |
| PC16/CLK16/TIN4 | | M26[2] |
| PC17/CLK15/TIN3/BRGO8 | | L26[2] |
| PC18/CLK14/TGATE2 | | M24[2] |
| PC19/CLK13/BRGO7/SPICLK | | L22[2] |
| PC20/CLK12/TGATE1/USB_OE | | K25[2] |
| PC21/CLK11/BRGO6 | | J25[2] |
| PC22/CLK10/DONE1 | FCC1_UT_TXPRTY | G26[2] |
| PC23/CLK9/BRGO5/DACK1 | | F26[2] |
| PC24/CLK8/TOUT4 | FCC2_UT8_TXD3 | G24[2] |
| PC25/CLK7/BRGO4 | FCC2_UT8_TXD2 | E25[2] |
| PC26/CLK6/TOUT3/TMCLK | | G23[2] |
| PC27/FCC3_TXD/FCC3_MII_TXD0/<br>FCC3_RMII_TXD0/CLK5/BRGO3 | | B23[2] |
| PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2 | FCC2_UT_RXADDR4 | E22[2] |
| PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1 | | E21[2] |
| PC30/CLK2/TOUT1 | FCC2_UT8_TXD3 | D21[2] |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PC31/CLK1/BRGO1 | | B20[2] |
| PD4/BRGO8/$\overline{\text{FCC3_RTS}}$/SMRXD2 | | AF23[2] |
| PD5/$\overline{\text{DONE1}}$ | FCC1_UT16_TXD3 | AE23[2] |
| PD6/$\overline{\text{DACK1}}$ | FCC1_UT16_TXD4 | AB21[2] |
| PD7/SMSYN1/FCC1_TXCLAV2 | FCC1_UTM_TXADDR3/<br>FCC1_UTS_TXADDR3/<br>FCC2_UTM_TXADDR4<br>FCC2_UTS_TXADDR1 | AD23[2] |
| PD8/SMRXD1/BRGO5 | FCC2_UT_TXPRTY | AD26[2] |
| PD9/SMTXD1/BRGO3 | FCC2_UT_RXPRTY | Y22[2] |
| PD10/L1CLKOB2/BRGO4 | FCC2_UT8_RXD1 | AB24[2] |
| PD11/$\overline{\text{L1RQB2}}$ | FCC2_UT8_RXD0<br>L1GNTB1 | Y23[2] |
| PD12 | | AA26[2] |
| PD13 | | W24[2] |
| PD14/L1CLKOC2/I2CSCL | FCC1_UT16_RXD0 | V22[2] |
| PD15/$\overline{\text{L1RQC2}}$/I2CSDA | FCC1_UT16_RXD1 | U26[2] |
| PD16/SPIMISO | FCC1_UT_TXPRTY | T23[2] |
| PD17/BRGO2/SPIMOSI | FCC1_UT_RXPRTY | R25[2] |
| PD18/SPICLK | FCC1_UTM_RXADDR4/<br>FCC1_UTS_RXADDR4/<br>FCC1_UTM_RXCLAV3/<br>FCC2_UTM_RXADDR3/<br>FCC2_UTS_RXADDR0 | P23[2] |
| PD19/SPISEL/BRGO1 | FCC1_UTM_TXADDR4/<br>FCC1_UTS_TXADDR4/<br>FCC1_UTM_TXCLAV3/<br>FCC2_UTM_TXADDR3/<br>FCC2_UTS_TXADDR0 | N22[2] |
| PD20/$\overline{\text{RTS4}}$/TENA4/L1RSYNCA2/<br>USB_TP | FCC1_UT16_RXD2 | M25[2] |
| PD21/TXD4/L1RXD0A2/L1RXDA2/<br>USB_TN | FCC1_UT16_RXD3 | L25[2] |
| PD22/RXD4L1TXD0A2/L1TXDA2/<br>USB_RXD | FCC1_UT16_TXD5 | J26[2] |
| PD23/$\overline{\text{RTS3}}$/TENA3 | FCC1_UT16_RXD4 | K22[2] |
| PD24/TXD3 | FCC1_UT16_RXD5 | G25[2] |
| PD25/RXD3 | FCC1_UT16_TXD6 | H24[2] |
| PD26/$\overline{\text{RTS2}}$/TENA2 | FCC1_UT16_RXD6 | F24[2] |

**Table 25. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8275/MPC8270 | MPC8275 only | |
| PD27/TXD2 | FCC1_UT16_RXD7 | H22[2] |
| PD28/RXD2 | FCC1_UT16_TXD7 | B22[2] |
| PD29/$\overline{\text{RTS1}}$/TENA1 | FCC1_UTM_RXADDR3/<br>FCC1_UTS_RXADDR3/<br>FCC1_UTM_RXCLAV2/<br>FCC2_UTM_RXADDR4/<br>FCC2_UTS_RXADDR1 | D22[2] |
| PD30/TXD1 | $\overline{\text{FCC2_UTM_TXENB}}$/<br>$\overline{\text{FCC2_UTS_TXENB}}$ | C21[2] |
| PD31/RXD1 | | E19[2] |
| VCCSYN | | D19 |
| VCCSYN1 | | K6 |
| CLKIN2 | | K21 |
| SPARE4[3] | | C14 |
| $\overline{\text{PCI_MODE}}$[4] | | AD24 |
| SPARE6[3] | | B15 |
| No connect[5] | | E17, C23 |
| I/O power | | E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9 |
| Core Power | | L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10 |
| Ground | | B18[6], A18[7], A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17 |

1 Should be tied to VDDH via a 2K Ω external pull-up resistor.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

3 Must be pulled down or left floating.
4 If PCI is not desired, must be pulled up or left floating.
5 Sphere is not connected to die.
6 GNDSYN (B18): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8275/MPC8270. New designs must connect B18 to GND and follow the suggestions in Section 4.6, "Layout Practices." Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.
7 XFC (A18) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8275/MPC8270 because there is no need for external capacitor to operate the PLL. New designs should connect A18 (XFC) pin to GND. Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to the current capacitor.

# 9 Package Description

This figure shows the side profile of the TBGA package to indicate the direction of the top surface view.

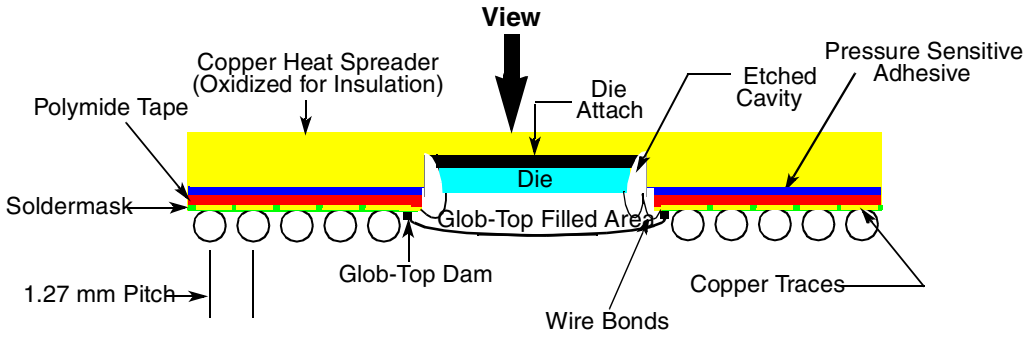



**Figure 15. Side View of the TBGA Package**

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

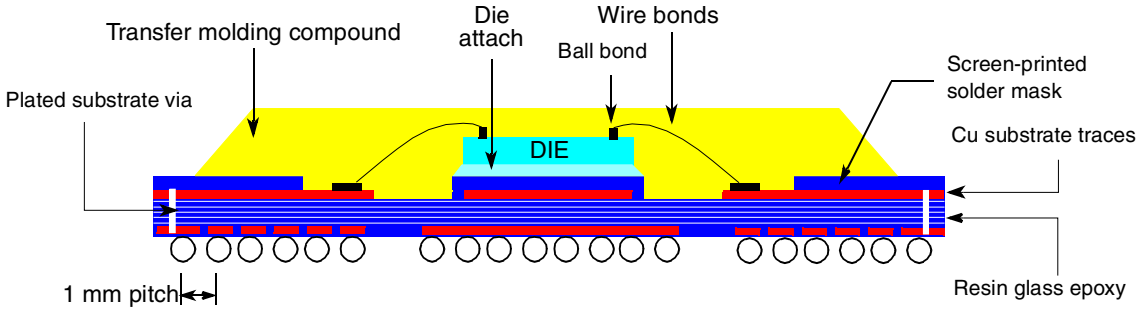



**Figure 16. Side View of the PBGA Package Remove**

## 9.1 Package Parameters

This table provides package parameters.

**NOTE: Temperature Reflow for the VR Package**

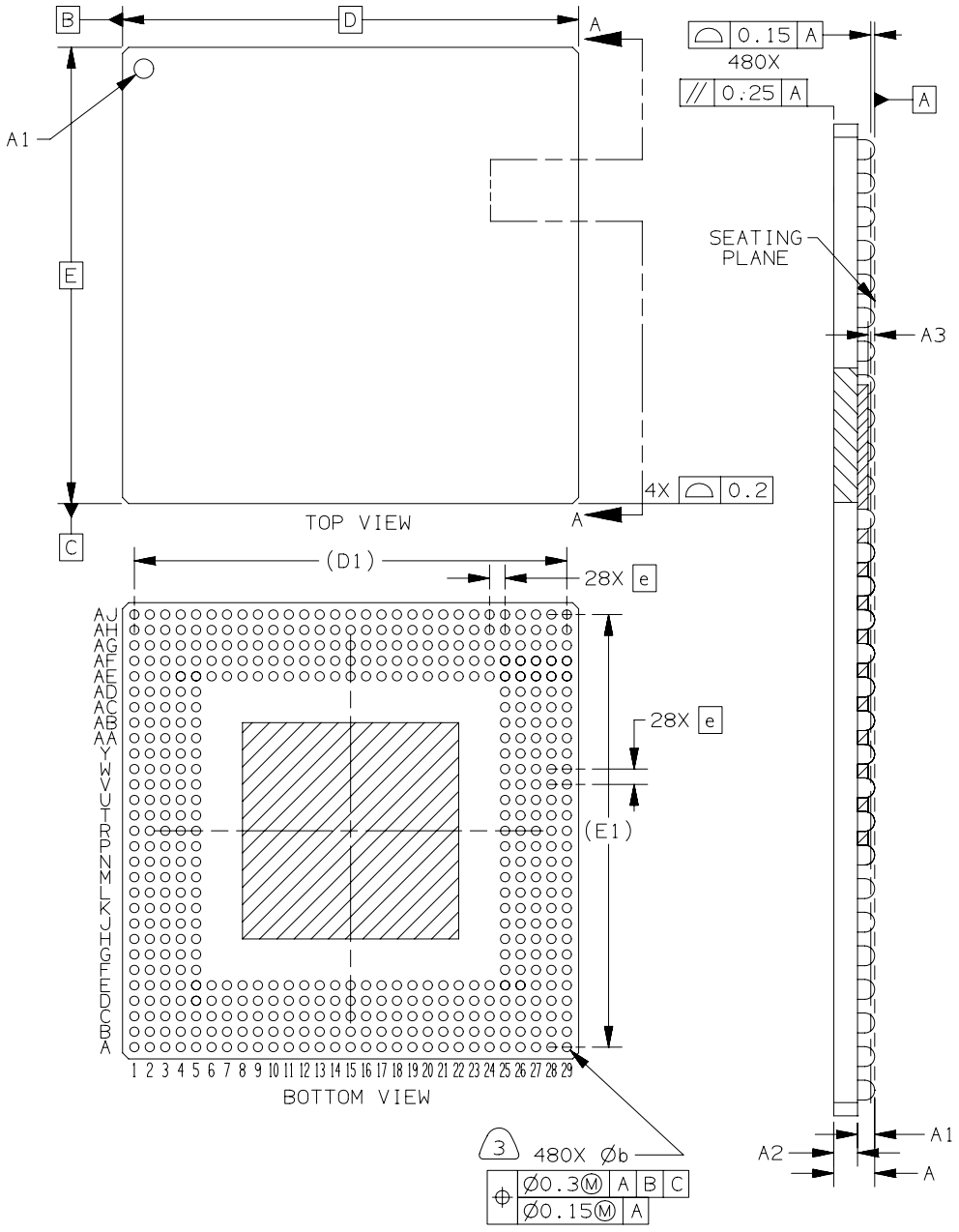
In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

**Table 26. Package Parameters**

| Package | SoCs | Outline (mm) | Type | Interconnects | Pitch (mm) | Nominal Unmounted Height (mm) |
|---|---|---|---|---|---|---|
| ZU | MPC8280<br>MPC8270 | 37.5 × 37.5 | TBGA | 480 | 1.27 | 1.55 |
| VV | MPC8280<br>MPC8270 | 37.5 × 37.5 | TBGA | 480 | 1.27 | 1.55 |
| VR | MPC8275VR<br>MPC8270VR | 27 × 27 | PBGA | 516 | 1 | 2.25 |
| ZQ | MPC8275ZQ<br>MPC8270ZQ | 27 × 27 | PBGA | 516 | 1 | 2.25 |

## 9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA (ZU/VV) package. See Table 2, “HiP7 PowerQUICC II Device Packages.”




| Dim | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.45 | 1.65 |
| A1 | 0.60 | 0.70 |
| A2 | 0.85 | 0.95 |
| A3 | 0.25 | — |
| b | 0.65 | 0.85 |
| D | 37.50 BSC | |
| D1 | 35.56 REF | |
| e | 1.27 BSC | |
| E | 37.50 BSC | |
| E1 | 35.56 REF | |

**Notes:**

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls.

**Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA**

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA (VR/ZQ) packages.

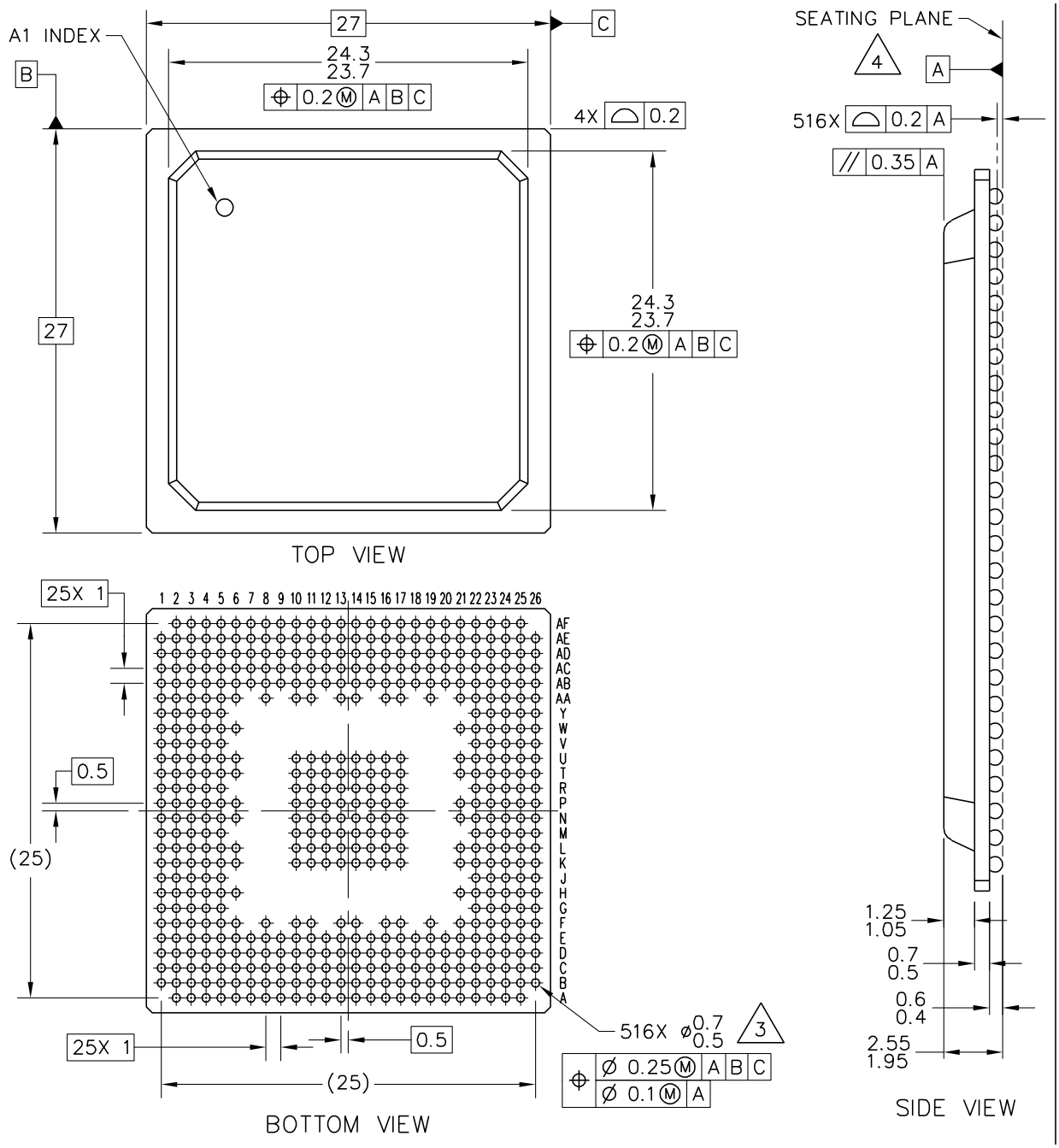



**Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA**

# 10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

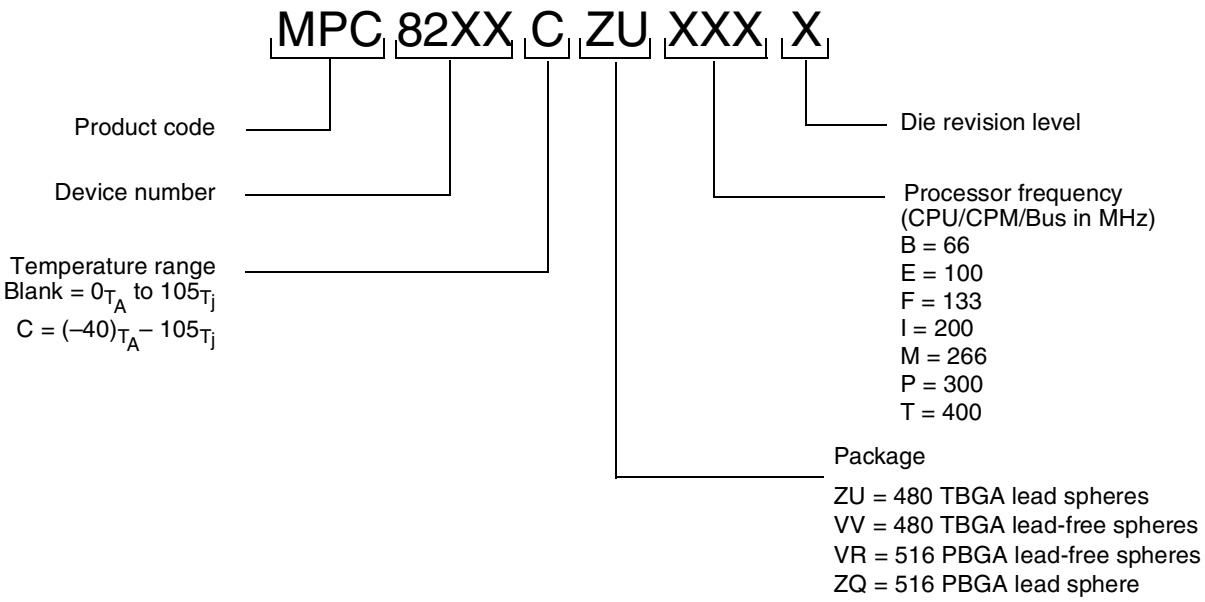



**Figure 19. Freescale Part Number Key**

# 11 Document Revision History

This table summarizes changes to this document.

**Table 27. Document Revision History**

| Revision | Date | Substantive Changes |
|---|---|---|
| 2 | 09/2011 | In Figure 19, “Freescale Part Number Key,” added speed decoding information below processor frequency information. |
| 1.8 | 07/2007 | • Updated the entire document, adding information on the VV package. |
| 1.7 | 12/2006 | • Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions. |
| 1.6 | 05/2006 | • Table 11: Added text to clarify that Data Bus Parity is not supported at 66 Mhz.<br>• Table 11: Added text to clarify that Data Bus ECC is supported at 66 Mhz<br>• Table 11: Added note to DP pins to show it is not supported at 66 MHz<br>• Table 12: Added note to support 1 ns hold time |
| 1.5 | 03/2006 | • Added Section 6.3, “JTAG Timings” |

**Table 27. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.4 | 11/2005 | • In Section 6.2, “SIU AC Characteristics”, modified the note on CLKIN Jitter and Duty Cycle.<br>• Modified Figure 17 to display all text. |
| 1.3 | 01/2005 | • Modification for correct display of assertion level (“overbar”) for some signals |
| 1.2 | 12/2004 | • Section 2: removed voltage tracking note<br>• Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset<br>• Table 5: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pullup removed.<br>• Table 5: Note 4 added regarding IIC compatibility<br>• Section 4.2: New information about jumper-to-case thermal resistance<br>• Section 4.3: New information about jumper-to-board thermal resistance<br>• Section 4.4: New information about estimation with simulation<br>• Section 4.6: Updated description of layout practices<br>• Section 6: Added sentence providing derating factor<br>• Section 6.1, “CPM AC Characteristics”: added Note: Rise/Fall Time on CPM Input Pins<br>• Table 9: updated values for following specs: sp42, sp43, sp42a<br>• Table 20: updated values for following specs: sp16b, sp18b, sp20, sp22<br>• Section 6.2: added spread sprectrum clocking note<br>• Table 11: combined specs sp11 and sp11a<br>• Sections 7.2, 7.3: unit of ns added to Tval notes<br>• Section 7, “Clock Configuration Modes”: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. |

**Table 27. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.0 | 2/2004 | • Removal of “Advance Information” and “Preliminary.” The MPC8280 is fully qualified.<br>• Table 2: New<br>• Figure 1: Modification to note 2<br>• Section 1.1: Core frequency range is 166–450 MHz<br>• Addition of ZQ (516 PBGA with Lead spheres) package references<br>• Table 4: VDD and VCCSYN modified to 1.45–1.60 V<br>• Note following Table 4: Modified<br>• Table 5: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see VIH row of Table 5)<br>• Table 5: Changed $I_{OL}$ for 60x signals to 6.0 mA<br>• Table 5: Moved QREQ to $V_{OL}$: $I_{OL}$= 3.2 mA<br>• Table 5: Addition of critical interrupt ($\overline{\text{CINT}}$) to $\overline{\text{IRQ5}}$ for $V_{OL}$ ($I_{OL}$ = 6.0mA)<br>• Table 10: Addition of $\Psi_{JT}$ and note 4<br>• Sections 4.1–4.5: New<br>• Table 12: Modified power values (+ 150mW to each)<br>• Table 14: Addition of note 2. Changed PCI impedance to 27 Ω.<br>• Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41<br>• Table 20: Changes to sp16a, sp18a, sp20 and sp21<br>• Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle<br>• Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz<br>• Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2.<br>• Table 18 through Table 37: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables.<br>• Table 23: Addition of note 1 to $\overline{\text{TRST}}$ (AH3) and $\overline{\text{PORESET}}$ (AG6)<br>• Table 23: Addition of RXD3 to CPM port pin PB14. Previously omitted.<br>• Table 23: Addition of critical interrupt ($\overline{\text{CINT}}$) to B21 and U4. Previously omitted.<br>• Table 23: Addition of note 5 to ‘No connect’ (AA1, AG4)<br>• Addition of “Note: Temperature Reflow for the VR Package" on page 76<br>• Table 25: Addition of note 1 to $\overline{\text{TRST}}$ (F22) and $\overline{\text{PORESET}}$ (B25)<br>• Table 25: Addition of previously omitted signals that are multiplexed with CPM port pins:<br>PA6—FCC2_UT_RXADDR3<br>PA7—FCC2_UT_TXADDR3<br>PA8—FCC2_UT_TXADDR4<br>PB14—RXD3<br>PC19—SPICLK<br>PC22—FCC1_UT_TXPRTY<br>PC28—FCC2_UT_RXADDR4<br>• Table 25: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1):<br>PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28]<br>• Table 25: Addition of critical interrupt ($\overline{\text{CINT}}$) to AC1 and B14. Previously omitted.<br>• Table 25: Addition of note 5 to ‘No connect’ (E17, C23) |

**Table 27. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 0.3 | 6/2003 | • Removal of notes stating “no local bus” on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support.<br>• References to “G2 core” changed to “G2_LE core.” See the *G2 Core Reference Manual* (G2CORERM/D).<br>• Addition of VCCSYN to “Note” below Table 4, and to note 3 of Table 5<br>• Figure 2: New<br>• Table 5: Addition of note 1<br>• Table 10: Addition of $\theta_{JB}$ and $\theta_{JC}$. Modifications to ZU package values.<br>• Table 12: Addition of various configurations, Modification of values. Addition of note 3.<br>• Table 9: Addition of 66 MHZ and 100 MHz values. Addition of sp42a/sp43a.<br>• Table 20: Addition of 66 MHZ and 100 MHz values<br>• Table 12: sp30 values. sp33b @100 MHz value. Removal of previous note 2. Modification of current note 2.<br>• Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes<br>• Section 6.2: Addition of note on PCI timing<br>• Table 18, Table 32, Table 33, Table 36, Table 37: Addition of note 1 concerning minimum operating frequencies<br>• Addition of statement before clock tables about selection of clock configuration and input frequency<br>• Table 23 and Table 25: Addition of note 1 to CPM pins |
| 0.2 | 11/2002 | Table 25, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 63) |
| 0.1 | — | Initial public release |

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