

200V Low Charge Injection 8-Channel High Voltage Analog Switch

Features

- ▶ HVCMOS® technology for high performance
- ▶ Very low quiescent power dissipation ($\sim 10\mu\text{A}$)
- ▶ Output on-resistance typically 11Ω
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz small signal frequency response
- ▶ -60dB typical off-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Serial shift register logic control with latches
- ▶ Flexible operating supply voltages
- ▶ Surface mount packages

Applications

- ▶ Medical ultrasound imaging
- ▶ Non-destructive evaluation

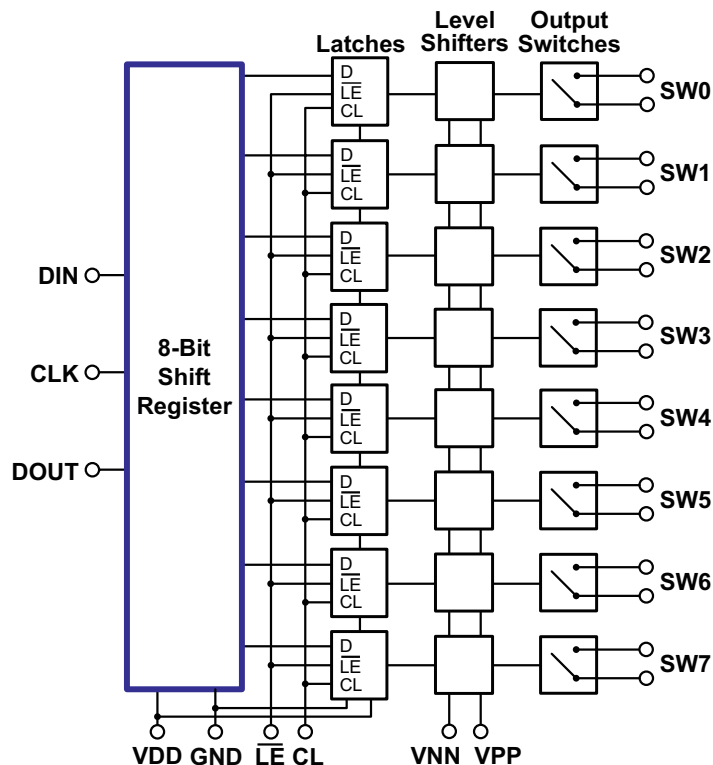
General Description

The Supertex HV219 is a low switch resistance, low charge injection, 8-channel, 200V, analog switch integrated circuit (IC) intended primarily for medical ultrasound imaging. The device can also be used for NDE (non-destructive evaluation) applications. The HV219 is a lower switch resistance, 11Ω versus 22Ω , version of the Supertex HV20220 device. The lower switch resistance will help reduce insertion loss. It has the same pin configuration as that of the Supertex HV20220PJ and the HV20220FG.

The device is manufactured using Supertex's HVCMOS® (high voltage CMOS) technology with high voltage bilateral DMOS structures for the outputs and low voltage CMOS logic for the input control. The outputs are configured as eight independent single pole single throw 11Ω analog switches. The input logic is an 8-bit serial to parallel shift register followed by an 8-bit parallel latch. The switch states are determined by the data in the latch. Logic high will correspond to a closed switch and logic low as an opened switch.

The HV219 is designed to operate on various combinations of high voltage supplies. For example the V_{PP} and V_{NN} supplies can be: +40V/-160V, +100V/-100V, or +160V/-40V. This allows the user to maximize the signal voltage for uni-polar negative, bi-polar, or uni-polar positive.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV219FG-G	48-Lead LQFP	250/Tray
HV219FG-G M931		1000/Reel
HV219PJ-G	28-Lead PLCC	38/Tube
HV219PJ-G M904		500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic power supply voltage	-0.5V to +15V
$V_{PP} - V_{NN}$ supply voltage	220V
V_{PP} positive high voltage supply	-0.5V to $V_{NN} + 200V$
V_{NN} negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to $V_{DD} + 0.3V$
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation: 28-Lead PLCC	1.2W
48-Lead LQFP	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

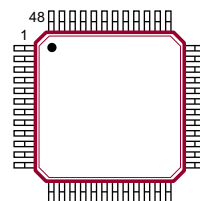
Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	4.5V to 13.2V
V_{PP}	Positive high voltage supply	40V to $V_{NN} + 200V$
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input logic voltage	$V_{DD} - 1.5V$ to V_{DD}
V_{IL}	Low-level input logic voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak	$V_{NN} + 10V$ to $V_{PP} - 10V$
T_A	Operating free air temperature	0°C to 70°C

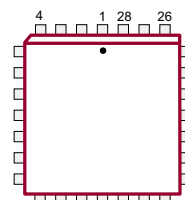
Power Up/Down Sequence

1. Power up/down sequence is arbitrary except GND must be powered up first and powered down last. This applies for applications powering GND of the IC with different voltages.
2. V_{SIG} must always be at or in between V_{PP} and V_{NN} or floating during power up/down transition.
3. Rise and fall times of the power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0ms.

Pin Configuration



48-Lead LQFP
(top view)



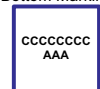
28-Lead PLCC
(top view)

Product Marking

Top Marking



Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

48-Lead LQFP

Top Marking



Bottom Marking



YY = Year Sealed
WW = Week Sealed
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C = Country of Origin*
A = Assembler ID*
— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

28-Lead PLCC

Typical Thermal Resistance

Package	θ_{ja}
48-Lead LQFP	52°C/W
28-Lead PLCC	48°C/W

DC Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R _{ONS}	Small signal switch on-resistance	-	15	-	13	19	-	24	Ω	I _{SIG} = 5.0mA	V _{PP} = +40V
		-	13	-	11	14	-	16		I _{SIG} = 200mA	V _{NN} = -160V
		-	13	-	11	14	-	15		I _{SIG} = 5.0mA	V _{PP} = +100V
		-	9.0	-	9.0	12	-	14		I _{SIG} = 200mA	V _{NN} = -100V
		-	12	-	10	13	-	15		I _{SIG} = 5.0mA	V _{PP} = +160V
		-	11	-	8	13	-	14		I _{SIG} = 200mA	V _{NN} = -40V
ΔR _{ONS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I _{SIG} = 5.0mA, V _{PP} = +100V, V _{NN} = -100V	
R _{ONL}	Large signal switch on-resistance	-	-	-	8.0	-	-	-	Ω	V _{SIG} = V _{PP} -10V, I _{SIG} = 1.0A	
I _{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	μA	V _{SIG} = V _{PP} -10V & V _{NN} +10V	
V _{OS}	DC offset switch off	-	300	-	100	300	-	300	mV	R _{LOAD} = 100kΩ	
	DC offset switch on	-	500	-	100	500	-	500	mV	R _{LOAD} = 100kΩ	
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches off	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-	μA	All switches off	
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches on, I _{SW} = 5.0mA	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-	μA	All switches on, I _{SW} = 5.0mA	
I _{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V _{SIG} duty cycle < 0.1%	
f _{SW}	Output switch frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I _{PP}	Average V _{PP} supply current	-	6.5	-	-	7.0	-	8.0	mA	V _{PP} = +40V V _{NN} = -160V	All output switches are turning on and off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V _{PP} = +100V V _{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V _{PP} = +160V V _{NN} = -40V	
I _{NN}	Average V _{NN} supply current	-	6.5	-	-	7.0	-	8.0	mA	V _{PP} = +40V V _{NN} = -160V	All output switches are turning on and off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V _{PP} = +100V V _{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V _{PP} = +160V V _{NN} = -40V	
I _{DD}	Average V _{DD} supply current	-	4.0	-	-	4.0	-	4.0	mA	f _{CLK} = 5.0MHz, V _{DD} = 5.0V	
I _{DDQ}	Quiescent V _{DD} supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I _{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = V _{DD} -0.7V	
I _{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = 0.7V	
C _{IN}	Large input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics (over recommended operating conditions, $V_{DD} = 5.0V$, unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set-up time before $\overline{LE}$ rises	150	-	150	-	-	150	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	150	-	150	-	-	150	-	ns	---
t_{DO}	Clock delay time to data out	-	150	-	-	150	-	150	ns	---
t_{WCL}	Time width of CL	150	-	150	-	-	150	-	ns	---
t_{SU}	Set-up time data to clock	15	-	15	8.0	-	20	-	ns	---
t_H	Hold time data from clock	35	-	35	-	-	35	-	ns	---
f_{CLK}	Clock frequency	-	5.0	-	-	5.0	-	5.0	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
t_r, t_f	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
T_{ON}	Turn-on time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V$, $R_{LOAD} = 10k\Omega$
T_{OFF}	Turn-off time	-	5.0	-	-	5.0	-	5.0	μs	
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +40V, V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V, V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V, V_{NN} = -40V$
K_O	Off isolation	-30	-	-30	-33	-	-	-	dB	$f = 5.0MHz$, 1.0K Ω //15pF load
		-58	-	-58	-	-	-	-		$f = 5.0MHz$, 50 Ω load
K_{CR}	Switch crosstalk	-	-	-60	-	-	-	-	dB	$f = 5.0MHz$, 50 Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	14	25	14	20	25	14	25	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	40	60	40	50	60	40	60	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	$V_{PP} = +40V$, $V_{NN} = -160V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	200	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +100V$, $V_{NN} = -100V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	200	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V$, $V_{NN} = -40V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	200	-	-		
QC	Charge injection	-	-	-	1450	-	-	-	pC	$V_{PP} = +40V$, $V_{NN} = -160V, V_{SIG} = 0V$
		-	-	-	1050	-	-	-		$V_{PP} = +100V$, $V_{NN} = -100V, V_{SIG} = 0V$
		-	-	-	550	-	-	-		$V_{PP} = +160V$, $V_{NN} = -40V, V_{SIG} = 0V$

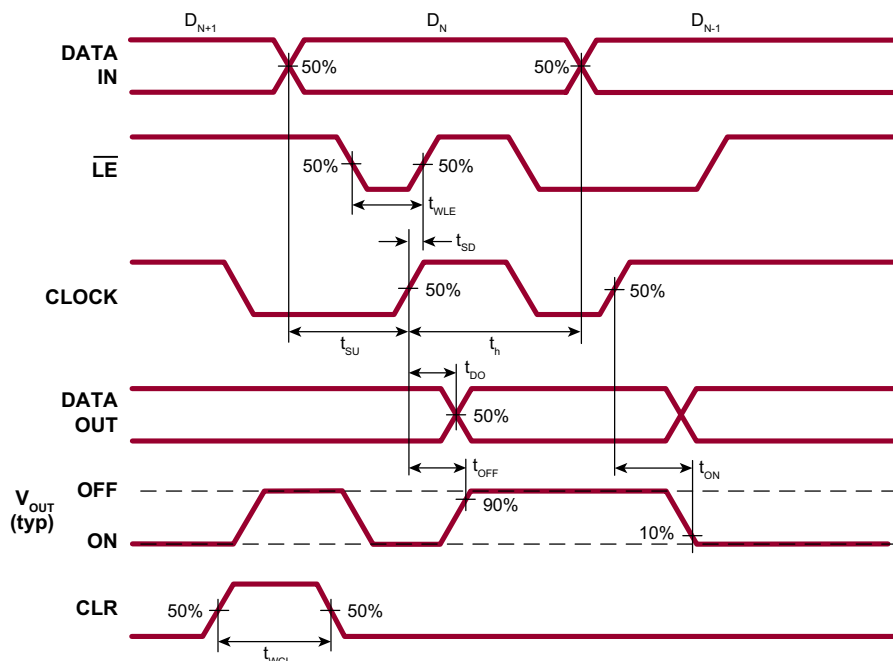
Truth Table

Data in 8-Bit Shift Register								$\overline{LE}$	CL	Output Switch State							
D0	D1	D2	D3	D4	D5	D6	D7			SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

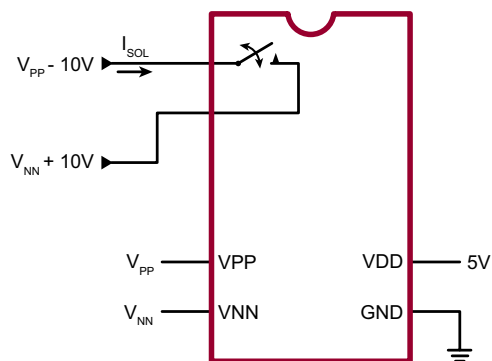
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition clock.
3. The switches go to a state retaining their present condition at the rising edge of the $\overline{LE}$.
4. When $\overline{LE}$ is low, the shift register data flows through the latch.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
6. The clear input overrides all other inputs.

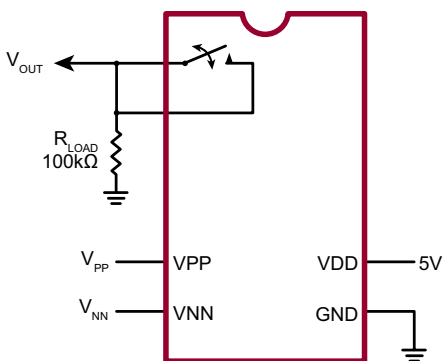
Logic Timing Waveforms



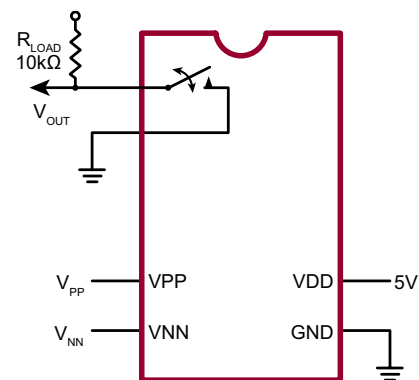
Test Circuits



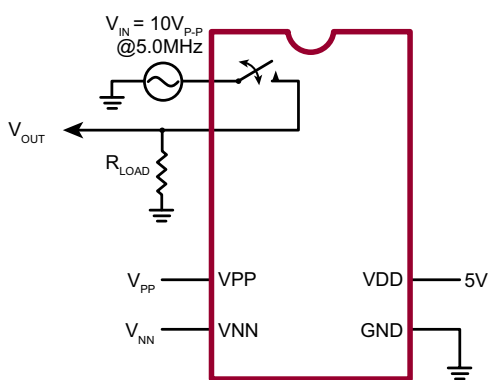
Switch OFF Leakage



DC Offset ON/OFF

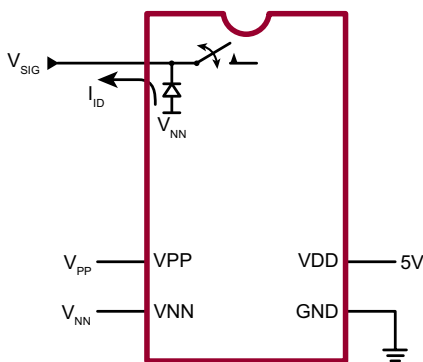


T_{ON}/T_{OFF} Test Circuit

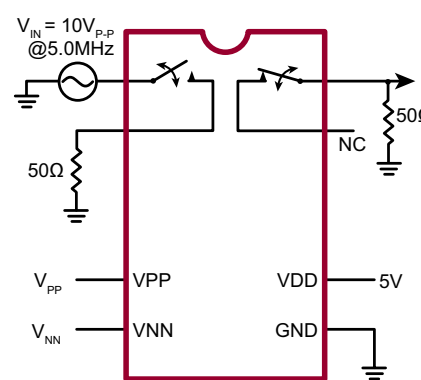


$$K_o = 20 \log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

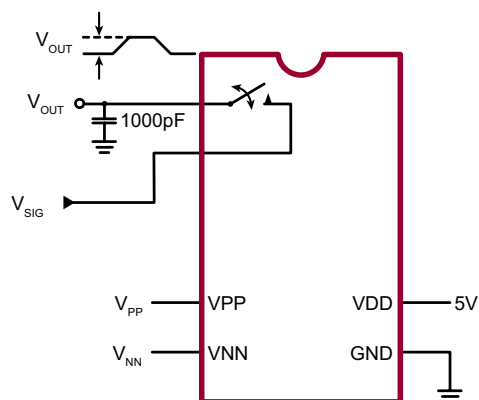


Isolation Diode Current



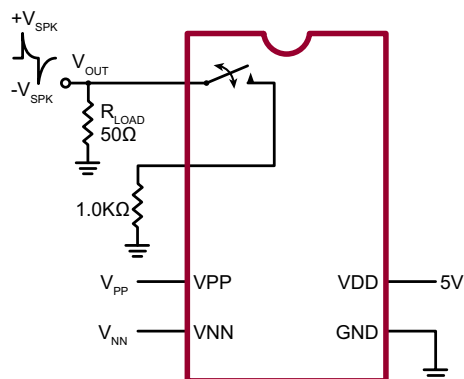
$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk



$$Q = 1000pF \times V_{OUT}$$

Charge Injection



Output Voltage Spike

Pin Description

48-Lead LQFP

Pin	Name
1	SW5
2	NC
3	SW4
4	NC
5	SW4
6	NC
7	NC
8	SW3
9	NC
10	SW3
11	NC
12	SW2

Pin	Name
13	NC
14	SW2
15	NC
16	SW1
17	NC
18	SW1
19	NC
20	SW0
21	NC
22	SW0
23	NC
24	VPP

Pin	Name
25	VNN
26	NC
27	NC
28	GND
29	VDD
30	NC
31	NC
32	NC
33	DIN
34	CLK
35	$\overline{LE}$
36	CLR

Pin	Name
37	DOUT
38	NC
39	SW7
40	NC
41	SW7
42	NC
43	SW6
44	NC
45	SW6
46	NC
47	SW5
48	NC

Pin Description

28-Lead PLCC

Pin	Name
1	SW3
2	SW3
3	SW2
4	SW2
5	SW1
6	SW1
7	SW0

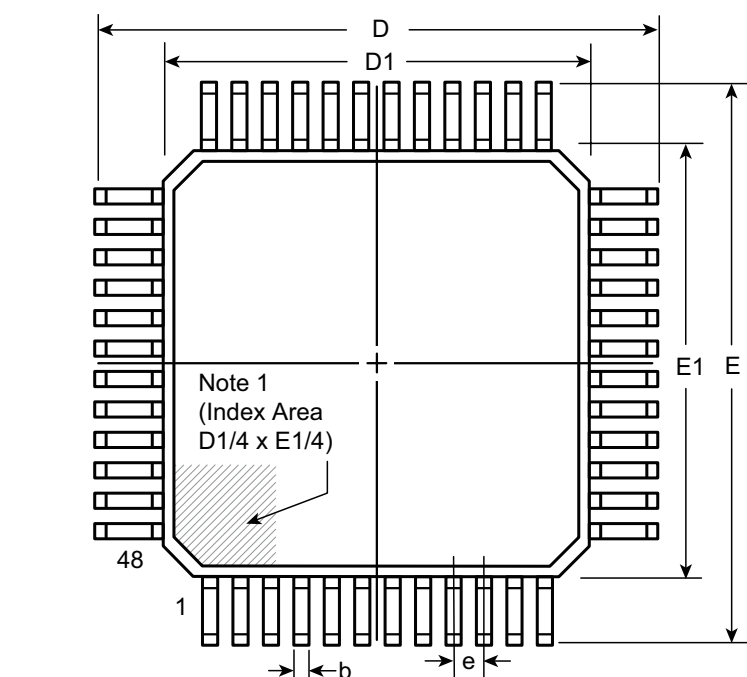
Pin	Name
8	SW0
9	NC
10	VPP
11	NC
12	VNN
13	GND
14	VDD

Pin	Name
15	NC
16	DIN
17	CLK
18	$\overline{LE}$
19	CL
20	DOUT
21	SW7

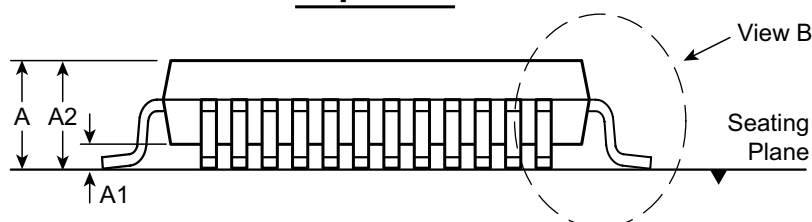
Pin	Name
22	SW7
23	SW6
24	SW6
25	SW5
26	SW5
27	SW4
28	SW4

48-Lead LQFP Package Outline (FG)

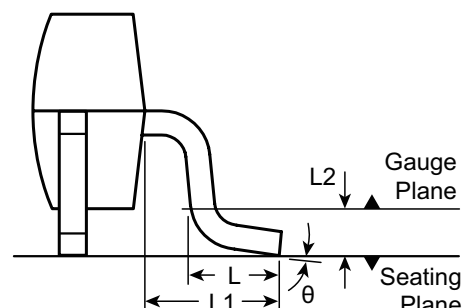
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



Side View



View B

Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

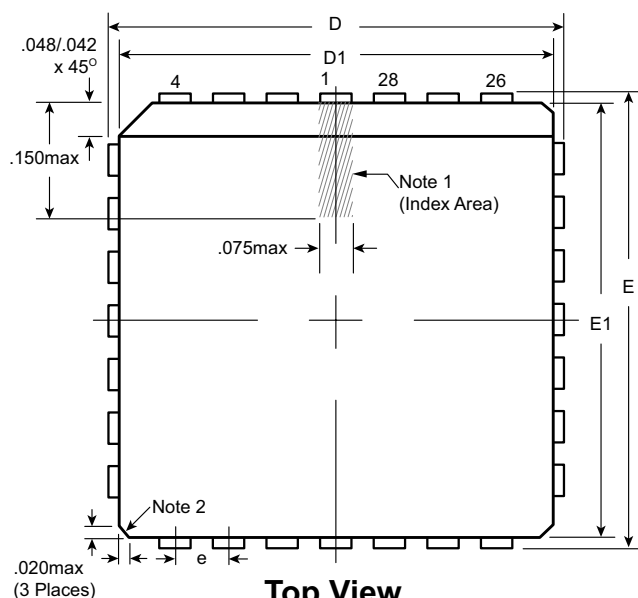
* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

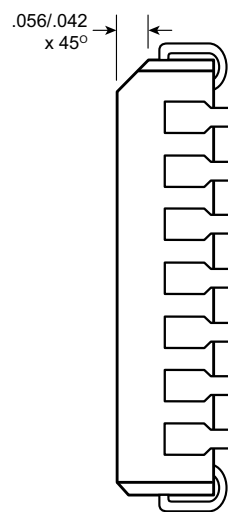
Supertex Doc. #: DSPD-48LQFPFG Version, D041309.

28-Lead PLCC Package Outline (PJ)

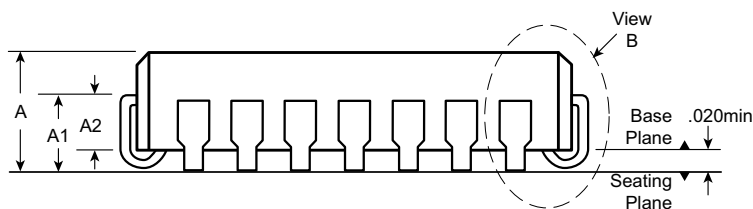
.453x.453in. body, .180in. height (max), .050in. pitch



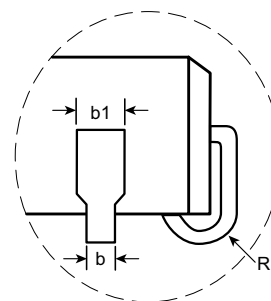
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC	.025
	NOM	.172	.105	-	-	-	.490	.453	.490	.453		.035
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456		.045

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

Supertex Doc. #: DSPD-28PLCCPJ, Version B031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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