Panasonic

# AN30183A

## 600mA Synchronous DC-DC Step Down Regulator (1ch)
## 300mA LDO Regulator (4ch)
## Multi Power Supply (High Efficiency Power LSI)

### FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic System
- DC-DC Step Down Regulator : 1-ch
  Input voltage Range VBAT :2.5V to 5.5V
  DVDD : 1.7V to 3.0V
  Output voltage Range 0.8 V to 2.4 V
  Up to 600 mA Output Current

- LDO Regulator : 4-ch
  Input voltage Range VBAT :2.5V to 5.5V
  DVDD : 1.7V to 3.0V
  Output voltage Range 1.0 V to 3.3 V
  Up to 300 mA Output Current

- $I^2C$ control (2-slave address selectable)
- 20 pin Wafer Level Chip Size Package (WLCSP)
  (Size : 1.56 mm × 2.06 mm, 0.4 mm Pitch)

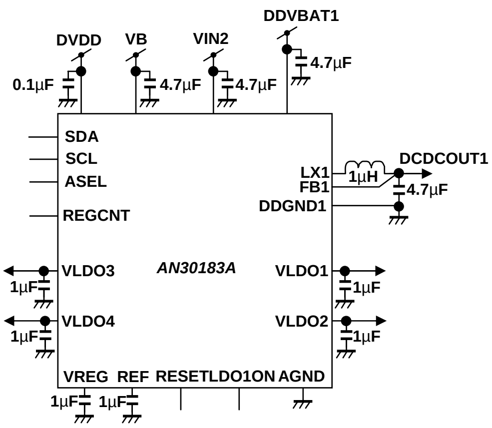
### DESCRIPTION

AN30183A is a multi power supply LSI which has High-Speed Response DC-DC Step Down Regulators (1-ch) and LDO Regulators (4-ch).
By this DC-DC system, when load current charges suddenly, it responds at high speed and minimizes the changes of output voltage.
Since it is possible to use capacitors with small capacitance and it is unnecessary to add external parts for system phase compensation, this IC realizes downsizing of set and reducing in the number of external parts.
The output DC of each power supply is variable by $I^2C$ control.

### APPLICATIONS

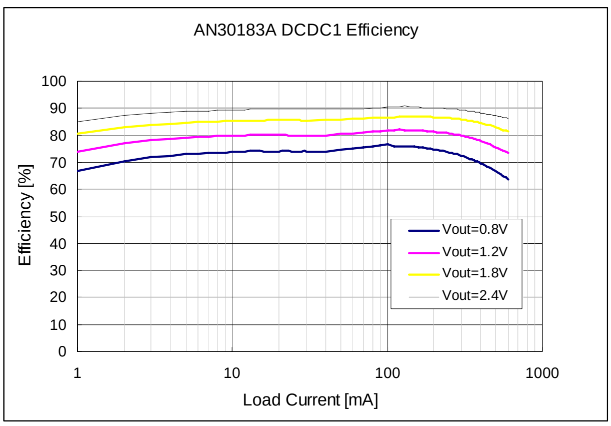
Mobile phone, Portable appliance, etc

### SIMPLIFIED APPLICATION




Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

### EFFICIENCY CURVE




Condition )
DDVBAT1 = DDVBAT2 = VB = VIN2 = 3.7V
Lo = 1.0 µH, Cout = 4.7 µF

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Supply voltage | VB,VIN2,DDVBAT1 | 6.0 | V | *1 |
| | DVDD | 3.6 | V | *1 |
| Output Current | $I_{IN}$ | — | A | *1 |
| Operating free-air temperature | $T_{opr}$ | – 30 to + 85 | °C | *2 |
| Operating junction temperature | $T_j$ | – 30 to + 150 | °C | *2 |
| Storage temperature | $T_{stg}$ | – 55 to + 150 | °C | *2 |
| Input Voltage Range | RESET,LDO1ON,FB1, REGCNT | – 0.3 to $V_{VBAT}$ + 0.3 | V | *1 *3 |
| | SCL,SDA,ASEL | – 0.3 to DVDD + 0.3 | V | *1 *3 |
| Output Voltage Range | LX1,VREG,REF,SDA LDO1,LDO2,LDO3,LDO4 | – 0.3 to $V_{VBAT}$ + 0.3 | V | *1 *3 |
| ESD | HBM (Human Body Model) | 2 | kV | — |

Notes) Do not apply external currents and voltages to any pin not specifically mentioned.

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.

*3:$V_{VBAT}$ is voltage for DDVBAT1 = VB = VIN2, ($V_{VBA}$ + 0.3) V must not be exceeded 6 V.

$V_{DVDD}$ is voltage for DVDD, ($V_{DVDD}$ + 0.3) V must not be exceeded 3.6 V.

## POWER DISSIPATION RATING

| PACKAGE | $\theta_{JA}$ | PD ( Ta = 25 °C) | PD ( Ta = 85 °C ) | Notes |
|---|---|---|---|---|
| 20 pin Wafer level chip size Package (WLCSP Type) | 359.0 °C / W | 0.348 W | 0.181 W | *1 |

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1:Glass Epoxy Substrate ( 4 Layers ) [ Glass-Epoxy: 50 X 50 X 0.8 t ( mm ) ]

Die Pad Exposed , Soldered.

## CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Pin Name | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage range | VB | 2.5 | 3.7 | 5.5 | V | *1 |
| | VIN2 | 2.5 | 3.7 | 5.5 | V | *1 |
| | DDVBAT1 | 2.5 | 3.7 | 5.5 | V | *1 |
| | DVDD | 1.7 | 1.85 | 3.0 | V | *1 |
| Input Voltage Range | RESET | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | LDO1ON | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | REGCNT | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | FB1 | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | SCL | – 0.3 | — | DVDD + 0.3 | V | *2 |
| | SDA | – 0.3 | — | DVDD + 0.3 | V | *2 |
| | ASEL | – 0.3 | — | DVDD + 0.3 | V | *2 |
| Output Voltage Rang | LX1 | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | VREG | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | REF | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | SDA | – 0.3 | — | DVDD + 0.3 | V | *2 |
| | VLDO1 | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | VLDO2 | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | VLDO3 | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |
| | VLDO4 | – 0.3 | — | $V_{VBAT}$ + 0.3 | V | *2 |

Note) Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND = DDGND1
$V_{VBAT}$ is voltage for DDVBAT1 = VB = VIN2.
*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : ($V_{VBAT}$ + 0.3) V must not be exceeded 6 V. (DVDD + 0.3) V must not be exceeded 3.6 V.

## ELECRTRICAL CHARACTERISTICS

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.7V, DVDD = 1.85V
DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Consumption current | | | | | | | |
| Consumption current 1 on active | IBAT_1 | only LDO1 (PS mode) ON | — | 10 | 20 | µA | — |
| Consumption current 2 on active | IBAT_2 | DCDC1, LDO1-4 = ON | — | 240 | 400 | µA | — |
| Static consumption current | IBAT_3 | DCDC1, LDO1-4 = OFF<br>RESET = “L” | — | 0.1 | 1.0 | µA | — |

## ELECRTRICAL CHARACTERISTICS (Continued)

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.7V, DVDD = 1.85V
DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| LDO1 – 4 ( Normal Mode ) - (LDO Regulator) | | | | | | | |
| Output voltage | VLDO | ILDO = – 150 mA<br>Vout = 1.85 V setting | 1.803 | 1.850 | 1.897 | V | — |
| Output current | ILDO | — | 300 | — | — | mA | — |
| Load regulation | DVLDO | Δ ILDO = – 10 µA → – 150 mA | –5 | 20 | 50 | mV | — |
| Line regulation | VLDOLR | VB = 3.1 V → 4.5 V<br>ILDO = – 150 mA<br>Vout = 1.85 V setting | – 10 | 0 | 10 | mV | — |
| Short-circuit current | ISTLDO | VB = 3.7 V<br>VLDO = 0 V | 35 | 100 | 255 | mA | — |
| LDO1 – 4 ( Power Save Mode ) - (LDO Regulator) | | | | | | | |
| Output voltage | VLDOPS | ILDO = – 5 mA<br>Vout = 1.85 V setting | 1.803 | 1.850 | 1.897 | V | — |
| Output current | ILDOPS | — | 10 | — | — | mA | — |
| Load regulation | DVLDOPS | Δ ILDO = – 10 µA → – 5 mA | – 5 | 20 | 50 | mV | — |
| Line regulation | VLDOLRPS | VB = 3.1 V → 4.5 V<br>ILDO = – 5 mA<br>Vout = 1.85 V setting | – 25 | 0 | 25 | mV | — |

## ELECRTRICAL CHARACTERISTICS (Continued)

$V_{VBAT}$(DDVBAT1= VB = VIN2) = 3.7V, DVDD = 1.85V
DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Conditions | Limits Min | Limits Typ | Limits Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| DCDC1 (DC-DC Step Down Regulator) | | | | | | | |
| Output voltage | VDCDC1 | IDCDC1 = – 300 mA<br>Vout = 1.2 V setting | 1.170 | 1.200 | 1.230 | V | — |
| Output current | IDCDC1 | — | 600 | — | — | mA | — |
| Load regulation | DVDCDC1 | Δ IDCDC1 = – 10 µA → – 500 mA<br>Vout = 1.2 V setting | — | 25 | 45 | mV | — |
| Line regulation | VDCDC1LR | DDVBAT1 = 3.1 V → 4.5 V<br>IDCDC1 = – 300 mA<br>Vout = 1.2 V setting | — | 4 | 13 | mV | — |
| Oscillation frequency | ISTDCDC1 | IDCDC1 = – 300 mA (CCM) | 2 | 3 | 4 | MHz | — |
| I/O characteristics of control terminal (RESET, LDO1ON, REGCNT) | | | | | | | |
| Low input voltage | VIL1 | Voltage recognized as low level | — | — | 0.45 | V | — |
| High input voltage | VIH1 | Voltage recognized as high level | 1.2 | — | — | V | — |
| Input pull-down resistance | PDR1 | — | 1 | 3 | 6 | MΩ | — |
| I/O characteristics of control terminal (ASEL) | | | | | | | |
| Low input voltage | VIL2 | Voltage recognized as low level | — | — | $V_{DVDD}$ × 0.3 | V | — |
| High input voltage | VIH2 | Voltage recognized as high level | $V_{DVDD}$ × 0.7 | — | — | V | — |

## APPLICATION INFORMATION

REFERENCE VALUES FOR DESIGN

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.7V, DVDD = 1.85V

$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Conditions | Reference values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| I²C Bus (Internal I/O Stage Characteristics) | | | | | | | |
| Low-level input voltage | VIL1 | Voltage which recognized that SDA and SCL are Low-level | – 0.5 | — | 0.3 × $V_{DVDD}$ | V | *1 *2 |
| High-level input voltage | VIH1 | Voltage which recognized that SDA and SCL are High-level | 0.7 × $V_{DVDD}$ | — | $V_{DVDD}$ max + 0.5 | V | *1 *2 |
| Low-level output voltage 1 | VOL1 | $V_{DVDD}$ > 2 V<br>SDA(sink current) = 3 mA | 0 | — | 0.4 | V | *2 |
| Low-level output voltage 2 | VOL2 | $V_{DVDD}$ < 2 V<br>SDA(sink current) = 3 mA | 0 | — | 0.2 × $V_{DVDD}$ | V | *2 |
| Input current each I/O pin | IL | SCL, SDA =<br>0.1 × $V_{DVDDmax}$ to<br>0.9 × $V_{DVDDmax}$ | – 10 | — | 10 | µA | *2 |
| SCL clock frequency | FOSC | — | 0 | — | 400 | kHz | *2 |

Notes) *1 : The input threshold voltage of I²C bus (Vth) is linked to $V_{DVDD}$.

In case the pull-up voltage is not $V_{DVDD}$, the threshold voltage (Vth) is fixed to (($V_{DVDD}$ / 2) ± (Schmitt width) / 2 ) and High-level, Low-level of input voltage are not specified.

In this case, pay attention to Low-level (max.) value ($V_{ILmax}$).

It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage ($V_{DVDD}$).

*2 :Checked by design, not production tested.

## APPLICATION INFORMATION (Continued)

REFERENCE VALUES FOR DESIGN

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.1V to 4.5V, $V_{DVDD}$ = 1.85V , DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Conditions | Reference values Min | Reference values Typ | Reference values Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| LDO1 – 4 ( Normal Mode ) - (LDO Regulator) | | | | | | | |
| Output voltage | VLDO | ILDO = – 150 mA<br>Vout = 1.85 V setting | 1.803 | 1.850 | 1.897 | V | *2 |
| Consumption current on active | IREGLDO | Normal mode<br>VB > Vout + 0.1 V or<br>VIN2 > Vout + 0.1 V | 25 | 50 | 75 | µA | *2 |
| I/O voltage difference | VSATLDO | ILDO = – 300 mA | 0.3 | — | — | V | *2 |
| Ripple rejection | VLDORR | ΔVB = 3.7 V ± 0.15 V<br>ILDO = – 150 mA<br>fvin = 100 Hz to 10 kHz | — | – 60 | – 40 | dB | *2 |
| Discharge resistance | RDISLDO | — | 50 | 100 | 200 | kΩ | *2 |
| Load change characteristic | LTRLDO | ILDO = – 10 µA ↔ – 100 mA | — | 30 | 150 | mV | *2 |
| LDO1 – 4 ( Power Save Mode ) - (LDO Regulator) | | | | | | | |
| Output voltage | VLDOPS | ILDO = – 5 mA<br>Vout = 1.85 V setting | 1.803 | 1.850 | 1.897 | V | *2 |
| Consumption current on active | IREGLDOPS | Power Save mode<br>VB > Vout + 0.1 V or<br>VIN2 > Vout + 0.1 V | 1 | 3 | 5 | µA | *2 |
| Ripple rejection | VLDOPSRR | ΔVB = 3.7 V ± 0.15 V<br>ILDO = – 5 mA<br>fvin = 100 Hz to 10 kHz | — | – 10 | – 5 | dB | *2 |
| Short-circuit current | ISTLDOPS | VB = 3.7 V<br>VLDO = 0 V | 5 | 20 | 40 | mA | *2 |

Notes) *2 :Checked by design, not production tested.

## APPLICATION INFORMATION (Continued)

REFERENCE VALUES FOR DESIGN

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.1V to 4.5V, DVDD = 1.85V , DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| | Parameter | Symbol | Conditions | Reference values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| DCDC1 (DC-DC Step Down Regulator) | | | | | | | | |
| | Output Voltage | VDCDC1 | IDCDC1 = – 300 mA<br>Vout = 1.2 V setting | 1.170 | 1.200 | 1.230 | V | *2 |
| | Consumption current on active | IREGDCCD1 | IDCDC1 = 0 mA | 10 | 25 | 40 | µA | *2 |
| | Output over current limit | ILIMDCDC1 | From FB1 × 100% to FB1 × 70%<br>VB = 3.7 V | — | 1.0 | 1.2 | A | *2 |
| | Efficiency 1 | EFFDCDC11 | DDVBAT1 = 3.4 V<br>VDCDC1 = 2.4 V<br>IDCDC1 = – 150 mA | 85 | 90 | — | % | *2 |
| | Efficiency 2 | EFFDCDC12 | DDVBAT1 = 3.7 V<br>VDCDC1 = 1.2 V<br>IDCDC1 = – 150 mA | 75 | 80 | — | % | *2 |
| | LX leak current | ILXL1 | DDVBAT1 = 5.5 V<br>DCDC1 = Disable<br>VLX1 = 0 V or 5.5 V | – 1 | 0 | 1 | µA | *2 |
| | Discharge resistance | RDISDCDC1 | — | 0.5 | 1.0 | 2.0 | kΩ | *2 |

Notes) *2 :Checked by design, not production tested.

## APPLICATION INFORMATION (Continued)

REFERENCE VALUES FOR DESIGN

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.1V to 4.5V, DVDD = 1.85V , DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | | Symbol | Conditions | Reference values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| I²C bus (Internal I/O stage characteristics) | | | | | | | | |
| | Hysteresis of Schmitt trigger input 1 | Vhys1 | $V_{IO}$ > 2 V, Hysteresis 1 of SDA, SCL | 0.05 × $V_{DVDD}$ | — | — | V | *2 |
| | Hysteresis of Schmitt trigger input 2 | Vhys2 | $V_{IO}$ < 2 V, Hysteresis 2 of SDA, SCL | 0.1 × $V_{DVDD}$ | — | — | V | *2 |
| | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ | Tof | Bus capacitance : 10 pF to 400 pF<br>$I_P \leq 6$ mA ($V_{OLmax}$ = 0.6 V)<br>$I_P$ : Max. sink current | 20 + 0.1 × $C_b$ | — | 250 | ns | *2 |
| | Pulse width of spikes which must be suppressed by the input filter | Tsp | — | 0 | — | 50 | ns | *2 |
| | Capacitance for each I/O pin | Ci | — | — | — | 10 | pF | *2 |
| I²C bus (Bus line specifications) | | | | | | | | |
| | Hold time (repeated) START condition | $t_{HD:STA}$ | The first clock pulse is generated after $t_{HD:STA}$. | 0.6 | — | — | µs | *2 |
| | Low period of the SCL clock | $t_{LOW}$ | — | 1.3 | — | — | µs | *2 |
| | High period of the SCL clock | $t_{HIGH}$ | — | 0.6 | — | — | µs | *2 |
| | Set-up time for a repeat START condition | $t_{SU:STA}$ | — | 0.6 | — | — | µs | *2 |
| | Data hold time | $t_{HD:DAT}$ | — | 0 | — | 0.9 | µs | *2 |
| | Data set-up time | $t_{SU:DAT}$ | — | 100 | — | — | ns | *2 |
| | Rise time of both SDA and SCL signals | $t_r$ | — | 20 + 0.1 × $C_b$ | — | 300 | ns | *2 |
| | Fall time of both SDA and SCL signals | $t_f$ | — | 20 + 0.1 × $C_b$ | — | 300 | ns | *2 |
| | Set-up time of STOP condition | $t_{SU:STO}$ | — | 0.6 | — | — | µs | *2 |
| | Bus free time between STOP and START condition | $t_{BUF}$ | — | 1.3 | — | — | µs | *2 |

Notes) *2 :Checked by design, not production tested.

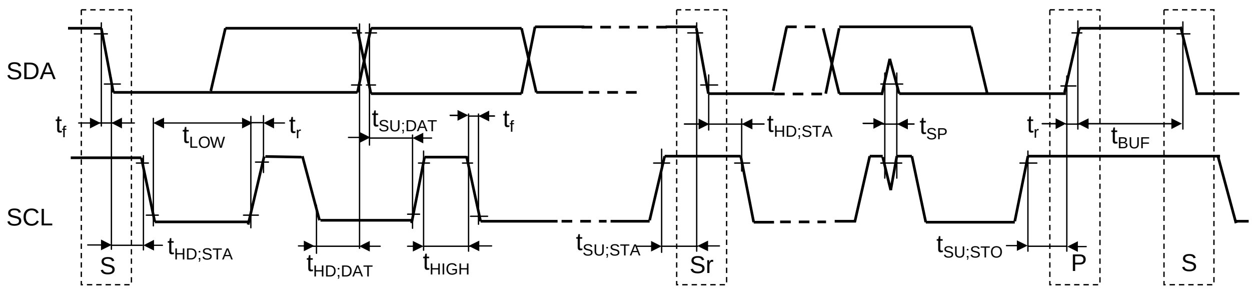
## APPLICATION INFORMATION (Continued)

REFERENCE VALUES FOR DESIGN

$V_{VBAT}$(DDVBAT1 = VB = VIN2) = 3.1V to 4.5V, DVDD = 1.85V , DC-DC : Co = 4.7 µF, Lo = 1 µH / LDO : Co =1.0 µF
$T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Conditions | Reference values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| I²C bus (Bus line specifications) (continued) | | | | | | | |
| Capacitive load for each bus line | $C_b$ | — | — | — | 400 | pF | *2 *3 |
| Noise margin at the Low-level for each connected device | $V_{nL}$ | — | 0.1 × $V_{DVDD}$ | — | — | V | *2 *3 |
| Noise margin at the High-level for each connected device | $V_{nH}$ | — | 0.2 × $V_{DVDD}$ | — | — | V | *2 *3 |
| Consumption current | | | | | | | |
| Static consumption current 2 | IBAT_4 | DDVBAT1 = VB = VIN2 = 3.7 V<br>DCDC1, LDO1 to 4 = OFF<br>RESET= "H" | — | 8 | 17 | µA | *2 |

Notes) *2 :Checked by design, not production tested.
*3 :The timing of Fast-mode devices in I²C-bus is specified as the following.
All values referred to $V_{IHmin}$ and $V_{ILmax}$ level.

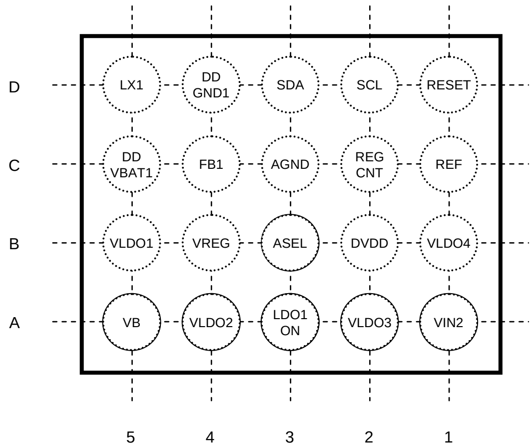



S : START condition
Sr : Repeat START condition
P : STOP condition

Notes) *2 :Checked by design, not production tested.

## PIN CONFIGURATION

TOP VIEW

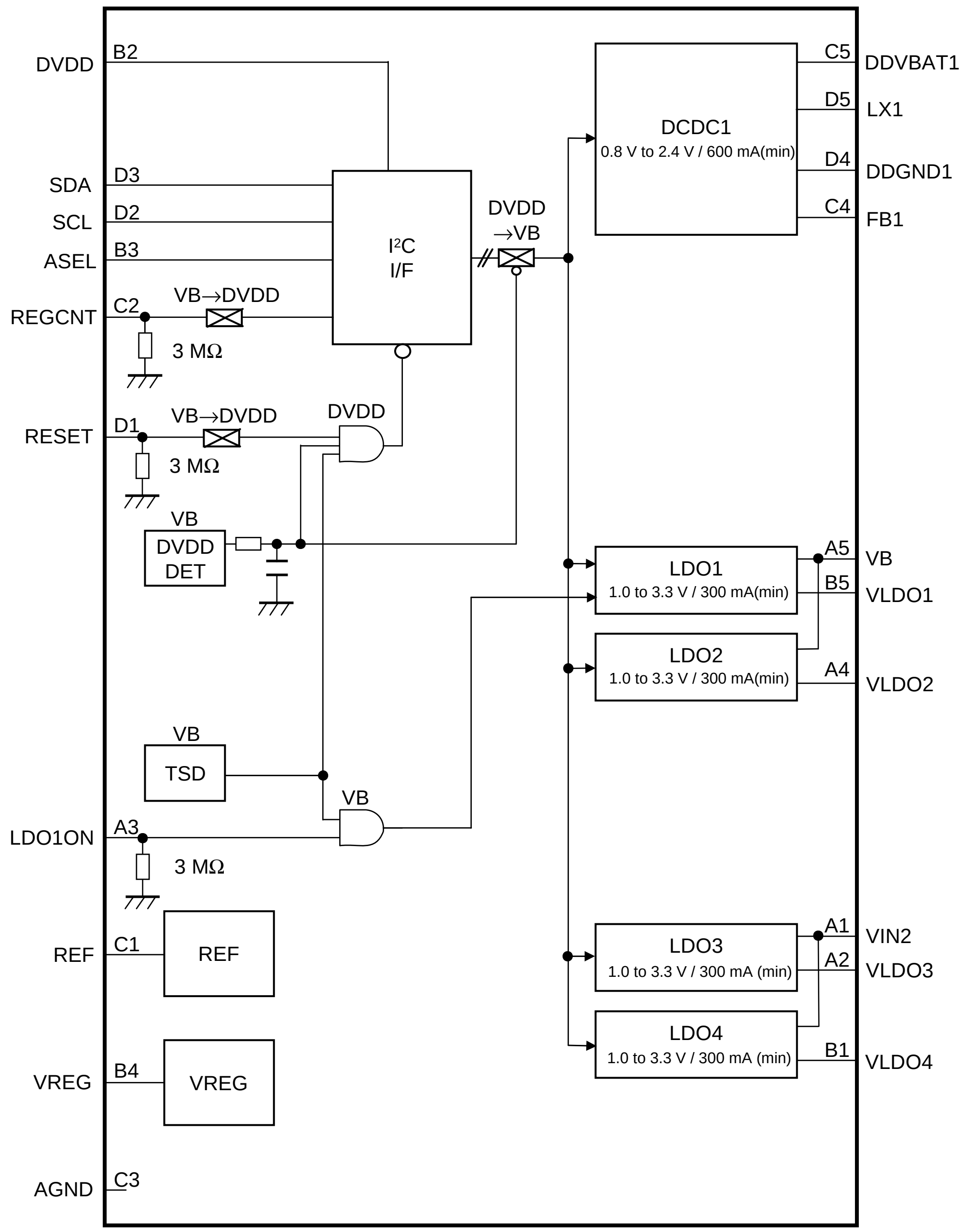



## PIN FUNCTIONS

| Pin No. | Pin name | Type | Description |
|---|---|---|---|
| A1 | VIN2 | Power Supply | Input for LDO3 and LDO4 |
| A2 | VLDO3 | Output | LDO3 output |
| A3 | LDO1ON | Input | LDO1 ON/OFF control |
| A4 | VLDO2 | Output | LDO2 output |
| A5 | VB | Power Supply | Input for LDO1, LDO2 and other VB |
| B1 | VLDO4 | Output | LDO4 output |
| B2 | DVDD | Power Supply | Power supply for Logic |
| B3 | ASEL | Input | $I^2C$ slave address select |
| B4 | VREG | Output | Reference output |
| B5 | VLDO1 | Output | LDO1 output |
| C1 | REF | Output | Reference output |
| C2 | REGCNT | Input | Control to select power setting |
| C3 | AGND | Ground | GND |
| C4 | FB1 | Input | DCDC1 voltage feedback |
| C5 | DDVBAT1 | Power Supply | DCDC1 input |
| D1 | RESET | Input | Reset input for Logic |
| D2 | SCL | Input | $I^2C$ clock input |
| D3 | SDA | Input/Output | $I^2C$ data input/output |
| D4 | DDGND1 | Ground | GND |
| D5 | LX1 | Output | DCDC1 switching |

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

## FUNCTIONAL BLOCK DIAGRAM



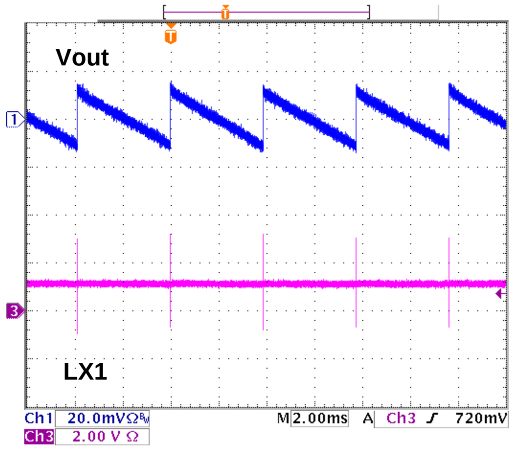

Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.
• This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

## TYPICAL CHARACTERISTICS CURVES

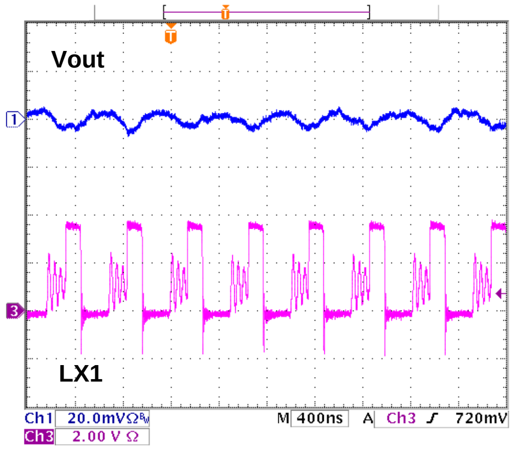
### (1) Output Ripple Voltage of DC-DC1

$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V , L1 = 1 µH , CDCDCOUT1 = 4.7 µF

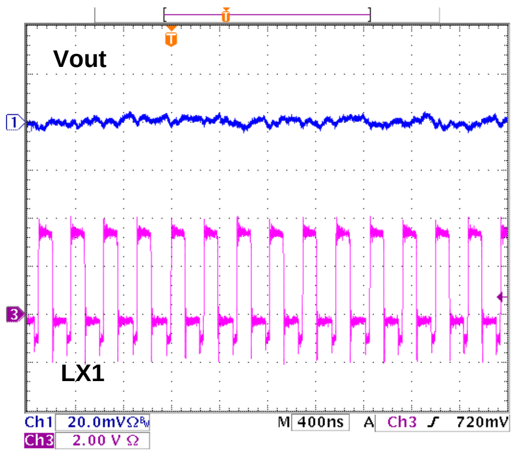
DC-DC1 , Iout = 0mA




DC-DC1 , Iout = 100mA




DC-DC1 , Iout = 600mA

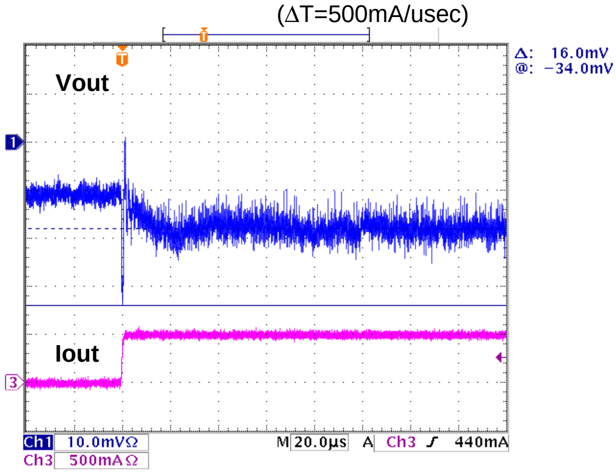


## TYPICAL CHARACTERISTICS CURVES (Continued)

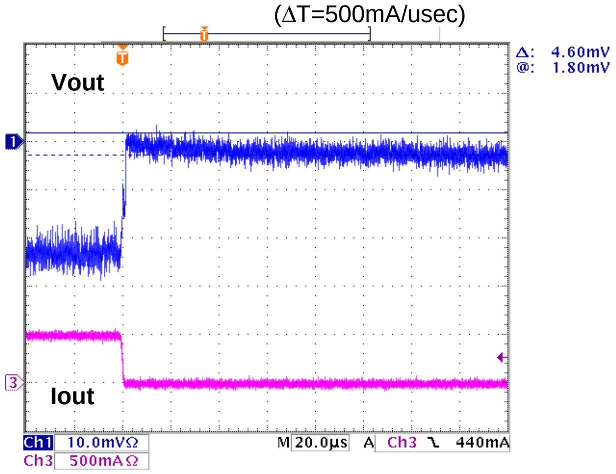
### (2) Load Transient of DC-DC1

$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V , L1 = 1 µH , CDCDCOUT1 = 4.7 µF

DC-DC1 , Iout = 10µA to 500mA
(ΔT=500mA/usec)



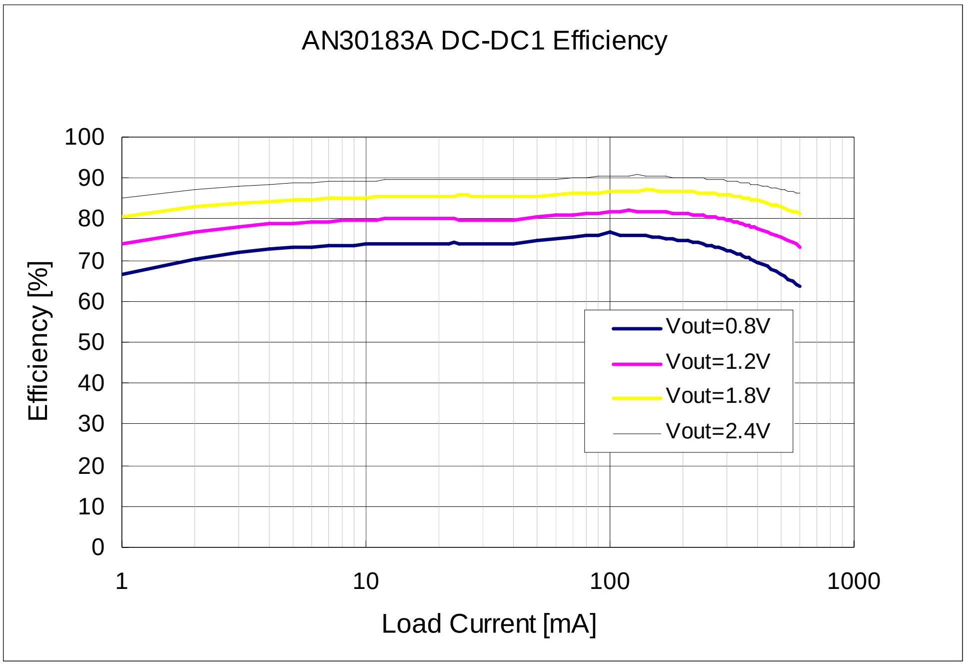

DC-DC1 , Iout = 500mA to 10µA
(ΔT=500mA/usec)



## TYPICAL CHARACTERISTICS CURVES (Continued)

**(3) Efficiency of DC-DC1**

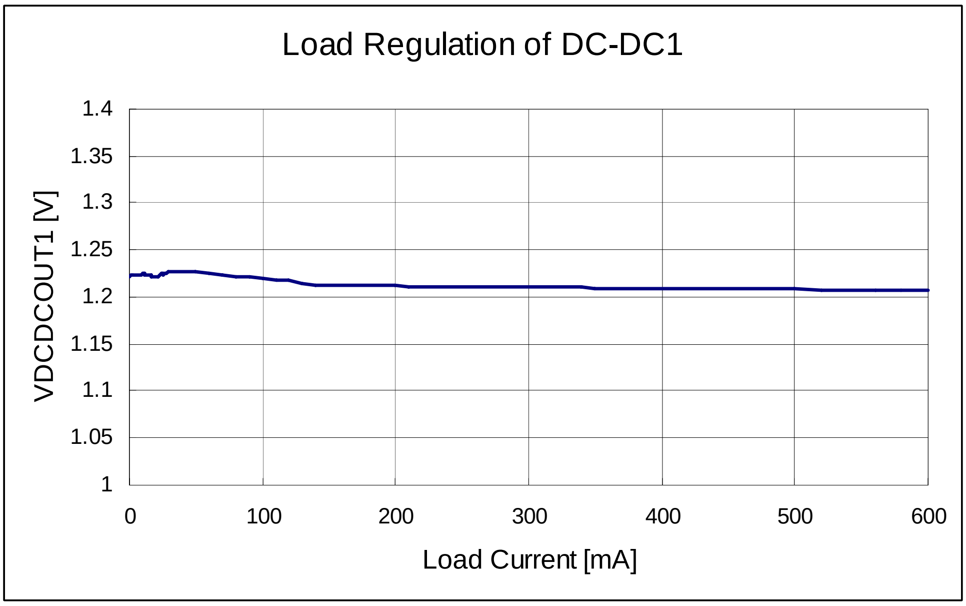
$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V , L1 = 1 µH , CDCDCOUT1 = 4.7 µF



## TYPICAL CHARACTERISTICS CURVES (Continued)

**(4) Load Regulation of DC-DC1**

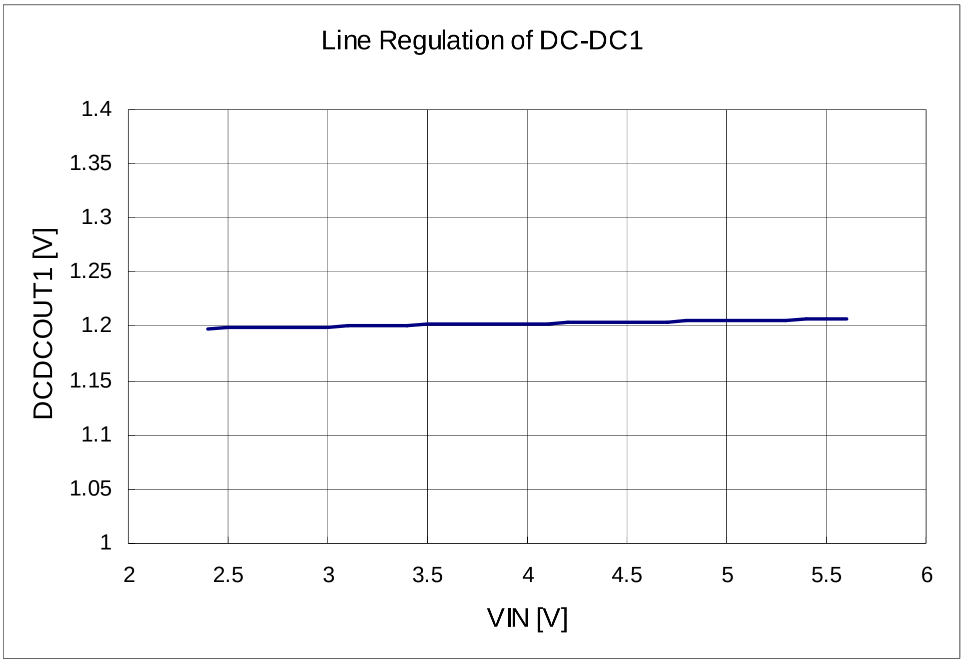
$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V , L1 = 1 µH , CDCDCOUT1 = 4.7 µF



## TYPICAL CHARACTERISTICS CURVES (Continued)

**(5) Line Regulation of DC-DC1**

Iout = 300mA, DC-DC1_Vout = 1.2 V, L1 = 1 µH , CDCDCOUT1 = 4.7 µF , $V_{IN}$ = 2.4V to 5.5V

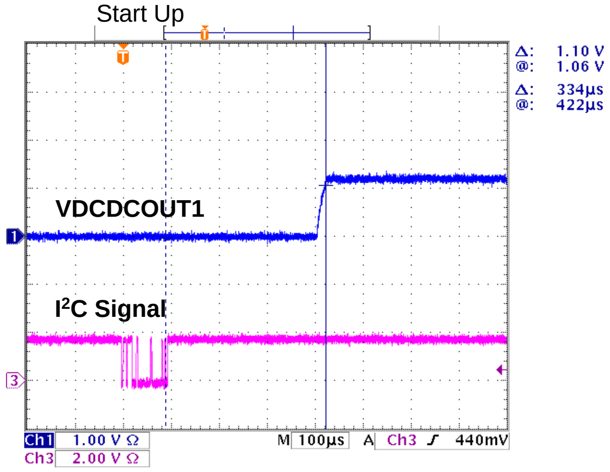


## TYPICAL CHARACTERISTICS CURVES (Continued)

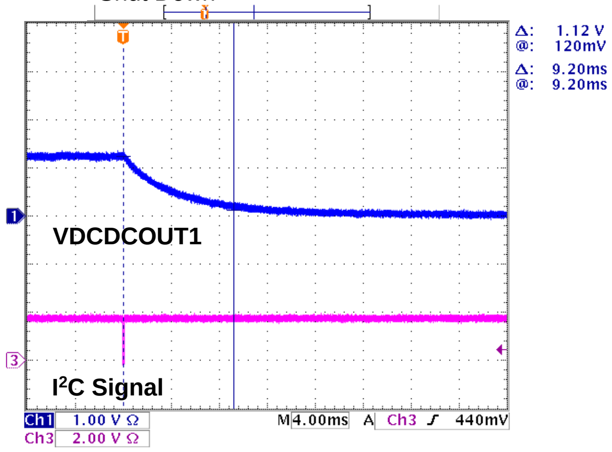
### (6) Start Up & Shut Down of DC-DC1

$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V, L1 = 1 µH , CDCDCOUT1 = 4.7 µF

DC-DC1 , RDCDCOUT1 = No Load
Start Up




DC-DC1 , RDCDCOUT1 = No Load
Shut Down



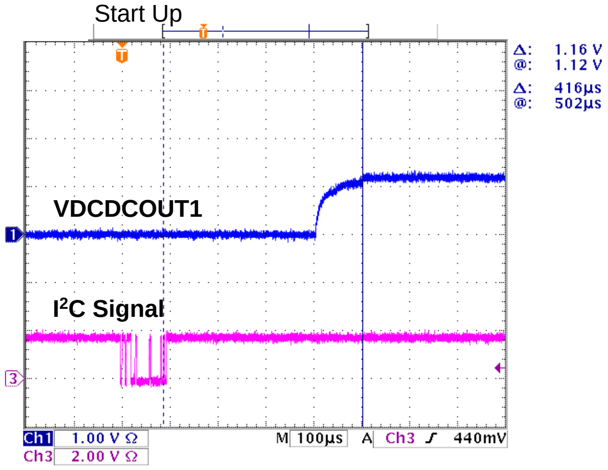
## TYPICAL CHARACTERISTICS CURVES (Continued)

**(7) Start Up & Shut Down of DC-DC1** (Continued)

$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V, L1 = 1 µH , CDCDCOUT1 = 4.7 µF

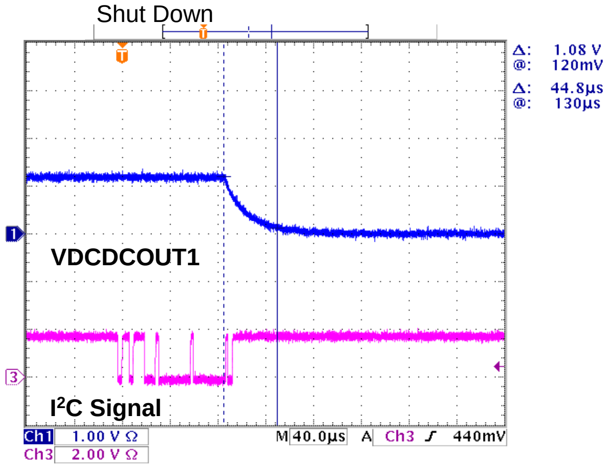
DC-DC1 , RDCDCOUT1 = 4Ω

Start Up




DC-DC1 , RDCDCOUT1 = 4Ω

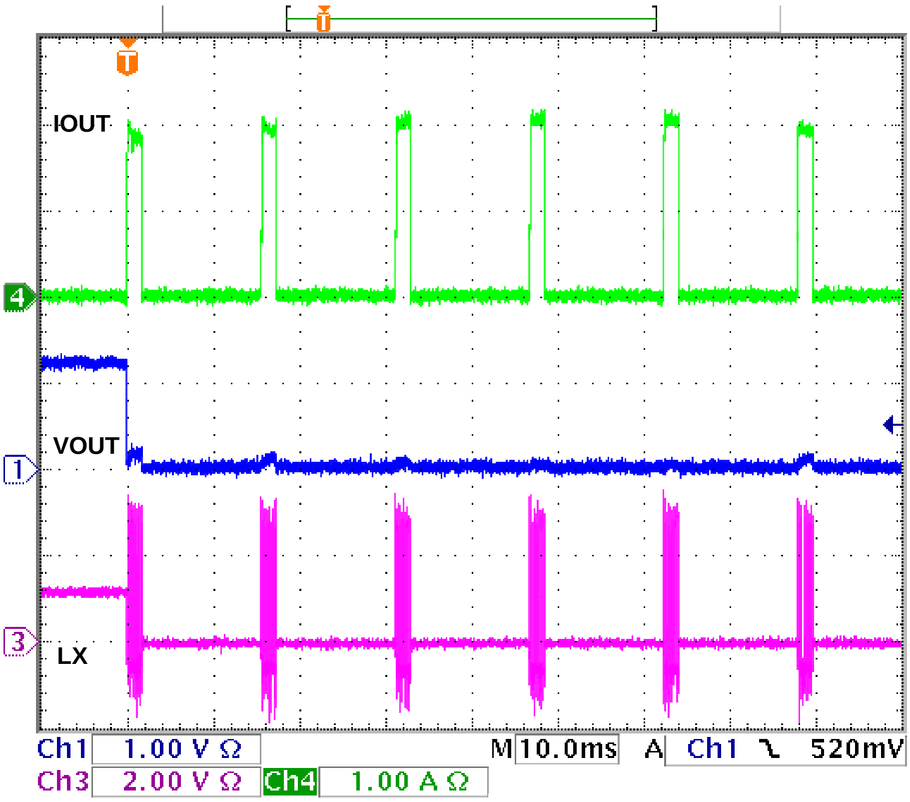
Shut Down



## TYPICAL CHARACTERISTICS CURVES (Continued)

**(8) Short Protection of DC-DC1**

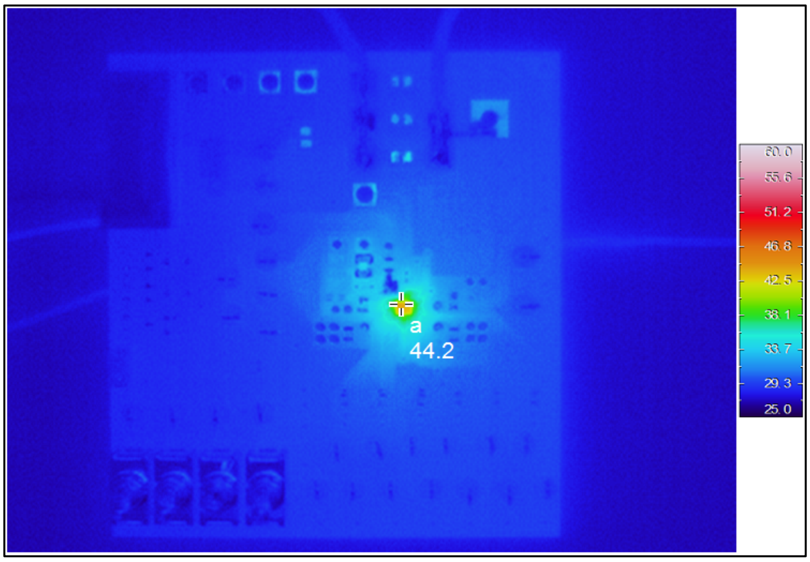
$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V, L1 = 1 µH , CDCDCOUT1 = 4.7 µF



## TYPICAL CHARACTERISTICS CURVES (Continued)

### (9) Thermal Performance of DC-DC1

$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V, ILoad = 600mA , L1 = 1 µH , CDCDCOUT1 = 4.7 µF

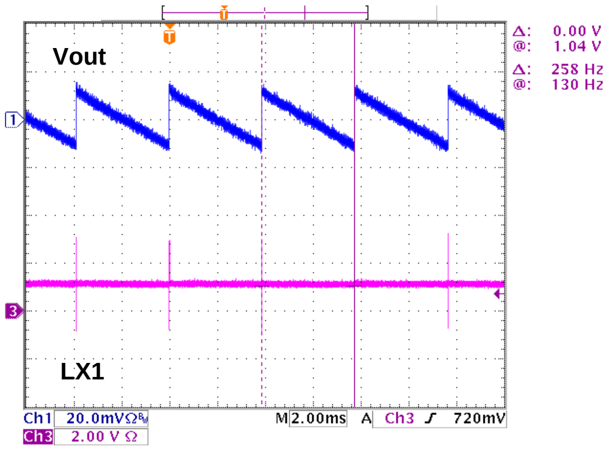


## TYPICAL CHARACTERISTICS CURVES (Continued)

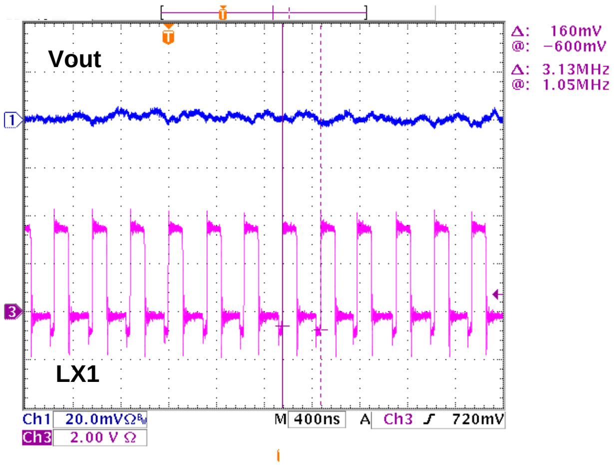
### (10) Frequency of DC-DC1

$V_{IN}$ = 3.7 V, DC-DC1_Vout = 1.2 V, L1 = 1 µH , CDCDCOUT1 = 4.7 µF

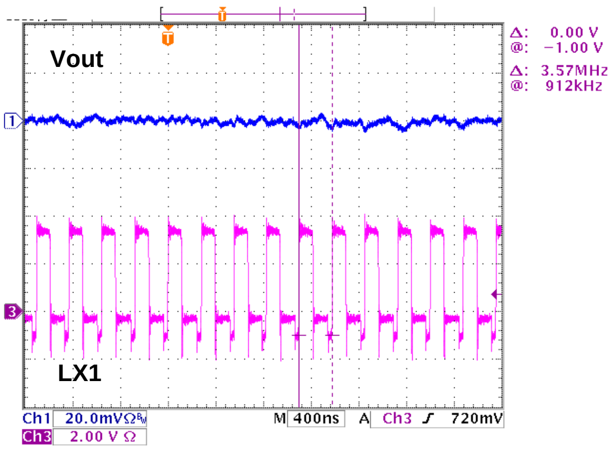
DC-DC1 , Iout = 0mA




DC-DC1 , Iout = 300mA




DC-DC1 , Iout = 600mA

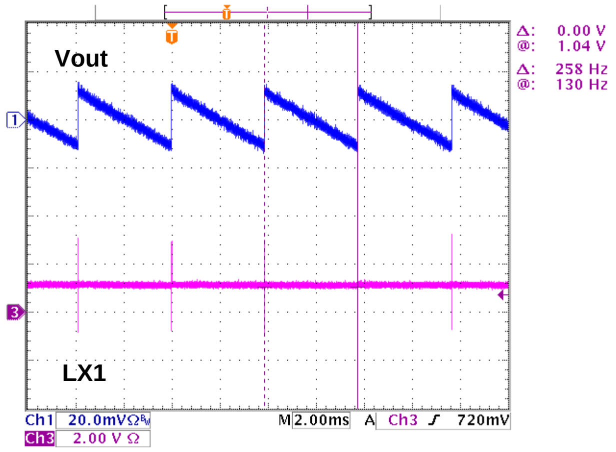


## TYPICAL CHARACTERISTICS CURVES (Continued)

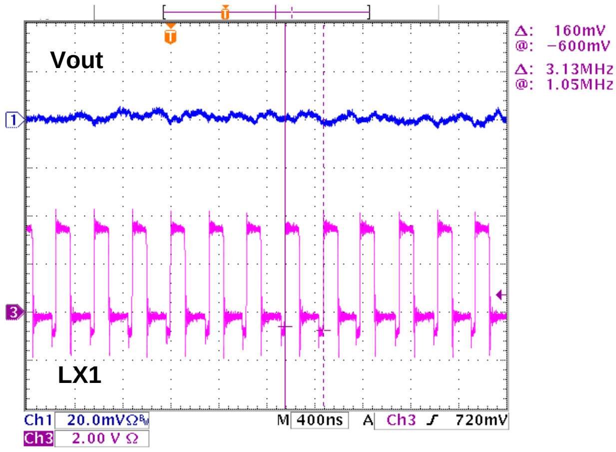
**(11) Frequency of DC-DC1** (Continued)

IOUT = 300mA, DC-DC1_Vout = 1.2 V, L1 = 1 µH , CDCDCOUT1 = 4.7 µF

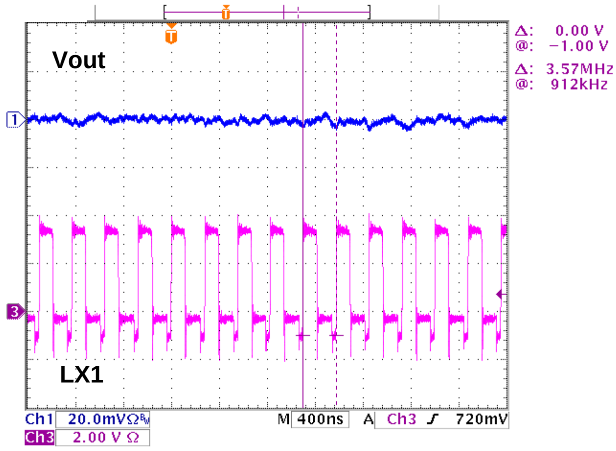
DC-DC1 , VIN = 2.5V




DC-DC1 , VIN = 3.7V




DC-DC1 , VIN = 5.5V



## OPERATION

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

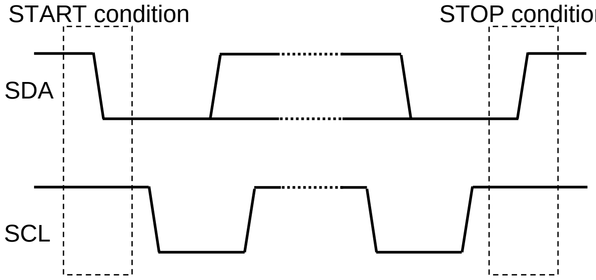
### 1. I$^2$C-bus Interface

a.) Basic Rules

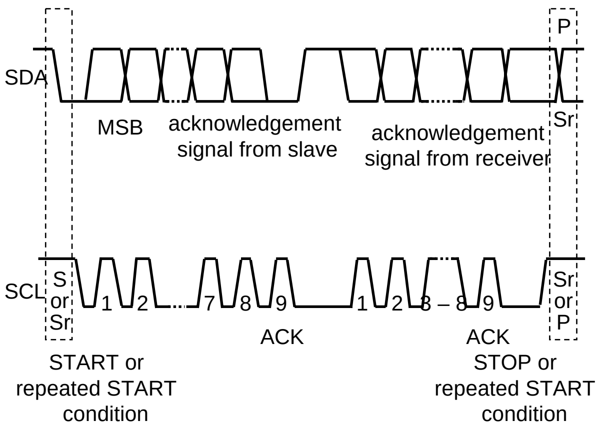
This IC, I2C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the HS-mode (to 3.4 Mbps). This IC will operate as a slave device in the I$^2$C-bus system. This IC will not operate as a master device. The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if the IC will be used in these mode systems. The I$^2$C is the brand of NXP.

b.) START and STOP conditions

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCL is High defines STOP condition. START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy. The bus is considered to be free again a certain time after the STOP condition.




Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

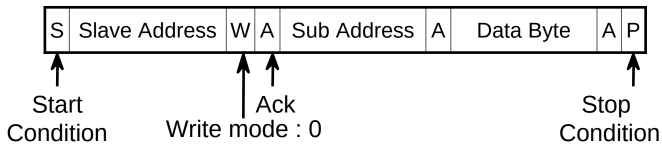



d.) Data format

Slave Address

| Pin ASEL | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Hex |
|---|---|---|---|---|---|---|---|---|---|
| Low | 1 | 1 | 1 | 0 | 0 | 1 | 0 | x | 6Eh |
| High | 1 | 1 | 1 | 0 | 0 | 1 | 1 | x | 6Fh |

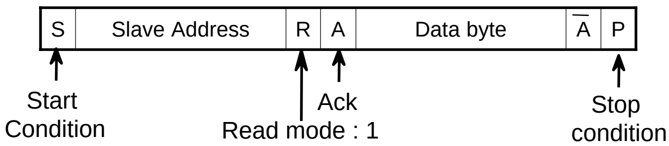
Write mode



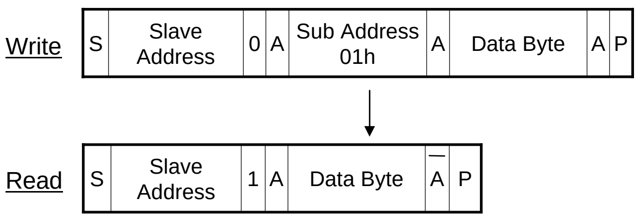

Read mode

d1.) When Sub address is not specified

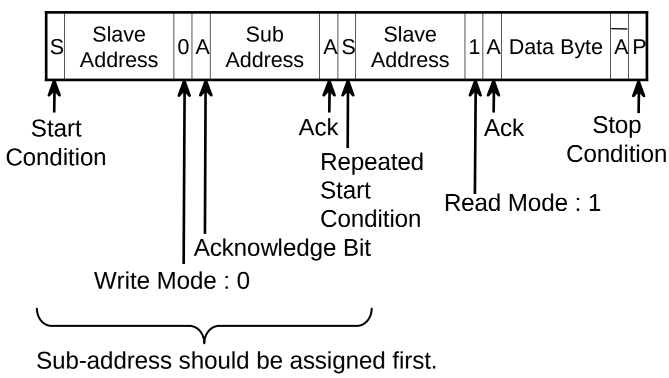
When data is read without assigning sub-address, it is possible to read the value of sub-address specified in Write mode immediately before.




Ex) When writing data into address and reading data from "01 h".




d2.) When Sub address is specified



## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 2. Register map

| Sub Address | R/W | Register Name | Bit | Data D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | R/W | CNT | Name | — | — | LD4ON | LD3ON | LD2ON | LD1ON | — | DD1ON |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | R/W | DAC1 | Name | — | | | | VDC1[3:0] | | | |
| | | | Default | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 02h | R/W | DAC2 | Name | VL2[3:0] | | | | VL1[3:0] | | | |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 03h | R/W | DAC3 | Name | VL4[3:0] | | | | VL3[3:0] | | | |
| | | | Default | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 04h | R/W | GROUP | Name | GPLD4 | GPLD3 | GPLD2 | — | GPDD | — | — | GPEN |
| | | | Default | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 05h | R/W | PSCNT | Name | — | — | — | — | LD4PS | LD3PS | LD2PS | LD1PS |
| | | | Default | — | — | 0 | 0 | 0 | 0 | 0 | 0 |
| 06h | R/W | ENSEL | Name | — | — | — | — | — | — | — | LDO1EN SEL |
| | | | Default | — | — | — | — | — | — | — | 1 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Default Voltage | — | — | LDO4 | LDO3 | LDO2 | LDO1 | — | DCDC1 |
| | — | — | 2.8V | 2.6V | 1.0V | 1.85V | — | 1.2V |

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00h | R/W | CNT | Name | — | — | LD4ON | LD3ON | LD2ON | LD1ON | — | DD1ON |
| | | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D5 : LDO4 ON/OFF select register
[0] : OFF (default)
[1] : ON

D4 : LDO3 ON/OFF select register
[0] : OFF (default)
[1] : ON

D3 : LDO2 ON/OFF select register
[0] : OFF (default)
[1] : ON

D2 : LDO1 ON/OFF select register
[0] : OFF (default)
[1] : ON

D0 : DCDC1 ON/OFF select register
[0] : OFF (default)
[1] : ON

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01h | R/W | DAC1 | Name | — | | | | VDC1[3:0] | | | |
| | | | Default | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

D3-0 : DCDC1 Register for output voltage setup

| VDC1[3:0] | | | | Output voltage [V] |
|---|---|---|---|---|
| D7 | D6 | D5 | D4 | |
| 0 | 0 | 0 | 0 | 0.80 |
| 0 | 0 | 0 | 1 | 0.85 |
| 0 | 0 | 1 | 0 | 0.90 |
| 0 | 0 | 1 | 1 | 0.95 |
| 0 | 1 | 0 | 0 | 1.00 |
| 0 | 1 | 0 | 1 | 1.05 |
| 0 | 1 | 1 | 0 | 1.10 |
| 0 | 1 | 1 | 1 | 1.15 |
| 1 | 0 | 0 | 0 | 1.20 (Default) |
| 1 | 0 | 0 | 1 | 1.30 |
| 1 | 0 | 1 | 0 | 1.40 |
| 1 | 0 | 1 | 1 | 1.50 |
| 1 | 1 | 0 | 0 | 1.65 |
| 1 | 1 | 0 | 1 | 1.80 |
| 1 | 1 | 1 | 0 | 1.85 |
| 1 | 1 | 1 | 1 | 2.40 |

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02h | R/W | DAC2 | Name | VL2[3:0] | | | | VL1[3:0] | | | |
| | | | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

D7-4 : LDO2 Register for output voltage setup

| VL2[3:0] | | | | Output voltage [V] |
|---|---|---|---|---|
| D7 | D6 | D5 | D4 | |
| 0 | 0 | 0 | 0 | 1.00 (Default) |
| 0 | 0 | 0 | 1 | 1.10 |
| 0 | 0 | 1 | 0 | 1.20 |
| 0 | 0 | 1 | 1 | 1.30 |
| 0 | 1 | 0 | 0 | 1.40 |
| 0 | 1 | 0 | 1 | 1.50 |
| 0 | 1 | 1 | 0 | 1.60 |
| 0 | 1 | 1 | 1 | 1.70 |
| 1 | 0 | 0 | 0 | 1.80 |
| 1 | 0 | 0 | 1 | 1.85 |
| 1 | 0 | 1 | 0 | 2.60 |
| 1 | 0 | 1 | 1 | 2.70 |
| 1 | 1 | 0 | 0 | 2.80 |
| 1 | 1 | 0 | 1 | 2.85 |
| 1 | 1 | 1 | 0 | 3.00 |
| 1 | 1 | 1 | 1 | 3.30 |

D3-0 : LDO1 Register for output voltage setup

| VL1[3:0] | | | | Output voltage [V] |
|---|---|---|---|---|
| D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | 1.00 |
| 0 | 0 | 0 | 1 | 1.10 |
| 0 | 0 | 1 | 0 | 1.20 |
| 0 | 0 | 1 | 1 | 1.30 |
| 0 | 1 | 0 | 0 | 1.40 |
| 0 | 1 | 0 | 1 | 1.50 |
| 0 | 1 | 1 | 0 | 1.60 |
| 0 | 1 | 1 | 1 | 1.70 |
| 1 | 0 | 0 | 0 | 1.80 |
| 1 | 0 | 0 | 1 | 1.85 (Default) |
| 1 | 0 | 1 | 0 | 1.90 |
| 1 | 0 | 1 | 1 | 2.70 |
| 1 | 1 | 0 | 0 | 2.80 |
| 1 | 1 | 0 | 1 | 2.85 |
| 1 | 1 | 1 | 0 | 3.00 |
| 1 | 1 | 1 | 1 | 3.30 |

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03h | R/W | DAC3 | Name | VL4[3:0] | | | | VL3[3:0] | | | |
| | | | Default | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

D7-4 : LDO4 Register for output voltage setup

| VL4[3:0] | | | | Output voltage [V] |
|---|---|---|---|---|
| D7 | D6 | D5 | D4 | |
| 0 | 0 | 0 | 0 | 1.00 |
| 0 | 0 | 0 | 1 | 1.10 |
| 0 | 0 | 1 | 0 | 1.20 |
| 0 | 0 | 1 | 1 | 1.30 |
| 0 | 1 | 0 | 0 | 1.40 |
| 0 | 1 | 0 | 1 | 1.50 |
| 0 | 1 | 1 | 0 | 1.60 |
| 0 | 1 | 1 | 1 | 1.70 |
| 1 | 0 | 0 | 0 | 1.80 |
| 1 | 0 | 0 | 1 | 1.85 |
| 1 | 0 | 1 | 0 | 2.60 |
| 1 | 0 | 1 | 1 | 2.70 |
| 1 | 1 | 0 | 0 | 2.80 (Default) |
| 1 | 1 | 0 | 1 | 2.85 |
| 1 | 1 | 1 | 0 | 3.00 |
| 1 | 1 | 1 | 1 | 3.30 |

D3-0 : LDO3 Register for output voltage setup

| VL3[3:0] | | | | Output voltage [V] |
|---|---|---|---|---|
| D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | 1.00 |
| 0 | 0 | 0 | 1 | 1.10 |
| 0 | 0 | 1 | 0 | 1.20 |
| 0 | 0 | 1 | 1 | 1.30 |
| 0 | 1 | 0 | 0 | 1.40 |
| 0 | 1 | 0 | 1 | 1.50 |
| 0 | 1 | 1 | 0 | 1.60 |
| 0 | 1 | 1 | 1 | 1.70 |
| 1 | 0 | 0 | 0 | 1.80 |
| 1 | 0 | 0 | 1 | 1.85 |
| 1 | 0 | 1 | 0 | 2.60 (Default) |
| 1 | 0 | 1 | 1 | 2.70 |
| 1 | 1 | 0 | 0 | 2.80 |
| 1 | 1 | 0 | 1 | 2.85 |
| 1 | 1 | 1 | 0 | 3.00 |
| 1 | 1 | 1 | 1 | 3.30 |

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04h | R/W | GROUP | Name | GPLD4 | GPLD3 | GPLD2 | — | GPDD | — | — | GPEN |
| | | | Default | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

* Please set it to normal mode when LDO starts.

D7 : External pin ON/OFF control for LDO4 select register
[0] : I2C control
[1] : External pin control (default)

D6 : External pin ON/OFF control for LDO3 select register
[0] : I2C control
[1] : External pin control (default)

D5 : External pin ON/OFF control for LDO2 select register
[0] : I2C control
[1] : External pin control (default)

D3 : External pin ON/OFF control for DCDC1 select register
[0] : I2C control
[1] : External pin control (default)

D0 : External pin control permit register
[0] : External pin control valid (default)
[1] : External pin control invalid

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

<REGCNT pin control – set up method>

(1) REGCNT Pin Control setup (excluding LDO1)

- Initial setup

1) Select the LDO/DCDC to be controlled by REGCNT
   (Address:04h Single Bit from D7-5, D3 should be set to "H")
   Set D0 to "H"
2) Set the LDO/DCDC Startup register mentioned above in ① to "H"
   (To control LDO1 set Address:00h D2:LDO1ON to "H")
   Set the LDO to be controlled to Normal Mode (Address:05h Default)

- Startup Control

3) LDO/DCDC selected in 1) above will startup when REGCNT is set to "H"
   Power Save Mode for the LDO can be controlled by the $I^2C$
   When the Startup register mentioned in 2) above (Address:00h) is set to "L", the LDO/DCDC will turn off.
4) The Startup for LDO/DCDC not selected in 1) can also be controlled by the $I^2C$
5) To turn off the LDO mentioned in 1) above, set the REGCNT to "L".
   When the LDO is turned OFF in the Power Save Mode, reset Address:05h to Normal Mode before turning on the LDO using the REGCNT pin.

- Example Using the REGCNT pin to control LDO2 and LDO3

1) ADDRESS 04h : DATA 61h
2) ADDRESS 00h : DATA 18h
3) Set REGCNT pin "L" to "H" : LDO2,3 Startup
4) Use $I^2C$ to control the Output Voltage and Power Save Mode settings
5) To stop LDO2 and LDO3, Set REGCNT from "H" to "L"

(2) Control using the $I^2C$ only

- Initial Setup
  No special settings required after RESET
  (ADDRESS 04h Bit D0 set to "L)

- (Startup control)
  The REGCNT pin should be set to "L" when using the $I^2C$ for LDO/DCDC Startup/Shutdown, Power Save Mode and Output Voltage Setup.

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05h | R/W | PSCNT | Name | — | — | — | — | LD4PS | LD3PS | LD2PS | LD1PS |
| | | | Default | — | — | 0 | 0 | 0 | 0 | 0 | 0 |

*Please set it to normal mode when LDO starts.

D3 : LDO4 Power save mode select register
[0] : Normal mode (default)
[1] : Power save mode

D2 : LDO3 Power save mode select register
[0] : Normal mode (default)
[1] : Power save mode

D1 : LDO2 Power save mode select register
[0] : Normal mode (default)
[1] : Power save mode

D0 : LDO1 Power save mode select register
[0] : Normal mode (default)
[1] : Power save mode

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 3. Register map details

| Sub Address | R/W | Register Name | Bit | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 06h | R/W | ENSEL | Name | — | — | — | — | — | — | — | LDO1EN SEL |
| | | | Default | — | — | — | — | — | — | — | 1 |

D0 : LDO1ENSEL

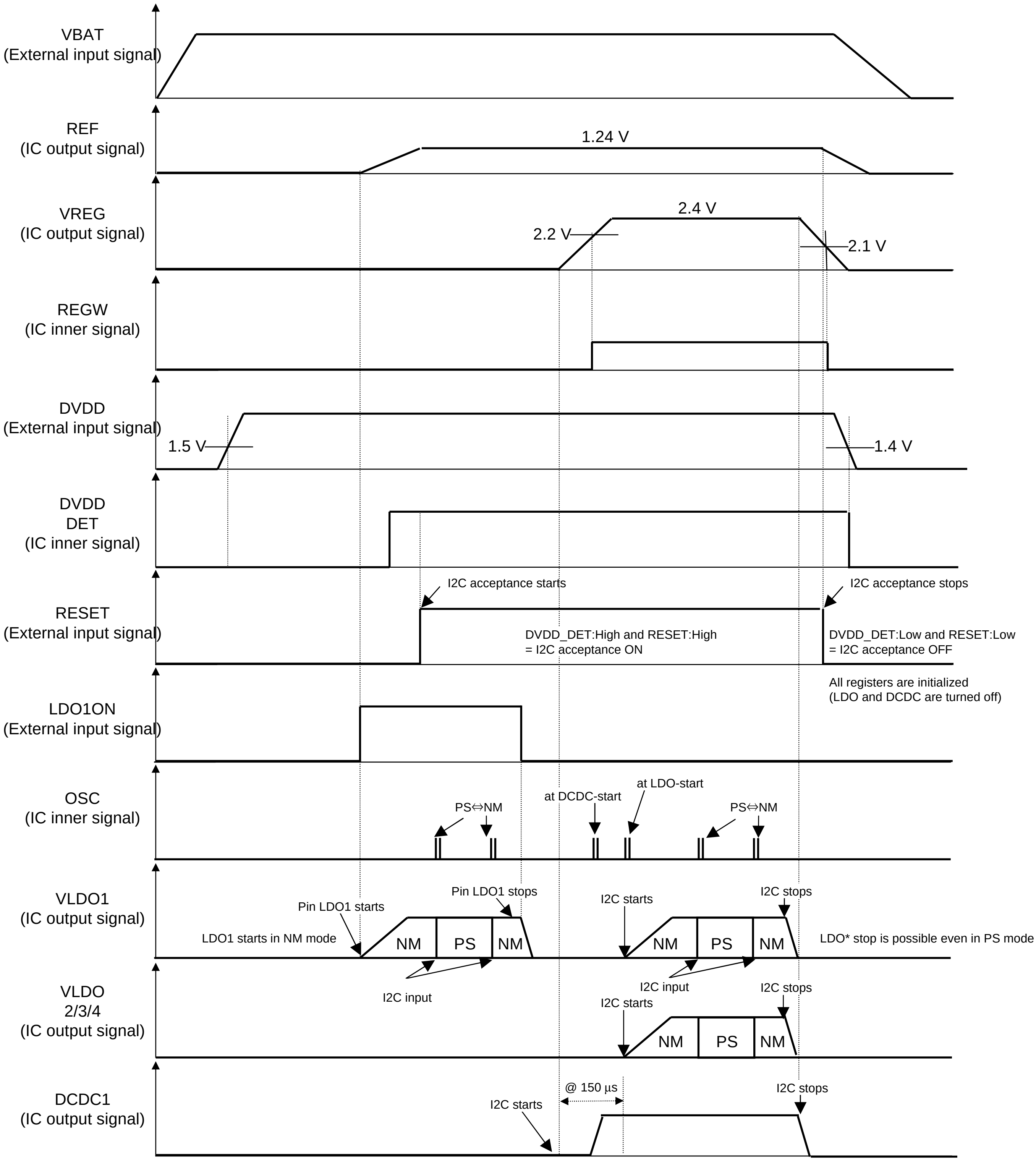
[0] : LDO1ON control invalid

[1] : LDO1ON control valid (default)

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

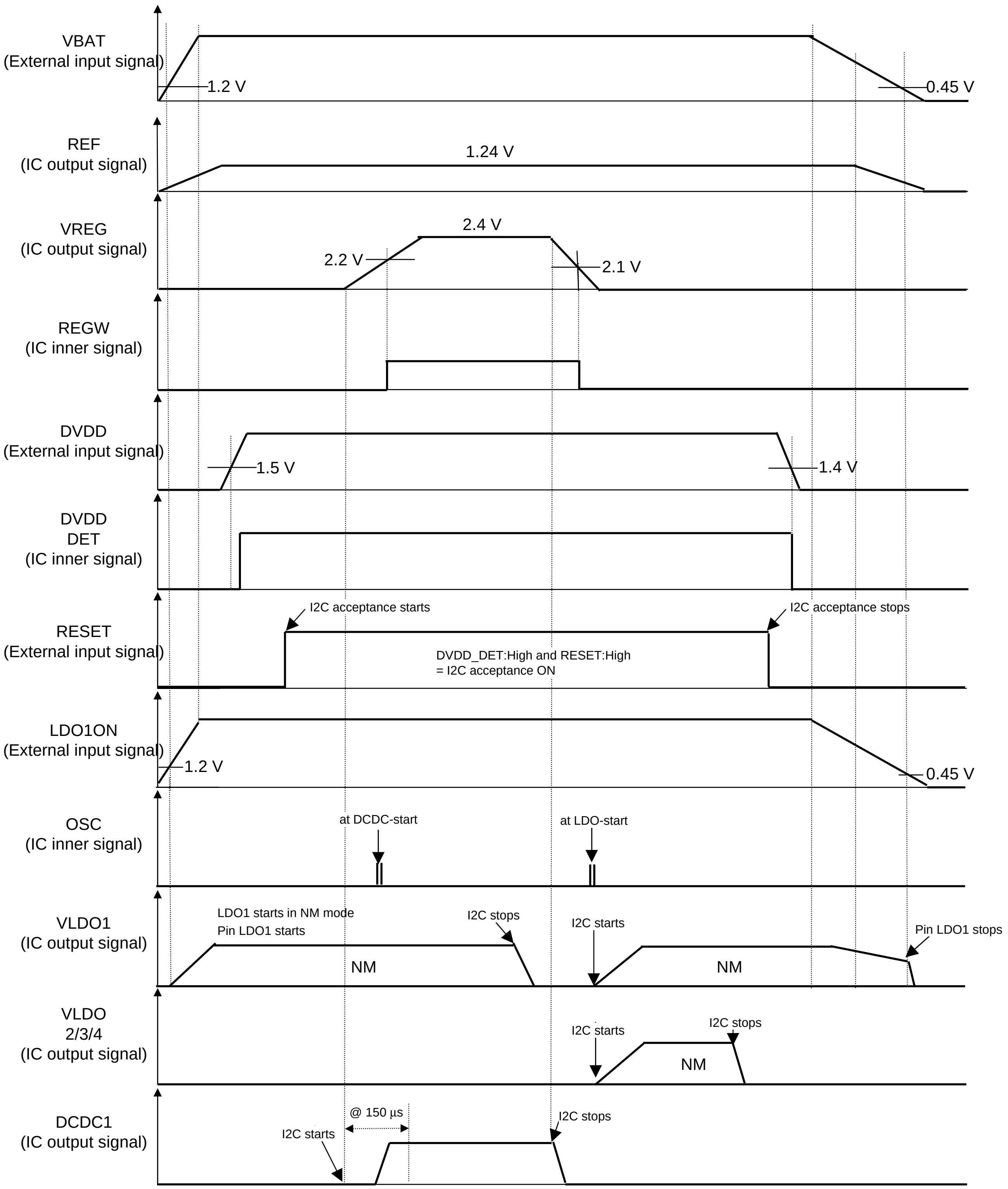
### 4. Timing Chart (Sequence – 1 (DVDD input externally))



## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

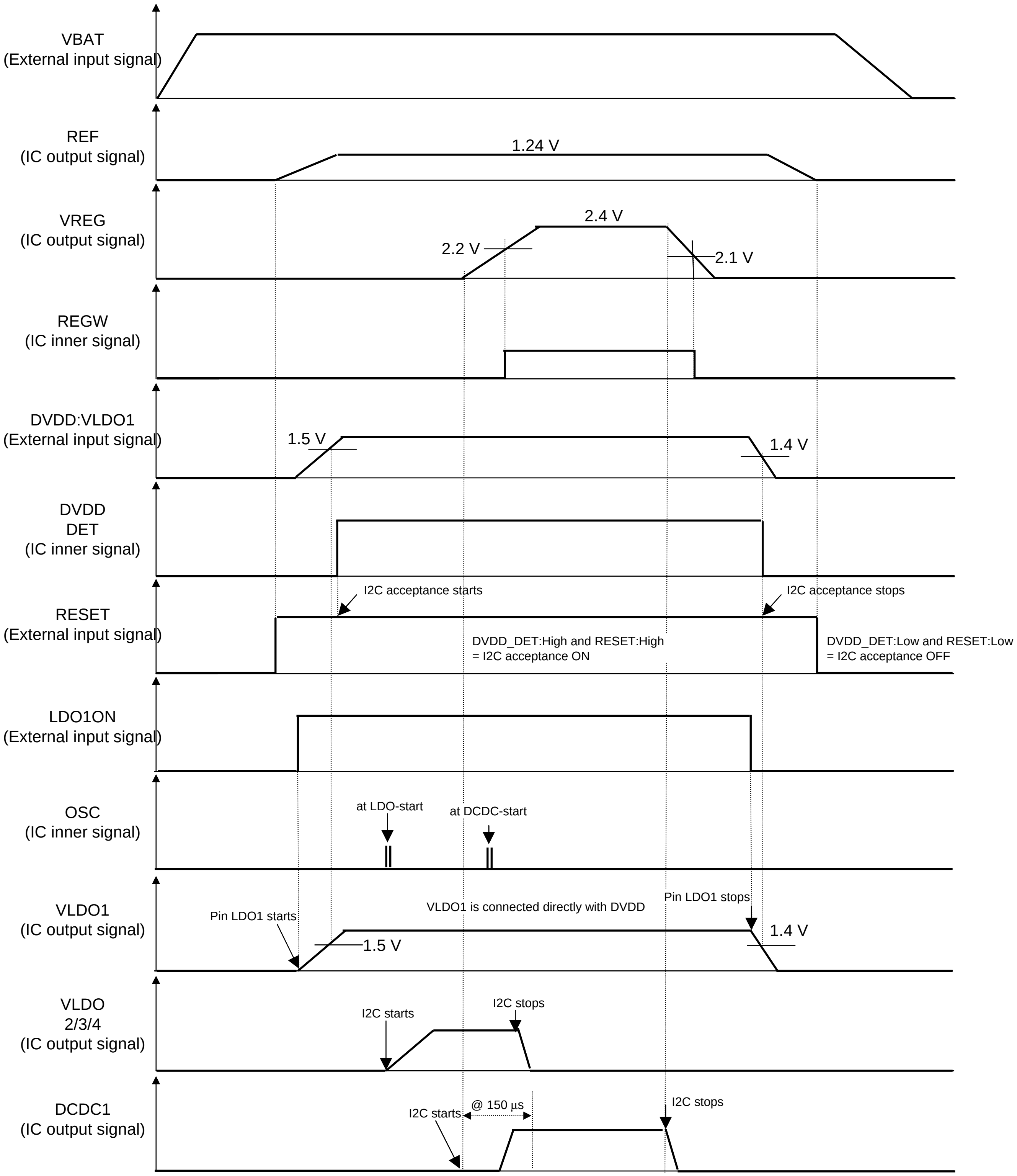
### 4. Timing Chart (Sequence – 2 (LDO1ON = fixed VBAT))



## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

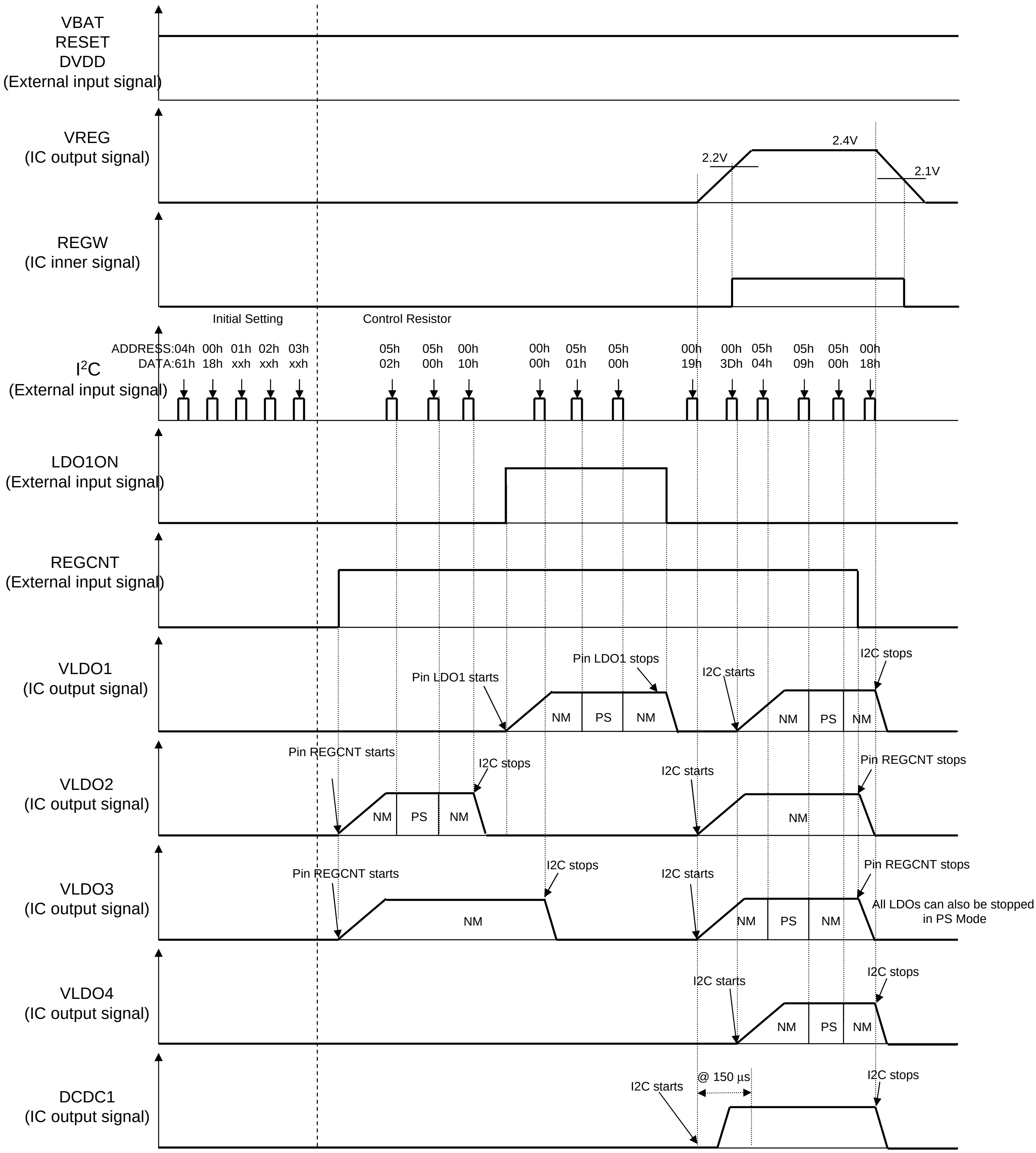
### 4. Timing Chart (Sequence – 3 (VLDO1 = connected DVDD))



## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

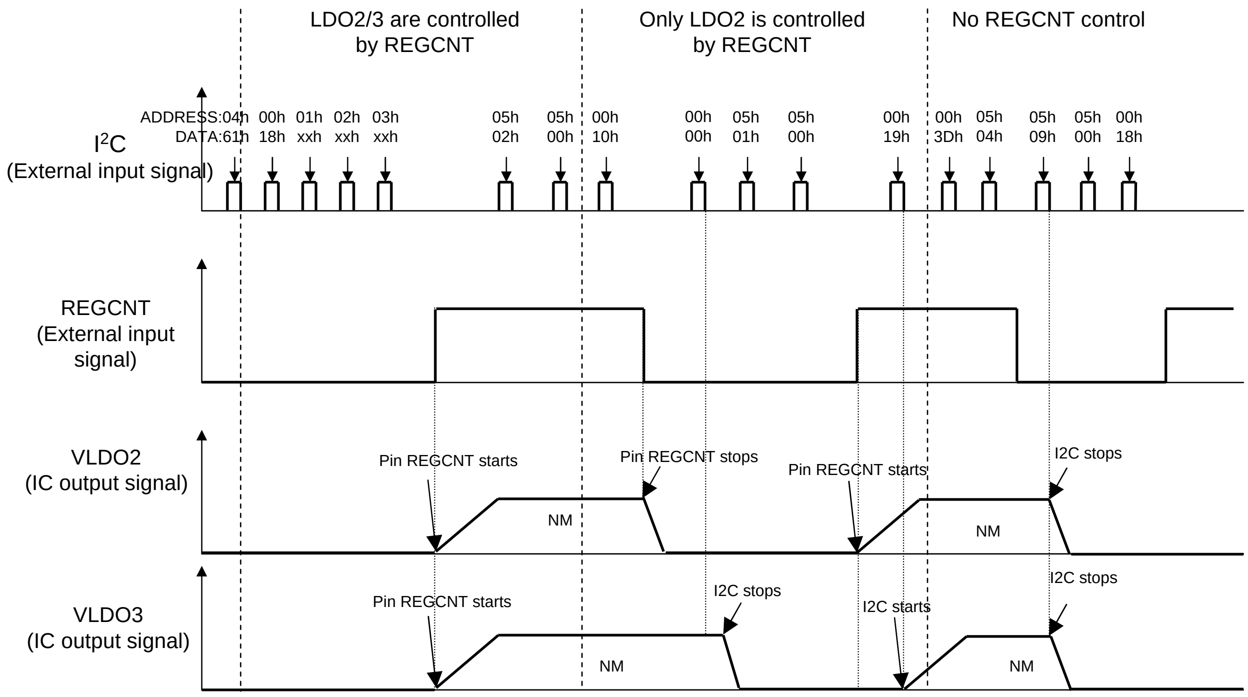
### 4. Timing Chart (Sequence – 4 (LDO2/3 are controlled by REGCNT))



## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 4. Timing Chart (Sequence – 4 (LDO2/3 are controlled by REGCNT)) (continued)



## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

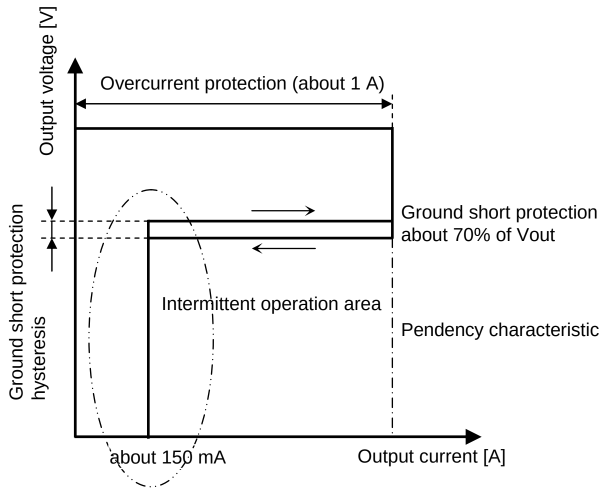
### 5. DC-DC Protection Operation

< Operation explanation >

(1) The Overcurrent protection operates at about 1 A (Typ).

(2) The Ground protection sequence is implemented when the output voltage decreases to about 70% of the set voltage.

(3) The Ground short protection operates intermittently. (2 ms : ON, 16 ms : OFF)




Operation explanation chart

### 6. DAC voltage Accuracy

DCDC1 (VBAT = 3.7 V , Iout = –300 mA)

| VDC1[3:0] | | | | Output voltage [V] | Accuracy [%] |
|---|---|---|---|---|---|
| D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0.80 | ±8.5 |
| 0 | 0 | 0 | 1 | 0.85 | ±6.5 |
| 0 | 0 | 1 | 0 | 0.90 | ±6.5 |
| 0 | 0 | 1 | 1 | 0.95 | ±6.0 |
| 0 | 1 | 0 | 0 | 1.00 | ±6.0 |
| 0 | 1 | 0 | 1 | 1.05 | ±5.0 |
| 0 | 1 | 1 | 0 | 1.10 | ±4.0 |
| 0 | 1 | 1 | 1 | 1.15 | ±3.5 |
| 1 | 0 | 0 | 0 | 1.20 (Default) | ±2.5 |
| 1 | 0 | 0 | 1 | 1.30 | ±3.0 |
| 1 | 0 | 1 | 0 | 1.40 | ±4.0 |
| 1 | 0 | 1 | 1 | 1.50 | ±3.0 |
| 1 | 1 | 0 | 0 | 1.65 | ±3.0 |
| 1 | 1 | 0 | 1 | 1.80 | ±4.0 |
| 1 | 1 | 1 | 0 | 1.85 | ±3.0 |
| 1 | 1 | 1 | 1 | 2.40 | ±3.0 |

## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 6. DAC Voltage Accuracy (continued)

LDO VBAT = 3.7 V (Normal-mode : Iout = – 150 mA, PS-mode : Iout = – 5 mA)

| VL1[3:0] | | | | Output voltage [V] | Accuracy [%] | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Normal-mode | | PS-mode | |
| D3 | D2 | D1 | D0 | | LDO1 | LDO2 to 4 | LDO1 | LDO2 to 4 |
| 0 | 0 | 0 | 0 | 1.00 | ±5.0 | ±5.0 | ±5.0 | ±5.0 |
| 0 | 0 | 0 | 1 | 1.10 | ±4.5 | ±4.5 | ±4.5 | ±4.5 |
| 0 | 0 | 1 | 0 | 1.20 | ±4.0 | ±4.0 | ±4.0 | ±4.0 |
| 0 | 0 | 1 | 1 | 1.30 | ±4.0 | ±4.0 | ±4.0 | ±4.0 |
| 0 | 1 | 0 | 0 | 1.40 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 0 | 1 | 0 | 1 | 1.50 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 0 | 1 | 1 | 0 | 1.60 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 0 | 1 | 1 | 1 | 1.70 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 1 | 0 | 0 | 0 | 1.80 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 1 | 0 | 0 | 1 | 1.85 | ±2.5 | ±2.5 | ±2.5 | ±2.5 |
| 1 | 0 | 1 | 0 | 1.90 | ±2.5 | — | ±2.5 | — |
| | | | | 2.60 | — | ±3.0 | — | ±3.0 |
| 1 | 0 | 1 | 1 | 2.70 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 1 | 1 | 0 | 0 | 2.80 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 1 | 1 | 0 | 1 | 2.85 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 1 | 1 | 1 | 0 | 3.00 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |
| 1 | 1 | 1 | 1 | 3.30 | ±3.0 | ±3.0 | ±3.0 | ±3.0 |

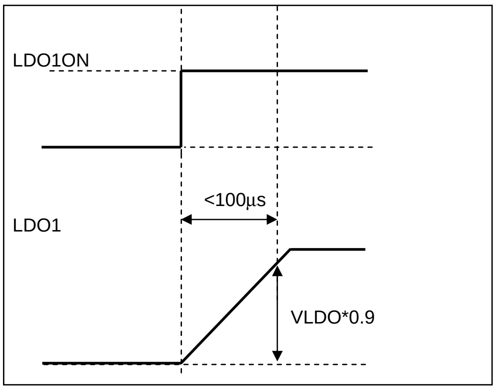
## OPERATION ( Continued )

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

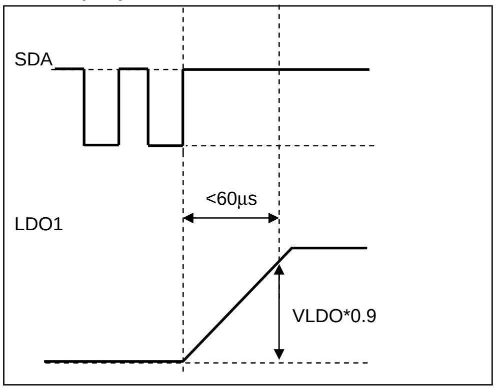
### 7. Start Up Timing from LDO1ON , REGCNT and I²C

(1) Start up LDO1

Start up by LDO1ON

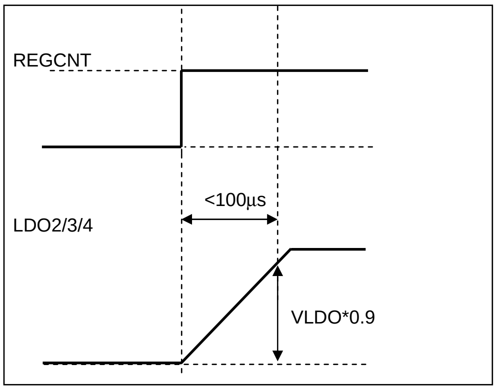



Start up by I2C

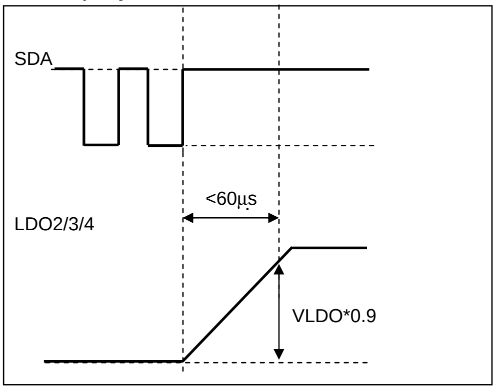



(2) Start up LDO2/3/4 and DCDC1

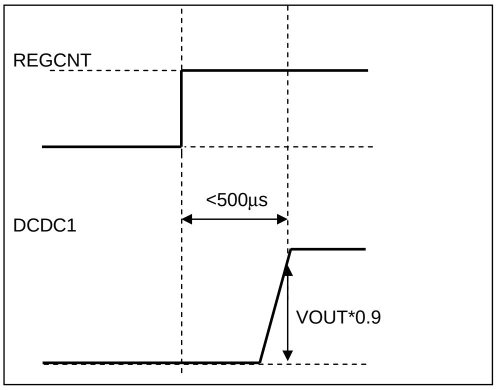
Start up by REGCNT



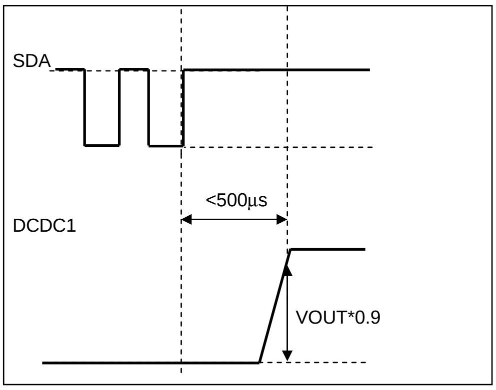

Start up by I2C




Start up by REGCNT




Start up by I2C



## APPLICATION INFORMATION

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 1.Application Circuit and Evaluation Board

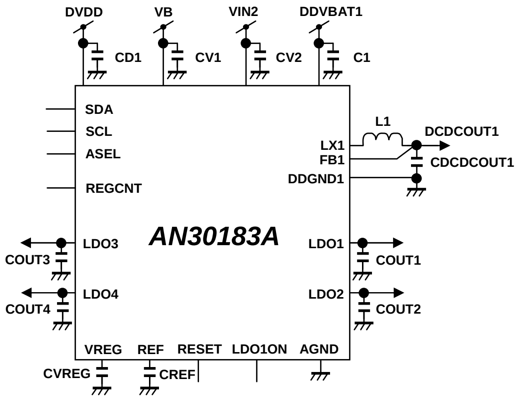



Figure : Application Circuit

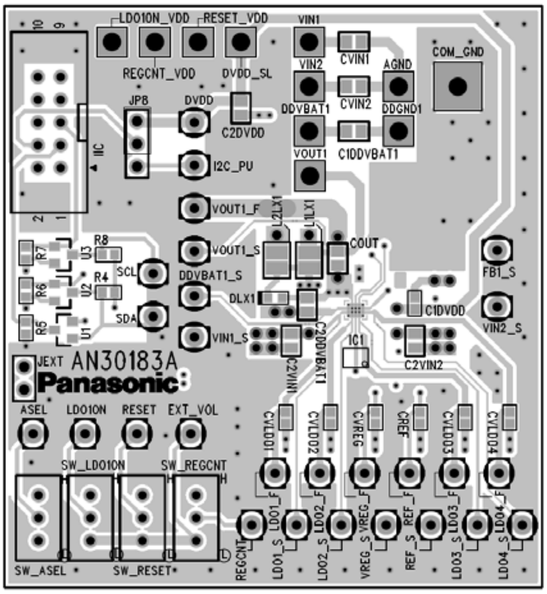


Figure : Top Layer with silk screen
( Top View ) with Evaluation Board

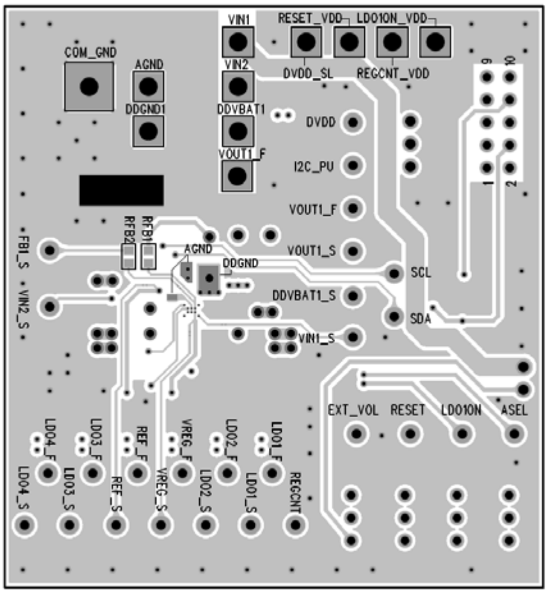


Figure : Bottom Layer with silk screen
( Bottom View ) with Evaluation Board

Notes) This application circuit and layout is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

## APPLICATION INFORMATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

### 2.RECOMMENDED COMPONENT

| Reference Designator | QTY | Value | Manufacturer | Part Number |
|---|---|---|---|---|
| C1 | 1 | 4.7µF | Murata | GRM21BB31C475KA87 |
| CV1 | 1 | 4.7µF | Murata | GRM21BB31C475KA87 |
| VC2 | 1 | 4.7µF | Murata | GRM21BB31C475KA87 |
| CD1 | 1 | 0.1µF | Murata | GRM188B11C104KA01 |
| L1 | 1 | 1.0 µH | FDK | MIPSZ2012D1R0 |
| CDCDCOUT1 | 1 | 4.7µF | Murata | GRM21BB31A475KA74 |
| COUT1 | 1 | 1.0µF | Murata | GRM185B31A105KE35 |
| COUT2 | 1 | 1.0µF | Murata | GRM185B31A105KE35 |
| COUT3 | 1 | 1.0µF | Murata | GRM185B31A105KE35 |
| COUT4 | 1 | 1.0µF | Murata | GRM185B31A105KE35 |
| CVREG | 1 | 1.0µF | Murata | GRM185B31A105KE35 |
| CREF | 1 | 1.0µF | Murata | GRM185B31A105KE35 |

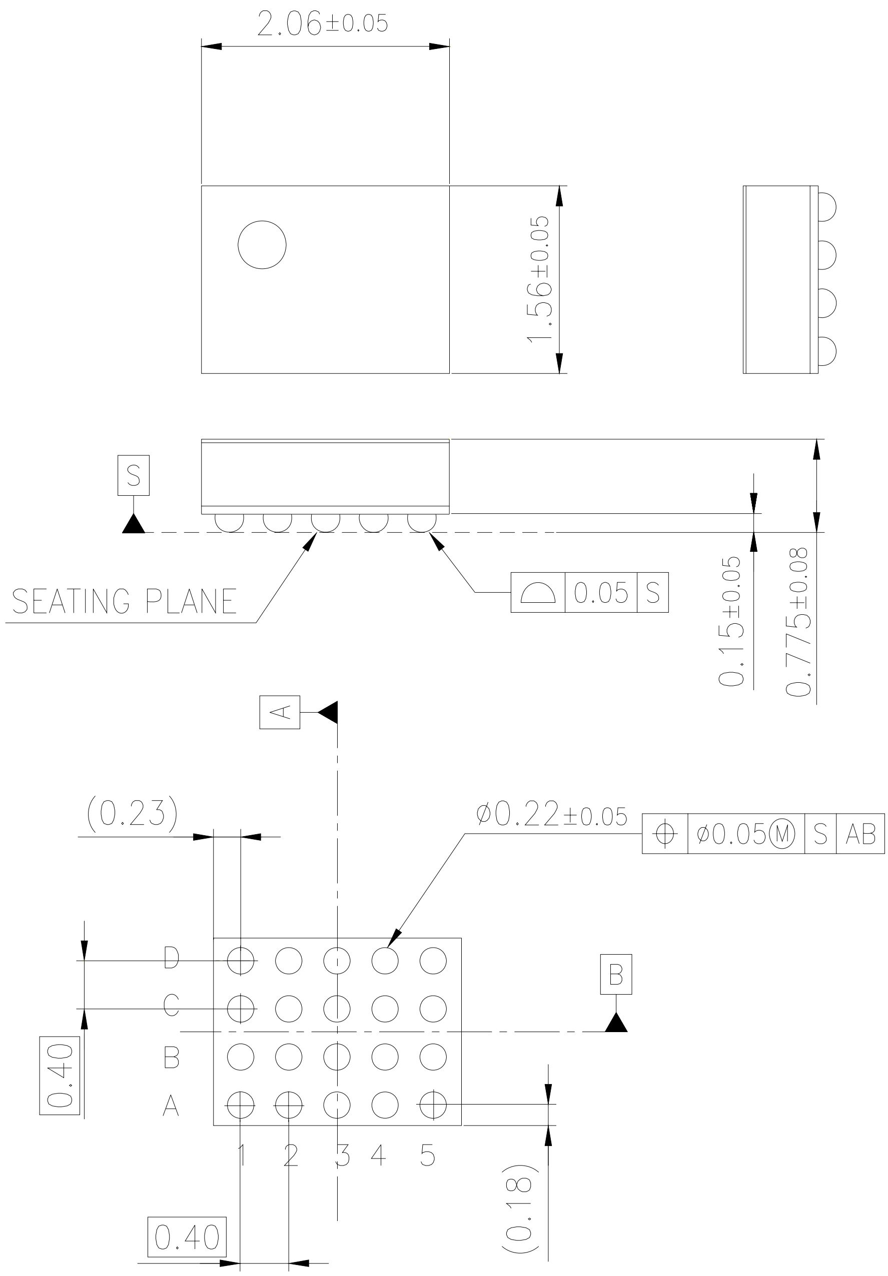
Figure : Recommended Component

## PACKAGE INFORMATION ( Reference Data )

Outline Drawing

Package Code : XBGA020-W-1621AEL

Unit:mm




| | |
|---|---|
| Body Materia l : | Br/Sb Free Epoxy resin |
| Reroute Material : | Cu |
| Bump : | SnAgCu |

## IMPORTANT NOTICE

1.The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

2.When using the LSI for new models, verify the safety including the long-term reliability for each product.

3.When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.

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Any applications other than the standard applications intended.
(1) Space appliance (such as artificial satellite, and rocket)
(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
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## USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Connect the metallic plates on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.