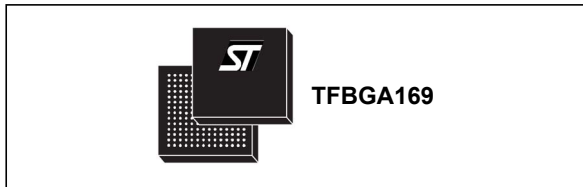

**Fully integrated GPS/Galileo/GLONASS/BeiDou/QZSS receiver
with high performance processing capability**

Datasheet - production data

**Features**

- STMicroelectronics® positioning receiver with 48 tracking channels and 2 fast acquisition channels supporting GPS, Galileo, GLONASS, BeiDou and QZSS systems
- Single die standalone receiver embedding RF Front-End and low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFB < 1 s in Hot start and 30 s in Cold Start
- High performance ARM946 MCU (up to 196 MHz)
- 256 Kbyte embedded SRAM
- FSMC external memory interface (NOR and SRAM)
- External SQI Flash interface
- 8 free running timers/ counters (32 bit)
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 3 UARTs
- 1 I²C master interface
- 1 Synchronous Serial Port (SSP, Motorola-SPI supported)
- USB2.0 full speed (12 MHz) with integrated physical layer transceiver
- 2 Controller Area Network (CAN) (STA8090EXGB only)
- 8 channels ADC (10 bits)
- 1 Secure-Digital Multimedia Memory Card Interfaces (SDMMC)

- 1 Multichannel Serial Port (MSP)
- Power Management Unit (PMU) embedding switching regulator
- Operating condition:
 - Main voltage regulator (V_{INL}): 1.6 V to 4.3 V
 - Backup voltage (V_{INB}): 1.6 V to 4.3 V
 - Digital voltage (V_{DD}): 1.0 V to 1.32 V
 - RF core voltage (V_{CC}): 1.2 V \pm 10%
 - IO Ring Voltage (V_{ddIO}): 1.8 V \pm 5% or 3.3 V \pm 10%
- Package:
 - TFPGA169 9 x 9 x 1.2 mm 0.65 pitch
- Ambient temperature range: -40/ +85 °C

Description

STA8090EXG belongs to Teseo III family products.

STA8090EXG is a highly integrated System-On-Chip GNSS receiver designed for high-flexible and cost effective solution addressing, trackers, hand-held, in-dash navigation and Telematics applications.

STA8090EXG embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including GPS, Galileo, GLONASS, BeiDou QZSS.

The STA8090EXG combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals. It embeds innovative power management unit for power consumption optimization.

STA8090EXGBD can run also TESEO-DRAW the STMicroelectronics dead reckoning firmware.

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1 Overview

STA8090EXG is one of the part number of Teseo III STA8090x series.

STA8090EXG is a highly integrated System-On-Chip GNSS receiver designed for high-flexible and cost effective solution addressing hand-held, in-dash navigation and Telematics applications.

STA8090EXG embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, European Galileo, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8090EXG ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, make this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

STA8090EXGBD can be offered also bundled with STMicroelectronics dead reckoning firmware called TESEO-DRAW; TESEO-DRAW firmware is a multi-sensors data fusion hub for Teseo family IC's.

STA8090EXG embeds innovative power management unit with switching regulator for power consumption optimization.

The extended voltage supply range from 1.6 V to 4.3 V, the 1.8 V and 3.3 V I/O compliance support make the STA8090EXG the suitable solution for different user applications.

The STA8090EXG combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals. It embeds FSMC for interfacing external memories (NOR and SRAM).

It supports USB2.0 standard at full speed (12 Mbps) with on-chip PHY.

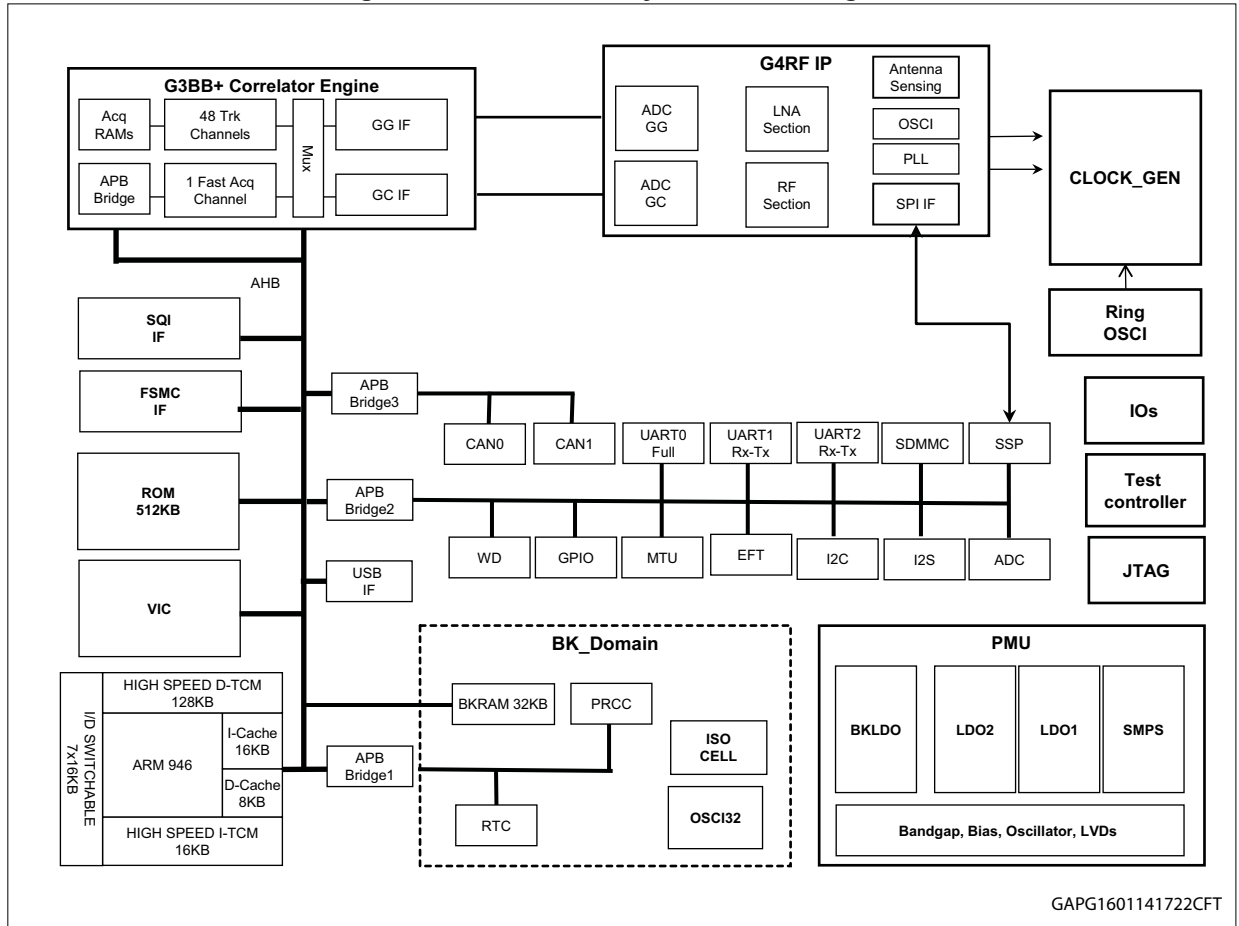
The chip embeds backup logic with real time clock.

The STA8090EXG, using STMicroelectronics CMOSRF Technology, is housed in a FBGA169 (9 x 9 x 1.2 mm) 0.65mm pitch package.

2 Pin description

2.1 Block diagram

Figure 1. STA8090EXG system block diagram





2.2 TFBG_A169 ball out

Table 1. TFBGA169 ball out with CAN (STA8090EXGBx)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|----------|------------|-------------|-------------|-------------|-------------|------------|------------|-----------|----------|-----------|-------------|-------------|------------|----------|
| A | VINM | VINM | FMSC_DATA8 | FMSC_DATA5 | FMSC_DATA3 | FMSC_DATA1 | UART0_DSR | UART0_CTS | VINL1 | VOL1 | GND | VINB | VOB | A |
| B | VLX | VLX | FMSC_DATA13 | FMSC_DATA11 | FMSC_DATA9 | FMSC_DATA0 | UART0_RX | UART0_RTS | SPI_DO | SPI_DI | SPI_CLK | SPI_CSN | GND | B |
| C | GND | GND | FMSC_DATA12 | FMSC_DATA4 | FMSC_DATA6 | UART0_DCD | UART0_TX | UART2_RX | ADC_IN5 | ADC_IN6 | ADC_IN2 | ADC_IN1 | ADC_IN4 | C |
| D | VOM | FMSC_DATA15 | FMSC_DATA2 | FMSC_DATA7 | GND | UART0_DTR | UART2_TX | GND | ADC_IN8 | VDD_ADC | ADC_IN3 | ADC_IN7 | Reserved | D |
| E | VDD_ANA | GND | FMSC_CS1 | FMSC_DATA10 | FMSC_DATA14 | VDDIO_R1 | VDDIO_FSMC | GPIO1 | GPIO0 | RTC_XTI | RTC_XTO | CAN0_RX | I2C_SD | E |
| F | GND | FMSC_BLN1 | FMSC_CS0 | FMSC_BLN0 | FMSC_WEN | GND | GND | VDDD | GND | WAKEUP1 | WAKEUP0 | CAN0_TX | I2C_CLK | F |
| G | FMSC_ADD16 | FMSC_ADV | FMSC_CLK | FMSC_CS2 | GND | GND | GND | VDDD | RSTn | VDD_SQI | SQI_SIO0/SI | SQI_SIO1/SO | SQI_SIO2 | G |
| H | FMSC_ADD13 | FMSC_OUTEN | FMSC_WTN | NC | TDO | VDDD | VDDD | VDDD | STDBYn | PMU_CFG | SQI_SIO3 | SQI_CLK | SQI_CEN | H |
| J | FMSC_ADD14 | FMSC_ADD10 | FMSC_ADD3 | FMSC_ADD15 | TDI | TCK | TRSTn | GPIO19 | GPIO11 | STDBY_OUT | GPIO3 | GPIO2 | VCC_PLL | J |
| K | FMSC_ADD11 | FMSC_ADD9 | FMSC_ADD5 | FMSC_ADD6 | FMSC_ADD12 | TMS | MMC_D1 | MMC_D3 | GPIO13 | GND | GND | XTAL_IN | XTAL_OUT | K |
| L | USB_DP | FMSC_ADD7 | FMSC_ADD21 | FMSC_ADD1 | FMSC_ADD8 | FMSC_ADD17 | MMC_CLK | GPIO12 | GPIO10 | GND | GND | ANT_SENSE2 | VCC_CHAIN | L |
| M | USB_DM | FMSC_ADD0 | FMSC_ADD2 | FMSC_ADD4 | FMSC_ADD20 | FMSC_ADD22 | MMC_D2 | TP_IF_P | GND_LNA | GND_LNA | GND_LNA | GND | ANT_SENSE1 | M |
| N | GND | VDDIO_R2 | FMSC_ADD19 | FMSC_ADD18 | FMSC_ADD23 | MMC_D0 | MMC_CMD | TP_IF_N | VCC_RF | LNA_IN | VOL2 | VINL2 | GND | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |



Table 2. TFBGA169 ball out no CAN

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|----------|------------|-------------|-------------|-------------|-------------|------------|------------|-----------|----------|-----------|-------------|-------------|------------|----------|
| A | VINM | VINM | FMSC_DATA8 | FMSC_DATA5 | FMSC_DATA3 | FMSC_DATA1 | UART0_DSR | UART0_CTS | VINL1 | VOL1 | GND | VINB | VOB | A |
| B | VLX | VLX | FMSC_DATA13 | FMSC_DATA11 | FMSC_DATA9 | FMSC_DATA0 | UART0_RX | UART0_RTS | SPI_DO | SPI_DI | SPI_CLK | SPI_CSN | GND | B |
| C | GND | GND | FMSC_DATA12 | FMSC_DATA4 | FMSC_DATA6 | UART0_DCD | UART0_TX | UART2_RX | ADC_IN5 | ADC_IN6 | ADC_IN2 | ADC_IN1 | ADC_IN4 | C |
| D | VOM | FMSC_DATA15 | FMSC_DATA2 | FMSC_DATA7 | GND | UART0_DTR | UART2_TX | GND | ADC_IN8 | VDD_ADC | ADC_IN3 | ADC_IN7 | Reserved | D |
| E | VDD_ANA | GND | FMSC_CS1 | FMSC_DATA10 | FMSC_DATA14 | VDDIO_R1 | VDDIO_FSMC | GPIO1 | GPIO0 | RTC_XT1 | RTC_XTO | UART0_RX | I2C_SD | E |
| F | GND | FMSC_BLN1 | FMSC_CS0 | FMSC_BLN0 | FMSC_WEN | GND | GND | VDDD | GND | WAKEUP1 | WAKEUP0 | UART0_TX | I2C_CLK | F |
| G | FMSC_ADD16 | FMSC_ADV | FMSC_CLK | FMSC_CS2 | GND | GND | GND | VDDD | RSTn | VDD_SQI | SQI_SIO0/SI | SQI_SIO1/SO | SQI_SIO2 | G |
| H | FMSC_ADD13 | FMSC_OUTEN | FMSC_WTN | NC | TDO | VDDD | VDDD | VDDD | STDBYn | PMU_CFG | SQI_SIO3 | SQI_CLK | SQI_CEN | H |
| J | FMSC_ADD14 | FMSC_ADD10 | FMSC_ADD3 | FMSC_ADD15 | TDI | TCK | TRSTn | GPIO19 | GPIO11 | STDBY_OUT | GPIO3 | GPIO2 | VCC_PLL | J |
| K | FMSC_ADD11 | FMSC_ADD9 | FMSC_ADD5 | FMSC_ADD6 | FMSC_ADD12 | TMS | MMC_D1 | MMC_D3 | GPIO13 | GND | GND | XTAL_IN | XTAL_OUT | K |
| L | USB_DP | FMSC_ADD7 | FMSC_ADD21 | FMSC_ADD1 | FMSC_ADD8 | FMSC_ADD17 | MMC_CLK | GPIO12 | GPIO10 | GND | GND | ANT_SENSE2 | VCC_CHAIN | L |
| M | USB_DM | FMSC_ADD0 | FMSC_ADD2 | FMSC_ADD4 | FMSC_ADD20 | FMSC_ADD22 | MMC_D2 | TP_IF_P | GND_LNA | GND_LNA | GND_LNA | GND | ANT_SENSE1 | M |
| N | GND | VDDIO_R2 | FMSC_ADD19 | FMSC_ADD18 | FMSC_ADD23 | MMC_D0 | MMC_CMD | TP_IF_N | VCC_RF | LNA_IN | VOL2 | VINL2 | GND | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

2.3 Power supply pins

Table 3. Power supply pins

| Symbol | I/O voltage | I/O | Description | STA8090EXG |
|------------|----------------|-----|--|--|
| VCC_CHAIN | 1.2 V | PWR | Analog supply voltage for RF chain (1.2 V) | L13 |
| VCC_PLL | 1.2 V | PWR | Analog supply voltage for PLL RF (1.2 V) | J13 |
| VCC_RF | 1.2 V | PWR | Analog supply voltage for RF (1.2 V) | N9 |
| VDD_ADC | 1.8 V | PWR | Digital supply voltage for ADC (1.8 V) | D10 |
| VDD_SQI | 1.8 V or 3.3 V | PWR | Digital supply voltage for SQI | G10 |
| VDDD | 1.1 V | PWR | Digital supply voltage | F8, G8, H6, H7, H8 |
| VDDIO_FSMC | 1.8 V or 3.3 V | PWR | Digital supply voltage for I/O ring FSMC (1.8 V or 3.3V) | E7 |
| VDDIO_R1 | 1.8 V or 3.3 V | PWR | Digital supply voltage for I/O ring 1 (1.8 V or 3.3V) | E6 |
| VDDIO_R2 | 3.3 V | PWR | Digital supply voltage for I/O ring 2 (3.3 V) | N2 |
| VINB | 1.6 V - 4.3 V | PWR | Backup LDO input supply voltage (1.6 V to 4.3 V) | A12 |
| VINL1 | 1.6 V - 4.3 V | PWR | LDO1 input supply voltage (1.6 V to 4.3 V) | A9 |
| VINL2 | 1.6 V - 4.3 V | PWR | LDO2 input supply voltage (1.6 V to 4.3 V) | N12 |
| VINM | 1.6 V - 4.3 V | PWR | SMPS coil input supply (1.6 V to 4.3 V) | A1, A2 |
| VDD_ANA | 1.6 V - 4.3 V | PWR | SMPS input supply (1.6 V to 4.3 V) | E1 |
| VLX | 0 V - 4.3 V | PWR | SMPS coil output | B1, B2 |
| VOB | 1.0 V | PWR | LDO backup output voltage (1.0 V) | A13 |
| VOL1 | 1.1 V or 1.8 V | PWR | LDO1 output voltage: PMU_CFG = high -> 1.1 V (it can be also configured to 1.2 V) PMU_CFG = low -> 1.8 V | A10 |
| VOL2 | 1.2 V | PWR | LDO2 output voltage (1.2 V) | N11 |
| VOM | 1.1 V or 1.8 V | PWR | SMPS output voltage PMU_CFG = high -> 1.8 V PMU_CFG = low -> 1.1 V (it can be also configured to 1.2 V) | D1 |
| GND | GND | GND | Ground | A11, B13, C1, C2, D5, D8, E2, F1, F6, F7, F9, G5, G6, G7, K10, K11, L10, L11, M12, N1, N13 |
| GND_LNA | GND | GND | Ground | M9, M10, M11 |

2.4 Main function pins

Table 4. Main function pins

| Symbol | I/O voltage | I/O | Description | STA8090EXG |
|-----------|-----------------------|-----|--|------------|
| ADC_IN1 | 1.4 V – 0 V typ range | I | ADC Analog input [1] | C12 |
| ADC_IN2 | 1.4 V – 0 V typ range | I | ADC Analog input [2] | C11 |
| ADC_IN3 | 1.4 V – 0 V typ range | I | ADC Analog input [3] | D11 |
| ADC_IN4 | 1.4 V – 0 V typ range | I | ADC Analog input [4] | C13 |
| ADC_IN5 | 1.4 V – 0 V typ range | I | ADC Analog input [5] | C9 |
| ADC_IN6 | 1.4 V – 0 V typ range | I | ADC Analog input [6] | C10 |
| ADC_IN7 | 1.4 V – 0 V typ range | I | ADC Analog input [7] | D12 |
| ADC_IN8 | 1.4 V – 0 V typ range | I | ADC Analog input [8] | D9 |
| PMU_CFG | 1.0 V | I | Power management unit config pin High -> VOL1 = 1.1 V, VOM = 1.8 V Low -> VOL1 = 1.8 V, VOM = 1.1 V | H10 |
| RSTn | 1.0 V | I | Reset Input with Schmitt-Trigger characteristics and noise filter. | G9 |
| RTC_XTI | 1.0 V (max) | I | Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit. | E10 |
| RTC_XTO | 1.0 V (max) | O | Output of the oscillator amplifier circuit. | E11 |
| STDBY_OUT | 1.0 V | O | When low, indicates the chip is in Standby mode | J10 |
| STDBYn | 1.0 V | I | When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply | H9 |
| WAKEUP0 | 1.0 V | I | WAKEUP from STANDBY mode | F11 |
| WAKEUP1 | 1.0 V | I | WAKEUP from STANDBY mode | F10 |

2.5 Test / emulated dedicated pins

Table 5. Test/emulated dedicated pins

| Symbol | I/O voltage | I/O | Description | STA8090EXG |
|---------|-------------|-----|-------------------------------|------------|
| TCK | VDDIO_R2 | I | JTAG Test Clock | J6 |
| TDI | VDDIO_R2 | I | JTAG Test Data In | J5 |
| TDO | VDDIO_R2 | O | JTAG Test Data Out | H5 |
| TMS | VDDIO_R2 | I | JTAG Test Mode Select | K6 |
| TRSTn | VDDIO_R2 | I | JTAG Test Circuit Reset | J7 |
| TP_IF_N | 1.2 V | O | Diff.Test Point for IF — Neg. | N8 |
| TP_IF_P | 1.2 V | O | Diff.Test Point for IF — Pos. | M8 |

2.6 FSMC external memory interface pins

Table 6. FSMC external memory interface pins

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|------------|-------------|-----|----------------------|------------|-------------------------|------------|
| FSMC_ADD0 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD0 | FSMC EMI address bus | M2 |
| | | I/O | AF1, AF2, AF3 | GPIO32 | General purpose I/O #32 | |
| FSMC_ADD1 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD1 | FSMC EMI address bus | L4 |
| | | I/O | AF1, AF2, AF3 | GPIO33 | General purpose I/O #33 | |
| FSMC_ADD2 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD2 | FSMC EMI address bus | M3 |
| | | I/O | AF1, AF2, AF3 | GPIO34 | General purpose I/O #34 | |
| FSMC_ADD3 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD3 | FSMC EMI address bus | J3 |
| | | I/O | AF1, AF2, AF3 | GPIO35 | General purpose I/O #35 | |
| FSMC_ADD4 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD4 | FSMC EMI address bus | M4 |
| | | I/O | AF1, AF2, AF3 | GPIO36 | General purpose I/O #36 | |
| FSMC_ADD5 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD5 | FSMC EMI address bus | K3 |
| | | I/O | AF1, AF2, AF3 | GPIO37 | General purpose I/O #37 | |
| FSMC_ADD6 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD6 | FSMC EMI address bus | K4 |
| | | I/O | AF1, AF2, AF3 | GPIO38 | General purpose I/O #38 | |
| FSMC_ADD7 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD7 | FSMC EMI address bus | L2 |
| | | I/O | AF1, AF2, AF3 | GPIO39 | General purpose I/O #39 | |
| FSMC_ADD8 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD8 | FSMC EMI address bus | L5 |
| | | I/O | AF1, AF2, AF3 | GPIO40 | General purpose I/O #40 | |
| FSMC_ADD9 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD9 | FSMC EMI address bus | K2 |
| | | I/O | AF1, AF2, AF3 | GPIO41 | General purpose I/O #41 | |
| FSMC_ADD10 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD10 | FSMC EMI address bus | J2 |
| | | I/O | AF1, AF2, AF3 | GPIO42 | General purpose I/O #42 | |

Table 6. FSMC external memory interface pins (continued)

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|------------|-------------|-----|----------------------|------------|--|------------|
| FSMC_ADD11 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD11 | FSMC EMI address bus | K1 |
| | | I/O | AF1, AF2, AF3 | GPIO43 | General purpose I/O #43 | |
| FSMC_ADD12 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD12 | FSMC EMI address bus | K5 |
| | | I/O | AF1, AF2, AF3 | GPIO44 | General purpose I/O #44 | |
| FSMC_ADD13 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD13 | FSMC EMI address bus. | H1 |
| | | I/O | AF1, AF2, AF3 | GPIO45 | General purpose I/O #45 | |
| FSMC_ADD14 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD14 | FSMC EMI address bus | J1 |
| | | I/O | AF1, AF2, AF3 | GPIO46 | General purpose I/O #46 | |
| FSMC_ADD15 | VDDIO_FSMC | O | AF0 (default) | FSMC_ADD15 | FSMC EMI address bus | J4 |
| | | I/O | AF1, AF2, AF3 | GPIO47 | General purpose I/O #47 | |
| FSMC_ADD16 | VDDIO_FSMC | O | — | FSMC_ADD16 | FSMC EMI address bus | G1 |
| FSMC_ADD17 | VDDIO_FSMC | O | — | FSMC_ADD17 | FSMC EMI address bus | L6 |
| FSMC_ADD18 | VDDIO_FSMC | O | — | FSMC_ADD18 | FSMC EMI address bus | N4 |
| FSMC_ADD19 | VDDIO_FSMC | O | — | FSMC_ADD19 | FSMC EMI address bus | N3 |
| FSMC_ADD20 | VDDIO_FSMC | O | — | FSMC_ADD20 | FSMC EMI address bus | M5 |
| FSMC_ADD21 | VDDIO_FSMC | O | — | FSMC_ADD21 | FSMC EMI address bus | L3 |
| FSMC_ADD22 | VDDIO_FSMC | O | — | FSMC_ADD22 | FSMC EMI address bus | M6 |
| FSMC_ADD23 | VDDIO_FSMC | O | — | FSMC_ADD23 | FSMC EMI address bus | N5 |
| FSMC_ADV | VDDIO_FSMC | O | — | FSMC_ADV | FSMC EMI Address Valid | G2 |
| FSMC_BLN0 | VDDIO_FSMC | O | — | FSMC_BLN0 | FSMC EMI Byte Lane | F4 |
| FSMC_BLN1 | VDDIO_FSMC | O | — | FSMC_BLN1 | FSMC EMI Byte Lane | F2 |
| FSMC_CLK | VDDIO_FSMC | O | — | FSMC_CLK | FSMC EMI Clk | G3 |
| FSMC_CS0 | VDDIO_FSMC | O | — | FSMC_CS0 | FSMC EMI Chip Select for External Memory Bank 0 | F3 |
| FSMC_CS1 | VDDIO_FSMC | O | — | FSMC_CS1 | FSMC EMI Chip Select for External Memory Bank 1 | E3 |
| FSMC_CS2 | VDDIO_FSMC | O | — | FSMC_CS2 | FSMC EMI Chip Select for External Memory Bank 2 / IO_Power Sel Ring FSMC | G4 |
| FSMC_DATA0 | VDDIO_FSMC | I/O | — | FSMC_DATA0 | FSMC EMI data bus | B6 |

Table 6. FSMC external memory interface pins (continued)

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|-------------|-------------|-----|----------------------|-------------|----------------------------|------------|
| FSMC_DATA1 | VDDIO_FSMC | I/O | — | FSMC_DATA1 | FSMC EMI data bus | A6 |
| FSMC_DATA2 | VDDIO_FSMC | I/O | — | FSMC_DATA2 | FSMC EMI data bus | D3 |
| FSMC_DATA3 | VDDIO_FSMC | I/O | — | FSMC_DATA3 | FSMC EMI data bus | A5 |
| FSMC_DATA4 | VDDIO_FSMC | I/O | — | FSMC_DATA4 | FSMC EMI data bus | C4 |
| FSMC_DATA5 | VDDIO_FSMC | I/O | — | FSMC_DATA5 | FSMC EMI data bus | A4 |
| FSMC_DATA6 | VDDIO_FSMC | I/O | — | FSMC_DATA6 | FSMC EMI data bus | C5 |
| FSMC_DATA7 | VDDIO_FSMC | I/O | — | FSMC_DATA7 | FSMC EMI data bus | D4 |
| FSMC_DATA8 | VDDIO_FSMC | I/O | — | FSMC_DATA8 | FSMC EMI data bus | A3 |
| FSMC_DATA9 | VDDIO_FSMC | I/O | — | FSMC_DATA9 | FSMC EMI data bus | B5 |
| FSMC_DATA10 | VDDIO_FSMC | I/O | — | FSMC_DATA10 | FSMC EMI data bus | E4 |
| FSMC_DATA11 | VDDIO_FSMC | I/O | — | FSMC_DATA11 | FSMC EMI data bus | B4 |
| FSMC_DATA12 | VDDIO_FSMC | I/O | — | FSMC_DATA12 | FSMC EMI data bus | C3 |
| FSMC_DATA13 | VDDIO_FSMC | I/O | — | FSMC_DATA13 | FSMC EMI data bus | B3 |
| FSMC_DATA14 | VDDIO_FSMC | I/O | — | FSMC_DATA14 | FSMC EMI data bus | E5 |
| FSMC_DATA15 | VDDIO_FSMC | I/O | — | FSMC_DATA15 | FSMC EMI data bus | D2 |
| FSMC_OUTEN | VDDIO_FSMC | O | — | FSMC_OUTEN | FSMC EMI Output Enable | H2 |
| FSMC_WEN | VDDIO_FSMC | O | — | FSMC_WEN | FSMC EMI Write Enable | F5 |
| FSMC_WTN | VDDIO_FSMC | I | — | FSMC_WTN | FSMC EMI Wait (SNOR, CRAM) | H3 |

2.7 SQI pins

Table 7. SQI pins

| Symbol | I/O voltage | I/O | Description | STA8090EXG |
|-------------|-------------|-----|---|------------|
| SQI_CEN | VDD_SQI | O | SQI Flash chip enable / IO_Power Sel Ring SQI | H13 |
| SQI_CLK | VDD_SQI | O | SQI Flash clock | H12 |
| SQI_SIO0/SI | VDD_SQI | I/O | SQI Flash data IO 0 / ser. I | G11 |
| SQI_SIO1/SO | VDD_SQI | I/O | SQI Flash data IO 1 / ser. O | G12 |
| SQI_SIO2 | VDD_SQI | I/O | SQI Flash data IO 2 | G13 |
| SQI_SIO3 | VDD_SQI | I/O | SQI Flash data IO 3 | H11 |

2.8 Communication interface pins

Table 8. Communication interface pins

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|------------------------|-------------|-----|----------------------|------------------------|--|------------|
| CAN0_RX ⁽¹⁾ | VDDIO_R2 | I | AF0 (default) | CAN0_RX ⁽¹⁾ | CAN0 receive data input | E12 |
| | | I | AF1 | UART0_RX | UART0_Rx data | |
| | | I/O | AF2 | Tsense | External temperature capture port | |
| | | I/O | AF3 | I2C_SD | I2C serial data | |
| CAN0_TX ⁽¹⁾ | VDDIO_R2 | O | AF0 (default) | CAN0_TX ⁽¹⁾ | CAN0 transmit data output | F12 |
| | | O | AF1 | UART0_TX | UART0 Tx data | |
| | | I/O | AF2 | GPIO7 | General purpose I/O #7 | |
| | | O | AF3 | I2C_CLK | I2C clock | |
| I2C_CLK | VDDIO_R2 | O | AF0 (default) | I2C_CLK | I2C clock | F13 |
| | | I/O | AF1 | GPIO8 | General purpose I/O #8 | |
| | | O | AF2 | CAN1_TX ⁽¹⁾ | CAN1 transmit data output | |
| | | O | AF3 | SPI_CLK | SPI clock | |
| I2C_SD | VDDIO_R2 | I/O | AF0 (default) | I2C_SD | I2C serial data | E13 |
| | | I/O | AF1 | GPIO9 | General purpose I/O #9 | |
| | | I | AF2 | CAN1_RX ⁽¹⁾ | CAN1 receive data input | |
| | | I/O | AF3 | SPI_CSN | SPI chip select active low | |
| SPI_CLK | VDDIO_R1 | O | AF0 (default) | SPI_CLK | SPI clock | B11 |
| | | I/O | AF1 | GPIO25 | General purpose I/O #25 | |
| | | O | AF2 | SQI_CLK | SQI Flash clock | |
| | | O | AF3 | MMC_CLK | Multimedia Clock line | |
| SPI_CSN | VDDIO_R1 | O | AF0 (default) | SPI_CSN | SPI chip select active low / IO_Power Sel Ring 1 | B12 |
| | | I/O | AF1 | GPIO24 | General purpose I/O #24 | |
| | | I/O | AF2 | SQI_CEN | SQI Flash chip enable | |
| | | I/O | AF3 | MMC_CMD | Multimedia card command line | |
| SPI_DI | VDDIO_R1 | I | AF0 (default) | SPI_DI | SPI serial data input / BOOT2 | B10 |
| | | I/O | AF1 | Tsense | External temperature capture port | |
| | | I/O | AF2 | SQI_SIO1/SO | SQI Flash data IO 1 / ser. 0 | |
| | | I/O | AF3 | MMC_D0 | Multimedia card data 0 | |

Table 8. Communication interface pins (continued)

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|-----------|-------------|-----|----------------------|---------------|---|------------|
| SPI_DO | VDDIO_R1 | O | AF0 (default) | SPI_DO | SPI serial data output | B9 |
| | | I/O | AF1 | GPIO27 | General purpose I/O #27 | |
| | | I/O | AF2 | SQI_SIO0/SI | SQI Flash data IO 0 / ser. 1 | |
| | | I/O | AF3 | MMC_D1 | Multimedia card data 1 | |
| UART0_CTS | VDDIO_R1 | I | AF0 (default) | UART0_CTS | UART0 clear to send | A8 |
| | | I/O | AF1 | GPIO15 | General purpose I/O #15 | |
| | | O | AF2 | i2s_out_sclk | MSP serial clock output | |
| | | O | AF3 | Clock GNSS | GNSS clock out | |
| UART0_DCD | VDDIO_R1 | I | AF0 (default) | UART0_DCD | UART0 data carrier detect | C6 |
| | | I/O | AF1 | GPIO17 | General purpose I/O #17 | |
| | | O | AF2 | i2s_out_sdata | MSP serial data output | |
| | | O | AF3 | Clock GNSS | GNSS clock out | |
| UART0_DSR | VDDIO_R1 | I | AF0 (default) | UART0_DSR | UART0 data set ready | A7 |
| | | I/O | AF1 | GPIO16 | General purpose I/O #16 | |
| | | O | AF2 | i2s_out_lrclk | MSP left/right clock output | |
| | | O | AF3 | Sign GC | GLONASS and BeiDou 3-bit coding output (Sign) | |
| UART0_DTR | VDDIO_R1 | O | AF0 (default) | UART0_DTR | UART0 data terminal read | D6 |
| | | I/O | AF1 | GPIO18 | General purpose I/O #18 | |
| | | I | AF2 | Timer_ICAPA | Extended Function Timer - Input Capture A | |
| | | O | AF3 | Mag_1 GG | GPS and Galileo 3-bit coding Output (MAG1) | |
| UART0_RTS | VDDIO_R1 | O | AF0 (default) | UART0_RTS | UART0 request to send | B8 |
| | | I/O | AF1 | GPIO14 | General purpose I/O #14 | |
| | | O | AF2 | TCXO_OUT | TCXO out clock | |
| | | O | AF3 | Sign GG | GPS and Galileo 3-bit coding output (Sign) | |
| UART0_RX | VDDIO_R1 | I | AF0 (default) | UART0_RX | UART0 Rx data | B7 |
| | | O | AF1 | SPI_DO | SPI serial data output | |
| | | I/O | AF2 | SQI_SIO2 | SQI Flash data IO 2 | |
| | | I | AF3 | Timer_ICAPA | Extended Function Timer - Input Capture A | |

Table 8. Communication interface pins (continued)

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|----------|-------------|-----|----------------------|------------------------|--|------------|
| UART0_TX | VDDIO_R1 | O | AF0 (default) | UART0_TX | UART0 Tx data / BOOT1 | C7 |
| | | I | AF1 | SPI_DI | SPI serial data input | |
| | | I/O | AF2 | SQI_SIO3 | SQI Flash data IO 3 | |
| | | O | AF3 | Timer_OCMPA | Extended Function Timer – Output Compare A | |
| UART2_RX | VDDIO_R1 | I | AF0 (default) | UART2_RX | UART2 Rx data | C8 |
| | | I/O | AF1 | GPIO28 | General purpose I/O #28 | |
| | | I/O | AF2 | I2C_SD | I2C serial data | |
| | | I/O | AF3 | MMC_D2 | Multimedia card data 2 | |
| UART2_TX | VDDIO_R1 | O | AF0 (default) | UART2_TX | UART2 Tx data / BOOT0 | D7 |
| | | I/O | AF1 | GPIO29 | General purpose I/O #29 | |
| | | O | AF2 | I2C_CLK | I2C clock | |
| | | I/O | AF3 | MMC_D3 | Multimedia card data 2 | |
| USB_DM | VDDIO_R2 | USB | AF0 | USB_DM | USB D- signal | M1 |
| | | I | AF1 (default) | UART1_RX | UART1 Rx data | |
| | | I | AF2 | CAN1_RX ⁽¹⁾ | CAN1 receive data input | |
| | | I/O | AF3 | I2C_SD | I2C serial data | |
| USB_DP | VDDIO_R2 | USB | AF0 | USB_DP | USB D+ signal | L1 |
| | | O | AF1 (default) | UART1_TX | UART1 Tx data | |
| | | O | AF2 | CAN1_TX ⁽¹⁾ | CAN1 transmit data output | |
| | | O | AF3 | I2C_CLK | I2C clock | |

1. Only for STA8090EXGBD and STA8090EXGB.

2.9 Multimedia card pins

Table 9. Multimedia card pins

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|---------|-------------|-----|----------------------|------------------------|---|------------|
| MMC_CLK | VDDIO_R2 | O | AF0 (default) | MMC_CLK | Multimedia Clock line | L7 |
| | | O | AF1 | i2s_out_lrclk | MSP left/right clock output | |
| | | I | AF2 | Timer_ICAPA | Extended Function Timer - Input Capture A | |
| | | I/O | AF3 | GPIO4 | General purpose I/O #4 | |
| MMC_CMD | VDDIO_R2 | I/O | AF0 (default) | MMC_CMD | Multimedia card command line | N7 |
| | | O | AF1 | i2s_out_sdata | MSP serial data output | |
| | | O | AF2 | CAN0_TX ⁽¹⁾ | CAN0 transmit data output | |
| | | I/O | AF3 | GPIO5 | General purpose I/O #5 | |
| MMC_D0 | VDDIO_R2 | I/O | AF0 (default) | MMC_D0 | Multimedia card data 0 | N6 |
| | | O | AF1 | i2s_out_sclk | MSP serial clock output | |
| | | I/O | AF2 | I2C_SD | I2C serial data | |
| | | I/O | AF3 | GPIO20 | General purpose I/O #20 | |
| MMC_D1 | VDDIO_R2 | I/O | AF0 (default) | MMC_D1 | Multimedia card data 1 | K7 |
| | | I | AF1 | i2s_in_sdata | MSP serial data input | |
| | | O | AF2 | Sign GC | GLONASS and BeiDou 3-bit coding output (Sign) | |
| | | I/O | AF3 | GPIO21 | General purpose I/O #21 | |
| MMC_D2 | VDDIO_R2 | I/O | AF0 (default) | MMC_D2 | Multimedia card data 2 | M7 |
| | | I/O | AF1 | Reserved | Reserved | |
| | | I | AF2 | CAN0_RX ⁽¹⁾ | CAN0 receive data input | |
| | | I/O | AF3 | Tsense | External temperature capture port | |
| MMC_D3 | VDDIO_R2 | I/O | AF0 (default) | MMC_D3 | Multimedia card data 3 | K8 |
| | | I/O | AF1 | Reserved | Reserved | |
| | | O | AF2 | Sign GG | GPS 3-bit coding output (Sign) | |
| | | I/O | AF3 | GPIO23 | General purpose I/O #23 | |

1. Only for STA8090EXGBD and STA8090EXGB.

2.10 General purpose pins

Table 10. General purpose pins

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|--------|-------------|-----|----------------------|--------------|---|------------|
| GPIO0 | VDDIO_R1 | I/O | AF0 (default) | GPIO0 | General purpose I/O #0 | E9 |
| | | I | AF1 | PPS_IN | Pulse per second input | |
| | | O | AF2 | Timer_OCMPB | Extended Function Timer – Output Compare B | |
| | | O | AF3 | Mag_0 GC | GLONASS and BeiDou 3-bit coding Output (MAG0) | |
| GPIO1 | VDDIO_R1 | I/O | AF0 (default) | GPIO1 | General purpose I/O #1 / BOOT3 | E8 |
| | | I | AF1 | i2s_in_sdata | MSP serial data input | |
| | | O | AF2 | PPS_OUT | Pulse per second output | |
| | | I/O | AF3 | Tsense | External temperature capture port | |
| GPIO2 | VDDIO_R2 | I/O | AF0 (default) | GPIO2 | General purpose I/O #2 | J12 |
| | | I | AF1 | Reserved | Reserved | |
| | | I | AF2 | Timer_ICAPB | Extended Function Timer - Input Capture B | |
| | | O | AF3 | Mag_1 GC | GLONASS and BeiDou 3-bit coding Output (MAG1) | |
| GPIO3 | VDDIO_R2 | I/O | AF0 (default) | GPIO3 | General purpose I/O #3 | J11 |
| | | I | AF1 | Reserved | Reserved | |
| | | O | AF2 | Timer_OCMPA | Extended Function Timer – Output Compare A | |
| | | O | AF3 | Mag_0 GG | GPS and Galileo 3-bit coding Output (MAG0) | |
| GPIO10 | VDDIO_R2 | I/O | AF0 (default), AF1 | GPIO10 | General purpose I/O #10 | L9 |
| | | I | AF2 | Timer_ICAPA | Extended Function Timer - Input Capture A | |
| | | O | AF3 | Timer_OCMPB | Extended Function Timer – Output Compare B | |
| GPIO11 | VDDIO_R2 | I/O | AF0 (default), AF1 | GPIO11 | General purpose I/O #11 | J9 |
| | | O | AF2 | Timer_OCMPA | Extended Function Timer – Output Compare A | |
| | | I | AF3 | Timer_ICAPB | Extended Function Timer - Input Capture B | |

Table 10. General purpose pins (continued)

| Symbol | I/O voltage | I/O | Alternative function | Function | Description | STA8090EXG |
|--------|-------------|-----|------------------------------|----------|-------------------------|------------|
| GPIO12 | VDDIO_R2 | I/O | AF0 (default), AF1, AF2, AF3 | GPIO12 | General purpose I/O #12 | L8 |
| GPIO13 | VDDIO_R2 | I/O | AF0 (default), AF1, AF2, AF3 | GPIO13 | General purpose I/O #13 | K9 |
| GPIO19 | VDDIO_R2 | I/O | AF0 (default), AF1, AF2, AF3 | GPIO19 | General purpose I/O #19 | J8 |

2.11 RF front-end pins

Table 11. RF front-end pins

| Symbol | I/O voltage | I/O | Description | STA8090EXG |
|------------|-------------|-----|--|------------|
| ANT_SENSE1 | 3.3 V | I | Antenna sensing input 1 | M13 |
| ANT_SENSE2 | 3.3 V | I | Antenna sensing input 2 | L12 |
| LNA_IN | 1.2 V | I | Low Noise Amplifier Input | N10 |
| XTAL_IN | 1.2 V | I | Input Side of Crystal Oscillator or TCXO Input | K12 |
| XTAL_OUT | 1.2 V | O | Output Side of Crystal Oscillator | K13 |

3 General description

3.1 RF front end

The RF front-end is able to down-convert both the GPS-Galileo signal from 1575.42 MHz to 4.092 MHz (4 Fo, being F0 = 1.023 MHz), the GLONASS signal from 1601.718 MHz to 8.57 MHz and the BeiDou signal from 1561.098 MHz to 10.23 MHz.

It embeds high performance LNA minimizing external component count and a LDO to supply the internal core facilitating requirements for external power supply. A three bits ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 64 Fo sampling clock for the baseband and 192 Fo clock for MCU subsystem.

3.2 GPS/Galileo/GLONASS/BeiDou Base Band (G3BB+) processor

STA8090EXG integrates G3BB+ proprietary IP, which is the ST last generation high-sensitivity Baseband processor fully compliant with GPS, Galileo, GLONASS and BeiDou systems.

The baseband receives, from the embedded RF Front-End, two separate IF signals coded in sign-magnitude digital format on 3 bits and the related clocks. The Galileo/GPS (GALGPS) and GLONASS/BeiDou (GNSCOM) signals at the base band inputs are centered on 4.092 MHz, 8.57 MHz and 10.23 MHz.

The baseband processes the two IF signals performing data codification, sample rate conversion and final frequency conversion to zero IF before acquisition and tracking correlations.

The baseband processor has the capability of acquiring and tracking the Galileo, GPS, GLONASS and BeiDou signals in a simultaneous or single way, or a combination of three, being GLONASS and BeiDou mutually exclusive. The number of tracking channels to be used is programmable; the not used tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format or in a ST binary format. The library includes support of ST self-trained assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with autonomous and server-based ephemeris prediction and extension.

3.3 MCU Subsystem

The implemented sub-system includes an AHB Lite bus matrix.

An ARM946 core is embedded in the sub-system and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be

configured by the ARM946 (see [Table 12: TCM Configuration](#)). ITCM can be configured as $N_i \times 16$ KB; DTCM can be configured as $128 + N_d \times 16$ KB, where $N_i + N_d = 8$, $N_i \geq 1$.

Table 12. TCM Configuration

| TCMcfg [2] | TCMcfg [1] | TCMcfg [0] | ITCM | DTCM |
|------------|------------|------------|--------|--------|
| 0 | 0 | 0 | 16 KB | 240 KB |
| 0 | 0 | 1 | 32 KB | 224 KB |
| 0 | 1 | 0 | 48 KB | 208 KB |
| 0 | 1 | 1 | 64 KB | 192 KB |
| 1 | 0 | 0 | 80 KB | 176 KB |
| 1 | 0 | 1 | 96 KB | 160 KB |
| 1 | 1 | 0 | 112 KB | 144 KB |
| 1 | 1 | 1 | 128 KB | 128 KB |

3.3.1 AHB slaves

- G3 APB port that allows to interface with the G3BB acquisition memory and control registers.
- 512 Kbytes ROM
- Vectored Interrupt Controller (VIC).
- FSMC external memory interface
- SQI flash memory controller
- 3 x ARM946 APB peripheral bus (APB1, APB2, APB3).

Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 64 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ.

The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

FS USB device controller

Full speed USB device with transceiver. It is an AHB slave. When active requires a 48 MHz clock XTAL_IN.

FSMC external memory interface

16-bit non-muxed memory interface for burst NOR Flash, SRAM and NAND.

SQI Flash interface

STA8090EXG includes a high-performance interface to Serial Quad Interface (SQI) NOR Flash chips, to support a low-cost simple implementation.

3.4 APB peripherals

3.4.1 CAN

The 2 CAN^(a) cores perform communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

CAN consists of the CAN core, message RAM, message handler, control registers and module. For communication on a CAN network, individual message objects are configured. The message objects and identifier masks for acceptance filtering of received messages are stored in the message RAM. All functions concerning the handling of messages are implemented in the message handler. These functions include acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN can be accessed directly by the CPU through the module interface. These registers are used to control/configure the CAN core and the message handler and to access the message RAM.

CAN features

- Supports CAN protocol version 2.0 part A and B
- 32 messages objects
- Each message object has its own identifier mask
- Maskable interrupt
- Disabled automatic re-transmission mode for time triggered CAN applications
- Programmable loop-back mode for self-test operation
- Two 16-bit module interfaces to the AMBA APB bus from ARM

3.4.2 EFT

The Extended Function Timer (EFT) consists of a 16-bit counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (input capture), generation of up to two output waveforms (output compare) and one PWM generation. Pulse lengths and waveform periods can be modulated from a very wide range using the timer prescaler.

a. Only for STA8090EXGBD and STA8090EXGB (see [Figure 5: Ordering information scheme](#)).

EFT features

- Programmable prescaler: f_{APB} divided from 1 to 256, prescaler register (0 to 255) value +1.
- Overflow status flag and maskable interrupts.
- Output compare functions with:
 - 2 dedicated 16-bit registers
 - 2 dedicated programmable signals
 - 2 dedicated status flags
 - 2 dedicated interrupt flags
- Input capture functions with:
 - 2 dedicated 16-bit registers
 - 2 dedicated active edge selection signals
 - 2 dedicated status flags
 - 2 dedicated interrupt flags
- Pulse Width Modulation mode (PWM).
- One Pulse Mode (OPM).
- PWM input mode.
- Timer global interrupt (5 internally ORed)
 - ICIA: timer input capture A interrupt
 - ICIB: timer input capture B interrupt
 - OCIA: timer output compare A interrupt
 - OCIB: timer output compare B interrupt
 - TOI: timer overflow interrupt

3.4.3 SSP

The SSP is a master interface for synchronous serial communication with peripheral devices that have Motorola SPI.

The SSP performs serial-to-parallel conversion on data received from a peripheral device on SPI_DI pin, and parallel-to-serial conversion on data written by CPU for transmission on SPI_DO pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 32 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO.

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SSPCLK from the on-chip clock. One combined interrupt is delivered, which is asserted from several internal maskable events.

SSP features

The SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode

3.4.4 UART

The UARTx (x = 0|1|2) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

UART features

The UARTx (x = 0|1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to $UARTCLK / 16$ (1.5 Mbps with $UARTCLK$ at 24 MHz), or up to $UARTCLK / 8$ (3.0 Mbps with $UARTCLK$ at 24 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8 bits of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Support of the modem control functions CTS, RTS, DCD, DSR, RTS, DTS and RI (UART0 only)
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

3.4.5 I2C

STA8090EXG includes an I2C interface configurable as master or slave.

3.4.6 SDMMC

STA8090EXG features an SD/MMC host.

3.4.7 MTU

The 2 Multi Timer Units provide access to eight interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in each MTU, allowing eight counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

3.4.8 WDT

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserved for the entire programmed period. You can enable or disable the watchdog unit as required.

Note: Watchdog is stalled when the ARM processor is in Debug mode.

3.4.9 GPIO

The GPIO block provides thirty-seven (37) programmable inputs or outputs. Each input or output can be controlled in two modes:

- software mode through an APB bus interface
- alternate mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

3.4.10 ADC

10 bit SAR ADC operating at 1.8 V analog supply. It can convert up to 8 single ended channels with analog input multiplexer at 500KSPS

3.4.11 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 32 Kbyte SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer+fractional part) to the 47-bit counter. Once set by the MCU this bit is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.4.12 MSP

The STA8090EXG provides one MSP transmitter block.

- Element (data) size from 8 to 32 bits, LSB or MSB first
- Programmable frequency shift clock for data transfer
- Direct interface to:
 - industry-standard codecs and serially connected A/D and D/A devices
 - IIS compliant devices
 - SPI compliant devices
- Transmit first-in, first-out memory buffers (FIFOs), 32 bit wide, 8 locations deep

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25^\circ\text{C}$.

4.3 Typical values

Unless otherwise specified, typical data are based on $T_A = 25^\circ\text{C}$, $V_{\text{ddio}} = 1.8\text{ V}$, $V_{\text{dd}} = 1.20\text{ V}$. They are given only as design guidelines and are not tested.

4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 13 lists the absolute maximum rating for STA8090EXG.

Table 13. Voltage characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------------|---|------|------|------|
| $V_{\text{CC_CHAIN}}$ | Analog supply voltage for RF chain (1.2 V) | -0.3 | 1.32 | V |
| $V_{\text{CC_PLL}}$ | Analog supply voltage for PLL RF (1.2 V) | -0.3 | 1.32 | V |
| $V_{\text{CC_RF}}$ | Analog supply voltage for RF (1.2 V) | -0.3 | 1.32 | V |
| $V_{\text{DD_ADC}}$ | Digital supply voltage for ADC (1.8 V) | -0.3 | 1.98 | V |
| $V_{\text{DD_SQI}}$ | Digital supply voltage for SQI | -0.3 | 3.63 | V |
| V_{DDD} | Power supply pins for the core logic. | -0.3 | 1.32 | V |
| $V_{\text{DDIO_FSMC}}$ | Digital supply voltage for FSMC I/O ring (1.8 V or 3.3 V) | -0.3 | 3.63 | V |
| $V_{\text{DDIO_R1}}$ | Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V) | -0.3 | 3.63 | V |
| $V_{\text{DDIO_R2}}$ | Digital supply voltage for I/O ring 2 (3.3 V) | -0.3 | 3.63 | V |
| V_{INB} | Backup LDO input supply voltage (1.6 V to 4.3 V) | -0.3 | 4.8 | V |

Table 13. Voltage characteristics (continued)

| Symbol | Parameter | Min. | Max. | Unit |
|----------------------|---|------|------|------|
| V _{INL1} | LDO1 input supply voltage (1.6 V to 4.3 V) | -0.3 | 4.8 | V |
| V _{INL2} | LDO2 input supply voltage (1.6 V to 4.3 V) | -0.3 | 4.8 | V |
| V _{INM} | SMPS coil input supply (1.6 V to 4.3 V) | -0.3 | 4.8 | V |
| V _{DD_ANA} | SMPS input supply (1.6 V to 4.3 V) | -0.3 | 4.8 | V |
| V _{ESD-HBM} | Electrostatic discharge, human body model ⁽¹⁾ | -2 | 2 | kV |
| V _{ESD-CDM} | Electrostatic discharge, charge device model ⁽²⁾ | -250 | 250 | V |

1. Balls sustaining only ±500 V are: A1, A2, A9, A10, A11, A12, A13, B1, B2, B13, C1, C2, D1, E1, E2, E10, E11, F1, N11, N12, N13.
2. Ball N10 (LNA_IN) sustains only ±100 V.

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 14. Thermal characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|--------------------|---|------|------|------|
| T _{oper} | Operative ambient temperature | -40 | 85 | °C |
| T _j | Operative junction temperature | -40 | 125 | °C |
| T _{st} | Storage temperature | -55 | 150 | °C |
| R _{j-amb} | Thermal resistance junction to ambient ⁽¹⁾ | | 41 | °C/W |

1. According to JEDEC specification on a 2 layers board.

Table 15. Frequency limits

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|------------------|------------------------------|--|------|------|------|------|
| F _{CLK} | Operating ARM9 CPU frequency | V _{DDD} = 1.2 V; T _C = 85 °C ⁽¹⁾ | — | — | 196 | MHz |
| F _{AHB} | AHB frequency | | — | — | 49 | MHz |

1. Not tested in production.

Table 16. Power consumption

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|----------------------------------|--|--|------|------|------|------|
| P _{RF} | RFIP power (total V _{INL2}) | G2 = GPS/Galileo; T _{amb} = 25 °C; V _{INL2} = 1.8 V | — | 25 | — | mW |
| | | G2 + GLONASS; T _{amb} = 25 °C; V _{INL2} = 1.8 V | — | 35 | — | mW |
| | | G2 + BeiDou; T _{amb} = 25 °C; V _{INL2} = 1.8 V | — | 35 | — | mW |
| P _{MVR} ⁽¹⁾ | Switchable area power; (total V _{INL1}) | f _{ARM} = 196 MHz; f _{AHB} = 49 MHz; T _{amb} = 25 °C; V _{INL1} = 1.8 V; UART active; other peripherals inactive | — | 90 | — | mW |
| P _{LPVR} ⁽¹⁾ | Always ON area power (total V _{INB}) | f _{ARM} = 196 MHz; f _{AHB} = 49 MHz; T _{amb} = 25 °C; V _{INB} = 3.3 V | — | 1 | — | mW |
| P _{IO} ⁽¹⁾ | IO rings power (total V _{DDIO_R1} + V _{DDIO_R2}) | f _{ARM} = 196 MHz; f _{AHB} = 49 MHz; T _{amb} = 25 °C; V _{INL1} = 1.8 V; UART active; other peripherals inactive | — | 4 | — | mW |
| I _{DStandby} | Standby mode supply current | RTC running = 32.768 KHz; | — | 29 | — | µA |
| I _{DDeepStandby} | Deep standby mode supply current ⁽²⁾ | T _{amb} = 25 °C; V _{INB} = 1.8 V | — | 7 | — | µA |

1. Not tested in production.
2. STDBY_OUT pin not supported in deep standby.

4.6 Recommended DC operating conditions

Table 17 lists the functional recommended operating DC parameters for STA8090EXG.

Table 17. Recommended DC operating conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------------|---|------|------|------|------|
| V _{CC_CHAIN} | Analog supply voltage for RF chain (1.2 V) | 1.08 | 1.20 | 1.32 | V |
| V _{CC_PLL} | Analog supply voltage for PLL RF (1.2 V) | 1.08 | 1.20 | 1.32 | V |
| V _{CC_RF} | Analog supply voltage for RF (1.2 V) | 1.08 | 1.20 | 1.32 | V |
| V _{DD_ADC} | Digital supply voltage for ADC (1.8 V) | 1.71 | 1.80 | 1.89 | V |
| V _{DD_SQI} | Digital supply voltage for SQI I/O ring (1.8 V) | 1.71 | 1.80 | 1.89 | V |
| | Digital supply voltage for SQI I/O ring (3.3 V) | 3.00 | 3.30 | 3.60 | V |

Table 17. Recommended DC operating conditions (continued)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------------|--|------|------|------|------|
| V _{DDD} | Power supply pins for the core logic. | 1.00 | 1.10 | 1.32 | V |
| V _{DDIO_FSMC} | Digital supply voltage for FSMC I/O ring (1.8 V) | 1.71 | 1.80 | 1.89 | V |
| | Digital supply voltage for FSMC I/O ring (3.3 V) | 3.00 | 3.30 | 3.60 | V |
| V _{DDIO_R1} | Digital supply voltage for I/O ring 1 (1.8 V) | 1.71 | 1.80 | 1.89 | V |
| | Digital supply voltage for I/O ring 1 (3.3 V) | 3.00 | 3.30 | 3.60 | V |
| V _{DDIO_R2} | Digital supply voltage for I/O ring 2 (3.3 V) | 3.00 | 3.30 | 3.60 | V |
| V _{INB} | Backup LDO input supply voltage (1.6 V to 4.3 V) | 1.60 | | 4.30 | V |
| V _{INL1} | LDO1 input supply voltage to generate 1.1 V and 1.2 V | 1.60 | | 4.30 | V |
| | LDO1 input supply voltage to generate 1.8 V | 2.10 | | 4.30 | V |
| V _{INL2} | LDO2 input supply voltage to generate 1.2 V | 1.60 | | 4.30 | V |
| V _{INM} | SMPS coil input supply voltage to generate 1.1 V and 1.2 V | 1.60 | | 4.30 | V |
| | SMPS coil input supply voltage to generate 1.8 V | 2.10 | | 4.30 | V |
| V _{DD_ANA} | SMPS input supply (1.6 V to 4.3 V) | 1.60 | | 4.30 | V |
| T _C | Operating case temperature | -40 | | 85 | °C |

4.7 DC characteristics

Table 18 specifies the SMPS voltage regulator characteristics.

Table 18. SMPS DC characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------|------------------------|---|------|------|------|------|
| V _{OM} | Output voltage (1.2 V) | $1.6\text{ V} \leq V_{INM} \leq 4.3\text{ V};$ $I_{OM} \leq 100\text{ mA}$ | 1.08 | 1.20 | 1.32 | V |
| | Output voltage (1.1 V) | $1.6\text{ V} \leq V_{INM} \leq 4.3\text{ V};$ $I_{OM} \leq 100\text{ mA}$ | 1.0 | 1.10 | 1.32 | V |
| | Output voltage (1.8 V) | $2.1\text{ V} \leq V_{INM} \leq 4.3\text{ V};$ $I_{OM} \leq 100\text{ mA}$ | 1.72 | 1.80 | 1.98 | V |
| I _{OM} | Output current | | 0 | — | 100 | mA |

Table 19 specifies the LDO1 voltage regulator characteristics.

Table 19. LDO1 DC characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|------------------|-----------------------|--|------|------|------|------|
| V _{OL1} | Output voltage (1.2V) | 1.6 V ≤ V _{INL1} ≤ 4.3 V; I _{OL1} ≤ 70 mA | 1.08 | 1.20 | 1.32 | V |
| | Output voltage (1.1V) | 1.6 V ≤ V _{INL1} ≤ 4.3 V; I _{OL1} ≤ 70 mA | 1.0 | 1.10 | 1.32 | V |
| | Output voltage (1.8V) | 2.1 V ≤ V _{INL1} ≤ 4.3 V; I _{OL1} ≤ 70 mA | 1.72 | 1.80 | 1.98 | V |
| I _{OL1} | Output current | | 0 | — | 70 | mA |

Table 20 specifies the LDO2 voltage regulator characteristics.

Table 20. LDO2 DC characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|------------------|----------------|--|------|------|------|------|
| V _{OL2} | Output voltage | 1.6 V ≤ V _{INL2} ≤ 4.3 V; I _{OL2} ≤ 30 mA | 1.08 | 1.20 | 1.32 | V |
| I _{OL2} | Output current | | 0 | — | 30 | mA |

Table 21 specifies the low voltage detection thresholds

Table 21. Low voltage detection thresholds

| Parameter | | Min. | Typ. | Max. | Unit |
|---|--|------|-------|------|------|
| Input LVD always on and main VRs ⁽¹⁾ | Upper voltage threshold | — | 1.680 | — | V |
| | Lower voltage threshold | — | 1.650 | — | V |
| Output LVD always on VR ⁽¹⁾ | Upper voltage threshold | — | 0.995 | — | V |
| | Lower voltage threshold | — | 0.935 | — | V |
| Output LVD main VR (1.1 V) ⁽¹⁾ | Upper voltage threshold @ V _{OL1/M} = 1.2 V | — | 1.142 | — | V |
| | Lower voltage threshold @ V _{OL1/M} = 1.2 V | — | 1.076 | — | V |
| | Upper voltage threshold @ V _{OL1/M} = 1.1 V | — | 1.048 | — | V |
| | Lower voltage threshold @ V _{OL1/M} = 1.1 V | — | 0.986 | — | V |
| Output LVD main VR (1.8 V) ⁽¹⁾ | Upper voltage threshold @ V _{OL1/M} = 1.8 V | — | 1.645 | — | V |
| | Lower voltage threshold @ V _{OL1/M} = 1.8 V | — | 1.626 | — | V |

1. Not tested in production.

Table 22 lists the DC characteristics for all the IO digital buffers except for the following input buffers: STBYn (H9), STDBY_OUT (J10), WAKEUP0 (F11), WAKEUP1 (F10), PMU_CFG (H10) and RSTn (G9).

Table 22. I/O buffers DC characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|----------------------------------|---------------------------|-------------------------|------|-------------------------|------|
| V _{IL} ⁽¹⁾ | Logical input low level voltage | V _{DDIO} = 1.8 V | -0.3 | — | 0.3 * V _{DDIO} | V |
| | | V _{DDIO} = 3.3V | -0.3 | — | 0.8 | V |
| V _{IH} ⁽¹⁾ | Logical input high level voltage | V _{DDIO} = 1.8 V | 0.7 * V _{DDIO} | — | V _{DDIO} + 0.3 | V |
| | | V _{DDIO} = 3.3V | 2.0 | — | V _{DDIO} + 0.3 | V |
| V _{HYST} ⁽²⁾ | Schmitt-trigger hysteresis | — | 50 | — | | mV |
| V _{OL} | Low level output voltage | V _{DDIO} = 1.8 V | | — | 0.4 | V |
| | | V _{DDIO} = 3.3V | | — | 0.4 | V |
| V _{OH} | High level output voltage | V _{DDIO} = 1.8 V | V _{DDIO} - 0.4 | — | | V |
| | | V _{DDIO} = 3.3V | V _{DDIO} - 0.4 | — | | V |

1. Excludes oscillator inputs RTC_XTI and XTAL_IN. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.

Table 23 lists the DC characteristics for the 1.0 V IO digital buffers input buffers: STBYn (H9), STDBY_OUT (J10), WAKEUP0 (F11), WAKEUP1 (F10), PMU_CFG (H10) and RSTn (G9).

Table 23. 1.0 V I/O buffers DC characteristics

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-----------------|----------------------------------|-------------------------|------------------------|-----|------------------------|------|
| V _{IL} | Logical input low level voltage | V _{OB} = 1.0 V | -0.3 | — | 0.35 * V _{OB} | V |
| V _{IH} | Logical input high level voltage | V _{OB} = 1.0 V | 0.65 * V _{OB} | — | V _{OB} + 0.3 | V |
| V _{OL} | Low level output voltage | V _{OB} = 1.0 V | | — | 0.2 | V |
| V _{OH} | High level output voltage | V _{OB} = 1.0 V | V _{OB} - 0.2 | — | | V |

4.8 AC characteristics

4.8.1 RF electrical specifications

Table 24. RFACHAIN – GALGPS filter and VGA

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|--------------------------------|--|--|-----|------------------|-----|------|
| S ₁₁ ⁽¹⁾ | Input return loss | GPS band | — | -8 | | dB |
| f _{IF} | IF frequency | PLL in default condition with 26Mhz as reference | — | 4.045 | | MHz |
| NF | Noise figure | NF overall chain with AGC set at 0 dB | — | 2 ⁽¹⁾ | | dB |
| C _G | Conversion gain from RF input to ADC input | VGA at max gain | — | 119 | | dB |
| | | VGA at min gain | — | 69 | | dB |

Table 24. RFACHAIN – GALGPS filter and VGA (continued)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-------------------|-----------------------------------|---------------------------------|-----|-------------------|--------------------|------|
| IP _{1dB} | RF-IF-VGA input compression point | VGA min | — | -80 | | dBm |
| IRR | Image rejection ratio | | — | 20 | | dB |
| BW _{GPS} | -3dB IF bandwidth | GPS mode | — | 2.4 | | MHz |
| BW _{GAL} | | Galileo mode | — | 4.8 | | MHz |
| ATT | Alias frequency rejection | F = 60 MHz (fs = 65.474 MHz) | — | 30 ⁽¹⁾ | | dB |
| T _{gGPS} | IF filter group delay variation | GPS mode | — | | 200 ⁽¹⁾ | ns |
| T _{gGAL} | | Galileo mode | — | | 30 ⁽¹⁾ | ns |

1. Not tested in production.

Table 25. RFCHAIN – GLONASS/BeiDou filter and VGA

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|------------------------|--|---|-----|-------------------|-------------------|------|
| S11 ⁽¹⁾ | Input return loss | GLONASS band | | -8 | | dB |
| | | BeiDou band | | -8 | | |
| f _{IFGNS/BDU} | IF frequency for GLONASS | PLL in default condition with 26 Mhz as reference | — | 8.519 | | MHz |
| | IF frequency for BeiDou | | — | 10.277 | | |
| NF | Noise figure | NF overall chain with AGC set at 0 dB | — | 2 ⁽¹⁾ | | dB |
| C _G | Conversion gain from RF input to ADC input | VGA at max gain | — | 118 | | dB |
| | | VGA at min gain | — | 68 | | dB |
| IP _{1dB} | RF-IF-VGA input compression point | VGA min | — | -80 | | dBm |
| IRR | Image rejection ratio | | — | 30 | | dB |
| BW _{GNS/BDU} | -3dB IF bandwidth | | — | 10 | | MHz |
| ATT | Alias frequency rejection | F = 53 MHz (fs = 65.474 MHz) | — | 30 ⁽¹⁾ | | dB |
| T _{gGNS/BDU} | IF filter group delay variation | | — | | 20 ⁽¹⁾ | ns |

1. Not tested in production.

Table 26. Synthesizer

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------------|---|------|----------|------|------|
| F _{TCXO_XTAL} | Input frequency for xtal amplifier ⁽¹⁾ | 10 | | 55 | MHz |
| R _{DIV} | Reference divider range | 1 | | 63 | |
| N _{DIV} | Loop divider range | 56 | | 2047 | |
| F _{LO} | LO operating frequency | | 3142.656 | | MHz |

1. That amplifier can be used also as a TCXO input buffer

4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator/buffer for RTC circuit.
- an OSCI oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF^(b), as shown on [Figure 2](#).

OSCI32 is disabled by default and must be enabled by setting bit28-OSCI_EN of PRCC_BACKUP_REG0 to have 32.768KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The recommended oscillator specifications are shown in [Table 27](#):

Table 27. Crystal recommended specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------|--|------|--------|------|------|
| F _{SXTAL} | Crystal frequency ⁽¹⁾ | — | 32.768 | — | kHz |
| LM _{SXTAL} | Motion inductance ⁽¹⁾ | — | 5 | — | kH |
| CM _{SXTAL} | Motional capacitance ⁽¹⁾ | — | 5.0 | — | fF |
| CO _{SXTAL} | Shunt capacitance ⁽¹⁾ | — | 1.3 | — | pF |
| ESR | Resonance resistance ⁽¹⁾ | — | — | 80 | kΩ |
| CL | External load capacitance ⁽¹⁾ | — | 18 | — | pF |

1. Not tested in production.

b. Using crystal with recommended characteristics as per [Table 27](#).

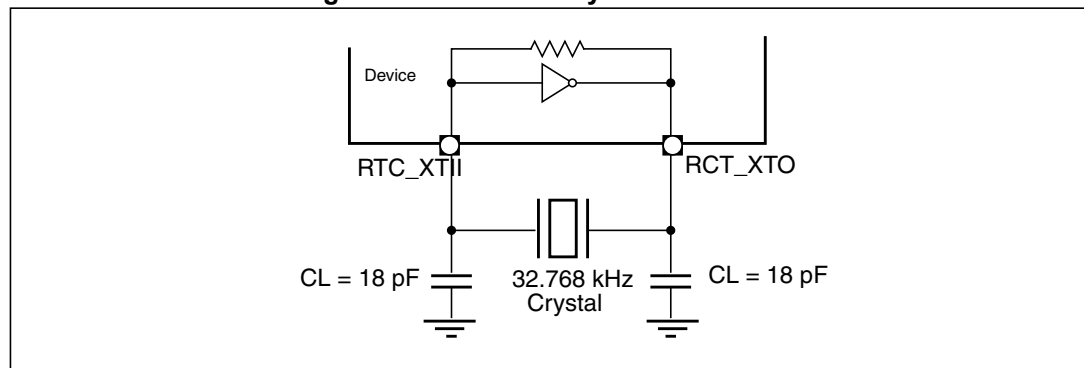
The oscillator amplifier specifications are shown in the following table:

Table 28. Oscillator amplifier specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------|--|------|------|------|------|
| T _S | Startup time ⁽¹⁾ | — | 0.3 | 0.6 | s |
| DL | Drive level ⁽¹⁾ | — | — | <0.1 | μW |
| RLC | Required load capacitance ⁽¹⁾ | — | 12.5 | — | pF |
| GM | Startup transconductance | 22.5 | 33.6 | — | μA/V |

1. Not tested in production.

Figure 2. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI_EN = 0b in PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 29. Characteristics of external slow clock input

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------------|-----------------------|------|------|------|------|
| T _{JIT} (cc) | Cycle-to-cycle jitter | -70 | — | 70 | ps |
| T _{JIT} (per) | Period jitter | -70 | — | 70 | ps |
| | Variation | -500 | — | 500 | ppm |
| T _{DUTY} | Duty cycle | 45 | — | 55 | % |

4.8.3 OSCI oscillator specifications

The supported values of the embedded BOOT ROM are 16.368 MHz, 24.00 MHz, 26.00 MHz and 48.00 MHz.

The default values supported by the GNSS binary image are 26 MHz and 48 MHz, to enable USB peripheral the 48 MHz is mandatory.

4.8.4 ADC specifications

This section gives the AC specification of the 10 bit Successive Approximation Register ADC embedded in STA8090EXG device. It is controlled by the ARM9 MCU through a

wrapper and an APB bridge as depicted in *Figure 3* and it has a maximum conversion rate of 1MSPS with 8 muxed analog input channels capability. An internal voltage reference is used and analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins.

Figure 3. SARADC connections

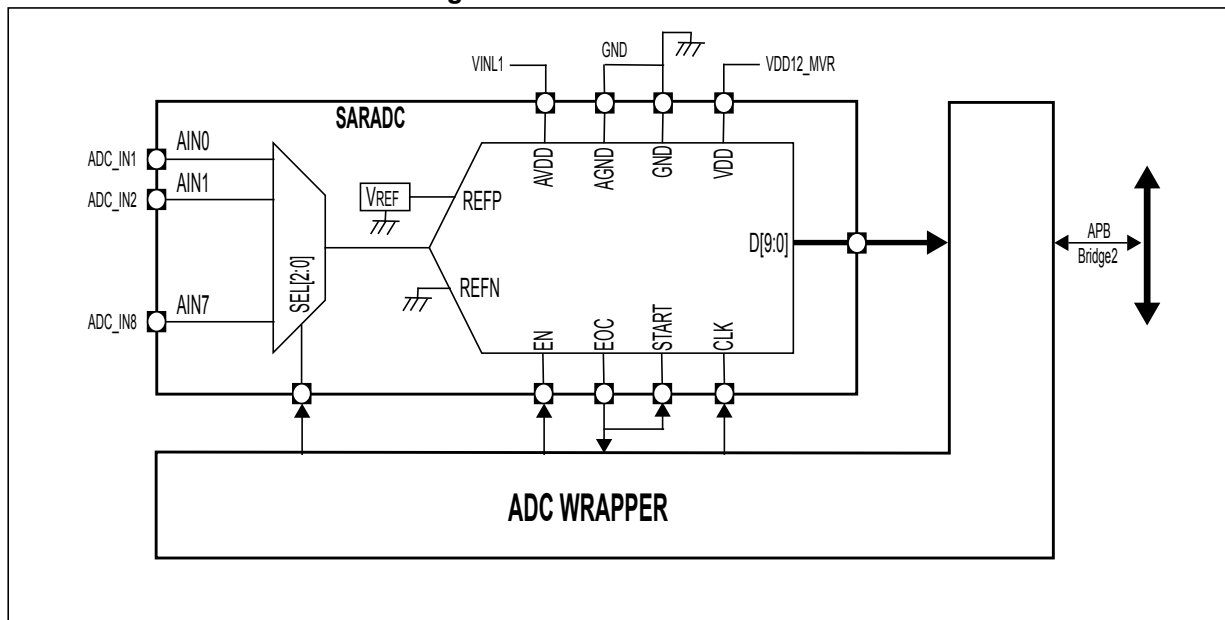


Table 30. SARADC specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------------------|--|-----------------------|------|--------------------------|--------|
| V _{ADCIN} | ADC_IN input range | V _{GND} -0.3 | — | V _{DD_ADC} +0.3 | V |
| V _{ADCCR} | Conversion range | V _{GND} | — | V _{REF} | V |
| V _{REF} | Voltage reference | 1.35 | 1.4 | 1.45 | V |
| C _{IN} | Input capacitance ⁽¹⁾ | 5.5 | 7.0 | 8.5 | pF |
| R _{IN} | Input mux resistance (total equivalent sampling resistance) ⁽²⁾ | 1.5 | 2.0 | 2.5 | kΩ |
| F _{CLK} | Clock frequency | 2.5 | — | 15 | MHz |
| δ _{CLK} | Clock duty cycle | 45 | 50 | 55 | % |
| T _{SUP} | Start up time ⁽¹⁾⁽³⁾ | — | — | 20 | μs |
| T _C | Conversion time | — | 14 | — | cycles |
| T _S | Sampling time | — | 3 | — | cycles |
| INL | Performance | — | — | < ±2 | LSB |
| DNL | | — | — | < ±2 | LSB |

1. Not tested in production.
2. Pad input capacitance included.
3. From EN = 1.

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 TFBGA169 9 x 9 x 1.2 mm package information

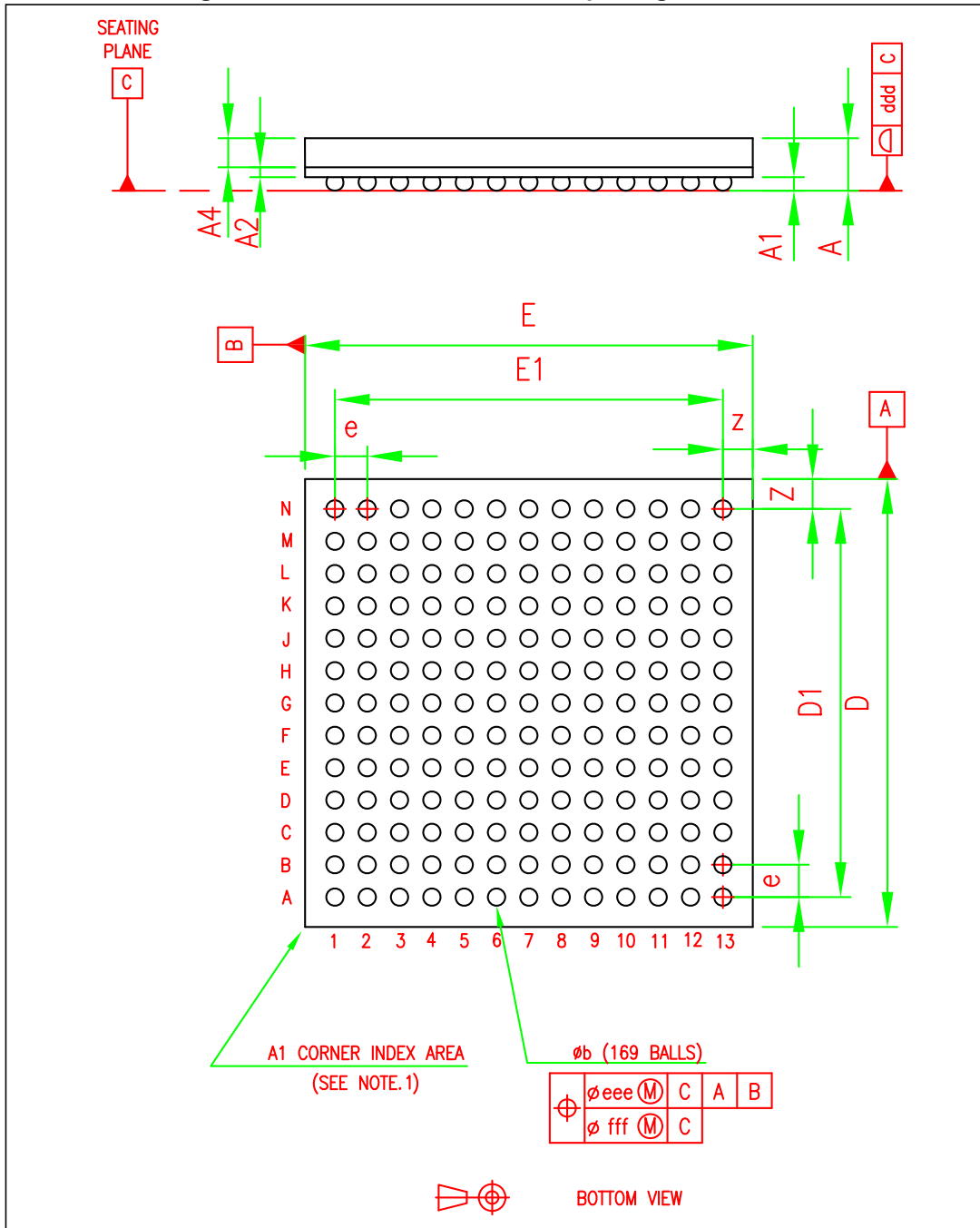
Table 31. TFBGA169 9 x 9 x 1.2 mm mechanical data

| Ref. dim | Data book (mm) | | | Drawing (mm) | | |
|--------------------|----------------|-------|------|--------------|-------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A ⁽¹⁾ | | | 1.20 | | | 1.07 |
| A1 ⁽²⁾ | 0.21 | | | 0.22 | 0.27 | 0.32 |
| A2 | | 0.20 | | 0.16 | 0.20 | 0.24 |
| A4 | | 0.585 | | 0.57 | 0.585 | 0.60 |
| b ⁽³⁾ | 0.30 | 0.35 | 0.40 | 0.30 | 0.35 | 0.40 |
| D | 8.85 | 9.00 | 9.15 | 8.90 | 9.00 | 9.10 |
| D1 | | 7.80 | | | 7.80 | |
| E | 9.85 | 9.00 | 9.15 | 8.90 | 9.00 | 9.10 |
| E1 | | 7.80 | | | 7.80 | |
| e | | 0.65 | | | 0.65 | |
| Z | | 0.60 | | | 0.60 | |
| ddd | | | 0.08 | | | 0.08 |
| eee ⁽⁴⁾ | | | 0.15 | | | 0.15 |
| fff ⁽⁵⁾ | | | 0.05 | | | 0.05 |

- TFBGA stands for Thin profile Fine Pitch Ball Grid Array.
 - The total profile height (Dim A) is measured from the seating plane to the top of the component
 - The maximum total package height is calculated by the following methodology:
 $A_{Max} = A1_{Typ} + A2_{Typ} + A4_{Typ} + \sqrt{A1^2 + A2^2 + A4^2}$ tolerance values
 - Thin profile: 1.00 mm < A ≤ 1.20 mm / Fine pitch: e < 1.00 mm pitch.
- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
 - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
- The typical ball diameter before mounting is 0.35 mm.
- The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

- The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ϕff perpendicular to datum C and located on true position as defined by e . The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone ϕff in the array is contained entirely in the respective zone ϕee above. The axis of each ball must lie simultaneously in both tolerance zones.

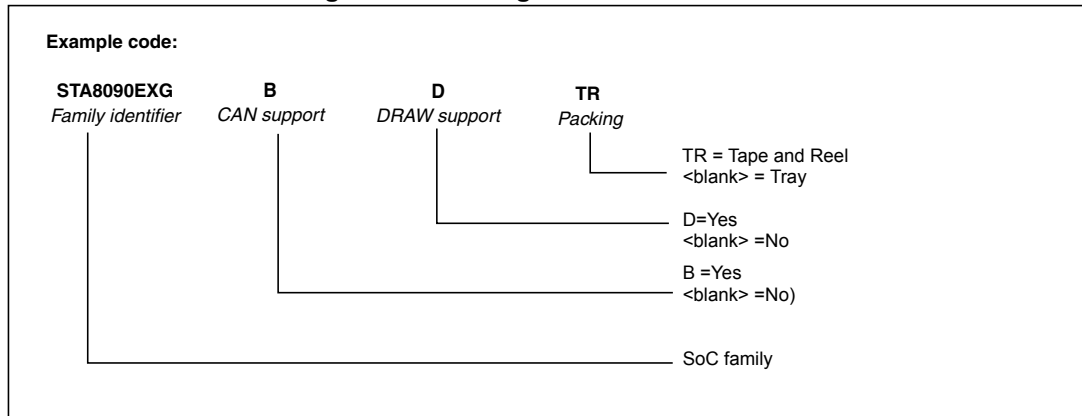
Figure 4. TFBGA169 9 x 9 x 1.2 mm package dimension



- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

6 Ordering information

Figure 5. Ordering information scheme



7 Revision history

Table 32. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 21-Nov-2014 | 1 | Initial release. |
| 30-Jun-2015 | 2 | <p>Updated <i>Features</i> and <i>Description</i> Updated <i>Chapter 1: Overview</i> <i>Table 3: Power supply pins:</i> – VOL1 VOM, VDDD: updated description Updated <i>Section 3.4.2: EFT</i> and <i>Section 3.4.4: UART</i> <i>Table 16: Power consumption:</i> – P_{RF}: updated typical value for GPS/Galileo – P_{MVR}, P_{LPVR}, P_{IO}: added note – I_{DSLEEP}: updated value <i>Table 17: Recommended DC operating conditions:</i> – V_{INL1}, V_{INL2}, V_{INM}: updated parameters <i>Table 18: SMPS DC characteristics:</i> – V_{OM}: set min and max values as TBD, removed condition for Output voltage at 1.0 V <i>Table 19: LDO1 DC characteristics:</i> – V_{OL1}: set min and max values as TBD, removed condition for Output voltage at 1.0 V <i>Table 20: LDO2 DC characteristics:</i> – V_{OL2}: set min and max values as TBD <i>Table 21: Low voltage detection thresholds:</i> – Output LVD main VR (1.1 V): removed condition for Output voltage at 1.0 V <i>Table 24: RFCHAIN – GALGPS filter and VGA:</i> – S11: Added note – C_G: updated values <i>Table 25: RFCHAIN – GLONASS/BeiDou filter and VGA:</i> – S11: Added note – C_G: updated values <i>Table 28: Oscillator amplifier specifications:</i> – T_S: updated minimum value Updated <i>Section 4.8.3: OSCI oscillator specifications</i></p> |
| 14-Dec-2015 | 3 | <p><i>Table 13: Voltage characteristics:</i> – V_{ESD-HBM}, V_{ESD-CDM}: updated values</p> |
| 30-May-2017 | 4 | <p>Changed from STA8090EXGA to STA8090EXGBD Updated <i>Table 16: Power consumption</i> Updated <i>Table 18: SMPS DC characteristics</i> Updated <i>Table 19: LDO1 DC characteristics</i> Updated <i>Table 20: LDO2 DC characteristics</i> Updated <i>Table 25: RFCHAIN – GLONASS/BeiDou filter and VGA</i> Updated <i>Table 26: Synthesizer</i> Updated <i>Figure 5: Ordering information scheme</i></p> |

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