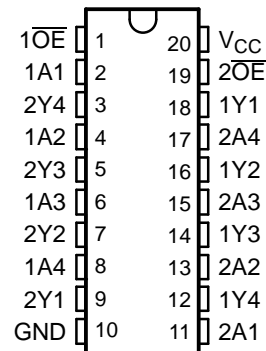


## FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- 2-V to 5.5-V  $V_{\text{CC}}$  Operation
- Max  $t_{\text{pd}}$  of 6.5 ns at 5 V
- Typical  $V_{\text{OLP}}$  (Output Ground Bounce)  $<0.8\text{ V}$  at  $V_{\text{CC}} = 3.3\text{ V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$
- Typical  $V_{\text{OHV}}$  (Output  $V_{\text{OH}}$  Undershoot)  $>2.3\text{ V}$  at  $V_{\text{CC}} = 3.3\text{ V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- $I_{\text{off}}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DW PACKAGE  
(TOP VIEW)



(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## DESCRIPTION/ORDERING INFORMATION

This octal buffer/line driver is designed for 2-V to 5.5-V  $V_{\text{CC}}$  operation.

The SN74LV244A-EP is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device is organized as two 4-bit line drivers with separate output-enable ( $\overline{\text{OE}}$ ) inputs. When  $\overline{\text{OE}}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{\text{OE}}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## ORDERING INFORMATION

$T_{\text{A}}$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – DW Reel of 2000	SN74LV244AMDWREP	LV244AMEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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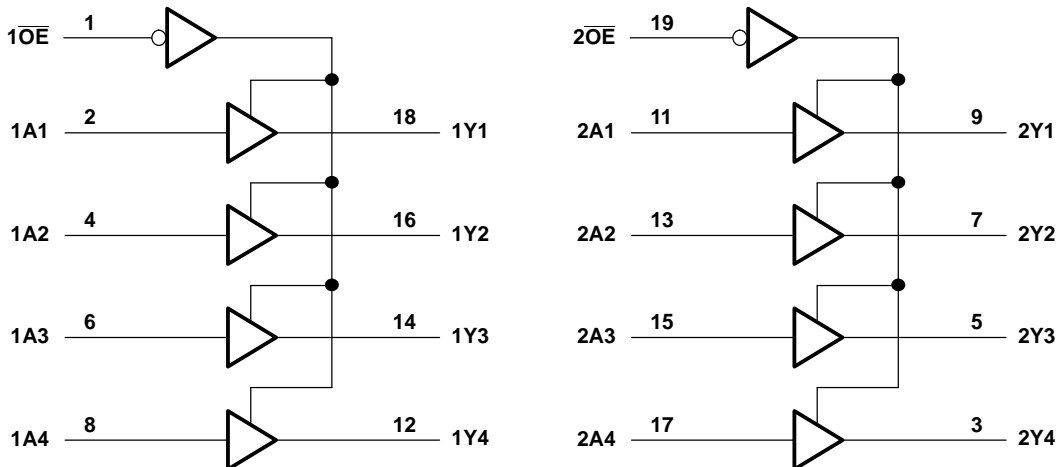
# SN74LV244A-EP OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS695–JANUARY 2006

**FUNCTION TABLE  
(EACH BUFFER)**

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Output voltage range applied in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current		$V_I < 0$	-20 mA
$I_{OK}$	Output clamp current		$V_O < 0$	-50 mA
$I_O$	Continuous output current		$V_O = 0$ to $V_{CC}$	$\pm 35$ mA
	Continuous current through $V_{CC}$ or GND			$\pm 70$ mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		58	$^{\circ}\text{C}/\text{W}$
$T_{stg}$	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$		
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3-state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	–50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	–2		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	–8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	–16		
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20		
$T_A$	Operating free-air temperature	–55	125	°C	

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LV244A-EP OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS695–JANUARY 2006

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			
	I <sub>OH</sub> = -8 mA	3 V	2.48			
	I <sub>OH</sub> = -16 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			
	I <sub>OL</sub> = 8 mA	3 V	0.44			
	I <sub>OL</sub> = 16 mA	4.5 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0	5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.3			pF

## Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	9.5	15.3	1	18	ns	
t <sub>en</sub>	$\overline{OE}$	Y		10.8	17.8	1	21	ns	
t <sub>dis</sub>	$\overline{OE}$	Y		13.4	19.2	1	21	ns	
t <sub>sk(o)</sub>							2	2	ns

## Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	6.8	11.9	1	13.5	ns	
t <sub>en</sub>	$\overline{OE}$	Y		7.8	14.1	1	16	ns	
t <sub>dis</sub>	$\overline{OE}$	Y		11	16	1	18	ns	
t <sub>sk(o)</sub>							1.5	1.5	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A	Y	$C_L = 50\text{ pF}$		4.9	7.5	1	8.5	ns
$t_{en}$	$\overline{OE}$	Y			5.6	9.3	1	10.5	ns
$t_{dis}$	$\overline{OE}$	Y			8.8	14.2	1	15.5	ns
$t_{sk(o)}$								1	ns

### Noise Characteristics<sup>(1)</sup>

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

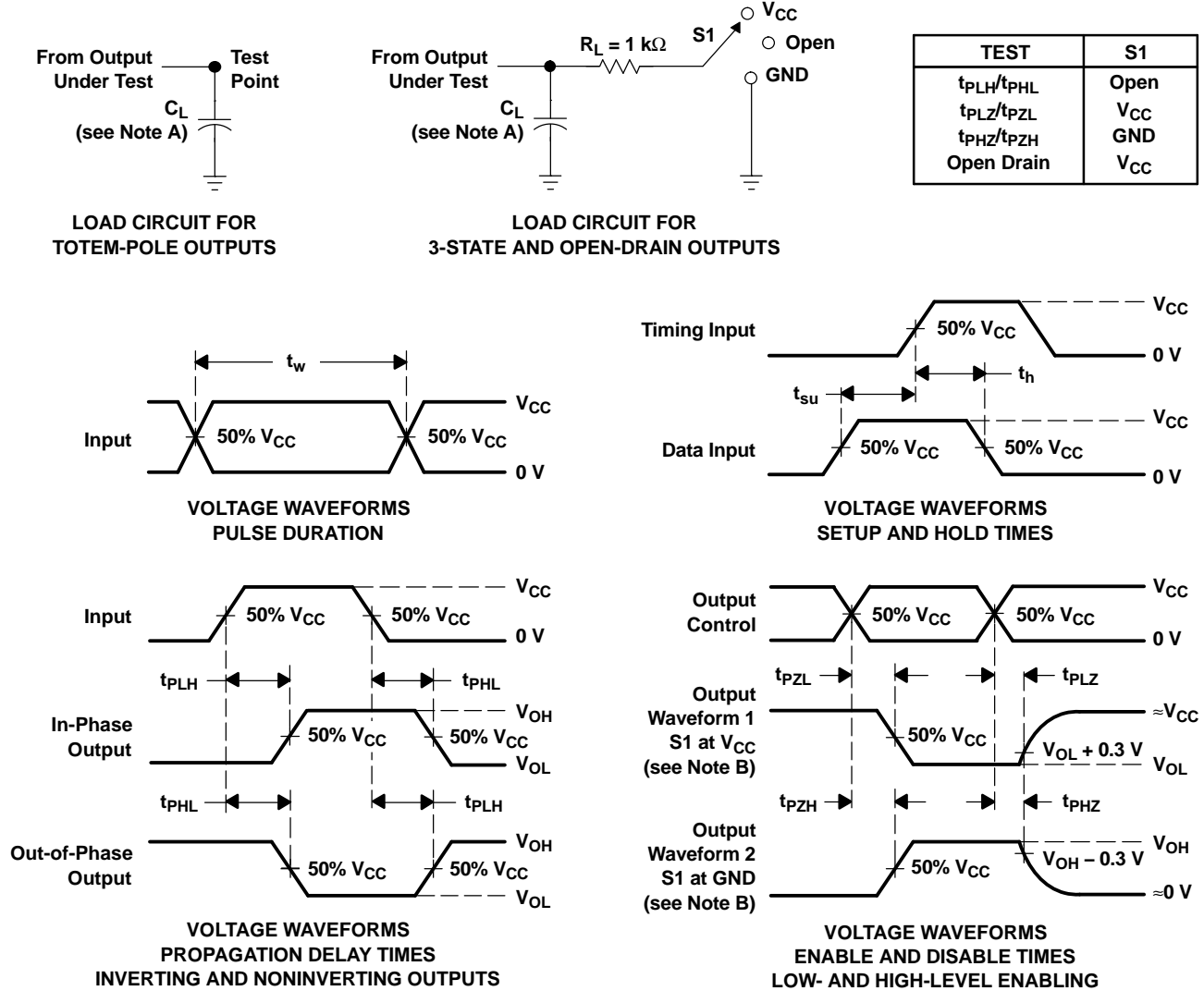
(1) Characteristics are for surface-mount packages only.

### Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 10\text{ MHz}$	3.3 V	14	pF
				5 V	16	

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
D. The outputs are measured one at a time, with one input transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV244AMDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV244AMEP	<a href="#">Samples</a>
V62/06604-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV244AMEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV244A-EP :**

- Catalog: [SN74LV244A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV244AMDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV244AMDWREP	SOIC	DW	20	2000	367.0	367.0	45.0

DW (R-PDSO-G20)

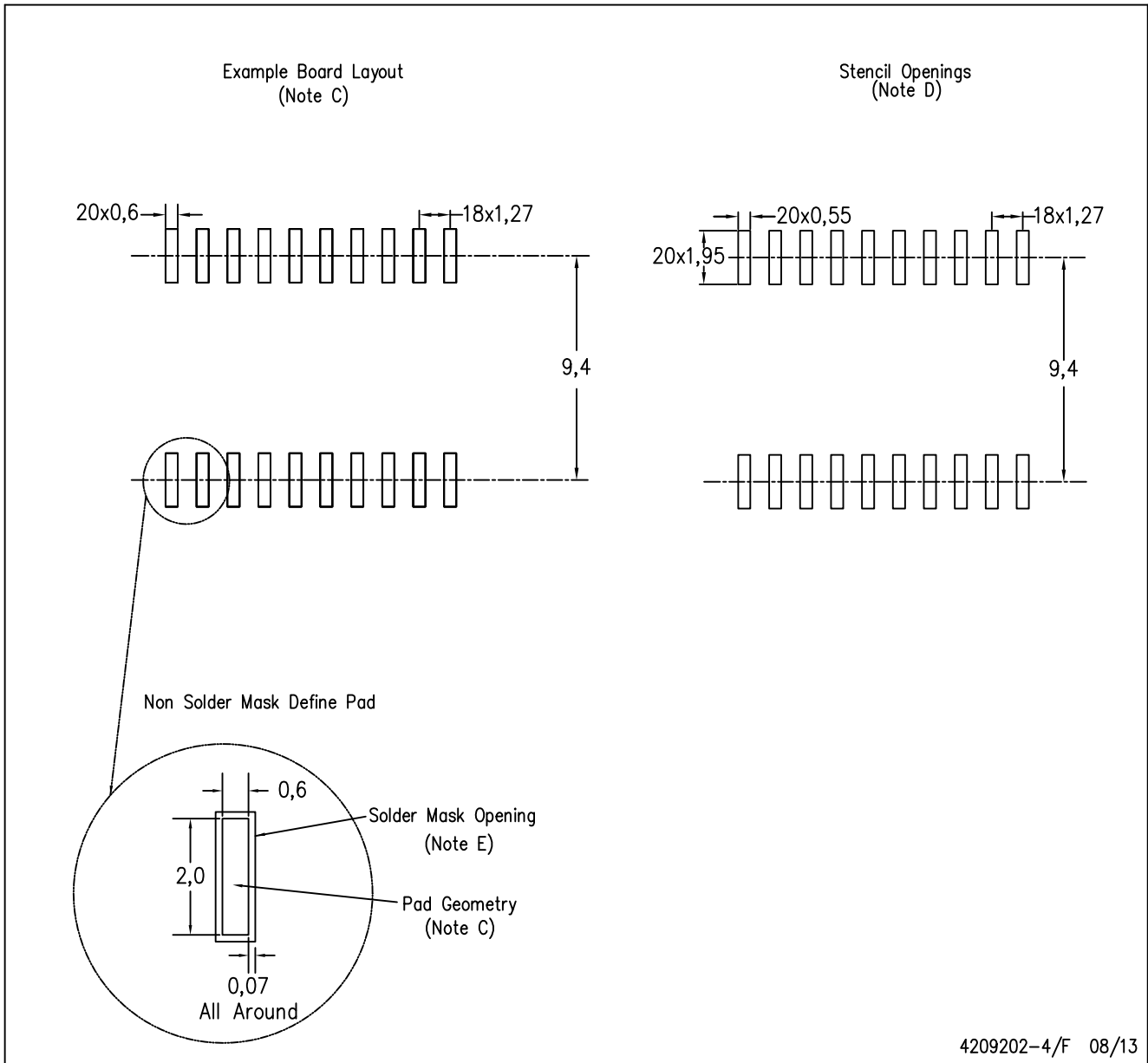
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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