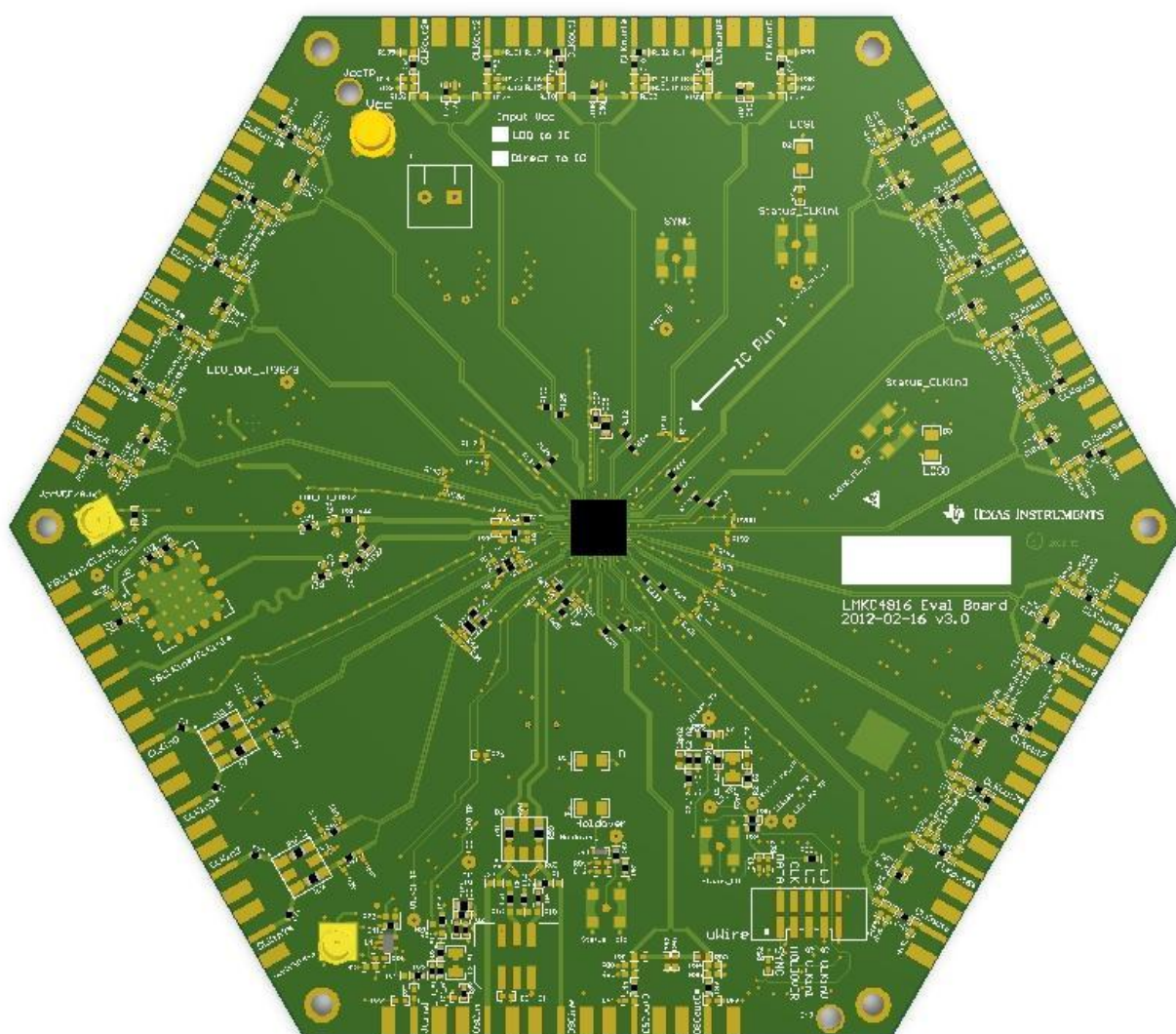




# TEXAS INSTRUMENTS

## LMK04816

### Low-Noise Clock Jitter Cleaner with Dual Loop PLLs



## LMK04816 Evaluation Board Operating Instructions

Texas Instruments

June 2012

# Table of Contents

|                                                                          |           |
|--------------------------------------------------------------------------|-----------|
| <b>TABLE OF CONTENTS.....</b>                                            | <b>2</b>  |
| <b>GENERAL DESCRIPTION.....</b>                                          | <b>4</b>  |
| EVALUATION BOARD KIT CONTENTS .....                                      | 4         |
| AVAILABLE LMK04816 EVALUATION BOARDS.....                                | 4         |
| AVAILABLE LMK04816 FAMILY DEVICES .....                                  | 4         |
| <b>QUICK START .....</b>                                                 | <b>5</b>  |
| DEFAULT CODELOADER MODES FOR EVALUATION BOARDS.....                      | 6         |
| <b>EXAMPLE: USING CODELOADER TO PROGRAM THE LMK04816 .....</b>           | <b>7</b>  |
| 1. START CODELOADER 4 APPLICATION.....                                   | 7         |
| 2. SELECT DEVICE .....                                                   | 7         |
| 3. PROGRAM/LOAD DEVICE.....                                              | 8         |
| 4. RESTORING A DEFAULT MODE.....                                         | 8         |
| 5. VISUAL CONFIRMATION OF FREQUENCY LOCK.....                            | 9         |
| 6. ENABLE CLOCK OUTPUTS.....                                             | 9         |
| <b>PLL LOOP FILTERS AND LOOP PARAMETERS.....</b>                         | <b>11</b> |
| PLL 1 LOOP FILTER .....                                                  | 11        |
| 122.88 MHz VCXO PLL .....                                                | 11        |
| PLL2 LOOP FILTER.....                                                    | 12        |
| <b>EVALUATION BOARD INPUTS AND OUTPUTS.....</b>                          | <b>13</b> |
| <b>RECOMMENDED TEST EQUIPMENT.....</b>                                   | <b>21</b> |
| <b>PROGRAMMING 0-DELAY MODE IN CODELOADER .....</b>                      | <b>22</b> |
| OVERVIEW.....                                                            | 22        |
| DUAL LOOP 0-DELAY MODE EXAMPLES .....                                    | 22        |
| <i>Programming Steps</i> .....                                           | 22        |
| <i>Details</i> .....                                                     | 22        |
| SINGLE LOOP 0-DELAY MODE EXAMPLES .....                                  | 24        |
| <i>Programming Steps</i> .....                                           | 24        |
| <i>Details</i> .....                                                     | 24        |
| <b>APPENDIX A: CODELOADER USAGE.....</b>                                 | <b>26</b> |
| PORT SETUP TAB .....                                                     | 26        |
| CLOCK OUTPUTS TAB .....                                                  | 27        |
| PLL1 TAB.....                                                            | 29        |
| <i>Setting the PLL1 VCO Frequency and PLL2 Reference Frequency</i> ..... | 30        |
| PLL2 TAB.....                                                            | 31        |
| BITS/PINS TAB .....                                                      | 32        |
| REGISTERS TAB.....                                                       | 37        |
| <b>APPENDIX B: TYPICAL PHASE NOISE PERFORMANCE PLOTS.....</b>            | <b>38</b> |
| PLL1.....                                                                | 38        |
| 122.88 MHz VCXO Phase Noise.....                                         | 38        |
| Clock Output Measurement Technique.....                                  | 39        |
| Buffered Phase Noise .....                                               | 39        |
| CLOCK OUTPUTS (CLKOUT) .....                                             | 40        |

|                                                                                        |           |
|----------------------------------------------------------------------------------------|-----------|
| LMK04816B CLKout Phase Noise.....                                                      | 40        |
| LMK04816B OSCout Phase Noise .....                                                     | 41        |
| <b>APPENDIX C: SCHEMATICS .....</b>                                                    | <b>43</b> |
| POWER SUPPLIES .....                                                                   | 43        |
| LMK04816B DEVICE WITH LOOP FILTER AND CRYSTAL CIRCUITS .....                           | 44        |
| REFERENCE INPUTS (CLKIN0, CLKIN1, & CLKIN2), EXTERNAL VCXO (OSCIN) & VCO CIRCUITS..... | 45        |
| CLOCK OUTPUTS (OScout0, CLKout0 to CLKout3) .....                                      | 46        |
| CLOCK OUTPUTS (CLKout4 to CLKout7) .....                                               | 47        |
| CLOCK OUTPUTS (CLKout8 to CLKout11) .....                                              | 48        |
| UWire HEADER, LOGIC I/O PORTS AND STATUS LEDs.....                                     | 49        |
| USB INTERFACE.....                                                                     | 50        |
| <b>APPENDIX D: BILL OF MATERIALS .....</b>                                             | <b>51</b> |
| <b>APPENDIX E: PCB LAYERS STACKUP.....</b>                                             | <b>56</b> |
| <b>APPENDIX F: PCB LAYOUT .....</b>                                                    | <b>57</b> |
| LAYER #1 – TOP .....                                                                   | 57        |
| LAYER #2 – RF GROUND PLANE (INVERTED) .....                                            | 58        |
| LAYER #3 – VCC PLANES .....                                                            | 59        |
| LAYER #4 – GROUND PLANE (INVERTED).....                                                | 60        |
| LAYER # 5 – VCC PLANES 2.....                                                          | 61        |
| LAYER #6 – BOTTOM.....                                                                 | 62        |
| LAYERS #1 AND 6 – TOP AND BOTTOM (COMPOSITE).....                                      | 63        |
| <b>APPENDIX G: PROPERLY CONFIGURING LPT PORT .....</b>                                 | <b>65</b> |
| LPT DRIVER LOADING.....                                                                | 65        |
| CORRECT LPT PORT/ADDRESS .....                                                         | 65        |
| CORRECT LPT MODE.....                                                                  | 66        |
| <b>APPENDIX H: TROUBLESHOOTING INFORMATION .....</b>                                   | <b>67</b> |
| 1) CONFIRM COMMUNICATIONS .....                                                        | 67        |
| 2) CONFIRM PLL1 OPERATION/LOCKING .....                                                | 67        |
| 3) CONFIRM PLL2 OPERATION/LOCKING .....                                                | 68        |

## General Description

The LMK04816 Evaluation Board simplifies evaluation of the LMK04816B Low-Noise Clock Jitter Cleaner with Dual Loop PLLs. Texas Instruments's *CodeLoader* software can be used to program the internal registers of the LMK04816B device through the MICROWIRE™ interface. The *CodeLoader* software will run on a Windows 2000 or Windows XP PC and can be downloaded from <http://www.ti.com/tool/codeloader/>.

## Evaluation Board Kit Contents

The evaluation board kit includes:

- (1) LMK04816 Evaluation Board from Table 1
- (1) CodeLoader uWire cable (LPT → uWire)

## Available LMK04816 Evaluation Boards

The LMK04816 Evaluation Board supports any of the four devices offered in the LMK04816 Family. A commercial-quality VCXO is also mounted to the board to provide a known reference point for evaluating device performance and functionality.

**Table 1: Available Evaluation Board Configurations**

| Evaluation Board ID | Device    | PLL1 VCXO                                         |
|---------------------|-----------|---------------------------------------------------|
| LMK04816BEVAL       | LMK04816B | 122.88 MHz Crystek VCXO<br>Model CVHD-950-122.880 |

## Available LMK04816 Family Devices

**Table 2: LMK04816B Devices**

| Device    | Reference Inputs | Buffered/<br>Divided<br>OSCin<br>Outputs | Programmable<br>LVDS/LVPECL/<br>LVC MOS<br>Outputs | VCO Frequency    |
|-----------|------------------|------------------------------------------|----------------------------------------------------|------------------|
| LMK04816B | 3                | 1                                        | 12                                                 | 2370 to 2600 MHz |

## Quick Start

Full evaluation board instructions are downloadable from the LMK04816B device product folder at [www.ti.com](http://www.ti.com).

1. Connect a power supply voltage of **5 V** to the Vcc SMA connector. The onboard LP3878-ADJ LDO regulator will output a low-noise 3.3 V supply to operate the device.
2. Connect a reference clock from a signal source to the CLKin1 SMA port. Use **122.88 MHz** for default. The reference frequency depends on the device programming.
3. Connect the uWire header to a PC parallel port using the CodeLoader cable. A USB interface is also available (search for “USB2UWIRE-IFACE” at [www.ti.com](http://www.ti.com)).
4. Program the device with a default mode using CodeLoader. Ctrl+L must be pressed at least once to load all registers. Alternatively click menu “Keyboard Controls” → “Load Device”. CodeLoader can be downloaded from [www.ti.com/tool/codeloader/](http://www.ti.com/tool/codeloader/).
5. Measurements may be made on an active output clock port via its SMA connector.

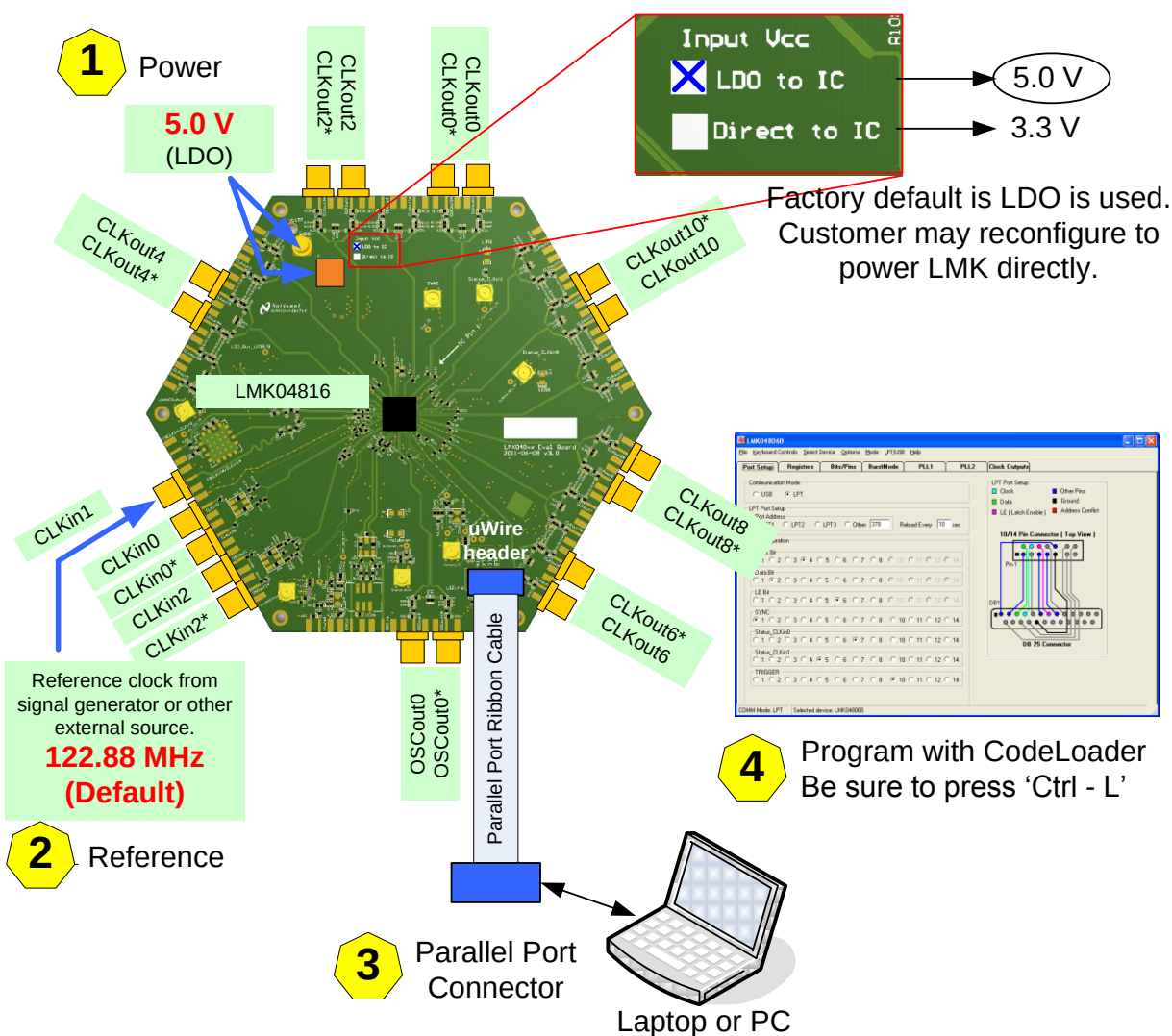


Figure 1: Quick Start Diagram

## Default CodeLoader Modes for Evaluation Boards

CodeLoader saves the state of the selected LMK04816B device when exiting the software. To ensure a common starting point, the following modes listed in Table 3 may be restored by clicking “Mode” and selecting the appropriate device configuration, as shown in Figure 2 in the case of the LMK04816 device. Similar default modes are available for each LMK04816B device in CodeLoader. Choose a mode with CLKIn0 for differential clock signal or CLKIn1 for a single ended signal.

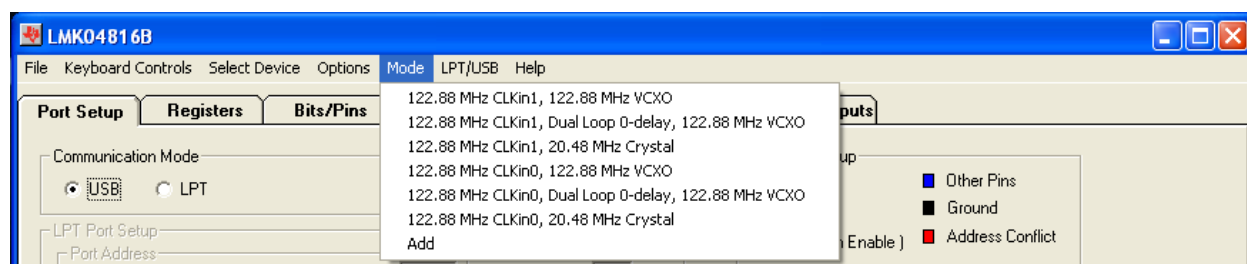


Figure 2: Selecting a Default Mode for the LMK04816 Device

After restoring a default mode, press Ctrl+L to program the device. The default modes also disable certain outputs, so make sure to enable the output under test to make measurements.

Table 3: Default CodeLoader Modes for LMK04816

| Default CodeLoader Mode                               | Device Mode                                             | CLKIn Frequency | OSCIn Frequency |
|-------------------------------------------------------|---------------------------------------------------------|-----------------|-----------------|
| 122.88 MHz CLKIn1, 122.88 MHz VCXO                    | Dual PLL, Internal VCO                                  | 122.88 MHz      | 122.88 MHz      |
| 122.88 MHz CLKIn1, Dual Loop 0-delay, 122.88 MHz VCXO | Dual PLL, Internal VCO, 0-Delay with Internal Feedback  | 122.88 MHz      | 122.88 MHz      |
| 122.88 MHz CLKIn1, 122.88 MHz VCXO                    | Dual PLL, Internal VCO, PLL2 Crystal Oscillator Enabled | 122.88 MHz      | 20.48 MHz       |
| 122.88 MHz CLKIn1, 122.88 MHz VCXO                    | Dual PLL, Internal VCO                                  | 122.88 MHz      | 122.88 MHz      |
| 122.88 MHz CLKIn1, Dual Loop 0-delay, 122.88 MHz VCXO | Dual PLL, Internal VCO, 0-Delay with Internal Feedback  | 122.88 MHz      | 122.88 MHz      |
| 122.88 MHz CLKIn1, 122.88 MHz VCXO                    | Dual PLL, Internal VCO, PLL2 Crystal Oscillator Enabled | 122.88 MHz      | 20.48 MHz       |

The next section outlines step-by-step procedures for using the evaluation board with the LMK04816. For boards with another part number, make sure to select the corresponding part number under the “Device” menu.



## Example: Using CodeLoader to Program the LMK04816

The purpose of this section is to walk the user through using CodeLoader 4 to make some measurements with the LMK04816 device as an example. For more information on CodeLoader refer to Appendix A: CodeLoader Usage or the CodeLoader 4 instructions located at <http://www.ti.com/tool/codeloader/>.

Before proceeding, be sure to follow the Quick Start section above to ensure proper connections.

### 1. Start CodeLoader 4 Application

Click “Start” → “Programs” → “CodeLoader 4” → “CodeLoader 4”

The CodeLoader 4 program is installed by default to the CodeLoader 4 application group.

### 2. Select Device

Click “Select Device” → “Clock Conditioners” → “LMK04816”

Once started CodeLoader 4 will load the last used device. To load a new device click “Select Device” from the menu bar, then select the subgroup and finally device to load. For this example, the LMK04816B is chosen. Selecting the device does cause the device to be programmed.

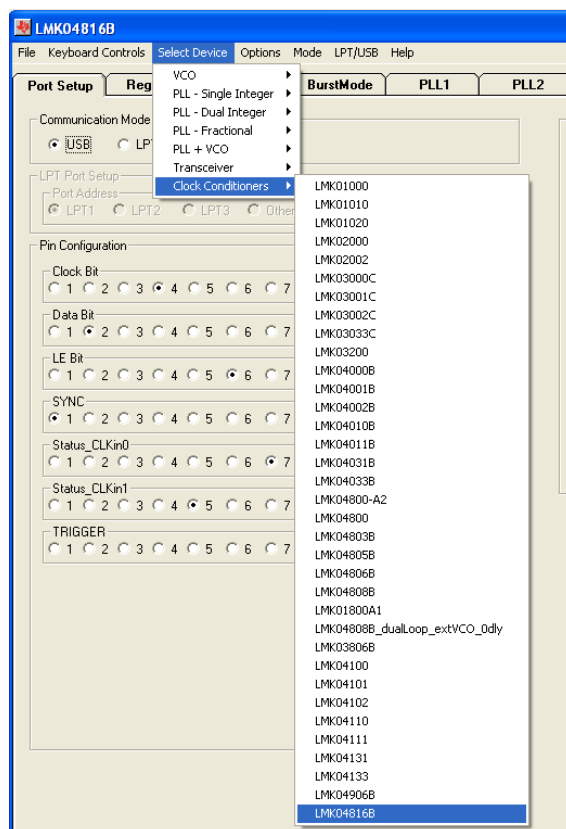


Figure 3 – Selecting the LMK04816B device

### 3. Program/Load Device

Assuming the Port Setup settings are correct, press the “Ctrl+L” shortcut or click “Keyboard Controls” → “Load Device” from the menu to program the device to the current state of the newly loaded LMK04816 file.



Once the device has been initially loaded, CodeLoader will automatically program changed registers so it is not necessary to re-load the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the “Options” → “AutoReload with Changes.”

Because a default mode will be restored in the next step, this step isn’t really needed but included to emphasize the importance of pressing “Ctrl+L” to load the device at least once after starting CodeLoader, restoring a mode, or restoring a saved setup using the File menu.

See Appendix A: CodeLoader Usage or the CodeLoader 4 instructions located at <http://www.ti.com/tool/codeloader/> for more information on Port Setup. Appendix H: Troubleshooting Information contains information on troubleshooting communications.

### 4. Restoring a Default Mode

Click “Mode” → “LMK04816, 122.88 MHz VCXO, 122.88 MHz CLKin1”; then press Ctrl+L.

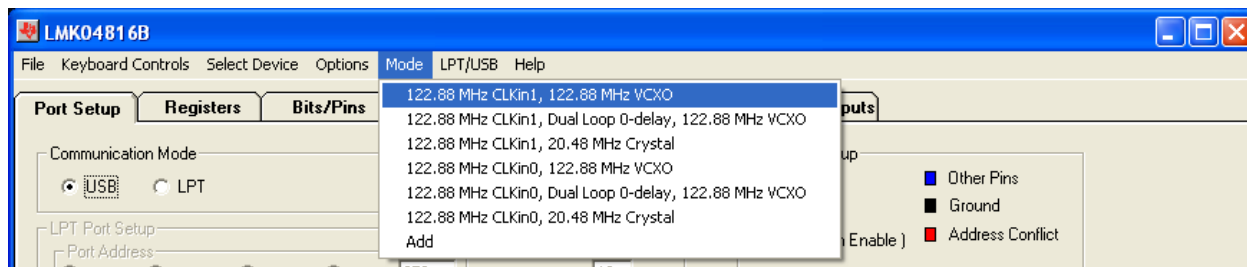


Figure 5: Setting the Default mode for LMK04816

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when CodeLoader is closed, it remembers the last settings used for a particular device. Again, remember to press Ctrl+L as the first step after loading a default mode.



## 5. Visual Confirmation of Frequency Lock

After a default mode is restored and loaded, LED D5 should illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKIn1. This assumes LD\_MUX = PLL1/2 DLD and LD\_TYPE = Active High, which are the default settings.

## 6. Enable Clock Outputs

While the LMK04816B offers programmable clock output buffer formats, the evaluation board is shipped with preconfigured output terminations to match the default buffer type for each output. Refer to the CLKout port description in the Evaluation Board Inputs and Outputs section.

To measure phase noise at one of the clock outputs, for example, CLKout0:

1. Click on the **Clock Outputs** tab,
2. Uncheck “Powerdown” in the Digital Delay box to enable the channel,
3. Set the following settings as needed:
  - a. Digital Delay value
  - b. Clock Divider value
  - c. Analog Delay select and Analog Delay value (if not “Bypassed”)
  - d. Clock Output type.

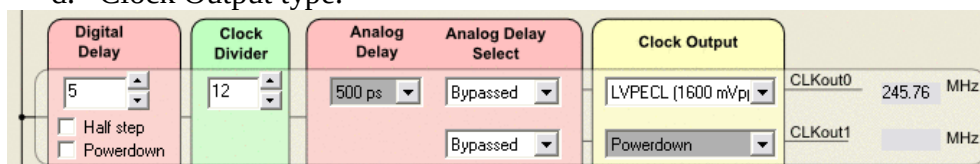


Figure 6: Setting Digital Delay, Clock Divider, Analog Delay, and Output Format for CLKout0

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended 50-ohm input as follows.
  - a. For LVDS:
    - i. A balun (like ADT2-1T) is recommended for differential-to-single-ended conversion.
  - b. For LVPECL:
    - i. A balun can be used, or
    - ii. One side of the LVPECL signal can be terminated with a 50-ohm load and the other side can be run single-ended to the instrument.
  - c. For LVCMOS:
    - i. There are two single-ended outputs, CLKoutX and CLKoutX\*, and each output can be set to Normal, Inverted, or Off. There are nine (9) combinations of LVCMOS modes in the Clock Output list.
    - ii. One side of the LVCMOS signal can be terminated with a 50-ohm load and the other side can be run single-ended to the instrument.
    - iii. A balun may also be used. Ensure CLKoutX and CLKoutX\* states are complementary to each other, i.e.:

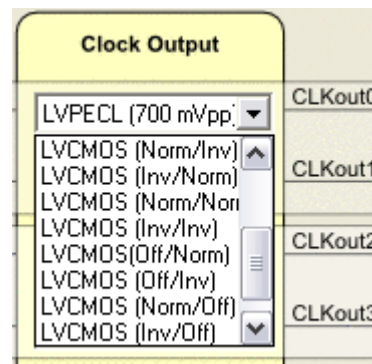


Figure 7: Setting LVCMOS modes

Norm/Inv or Inv/Norm.

5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

See Appendix B: Typical Phase Noise Performance Plots for phase noise plots of the clock outputs.

National's Clock Design Tool can be used to calculate divider values to achieve desired clock output frequencies. See: <http://www.ti.com/tool/codeloader/>.

## PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO or crystal resonator) for the phase noise of a "dirty" reference clock. The first PLL is typically configured with a narrow loop bandwidth in order to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference.

The loop filters on the LMK04816 evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 100 Hz), while the loop filter of PLL2 has been configured for a wide loop bandwidth (> 100 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. The following tables contain the parameters for PLL1 and PLL2 for each oscillator option.

National's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: <http://www.ti.com/tool/codeloader/>.

### PLL 1 Loop Filter

Table 4: PLL1 Loop Filter Parameters for Crystek 122.88 MHz VCXO

| 122.88 MHz VCXO PLL       |                |                        |                       |
|---------------------------|----------------|------------------------|-----------------------|
| Phase Margin              | 49°            | K $\phi$ (Charge Pump) | 100 $\mu$ A           |
| Loop Bandwidth            | 12 Hz          | Phase Detector Freq    | 1.024 MHz             |
|                           |                | VCO Gain               | 2.5 kHz/Volt          |
| Reference Clock Frequency | 122.88 MHz     | Output Frequency       | 122.88 MHz (To PLL 2) |
| Loop Filter Components    | C1_A1 = 100 nF | C2_A1 = 680 nF         | R2_A1 = 39 k $\Omega$ |

**Note:** PLL Loop Bandwidth is a function of K $\phi$ , K<sub>vco</sub>, N as well as loop components. Changing K $\phi$  and N will change the loop bandwidth.

## PLL2 Loop Filter

Table 5: PLL2 Loop Filter Parameters for LMK04816B

|                              | LMK04816B |            |
|------------------------------|-----------|------------|
| C1_A2                        | 0.047     | nF         |
| C2_A2                        | 3.9       | nF         |
| C3 (internal)                | 0         | nF         |
| C4 (internal)                | 0         | nF         |
| R2_A2                        | 0.62      | k $\Omega$ |
| R3 (internal)                | 0.2       | k $\Omega$ |
| R4 (internal)                | 0.2       | k $\Omega$ |
| Charge Pump Current, $K\phi$ | 3.2       | mA         |
| Phase Detector Frequency     | 122.88    | MHz        |
| Frequency                    | 2457.6    | MHz        |
| $Kvco$                       | 18.8      | MHz/V      |
| N                            | 20        |            |
| Phase Margin                 | 75        | degrees    |
| Loop Bandwidth               | 321       | kHz        |

**Note:** PLL Loop Bandwidth is a function of  $K\phi$ ,  $Kvco$ , N as well as loop components. Changing  $K\phi$  and N will change the loop bandwidth.

## Evaluation Board Inputs and Outputs

The following table contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable CodeLoader programming controls are noted for convenience. Refer to the LMK04816 Family Datasheet for complete register programming information.

**Table 6: Evaluation Board Inputs and Outputs**

| Connector Name                                                                                                                                                                                                                                                                                                                              | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|---------------------------|---------|---------|---------|--------|---------|---------|---------|--------|---------|----------------|---------|---------------|---------|----------------|---------|---------------|---------|----------------|---------|---------------|----------|---------|----------|--------|
| <p><u>Populated:</u><br/>CLKout0, CLKout0*,<br/>CLKout2, CLKout2*,<br/>CLKout4, CLKout4*,<br/>CLKout6, CLKout6*,<br/>CLKout8, CLKout8*,<br/>CLKout10, CLKout10*</p> <p><u>Not Populated:</u><br/>CLKout1, CLKout1*,<br/>CLKout3, CLKout3*,<br/>CLKout5, CLKout5*,<br/>CLKout7, CLKout7*,<br/>CLKout9, CLKout9*,<br/>CLKout11, CLKout11*</p> | Analog, Output            | <p>Clock outputs with programmable output buffers.</p> <p>The output terminations by default on the evaluation board are shown below, and the output type selected by default in CodeLoader is indicated by an asterisk (*):</p> <table><tr><th>Clock output pair</th><th>Default Board Termination</th></tr><tr><td>CLKout0</td><td>LVPECL*</td></tr><tr><td>CLKout1</td><td>LVPECL</td></tr><tr><td>CLKout2</td><td>LVPECL*</td></tr><tr><td>CLKout3</td><td>LVPECL</td></tr><tr><td>CLKout4</td><td>LVDS* / LVCMOS</td></tr><tr><td>CLKout5</td><td>LVDS / LVCMOS</td></tr><tr><td>CLKout6</td><td>LVDS* / LVCMOS</td></tr><tr><td>CLKout7</td><td>LVDS / LVCMOS</td></tr><tr><td>CLKout8</td><td>LVDS* / LVCMOS</td></tr><tr><td>CLKout9</td><td>LVDS / LVCMOS</td></tr><tr><td>CLKout10</td><td>LVPECL*</td></tr><tr><td>CLKout11</td><td>LVPECL</td></tr></table> <p>Each CLKout pair has a programmable LVDS, LVPECL, or LVCMOS buffer. The output buffer type can be selected in CodeLoader in the <b>Clock Outputs</b> tab via the CLKoutX_TYPE control.</p> <p>All clock outputs are AC-coupled to allow safe testing with RF test equipment.</p> <p>All LVPECL clock outputs are source-terminated using 240-ohm resistors.</p> <p>If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state).</p> | Clock output pair | Default Board Termination | CLKout0 | LVPECL* | CLKout1 | LVPECL | CLKout2 | LVPECL* | CLKout3 | LVPECL | CLKout4 | LVDS* / LVCMOS | CLKout5 | LVDS / LVCMOS | CLKout6 | LVDS* / LVCMOS | CLKout7 | LVDS / LVCMOS | CLKout8 | LVDS* / LVCMOS | CLKout9 | LVDS / LVCMOS | CLKout10 | LVPECL* | CLKout11 | LVPECL |
| Clock output pair                                                                                                                                                                                                                                                                                                                           | Default Board Termination |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout0                                                                                                                                                                                                                                                                                                                                     | LVPECL*                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout1                                                                                                                                                                                                                                                                                                                                     | LVPECL                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout2                                                                                                                                                                                                                                                                                                                                     | LVPECL*                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout3                                                                                                                                                                                                                                                                                                                                     | LVPECL                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout4                                                                                                                                                                                                                                                                                                                                     | LVDS* / LVCMOS            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout5                                                                                                                                                                                                                                                                                                                                     | LVDS / LVCMOS             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout6                                                                                                                                                                                                                                                                                                                                     | LVDS* / LVCMOS            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout7                                                                                                                                                                                                                                                                                                                                     | LVDS / LVCMOS             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout8                                                                                                                                                                                                                                                                                                                                     | LVDS* / LVCMOS            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout9                                                                                                                                                                                                                                                                                                                                     | LVDS / LVCMOS             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout10                                                                                                                                                                                                                                                                                                                                    | LVPECL*                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |
| CLKout11                                                                                                                                                                                                                                                                                                                                    | LVPECL                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                   |                           |         |         |         |        |         |         |         |        |         |                |         |               |         |                |         |               |         |                |         |               |          |         |          |        |

| Connector Name                          | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                 |                           |         |                |
|-----------------------------------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------|---------|----------------|
| <u>Populated:</u><br>OSCout0, OSCout0*, | Analog, Output            | <p>Buffered output of OSCin port.</p> <p>The output terminations on the evaluation board are shown below, the output type selected by default in CodeLoader is indicated by an asterisk (*):</p> <table><tr><th>OSC output pair</th><th>Default Board Termination</th></tr><tr><td>OSCout0</td><td>LVDS* / LVCMOS</td></tr></table> <p>Only OSCout0 has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout0 buffer type can be selected in CodeLoader on the <b>Clock Outputs</b> tab via the OSCout0_TYPE control.</p> <p>OSCout0 is AC-coupled to allow safe testing with RF test equipment.</p> <p>If OSCout0 is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state).</p> | OSC output pair | Default Board Termination | OSCout0 | LVDS* / LVCMOS |
| OSC output pair                         | Default Board Termination |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                           |         |                |
| OSCout0                                 | LVDS* / LVCMOS            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                           |         |                |
| Vcc                                     | Power, Input              | <p>Main power supply input for the evaluation board.</p> <p>A 3.9 V DC power source applied to this SMA will, by default, source the onboard LDO regulators that power the inner layer planes that supply the LMK04816B and its auxiliary circuits (e.g. VCXO).</p> <p>The LMK04816B contains internal voltage regulators for the VCO, PLL and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance.</p> <p>On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See schematics for more details.</p>                                                         |                 |                           |         |                |
| <u>Populated:</u><br>J1                 | Power, Input              | <p>Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND). Apply power to either Vcc SMA or J1, but not both.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                 |                           |         |                |
| <u>Populated:</u><br>VccVCO/Aux         | Power, Input              | <p>Optional Vcc input to power the VCO circuit if separated voltage rails are needed. The VccVCO/Aux input can power these circuits directly or supply the on-board LDO regulators. 0 Ω resistor options provide flexibility to route power.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                 |                           |         |                |

| Connector Name                   | Signal Type, Input/Output | Description                                                                                                                                                                                                                                        |
|----------------------------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <u>Populated:</u><br>VccVCXO/Aux | Power, Input              | Optional Vcc input to power the VCXO circuit if separated voltage rails are needed. The VccVCXO/Aux input can power these circuits directly or supply the on-board LDO regulators. 0 $\Omega$ resistor options provide flexibility to route power. |



| Connector Name                                                                                                                         | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |       |       |     |     |       |              |            |     |     |     |              |      |      |     |     |
|----------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-----|-----|-------|--------------|------------|-----|-----|-----|--------------|------|------|-----|-----|
| <p><u>Populated:</u><br/>CLKin0, CLKin0*,<br/>FBCLKin*/CLKin1*,<br/>CLKin2/CLKin2*</p> <p><u>Not Populated:</u><br/>FBCLKin/CLKin1</p> | Analog, Input             | <p>Reference Clock Inputs for PLL1 (CLKin0, 1, 2). CLKin1 can alternatively be used as an External Feedback Clock Input (FBCLKin) in 0-delay mode or an RF Input (Fin) in External VCO mode.</p> <p><b>Reference Clock Inputs for PLL1 (CLKin0, 1, 2)</b><br/>FBCLKin/CLKin1* is configured by default for a single-ended reference clock input from a 50-ohm source. The non-driven input pin (FBCLKin/CLKin1) is connected to GND with a 0.1 uF. CLKin0/CLKin0* is configured by default for a differential reference clock input from a 50-ohm source.</p> <p>CLKin1* is the default reference clock input selected in CodeLoader. The clock input selection mode can be programmed on the <b>Bits/Pins</b> tab via the CLKin_Select_MODE control. Refer to the LMK04816 Family Datasheet section “Input Clock Switching” for more information.</p> <p><b>AC coupled Input Clock Swing Levels</b></p> <table><tr><th>Input</th><th>Mode</th><th>Min</th><th>Max</th><th>Units</th></tr><tr><td>Differential</td><td>Bipolar or</td><td>0.5</td><td>3.1</td><td>Vpp</td></tr><tr><td>Single Ended</td><td>CMOS</td><td>0.25</td><td>2.4</td><td>Vpp</td></tr></table> <p><b>External Feedback Input (FBCLKin) for 0-Delay</b><br/>CLKin1 is shared for use with FBCLKin as an external feedback clock input to PLL1 for 0-delay mode. See section, Programming 0-Delay Mode in CodeLoader below, for more details on using 0-delay mode with the evaluation board and the evaluation board software.</p> <p><b>RF Input (Fin) for External VCO</b><br/>CLKin1 is also shared for use with Fin as an RF input for external VCO mode using the onboard VCO footprint (U3) or add-on VCO board. To enable Dual PLL mode with External VCO, the following registers must be properly configured in CodeLoader:</p> <ul style="list-style-type: none"><li>MODE = (3) Dual PLL, Ext VCO (Fin), (5) Dual PLL, Ext VCO, 0-Delay, (11) PLL2, Ext VCO (Fin)</li></ul> | Input | Mode  | Min | Max | Units | Differential | Bipolar or | 0.5 | 3.1 | Vpp | Single Ended | CMOS | 0.25 | 2.4 | Vpp |
| Input                                                                                                                                  | Mode                      | Min                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Max   | Units |     |     |       |              |            |     |     |     |              |      |      |     |     |
| Differential                                                                                                                           | Bipolar or                | 0.5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 3.1   | Vpp   |     |     |       |              |            |     |     |     |              |      |      |     |     |
| Single Ended                                                                                                                           | CMOS                      | 0.25                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 2.4   | Vpp   |     |     |       |              |            |     |     |     |              |      |      |     |     |

| Connector Name                                                                                     | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------------------------------------------------------------------------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <u>Not populated:</u><br>OSCin, OSCin*                                                             | Analog, Input             | <p>Feedback VCXO clock input to PLL1 and Reference clock input to PLL2.</p> <p>By default, these SMAs are not connected to the traces going to the OSCin/OSCin* pins of the LMK04816B. Instead, the single-ended output of the onboard VCXO (U2) drives the OSCin* input of the device and the OSCin input of the device is connected to GND with 0.1 uF.</p> <p>A VCXO add-on board may be optionally attached via these SMA connectors with minor modification to the components going to the OSCin/OSCin* pins of device. This is useful if the VCXO footprint does not accommodate the desired VCXO device.</p> <p>A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF.</p> <p>Refer to the LMK04816 Family Datasheet section “Electrical Characteristics” for PLL2 Reference Input (OSCin) specifications.</p> |
| <u>Test point:</u><br>VTUNE1_TP<br><br><u>Not populated:</u><br>Vtune1                             | Analog, Output            | <p>Tuning voltage output from the loop filter for PLL1.</p> <p>If a VCXO add-on board is used, this tuning voltage can be connected to the voltage control pin of the external VCXO when this SMA connector is installed and connected through R72 by the user.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <u>Test point:</u><br>VTUNE2_TP                                                                    | Analog, Output            | <p>Tuning voltage output from the loop filter for PLL2.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <u>Populated:</u><br>uWire<br><br><u>Test points:</u><br>DATAuWire_TP<br>CLKuWIRE_TP<br>LEuWIRE_TP | CMOS, Input/Output        | <p>10-pin header for uWire programming interface and programmable logic I/O pins for the LMK04816B.</p> <p>The uWire interface includes CLKuWire, DATAuWire, and LEuWire signals.</p> <p>The programmable logic I/O signals accessible through this header include: SYNC, Status_Holdover, Status_LD, Status_CLKin0, and Status_CLKin1. These logic I/O signals also have dedicated SMAs and test points.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| Connector Name                                                                         | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------------------------------------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><u>Test point:</u><br/>LD_TP</p> <p><u>Not populated:</u><br/>Status_LD</p>         | CMOS, Output              | <p>Programmable status output pin. By default, set to output the digital lock detect status signal for PLL1 and PLL2 combined.</p> <p>In the default CodeLoader modes, LED D5 will illuminate green when PLL lock is detected by the LMK04816B (output is high) and turn off when lock is lost (output is low).</p> <p>The status output signal for the Status_LD pin can be selected on the <b>Bits/Pins</b> tab via the LD_MUX control.</p> <p>Refer to the LMK04816 Family Datasheet section “Status Pins” and “Digital Lock Detect” for more information.</p> <p>Note: Before a high-frequency internal signal (e.g. PLL divider output signal) is selected by LD_MUX, it is suggested to first remove the 270 ohm resistor to prevent the LED from loading the output.</p> |
| <p><u>Test point:</u><br/>Holdover_TP</p> <p><u>Not populated:</u><br/>Status_Hold</p> | CMOS, Output              | <p>Programmable status output pin. By default, set to the output holdover mode status signal.</p> <p>In the default CodeLoader mode, LED D8 will illuminate red when holdover mode is active (output is high) and turn off when holdover mode is not active (output is low).</p> <p>The status output signal for the Status_Holdover pin can be selected on the <b>Bits/Pins</b> tab via the HOLDOVER_MUX control.</p> <p>Refer to the LMK04816 Family Datasheet section “Status Pins” and “Holdover Mode” for more information.</p> <p>Note: Before a high-frequency internal signal (e.g. PLL divider output signal) is selected by HOLDOVER_MUX, it is suggested to first remove the 270 ohm resistor to prevent the LED from loading the output.</p>                        |

| Connector Name                                                                                                    | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
|-------------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|--------------|---|---|--------|---|---|--------|---|---|----------|---|---|----------|---------------|---------------|--------------|---|---|--------|---|---|--------|---|---|----------|
| <p>Test point:<br/>CLKin0_SEL_TP<br/>CLKin1_SEL_TP</p> <p>Not populated:<br/>Status_CLKin0,<br/>Status_CLKin1</p> | CMOS,<br>Input/Output     | <p>Programmable status I/O pins. By default, set as input pins for controlling input clock switching of CLKin0 and CLKin1.</p> <p>These inputs will not be functional because CLKin_Select_MODE is set to 0 (CLKin0 Manual) by default in the <b>Bits/Pins</b> tab in CodeLoader. To enable input clock switching, CLKin_Select_MODE must be 3 or 6 and Status_CLKinX_TYPE must be 0 to 3 (pin enabled as an input).</p> <p><b>Input Clock Switching – Pin Select Mode</b><br/>When CLKin_SELECT_MODE is 3, the Status_CLKinX pins select which clock input is active as follows:</p> <table> <tr> <th>Status_CLKin1</th><th>Status_CLKin0</th><th>Active Clock</th></tr> <tr> <td>0</td><td>0</td><td>CLKin0</td></tr> <tr> <td>0</td><td>1</td><td>CLKin1</td></tr> <tr> <td>1</td><td>0</td><td>Reserved</td></tr> <tr> <td>1</td><td>1</td><td>Holdover</td></tr> </table> <p><b>Input Clock Switching – Auto with Pin Select</b><br/>When CLKin_SELECT_MODE is 6, the active clock is selected using the Status_CLKinX pins upon an input clock switch event as follows:</p> <table> <tr> <th>Status_CLKin1</th><th>Status_CLKin0</th><th>Active Clock</th></tr> <tr> <td>X</td><td>0</td><td>CLKin0</td></tr> <tr> <td>1</td><td>0</td><td>CLKin1</td></tr> <tr> <td>0</td><td>0</td><td>Reserved</td></tr> </table> <p>Refer to the LMK04816 Family Datasheet section “Input Clock Switching” for more information.</p> <p><b>Status Outputs</b><br/>When Status_CLKinX_TYPE is 3 to 6 (pin enabled as an output), the status output signal for the corresponding Status_CLKinX pin can be programmed on the <b>Bits/Pins</b> tab via the Status_CLKinX_MUX control.</p> <p>Refer to the LMK04816 Family Datasheet section “Status Pins” for more information.</p> | Status_CLKin1 | Status_CLKin0 | Active Clock | 0 | 0 | CLKin0 | 0 | 1 | CLKin1 | 1 | 0 | Reserved | 1 | 1 | Holdover | Status_CLKin1 | Status_CLKin0 | Active Clock | X | 0 | CLKin0 | 1 | 0 | CLKin1 | 0 | 0 | Reserved |
| Status_CLKin1                                                                                                     | Status_CLKin0             | Active Clock                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| 0                                                                                                                 | 0                         | CLKin0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| 0                                                                                                                 | 1                         | CLKin1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| 1                                                                                                                 | 0                         | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| 1                                                                                                                 | 1                         | Holdover                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| Status_CLKin1                                                                                                     | Status_CLKin0             | Active Clock                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| X                                                                                                                 | 0                         | CLKin0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| 1                                                                                                                 | 0                         | CLKin1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |
| 0                                                                                                                 | 0                         | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |               |              |   |   |        |   |   |        |   |   |          |   |   |          |               |               |              |   |   |        |   |   |        |   |   |          |

| Connector Name                                                              | Signal Type, Input/Output | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------------------------------------------------------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><u>Test point:</u><br/>SYNC_TP</p> <p><u>Not populated:</u><br/>SYNC</p> | CMOS, Input/Output        | <p>Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect.</p> <p>In the default CodeLoader mode, SYNC will asserted when the SYNC pin is low and the outputs to be synchronized will be held in a logic low state. When SYNC is unasserted, the clock outputs to be synchronized are activated and will be initially phase aligned with each other except for outputs programmed with different digital delay values.</p> <p>A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the <b>Bits/Pins</b> tab in CodeLoader.</p> <p>Refer to the LMK04816 Family Datasheet section “Clock Output Synchronization” for more information.</p> <p><b>Status Output</b><br/>When SYNC_MUX is 3 to 6 (pin enabled as output), a status signal for the SYNC pin can be selected on the <b>Bits/Pins</b> tab via the SYNC_MUX control.</p> |

## Recommended Test Equipment

### **Power Supply**

The Power Supply should be a low noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

### **Phase Noise / Spectrum Analyzer**

To measure phase noise and RMS jitter, an Agilent E5052 Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

### **Oscilloscope**

To measure the output clocks for AC performance, such as rise time or fall time, propagation delay, or skew, it is suggested to use a real-time oscilloscope with at least 1 GHz analog input bandwidth (2.5+ GHz recommended) with 50 ohm inputs and 10+ Gsps sample rate. To evaluate clock synchronization or phase alignment between multiple clock outputs, it's recommended to use phase-matched, 50-ohm cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

## Programming 0-Delay Mode in CodeLoader

### Overview

When enabling the 0-Delay mode the feedback path of the VCO is altered to include a clock output. See the datasheet for more details on 0-Delay functionality.

The current version of the CodeLoader software does not include this extra divider in the frequency calculations when in holdover mode. To successfully lock the LMK04816 device in a 0-Delay mode the user must program the device “manually” account for this divider. Programming “manually” means that the VCO frequency and therefore the clock output frequencies displayed by the CodeLoader software may be incorrect. For the LMK04816 device to lock properly the **divider values** must be programmed correctly. The frequencies displayed in the application are only for the benefit of the user and for proper automatic programming of the OSCin\_FREQ register which will not be affected by 0-Delay.

When using the device in Dual Loop mode vs. Single Loop mode different procedures are used to cause the device to lock when using the CodeLoader software. The following two sections describe the process for when the LMK04816 device is programmed for a Dual Loop mode and Single Loop mode respectively. Each section contains a brief introduction, the programming steps to execute to make the device lock, and finally a detailed section discussing the workaround and some example cases.

### Dual Loop 0-Delay Mode Examples

In Dual Loop 0-Delay Modes, MODE = 2 or MODE = 5, the feedback from the VCXO of PLL1 to the PLL1 N divider is broken and a clock output will drive the PLL1 N divider. This permits phase alignment between the clock output and the clock input (0-Delay). As such, the PLL1\_N and PLL1\_R divide values may need to be adjusted to permit the LMK04816 to lock.

### Programming Steps

1. Program a Dual Loop 0-Delay mode.
2. Enable the feedback mux. EN\_FEEDBACK\_MUX = 1.
3. Select clock output for feedback with the feedback mux. FEEDBACK\_MUX = User value.
4. Program the VCXO (VCO) frequency of PLL1 tab to the clock output frequency selected by the feedback mux.

If for any reason the CLKout frequency is less than the phase detector frequency, the PLL1 R divider must be increased so that the phase detector is at the same or lower value than the CLKout frequency.

### Details

When using the CodeLoader software in Dual Loop 0-Delay mode, programming the VCXO (VCO) frequency of the PLL1 tab to the frequency of the fed back output clock will re-program the PLL1 N divider to allow the LMK04816 will be able to lock. The PLL1 loop has been altered and actual VCXO no longer directly feeds into PLL1 N divider. The VCXO is only used

by the reference input of PLL2 now. The PLL2 reference frequency will remain at the VCXO frequency.

When the PLL1 VCXO frequency is different from the PLL2 reference frequency, a warning will be displayed on the clock outputs tab informing the user that PLL1 VCO and PLL2 reference frequency are mismatched and the one or more of the PLLs are out of lock. While there still could be an error in the divider values which may cause a non-locked PLL, this warning by itself may no longer be assumed true. It is up to the user to ensure the PLL dividers are programmed correctly.

To illustrate the proper programming of the LMK04816 device in dual loop 0-delay mode the following case examples are provided. Note that in one of the cases, the feedback frequency from the clock output matches the VCXO frequency and CodeLoader will display the proper frequency values.

Dual Loop 0-Delay (MODE=2 or 5) Case 1: For example the default configuration, 122.88 MHz CLKIn, 122.88 MHz VCXO, of the LMK04816 has the following register programming.

|                                      | Case 1:<br>Default Mode<br><br>No 0-Delay | Case2:<br>Default 0-Delay<br>Mode<br>(CLKout8 =<br>122.88 MHz) | Case 3:<br>Default 0-Delay<br>Mode (Updated<br>CLKout8 =<br>245.76 MHz) | Case 4:<br>Default 0-Delay<br>Mode (Updated<br>CLKout8 =<br>61.44 MHz) |
|--------------------------------------|-------------------------------------------|----------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------|
| Actual PLL1<br>VCXO Frequency        | 122.88                                    | 122.88                                                         | 122.88                                                                  | 122.88                                                                 |
| Reported PLL1<br>VCXO Frequency      | 122.88                                    | 122.88                                                         | <b>61.44</b>                                                            | <b>245.76</b>                                                          |
| PLL1 N                               | 120                                       | 120                                                            | 60                                                                      | 240                                                                    |
| Actual PLL2<br>VCO Frequency         | 2949.12 MHz                               | 2949.12 MHz                                                    | 2949.12 MHz                                                             | 2949.12 MHz                                                            |
| Reported PLL2<br>VCO Frequency       | 2949.12 MHz                               | 2949.12 MHz                                                    | 2949.12 MHz                                                             | 2949.12 MHz                                                            |
| PLL2_N                               | 12                                        | 12                                                             | 12                                                                      | 12                                                                     |
| PLL2_P (Pre-N)                       | 2                                         | 2                                                              | 2                                                                       | 2                                                                      |
| PLL2 VCO Divider                     | Bypassed                                  | Bypassed                                                       | Bypassed                                                                | Bypassed                                                               |
| CLKout8 Divide                       | 12                                        | 24                                                             | 12                                                                      | 48                                                                     |
| Actual CLKout8<br>Output Frequency   | <b>245.76 MHz</b>                         | <b>122.88 MHz</b>                                              | <b>245.76 MHz</b>                                                       | <b>61.44 MHz</b>                                                       |
| Reported CLKout8<br>Output Frequency | 245.76 MHz                                | 122.88 MHz                                                     | 245.76 MHz                                                              | 61.44 MHz                                                              |



## Single Loop 0-Delay Mode Examples

In Single Loop 0-Delay Mode,  $MODE = 8$ , the feedback from the VCO of PLL2 to the PLL2\_P/PLL2\_N divider is broken and a fed back clock output will drive the PLL2\_N divider directly. This permits phase alignment between the clock output and the OSCin input (0-Delay). As such, the PLL2\_N, PLL2\_R, and PLL2\_N\_CAL divide values may need to be adjusted to permit the LMK04816 to lock.

### Programming Steps

1. Program the Single Loop 0-Delay mode.
2. Enable the feedback mux.  $EN\_FEEDBACK\_MUX = 1$ .
3. Select clock output for feedback with the feedback mux.  $FEEDBACK\_MUX = \text{User value}$ .
4. Program the VCO frequency of PLL2 tab to: The actual VCO frequency \* PLL2\_P / (which is PLL2 PreN) / CLKout Divider.
  - Entered CodeLoader 4 VCO Frequency = Actual VCO Frequency \* PLL2\_P / CLKout Divider.
5. Updated the PLL2\_N\_CAL register on the Bits/Pins tab to the N value when in non-0-Delay mode.
6. Press Ctrl-L to cause all registers to be programmed.
  - The reason is to cause the programming of register R30 to start the VCO calibration routine now that the proper PLL2\_N\_CAL value is programmed.
  - PLL2\_N\_CAL value is automatically updated when a new VCO frequency is entered and the PLL2\_N value is calculated. In this case the VCO frequency entered is wrong and the PLL2\_N\_CAL value will be incorrect.

If for any reason the CLKout frequency is less than the phase detector frequency, the PLL2\_R divider must be increased so that the phase detector is at the same or lower value than the CLKout frequency.

### Details

The 0-Delay mode for Single Loop mode is more complicated to program than for Dual Loop mode in part because of the PLL2\_N\_CAL register. When performing the VCO calibration the device uses PLL2\_N\_CAL for in non-0-Delay mode. Once the VCO is calibrated the device enters 0-Delay mode. For more information on the PLL programming equations, refer to PLL PROGRAMMING in the applications section of the datasheet.

In Table 7 case 1 illustrates the register programming when not using 0-Delay.

Case 2 shows 0-Delay with a clock out divider of 2. Since  $PLL2\_P = 2$ , this substitution of which circuit is performing the divide by two results in no impact on the software. All the values display correctly.

Case 3 shows 0-Delay mode with a CLKout divider not equal to the PLL2\_P value. So the proper frequency to program in the VCO to lock the VCO to 2949.12 MHz will be 491.52 MHz. This is calculated by Actual VCO Frequency \* PLL2\_P / CLKoutX\_Y\_DIV.

Case 4 shows 0-Delay mode with CLKout divider not equal to the PLL2\_P value; however the CLKout frequency will be less than the current phase detector frequency. This requires PLL2\_R to be increased from a value of 1 to 2 to reduce the PLL2 phase detector frequency from 122.88 MHz to 61.44 MHz. Now the adjusted VCO frequency can be programmed to allow PLL2 to lock.

In any case where the actual VCO frequency and the display VCO frequency are not equal the user is required to manually update the PLL2\_N\_CAL register with the PLL2\_N value to be used as if the device were operating in the non-0-Delay mode. Once this update has been performed, Ctrl-L will reload the part and cause the VCO calibration to occur with the proper PLL2\_N\_CAL value.

**Table 7 - Single PLL 0-Delay Operation Examples**

|                                      | Case 1:<br>Default Mode<br><br>No 0-Delay | Case 2:<br>Default 0-Delay<br>Mode<br>(CLKout8 =<br>1474.56 MHz) | Case 3:<br>Default 0-Delay<br>Mode (Updated<br>CLKout8 =<br>245.76 MHz) | Case 4:<br>Default 0-Delay<br>Mode (Updated<br>CLKout8 =<br>61.44 MHz) |
|--------------------------------------|-------------------------------------------|------------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------|
| Actual PLL2<br>VCO Frequency         | 2949.12 MHz                               | 2949.12 MHz                                                      | 2949.12 MHz                                                             | 2949.12 MHz                                                            |
| Reported PLL2<br>VCO Frequency       | 2949.12 MHz                               | 2949.12 MHz                                                      | <b>491.52 MHz</b>                                                       | <b>122.88 MHz</b>                                                      |
| <b>PLL2_R</b>                        | 1                                         | 1                                                                | 1                                                                       | <b>2</b>                                                               |
| <b>PLL2_N</b>                        | 12                                        | 12                                                               | <b>2</b>                                                                | <b>1</b>                                                               |
| <b>PLL2_N_CAL</b>                    | <b>12</b>                                 | <b>12</b>                                                        | <b>12</b>                                                               | <b>24</b>                                                              |
| PLL2_P (Pre-N)                       | 2                                         | 2                                                                | 2                                                                       | 2                                                                      |
| PLL2 VCO Divider                     | Bypassed                                  | Bypassed                                                         | Bypassed                                                                | Bypassed                                                               |
| CLKout8 Divide                       | 12                                        | 2                                                                | 12                                                                      | 48                                                                     |
| Actual CLKout8<br>Output Frequency   | <b>245.76</b>                             | <b>1474.56 MHz</b>                                               | <b>245.76 MHz</b>                                                       | <b>61.44 MHz</b>                                                       |
| Reported CLKout8<br>Output Frequency | 245.76                                    | 1474.56 MHz                                                      | <b>40.96 MHz</b>                                                        | <b>2.56 MHz</b>                                                        |

## Appendix A: CodeLoader Usage

Code Loader is used to program the evaluation board with either an LPT port using the included CodeLoader cable or with a USB port using the optional USB-to-uWire cable available from <http://store.ti.com/>. The part number is USB2UWIRE-IFACE.

### Port Setup Tab

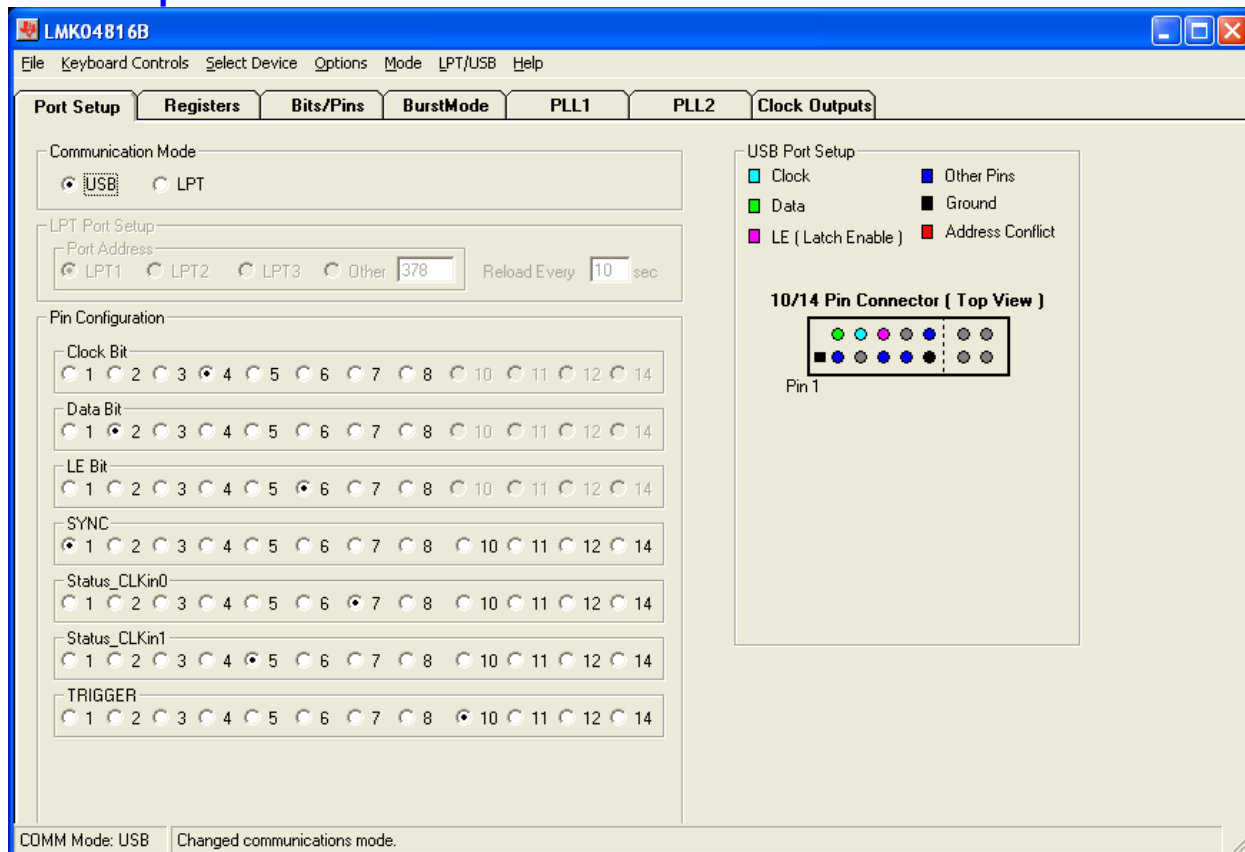


Figure 8: Port Setup tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

The Pin Configuration field is hardware dependent and normally **does not** need to be changed by the user. Figure 8 shows the default settings.

## Clock Outputs Tab

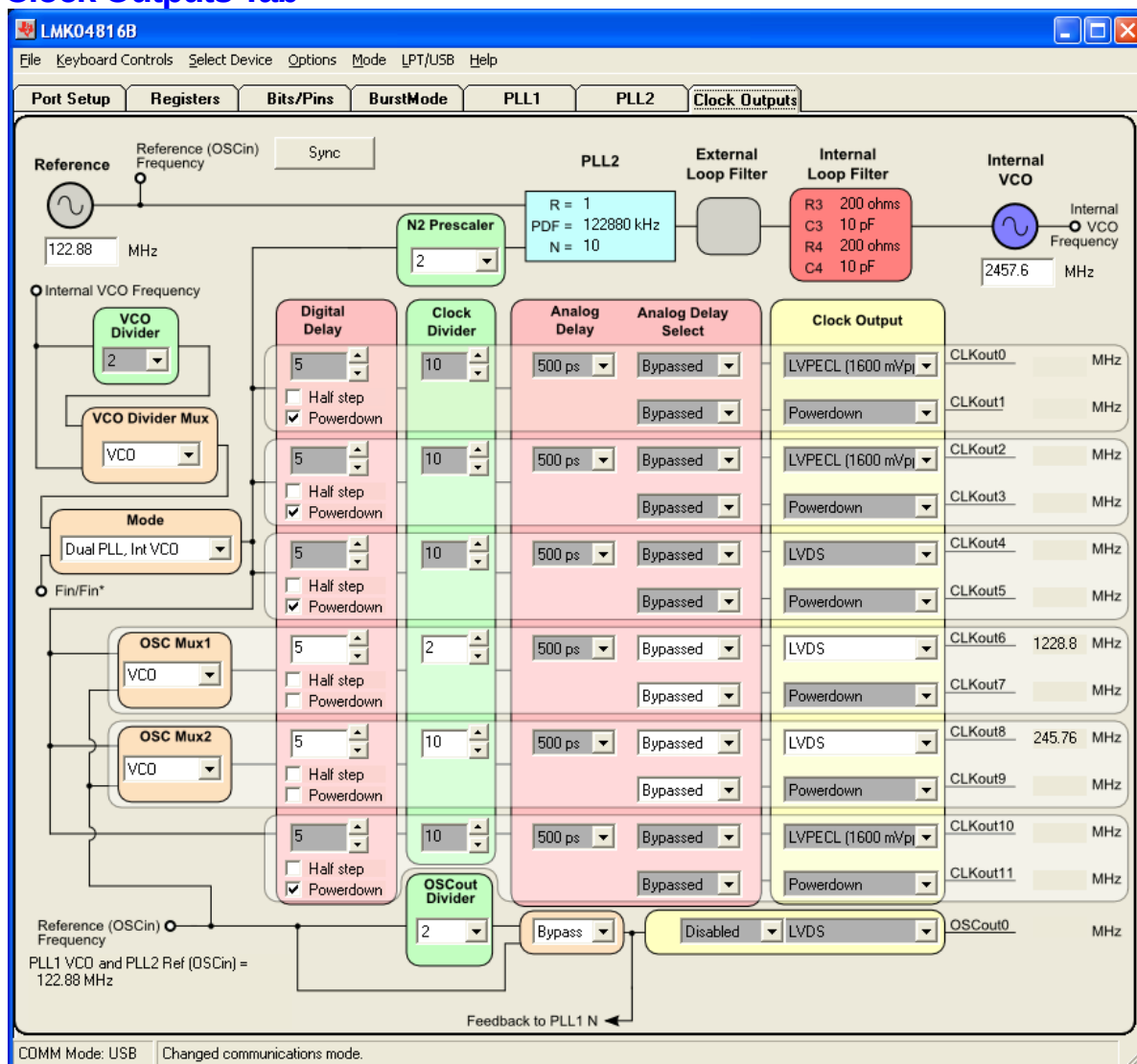


Figure 9: Clock Outputs tab

The **Clock Outputs** tab allows the user to control the output channel blocks, including:

- Clock Group Source from either VCO or OSCin (via OSC Mux1 and OSC Mux2)
- Channel Powerdown (affects digital and analog delay, clock divider, and buffer blocks)
- Digital Delay value and Half Step
- Clock Divide value
- Analog Delay value and Delay bypass/enable (per output)
- Clock Output format (per output)

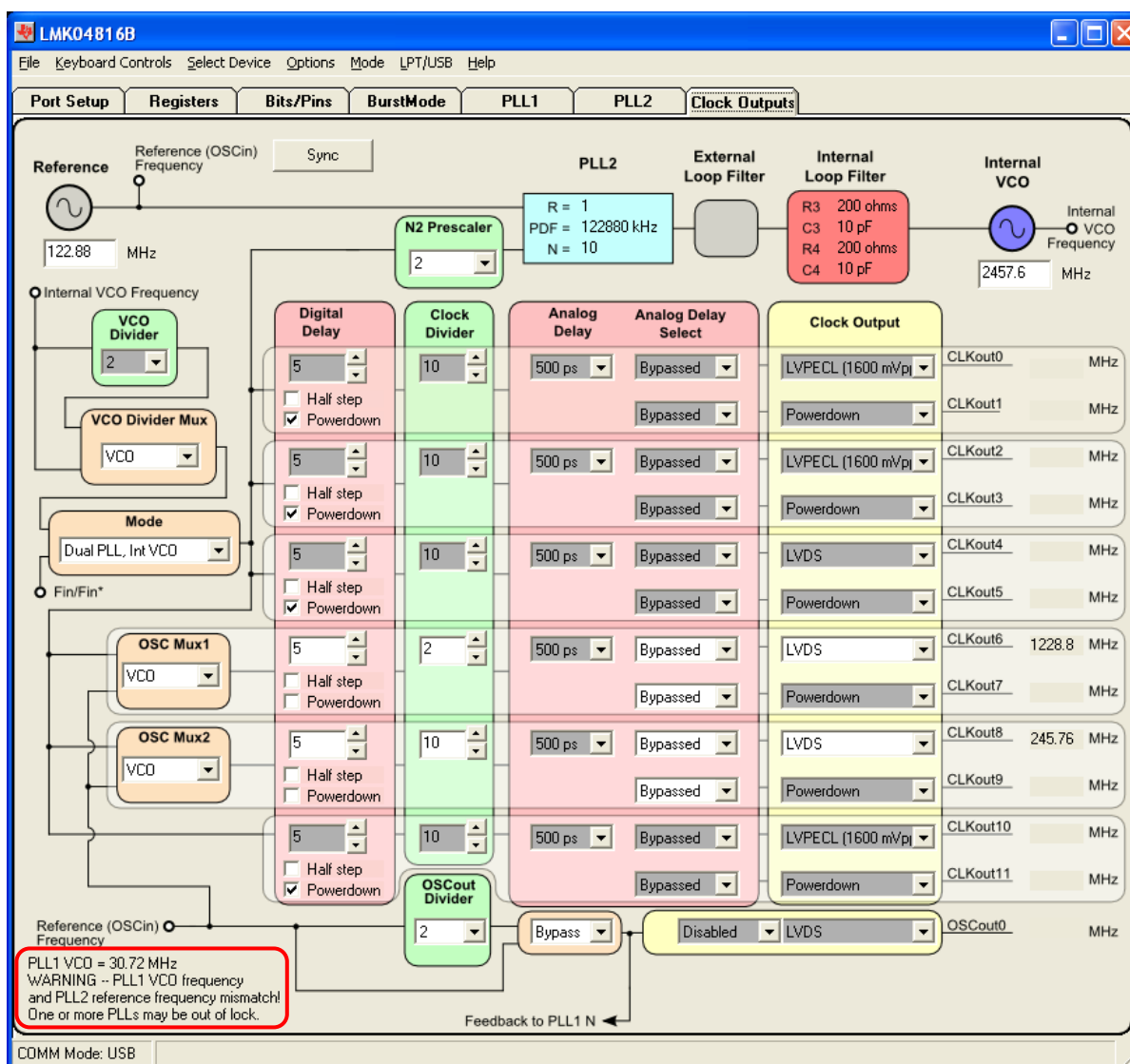
This tab also allows the user to select the VCO Divider value (2 to 8). Note that the *total* PLL2 N divider value is the product of the VCO Divider value and the PLL N Prescaler and N Counter values (shown in the **PLL2** tab), and is given by:

$$\text{PLL2 N Total} = \text{VCO Divider} * \text{PLL2 N Prescaler} * \text{PLL2 N Counter}$$

Clicking on the cyan-colored PLL2 block that contains R, PDF and N values will bring the **PLL2** tab into focus where these values may be modified, if needed.

Clicking on the values in the box containing the Internal Loop Filter component (R3, C3, R4, C4) allow one to step through the possible values. Left click to increase the component value, and right click to decrease the value. These values can also be changed in the **Bits/Pins** tab.

The Reference Oscillator value field may be changed in either the **Clock Outputs** tab or the **PLL2** tab. The PLL2 Reference frequency should match the frequency of the onboard VCXO or Crystal (i.e. VCO frequency in the **PLL1** tab); if not, a warning message will appear to indicate that the PLL(s) may be out of lock, as highlighted by the red box in Figure 10.



**Figure 10: Warning message indicating mismatch between PLL1 VCO frequency (30.72MHz) and PLL2 reference frequency (122.88 MHz)**

## PLL1 Tab

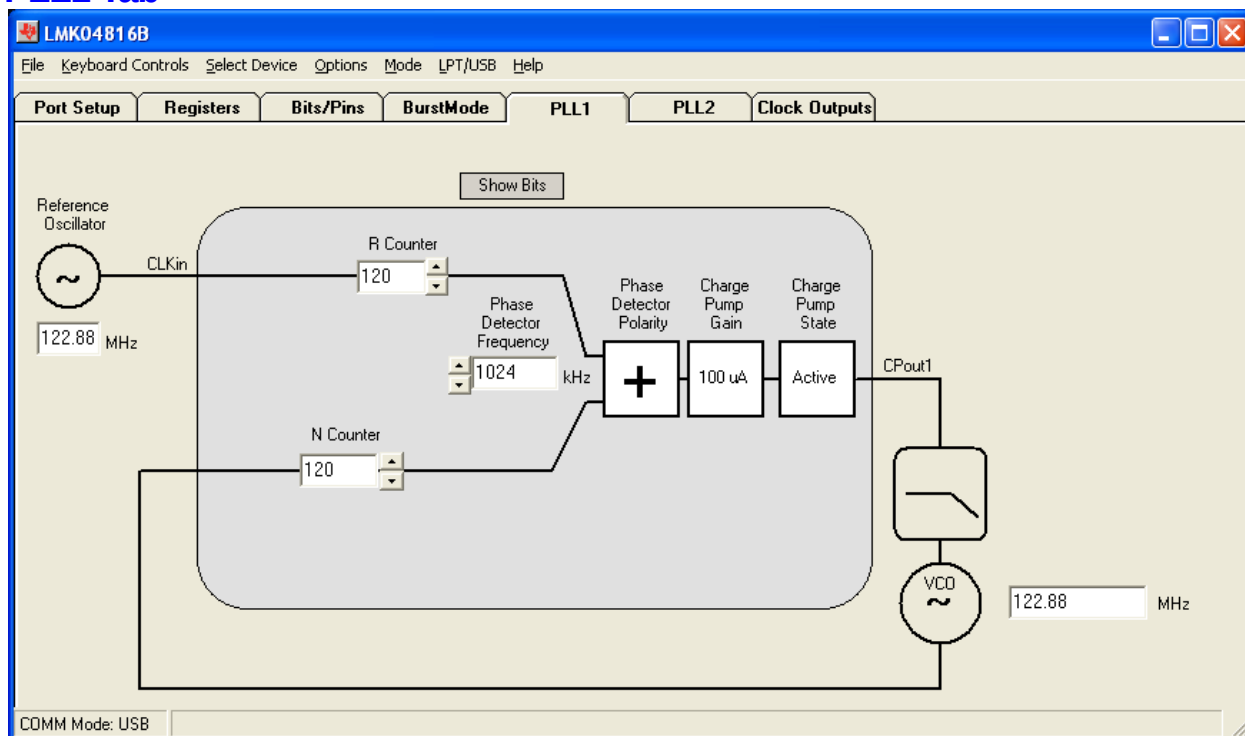


Figure 11: PLL1 tab

The PLL1 tab allows the user to change the following parameters in Table 8.

Table 8: Registers Controls and Descriptions in PLL1 tab

| Control Name                         | Register Name | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reference Oscillator Frequency (MHz) | n/a           | CLKin frequency of the selected reference clock.                                                                                                                                                                                                                                                                                                                                                                    |
| Phase Detector Frequency (MHz)       | n/a           | PLL1 Phase Detector Frequency (PDF). This value is calculated as:<br>$\text{PLL1 PDF} = \text{CLKin Frequency} / (\text{PLL1\_R} * \text{CLKinX\_PreR\_DIV})$ where CLKinX_PreR_DIV is the predivider value of the selected input clock.                                                                                                                                                                            |
| VCO Frequency (MHz)                  | n/a           | The VCO Frequency should be the OSCin frequency, except when operating in Dual PLL with 0-delay feedback. This value is calculated as:<br>$\text{VCO Freq (OSCin freq)} = \text{PLL1 PDF} * \text{PLL1\_N}$ In Dual PLL mode with 0-delay feedback, the VCO frequency should be set to the feedback clock input frequency. See the section Setting the PLL1 VCO Frequency and PLL2 Reference Frequency for details. |
| R Counter                            | PLL1_R        | PLL1 R Counter value (1 to 16383).                                                                                                                                                                                                                                                                                                                                                                                  |

|                         |              |                                                                                                                  |
|-------------------------|--------------|------------------------------------------------------------------------------------------------------------------|
| N Counter               | PLL1_N       | PLL1 N Counter value (1 to 16383).                                                                               |
| Phase Detector Polarity | PLL1_CP_POL  | PLL1 Phase Detector Polarity.<br>Click on the polarity sign to toggle polarity “+” or “-”.                       |
| Charge Pump Gain        | PLL1_CP_GAIN | PLL1 Charge Pump Gain.<br>Left-click/right-click to increase/decrease charge pump gain (100, 200, 400, 1600 uA). |
| Charge Pump State       | PLL1_CP_TRI  | PLL1 Charge Pump State.<br>Click to toggle between Active and Tri-State.                                         |

## Setting the PLL1 VCO Frequency and PLL2 Reference Frequency

When operating in Dual PLL mode without 0-delay feedback, the VCO frequency value on the **PLL1** tab must match the Reference Oscillator (OSCin) frequency value on the **PLL2** tab; otherwise, the one or both PLLs may be out of lock. Updating the Reference Oscillator frequency on the **PLL2** tab will automatically update the value of OSCin\_FREQ on the **Bits/Pins** tab.

However, when operating in Dual PLL mode with 0-delay feedback, it may be valid for the VCO frequency value on the **PLL1** tab to be different from the Reference Oscillator (OSCin) frequency value on the **PLL2** tab. This is because in 0-delay mode, the PLL1 feedback clock is taken from an output clock instead of the OSCin clock. For example, if the CLKin frequency (to PLL1\_R) is 30.72 MHz, the 0-delay feedback clock frequency (to PLL1\_N) is 30.72 MHz, and the VCXO frequency is 122.88 MHz, then the VCO frequency value on the **PLL1** tab should be 30.72 MHz (0-delay feedback frequency) and the Reference Oscillator frequency value on the **PLL2** tab should be 122.88 MHz (VCXO frequency). Because of the mismatched frequencies, a warning message will indicate this condition on the **Clock Outputs** tab but may be disregarded in a case like this.

## PLL2 Tab

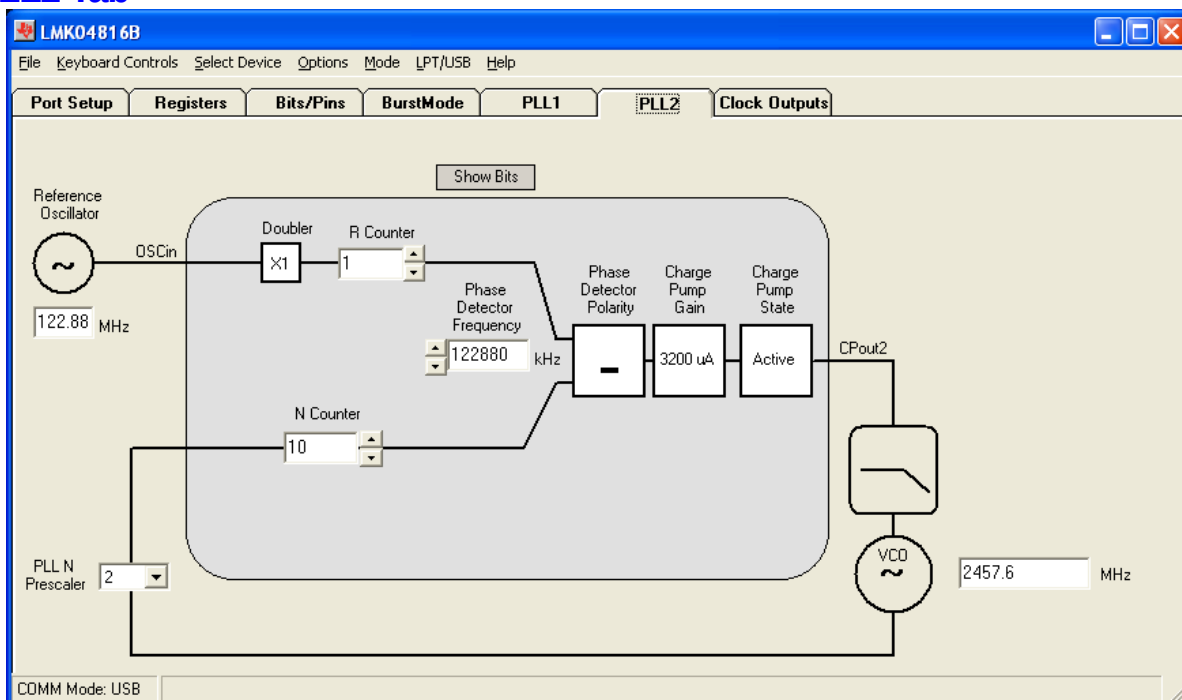


Figure 12: PLL2 tab

The PLL2 tab allows the user to change the following parameters in Table 9.

Table 9: Registers Controls and Descriptions in PLL2 tab

| Control Name                         | Register Name  | Description                                                                                                                                                                                                                      |
|--------------------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reference Oscillator Frequency (MHz) | OSCin_FREQ     | OSCin frequency from the External VCXO or Crystal.                                                                                                                                                                               |
| Phase Detector Frequency (MHz)       | n/s            | PLL2 Phase Detector Frequency (PDF). This value is calculated as:<br>$\text{PLL2 PDF} = \text{OSCin Frequency} * (2^{\text{EN\_PLL2\_REF\_2X}}) / \text{PLL2\_R}.$                                                               |
| VCO Frequency (MHz)                  | n/a            | Internal VCO Frequency should be within the allowable range of the LMK04816B device.<br>This value is calculated as:<br>$\text{VCO Frequency} = \text{PLL2 PDF} * (\text{PLL2\_N} * \text{PLL2\_P} * \text{VCO divider value}).$ |
| Doubler                              | EN_PLL2_REF_2X | PLL2 Doubler.<br>0 = Bypass Doubler<br>1 = Enable Doubler                                                                                                                                                                        |
| R Counter                            | PLL2_R         | PLL2 R Counter value (1 to 4095).                                                                                                                                                                                                |
| N Counter                            | PLL2_N         | PLL2 N Counter value (1 to 262143).                                                                                                                                                                                              |
| PLL N Prescaler                      | PLL2_P         | PLL2 N Prescaler value (2 to 8).                                                                                                                                                                                                 |



|                         |              |                                                                                                                   |
|-------------------------|--------------|-------------------------------------------------------------------------------------------------------------------|
| Phase Detector Polarity | PLL2_CP_POL  | PLL2 Phase Detector Polarity.<br>Click on the polarity sign to toggle polarity “+” or “-”.                        |
| Charge Pump Gain        | PLL2_CP_GAIN | PLL2 Charge Pump Gain.<br>Left-click/right-click to increase/decrease charge pump gain (100, 400, 1600, 3200 uA). |
| Charge Pump State       | PLL2_CP_TRI  | PLL2 Charge Pump State.<br>Click to toggle between Active and Tri-State.                                          |

Changes made on this tab will be reflected in the **Clock Outputs** tab. The VCO Frequency should conform to the specified internal VCO frequency range for the LMK04816B device (per Table 2).

## Bits/Pins Tab

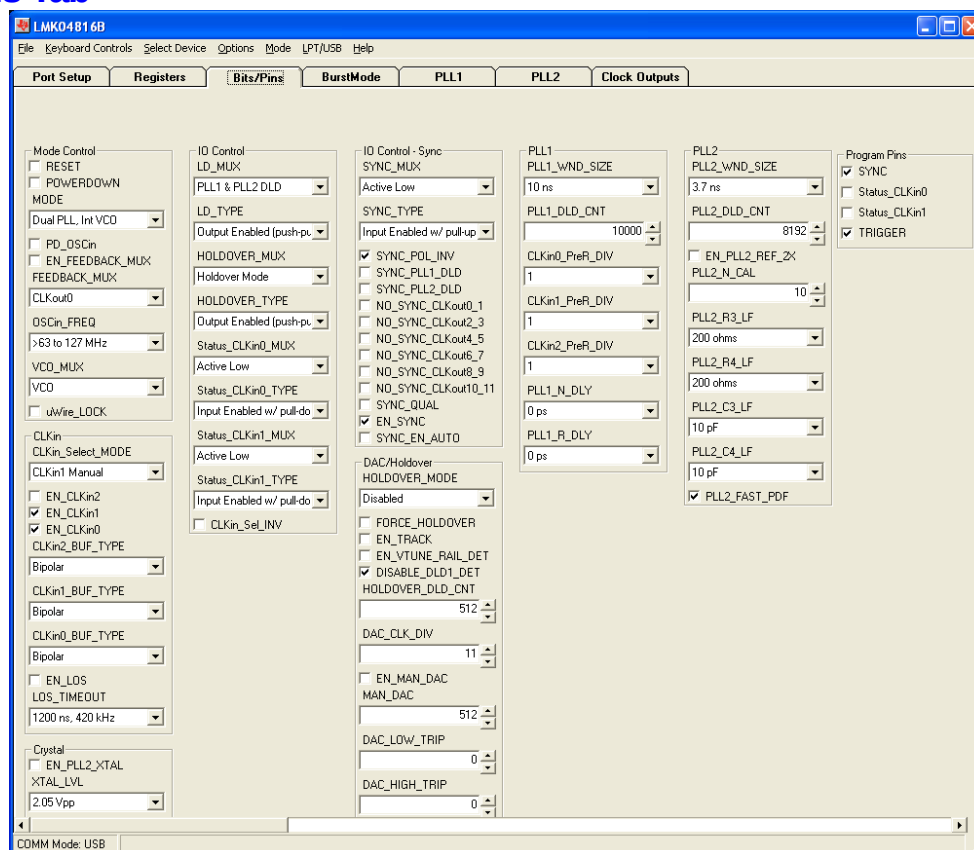


Figure 13: Bits/Pins tab

The **Bits/Pins** tab allows the user to program bits directly, many of which are not available on other tabs. Brief descriptions for the controls on this tab are provided in Table 10 to supplement the datasheet. Refer to the LMK04816 Family Datasheet for more information.

**TIP:** Right-clicking any register name in the **Bits/Pins** tab will display a Help prompt with the register address, data bit location/length, and a brief register description.

**Table 10: Register Controls and Descriptions on Bits/Pins tab**

| Group        | Register Name     | Description                                                                                                                                                                                                                                        |
|--------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Mode Control | RESET             | Resets the device to default register values. RESET must be cleared for normal operation to prevent an unintended reset every time R0 is programmed.                                                                                               |
|              | POWERDOWN         | Places the device in powerdown mode.                                                                                                                                                                                                               |
|              | MODE              | Selects the operating mode (topology) for the LMK04816 device.                                                                                                                                                                                     |
|              | PD_OSCin          | Powers down the OSCin buffer. For use in Clock Distribution mode if OSCin path is not used.                                                                                                                                                        |
|              | FEEDBACK_MUX      | Selects the feedback source for 0-delay mode.                                                                                                                                                                                                      |
|              | OSCin_FREQ        | Must be set to the OSCin frequency range for PLL2. Used for proper operation of the internal VCO calibration routine.<br>Entering a reference oscillator frequency on PLL2 tab will automatically update OSCin_FREQ to the proper frequency range. |
|              | VCO_MUX           | Selects between VCO and VCO divider to drive the clock distribution path. The VCO divider is only valid if MODE is selecting the Internal VCO.                                                                                                     |
|              | uWire_LOCK        | When checked, no other uWire programming will have effect. Must be unchecked to enable uWire programming of registers R0 to R30.                                                                                                                   |
| CLKin        | CLKin_Select_MODE | Selects operational mode for how the device selects the reference clock for PLL1.                                                                                                                                                                  |
|              | EN_CLKin1         | Enables CLKin1 as a usable reference input during auto switching mode.                                                                                                                                                                             |
|              | EN_CLKin0         | Enables CLKin0 as a usable reference input during auto switching mode.                                                                                                                                                                             |
|              | EN_CLKin2         | Enables CLKin2 as a usable reference input during auto switching mode.                                                                                                                                                                             |
|              | CLKinX_BUF_TYPE   | Selects the CLKinX input buffer to Bipolar (internal 0 mV offset) or MOS (internal 55 mV offset).                                                                                                                                                  |
|              | EN_LOS            | Enable the Loss-Of-Signal (LOS) detect circuitry.                                                                                                                                                                                                  |
|              | LOS_TIMEOUT       | Sets the timeout value for the LOS detect circuitry to assert a loss of signal state on a clock input.                                                                                                                                             |
| Crystal      | EN_PLL2_XTAL      | Enables Crystal Oscillator                                                                                                                                                                                                                         |
|              | XTAL_LVL          | Sets peak amplitude on the tunable crystal. Values listed are for a 20.48 MHz crystal.                                                                                                                                                             |
| IO Control   | LD_MUX            | Sets the selected signal on the Status_LD pin.                                                                                                                                                                                                     |
|              | LD_TYPE           | Sets I/O pin type on the Status_LD pin.                                                                                                                                                                                                            |
|              | HOLDOVER_MUX      | Sets the selected signal on the Status_HOLDOVER pin.                                                                                                                                                                                               |

|                   |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                   | HOLDOVER_TYPE      | Sets I/O pin type on the Status_Holdover pin.                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                   | Status_CLKin0_MUX  | Sets the selected signal on the Status_CLKin0 pin.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                   | Status_CLKin0_TYPE | Sets I/O pin type on the Status_CLKin0 pin.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                   | Status_CLKin1_MUX  | Sets the selected signal on the Status_CLKin1 pin.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                   | Status_CLKin1_TYPE | Sets I/O pin type on the Status_CLKin1 pin.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                   | CLKin_Sel_INV      | Inverts the Status_CLKin0/1 pin polarity when set to an input type. Significant when CLKin_SELECT_MODE is 3 or 6.                                                                                                                                                                                                                                                                                                                                                            |
| IO Control – Sync | SYNC_MUX           | Sets the selected signal on the SYNC pin.                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                   | SYNC_TYPE          | Sets I/O pin type on the SYNC pin.                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                   | SYNC_POL_INV       | Sets polarity on SYNC input to active low when checked. Toggling this bit will initiate a SYNC event.                                                                                                                                                                                                                                                                                                                                                                        |
|                   | SYNC_PLL1_DLD      | Engage SYNC mode until PLL1 DLD is true                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                   | SYNC_PLL2_DLD      | Engage SYNC mode until PLL2 DLD is true                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                   | NO_SYNC_CLKoutX_Y  | Synchronization will not affect selected clock outputs, where X = even-numbered output and Y = odd-numbered output.                                                                                                                                                                                                                                                                                                                                                          |
|                   | SYNC_QUAL          | Sets the SYNC to qualify mode for dynamic digital delay.                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                   | EN_SYNC            | Must be set when using SYNC, but may be cleared after the SYNC event. When using dynamic digital delay (SYNC_QUAL = 1), EN_SYNC must always be set.<br>Changing this value from 0 to 1 can cause a SYNC event, so clocks which should not be SYNCed when setting this bit should have the NO_SYNC_CLKoutX_Y bit set.<br><b>NOTE:</b> This bit is not a valid method of generating a SYNC event. Use one of the other SYNC generation methods to ensure a proper SYNC occurs. |
| DAC/Holdover      | SYNC_EN_AUTO       | Enable auto SYNC when R0 to R5 is written.                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|                   | HOLDOVER_MODE      | Sets holdover mode to be disabled or enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                   | FORCE_HOLDOVER     | Engages holdover when checked regardless of HOLDOVER_MODE value. Turns the DAC on.                                                                                                                                                                                                                                                                                                                                                                                           |
|                   | EN_TRACK           | Enables DAC tracking. DAC tracks the PLL1 Vtune to provide for an accurate HOLDOVER mode. DAC_CLK_DIV should also be set so that DAC update rate is $\leq 100$ kHz.                                                                                                                                                                                                                                                                                                          |
|                   | EN_VTUNE_RAIL_DET  | Allows rail-to-rail operation of VCXO with default of 0. Allows use of DAC_LOW_TRIP, DAC_HIGH_TRIP. Must be used with EN_MAC_DAC = 1. CLKin_SELECT_MODE must be 4 or 6 (auto mode) to use.                                                                                                                                                                                                                                                                                   |

|      |                 |                                                                                                                                                                                                                                                                   |
|------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | HOLD_DLD_CNT    | In HOLDOVER mode, wait for this many clocks of PLL1 PDF within the tolerances of PLL1_WND_SIZE before exiting holdover mode.                                                                                                                                      |
|      | DAC_CLK_DIV     | DAC update clock is the PLL1 phase detector divided by this divisor. For proper operation, DAC update clock rate should be $\leq 100$ kHz.<br>DAC update rate = PLL1 phase detector frequency / DAC_CLK_DIV                                                       |
|      | EN_MAN_DAC      | Enables manual DAC mode and set DAC voltage when in holdover.                                                                                                                                                                                                     |
|      | MAN_DAC         | Sets the value for the DAC when EN_MAN_DAC is 1 and holdover is engaged. Readback from this register is the current DAC value whether in manual DAC mode or DAC tracking mode                                                                                     |
|      | DAC_LOW_TRIP    | Value from GND in $\sim 50$ mV steps at which a clock switch event is generated. If Holdover mode is enabled, it will be engaged upon the clock switch event.<br>NOTE: EN_VTUNE_RAIL_DET must be enabled for this to be valid.                                    |
|      | DAC_HIGH_TRIP   | Value from VCC (3.3V) in $\sim 50$ mV steps at which clock switch event is generated. If Holdover mode is enabled, it will be engaged upon the clock switch event.<br>NOTE: EN_VTUNE_RAIL_DET must be enabled for this to be valid.                               |
| PLL1 | PLL1_WND_SIZE   | If the phase error between the PLL1 reference and feedback clocks is less than specified time, then the PLL1 lock counter increments.<br>NOTE: Final lock detect valid signal is determined when the PLL1 lock counter meets or exceeds the PLL1_DLD_CNT value.   |
|      | PLL1_DLD_CNT    | The reference and feedback of PLL1 must be within the window of phase error as specified by PLL1_WND_SIZE for this many cycles before PLL1 digital lock detect is asserted.                                                                                       |
|      | CLKinX_PreR_DIV | The PreR dividers divide the CLKinX reference before the PLL1_R divider.<br>Unique divides on individual CLKinX signals allows switchover from one clock input to another clock input without needing to reprogram the PLL1_R divider to keep the device in lock. |
|      | PLL1_N_DLY      | N delay causes clock outputs to lead clock input when in a 0-delay mode. Increasing the N delay value increases the output phase lead relative to the input.                                                                                                      |

|              |                |                                                                                                                                                                                                 |
|--------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|              | PLL1_R_DLY     | R delay causes clock outputs to lag clock input when in a 0-delay mode. Increasing the R delay value increases the output phase lag relative to the input.                                      |
| PLL2         | PLL2_WND_SIZE  | If the phase error between the PLL2 reference and feedback clock is less than specified time, then the PLL2 lock counter increments.                                                            |
|              | PLL2_DLD_CNT   | The reference and feedback of PLL2 must be within the window of phase error as specified by PLL2_WND_SIZE for this many cycles before PLL2 digital lock detect is asserted.                     |
|              | EN_PLL2_REF_2X | Enables the doubler block to double the reference frequency into the PLL2 R counter. This can allow for frequency of 2/3, 2/5, etc. of OSCin to be used at the phase detector of PLL2.          |
|              | PLL2_N_CAL     | The PLL2_N_CAL register contains the N value used for the VCO calibration routine. Except during 0-delay modes, the PLL2_N and PLL2_N_CAL registers will be exactly the same.                   |
|              | PLL2_R3_LF     | Set the corresponding integrated PLL2 loop filter values: R3, R4, C3, and C4.<br>It is also possible to set these values by clicking on the loop filter values on the <b>Clock Outputs</b> tab. |
|              | PLL2_R4_LF     |                                                                                                                                                                                                 |
|              | PLL2_C3_LF     |                                                                                                                                                                                                 |
|              | PLL2_C4_LF     |                                                                                                                                                                                                 |
|              | PLL2_FAST_PDF  | Enable this bit when using a PLL2 phase detector frequency > 100 MHz.                                                                                                                           |
| Program Pins | SYNC           | Sets these pins on the uWire header to logic high (checked) or logic low (unchecked).                                                                                                           |
|              | Status_CLKin0  |                                                                                                                                                                                                 |
|              | Status_CLKin1  |                                                                                                                                                                                                 |

## Registers Tab

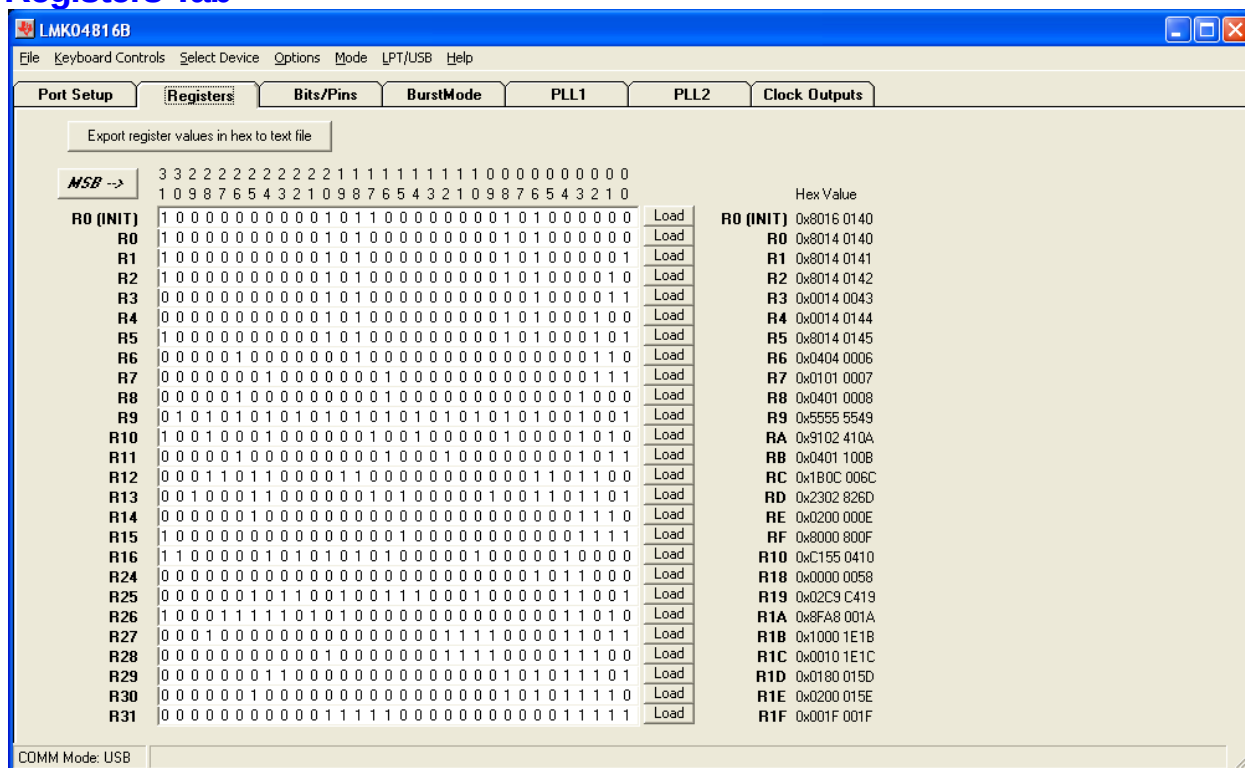


Figure 14: Registers Tab

The Registers tab shows the value of each register. This is convenient for programming the device to the desired settings, then exporting to a text file the register values in hexadecimal for use in your own application.

By clicking in the “bit field” it is possible to manually change the value of registers by typing ‘1’ and ‘0.’

## Appendix B: Typical Phase Noise Performance Plots

### PLL1

The LMK04816B's dual PLL architecture achieves ultra low jitter and phase noise by allowing the external VCXO or Crystal's phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies. This results in the best overall noise and jitter performance.

Table 11 lists the test conditions used for output clock phase noise measurements with the Crystek 122.88 MHz VCXO.

**Table 11: LMK04816B Test Conditions**

| Parameter                      | Value                                                |
|--------------------------------|------------------------------------------------------|
| PLL1 Reference clock input     | CLKin0 single-ended input, CLKin0* AC-coupled to GND |
| PLL1 Reference Clock frequency | 122.88 MHz                                           |
| PLL1 Phase detector frequency  | 122.88 MHz                                           |
| PLL1 Charge Pump Gain          | 100 uA                                               |
| VCXO frequency                 | 122.88 MHz                                           |
| PLL2 phase detector frequency  | 122.88 MHz                                           |
| PLL2 Charge Pump Gain          | 3200 uA                                              |
| PLL2 REF2X mode                | Disabled                                             |

### 122.88 MHz VCXO Phase Noise

The phase noise of the reference is masked by the phase noise of this VCXO by using a narrow loop bandwidth for PLL1 while retaining the frequency accuracy of the reference clock input. This VCXO sets the reference noise to PLL2. Figure 15 shows the open loop typical phase noise performance of the CVHD-950-122.88 Crystek VCXO.

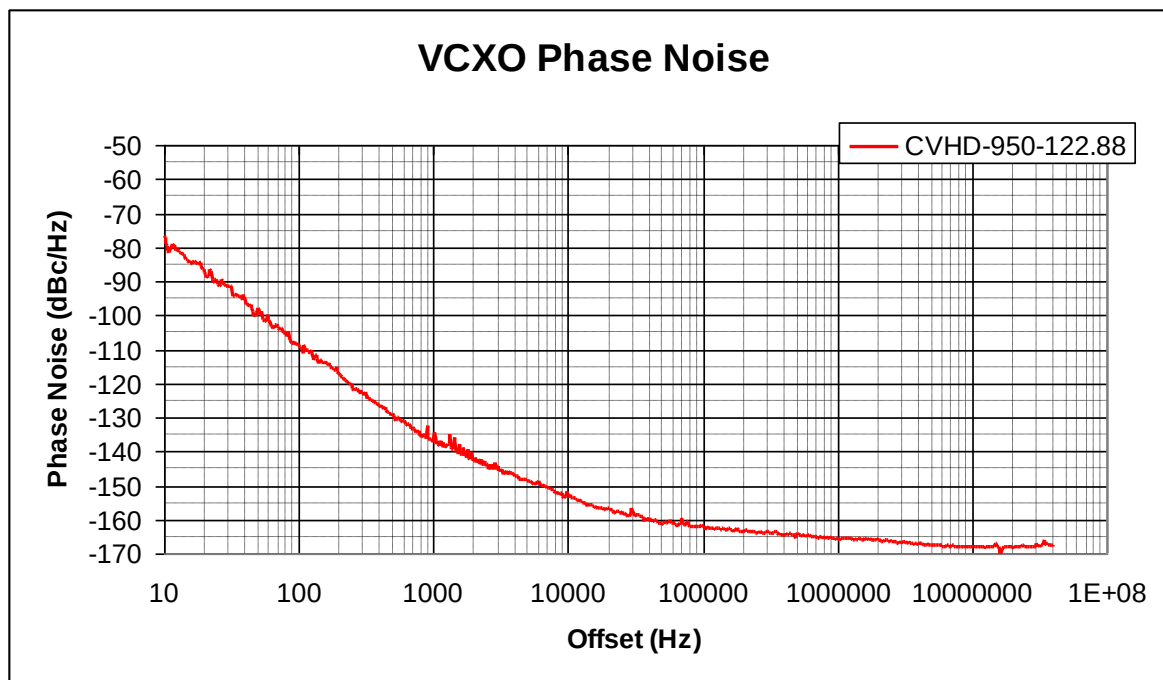


Figure 15: Crystek CVHD-950-122.88 MHz VCXO Phase Noise at 122.88 MHz

Table 12: VCXO Phase Noise at 122.88 MHz (dBc/Hz)

| Offset  | Phase Noise |
|---------|-------------|
| 10 Hz   | -76.6       |
| 100 Hz  | -108.9      |
| 1 kHz   | -137.4      |
| 10 kHz  | -153.3      |
| 100 kHz | -162.0      |
| 1 MHz   | -165.7      |
| 10 MHz  | -168.1      |
| 40 MHz  | -168.1      |

Table 13: VCXO RMS Jitter to high offset of 20 MHz at 122.88 MHz (rms fs)

| Low Offset | Jitter |
|------------|--------|
| 10 Hz      | 515.4  |
| 100 Hz     | 60.5   |
| 1 kHz      | 36.2   |
| 10 kHz     | 35.0   |
| 100 kHz    | 34.5   |
| 1 MHz      | 32.9   |
| 10 MHz     | 22.7   |

## Clock Output Measurement Technique

The same technique was used to measure phase noise for all three output types available on the programmable OSCout and CLKout buffers. This was achieved by terminating one side of the LVPECL, LVDS, or LVC MOS output with a 50-ohm load, and measuring the other side single-ended using an Agilent E5052B Source Signal Analyzer.

## Buffered Phase Noise

Both OSCout0 and OSCout1 frequencies are 122.88 MHz since the OSCout Divider is bypassed. OSCout0 is programmed to LVC MOS mode.



## Clock Outputs (CLKout)

The LMK04816 Family features programmable LVDS, LVPECL, and LVCMOS buffer modes for the CLKoutX and OSCout0 output pairs. Included below are various phase noise measurements for each output format.

### LMK04816B CLKout Phase Noise

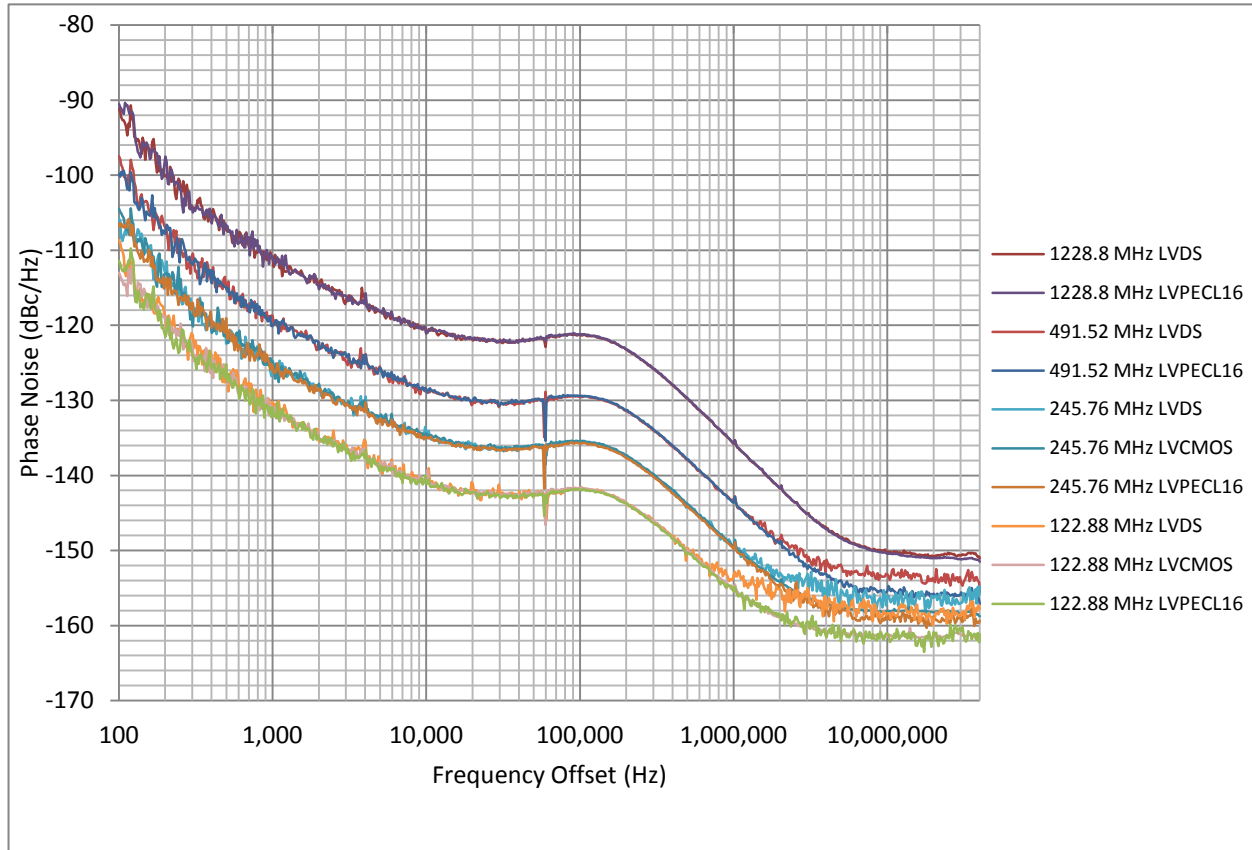


Figure 16: LMK04816B CLKout Phase Noise

Table 14: LMK04816B Phase Noise (dBc/Hz) Phase Noise and RMS Jitter (fs)

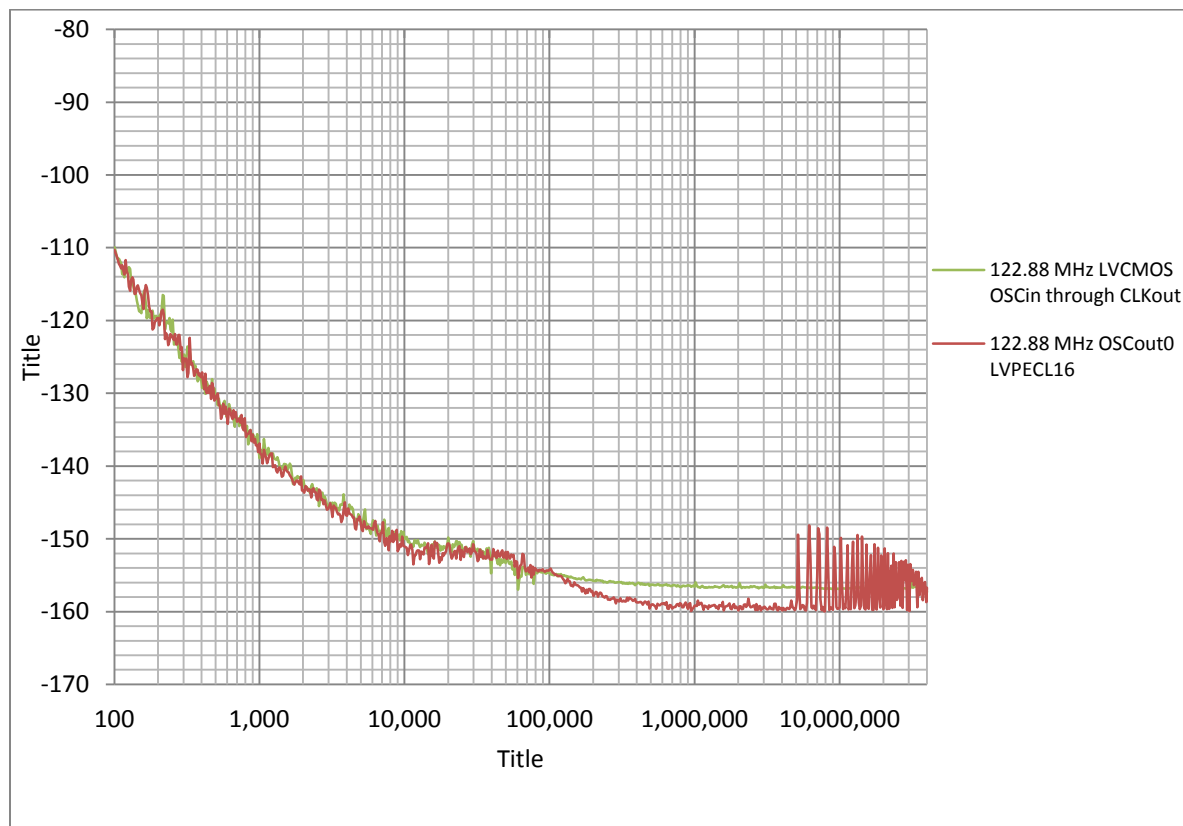
| Offset                              | 1228.80 MHz<br>LVDS | 1228.80 MHz<br>LVPECL | 491.52 MHz<br>LVDS | 491.52 MHz<br>LVPECL |
|-------------------------------------|---------------------|-----------------------|--------------------|----------------------|
| 100 Hz                              | -91.2               | -90.5                 | -97.5              | -98.2                |
| 1 kHz                               | -111.2              | -110.8                | -118.7             | -119.4               |
| 10 kHz                              | -121.0              | -121.1                | -128.5             | -128.6               |
| 100 kHz                             | -121.3              | -121.2                | -129.5             | -129.5               |
| 800 kHz                             | -133.8              | -133.7                | -141.9             | -141.9               |
| 1 MHz                               | -135.8              | -135.7                | -143.4             | -143.8               |
| 10 MHz                              | -150.2              | -150.4                | -153.1             | -155.7               |
| 20 MHz                              | -150.8              | -151.0                | -153.8             | -155.7               |
| RMS Jitter (fs)<br>10 kHz to 20 MHz | 92.9                | 93.4                  | 97.5               | 94.5                 |
| RMS Jitter (fs)<br>100 Hz to 20 MHz | 104.0               | 105.3                 | 109.0              | 105.4                |

For the LMK04816B, the internal VCO frequency is 2457.60 MHz. The divide-by-10 CLKout frequency is 245.76 MHz, and the divide-by-20 CLKout frequency is 122.88 MHz.

**Table 15: LMK04816B Phase Noise and RMS Jitter for Different CLKout Output Formats and Frequencies**

| Offset                              | 245.76<br>LVDS | 245.76<br>LVCMOS | 245.76<br>LVPECL | 122.88<br>LVDS | 122.88<br>LVCMOS | 122.88<br>LVPECL |
|-------------------------------------|----------------|------------------|------------------|----------------|------------------|------------------|
| 100 Hz                              | -105.8         | -104.5           | -106.5           | -108.6         | -113.0           | -111.4           |
| 1 kHz                               | -124.7         | -124.9           | -125.4           | -130.2         | -132.1           | -131.0           |
| 10 kHz                              | -134.8         | -134.4           | -134.9           | -140.7         | -140.7           | -141.0           |
| 100 kHz                             | -135.5         | -135.4           | -135.8           | -141.7         | -141.7           | -141.9           |
| 800 kHz                             | -147.8         | -147.7           | -148.0           | -152.6         | -153.5           | -154.1           |
| 1 MHz                               | -149.6         | -149.4           | -149.7           | -153.3         | -155.2           | -155.5           |
| 10 MHz                              | -156.1         | -158.1           | -158.4           | -158.4         | -161.5           | -161.1           |
| 20 MHz                              | -156.3         | -158.2           | -158.9           | -159.5         | -161.6           | -161.3           |
| RMS Jitter (fs)<br>10 kHz to 20 MHz | 106.9          | 101.5            | 96.4             | 134.2          | 109.7            | 108.2            |
| RMS Jitter (fs)<br>100 Hz to 20 MHz | 116.8          | 112.4            | 106.4            | 143.2          | 118.9            | 117.9            |

## LMK04816B OSCout Phase Noise



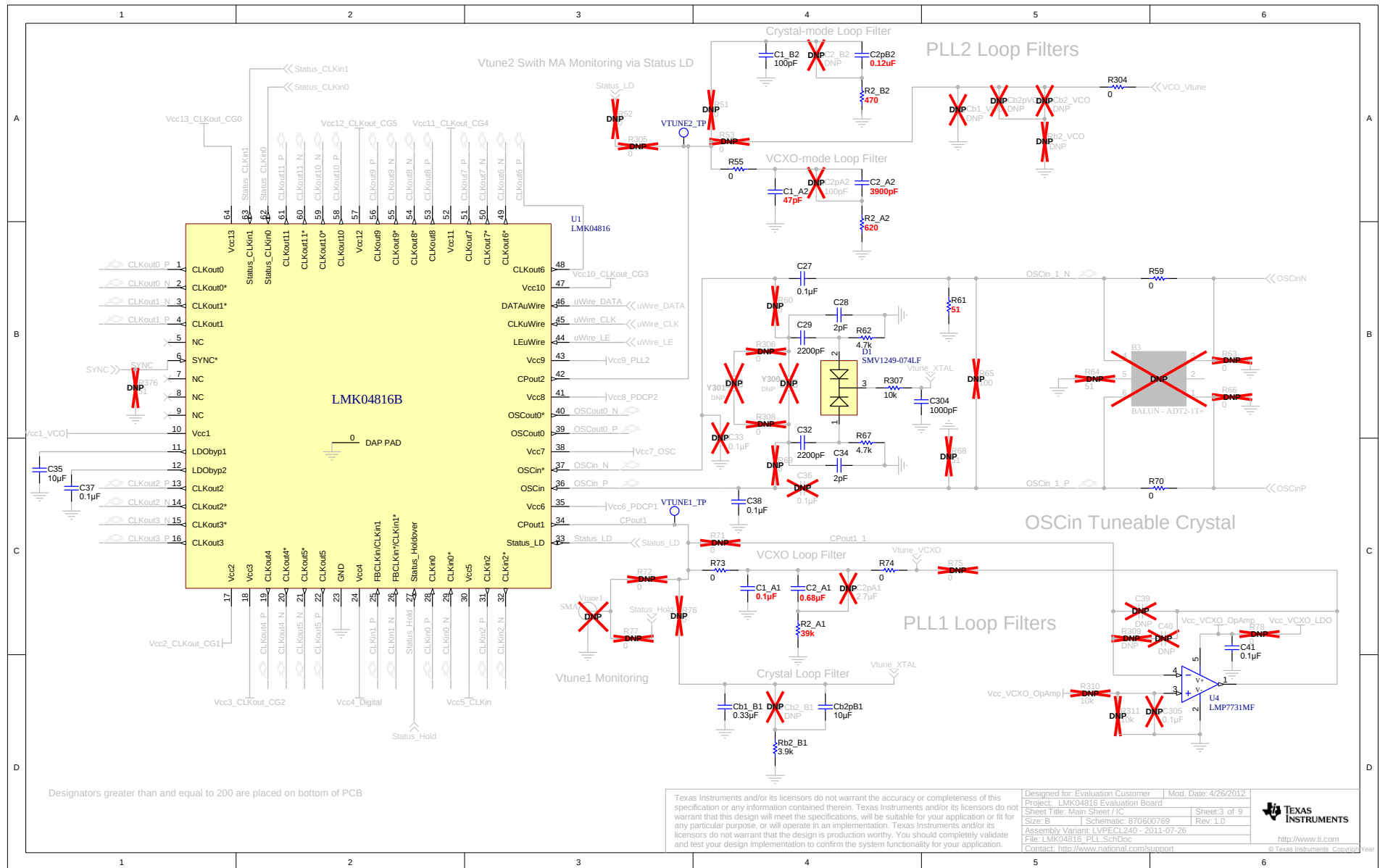
**Figure 17: LMK04816B OSCout Phase Noise**

**Table 16: LMK04816B OSCout Phase Noise and RMS Jitter (fs)**

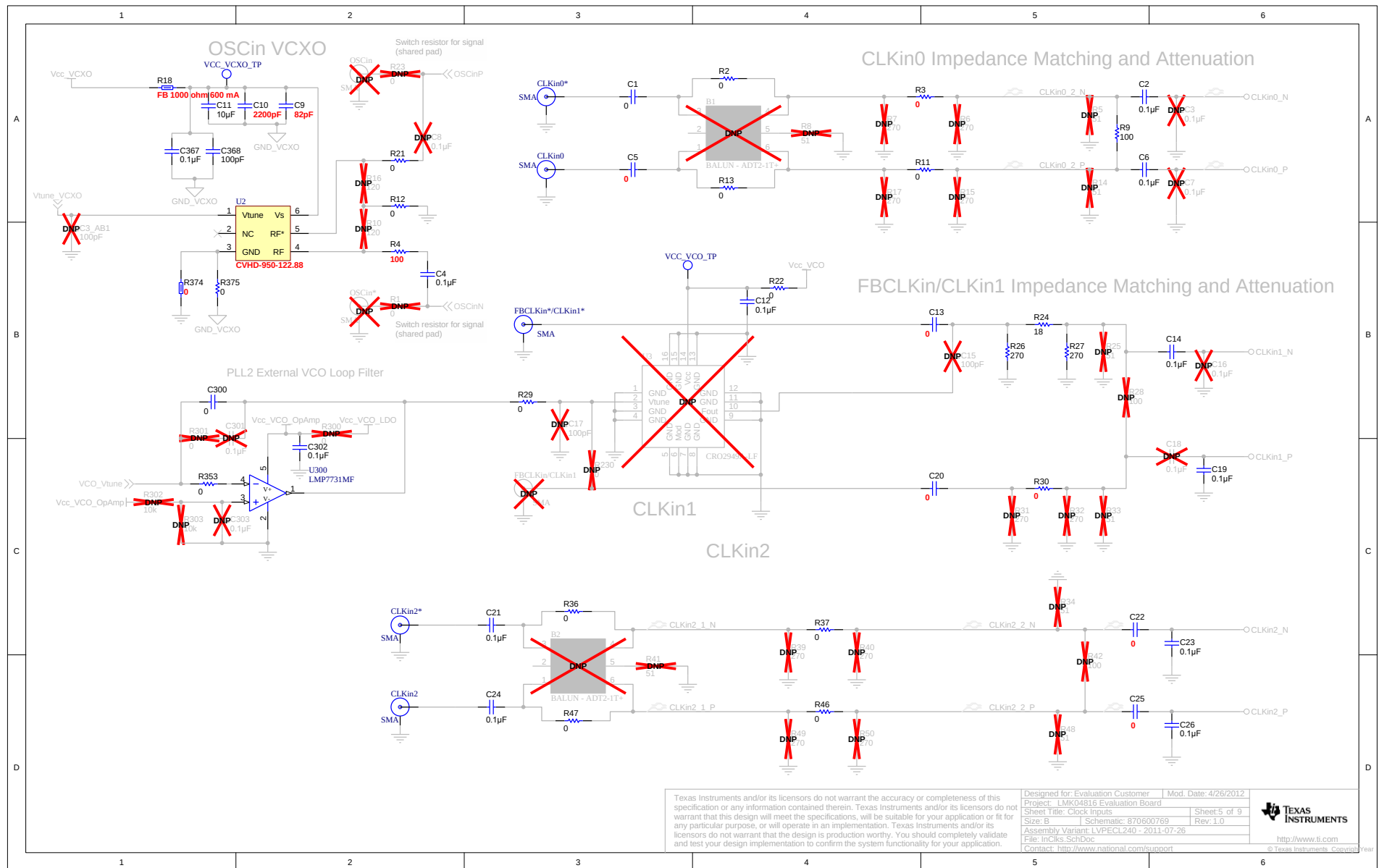
| Offset                                     | OSCout0<br>LVPECL | OSCin thru<br>CLKout |
|--------------------------------------------|-------------------|----------------------|
| <b>100 Hz</b>                              | -110.3            | -110.0               |
| <b>1 kHz</b>                               | -136.9            | -138.9               |
| <b>10 kHz</b>                              | -151.1            | -150.0               |
| <b>100 kHz</b>                             | -154.3            | -154.6               |
| <b>800 kHz</b>                             | -158.9            | -156.6               |
| <b>1 MHz</b>                               | -159.2            | -156.6               |
| <b>10 MHz</b>                              | -159.4            | -156.8               |
| <b>20 MHz</b>                              | -157.6            | -156.9               |
| <b>RMS Jitter (fs)</b><br>10 kHz to 20 MHz | 138.4             | 120.0                |
| <b>RMS Jitter (fs)</b><br>100 Hz to 20 MHz | 143.7             | 126.2                |



## LMK04816B Device with Loop Filter and Crystal Circuits

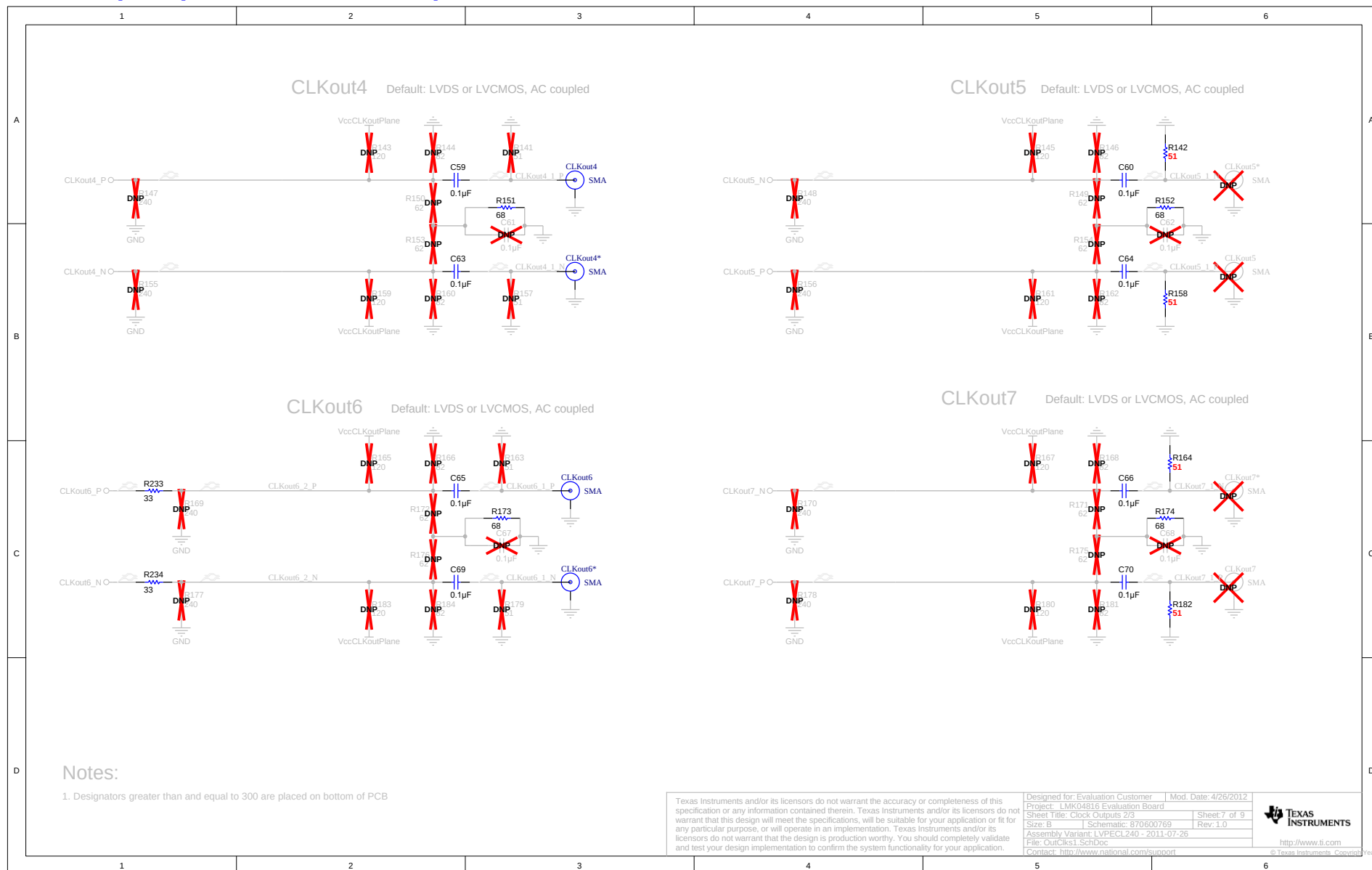


## Reference Inputs (CLKin0, CLKin1, & CLKin2), External VCXO (OSCin) & VCO Circuits



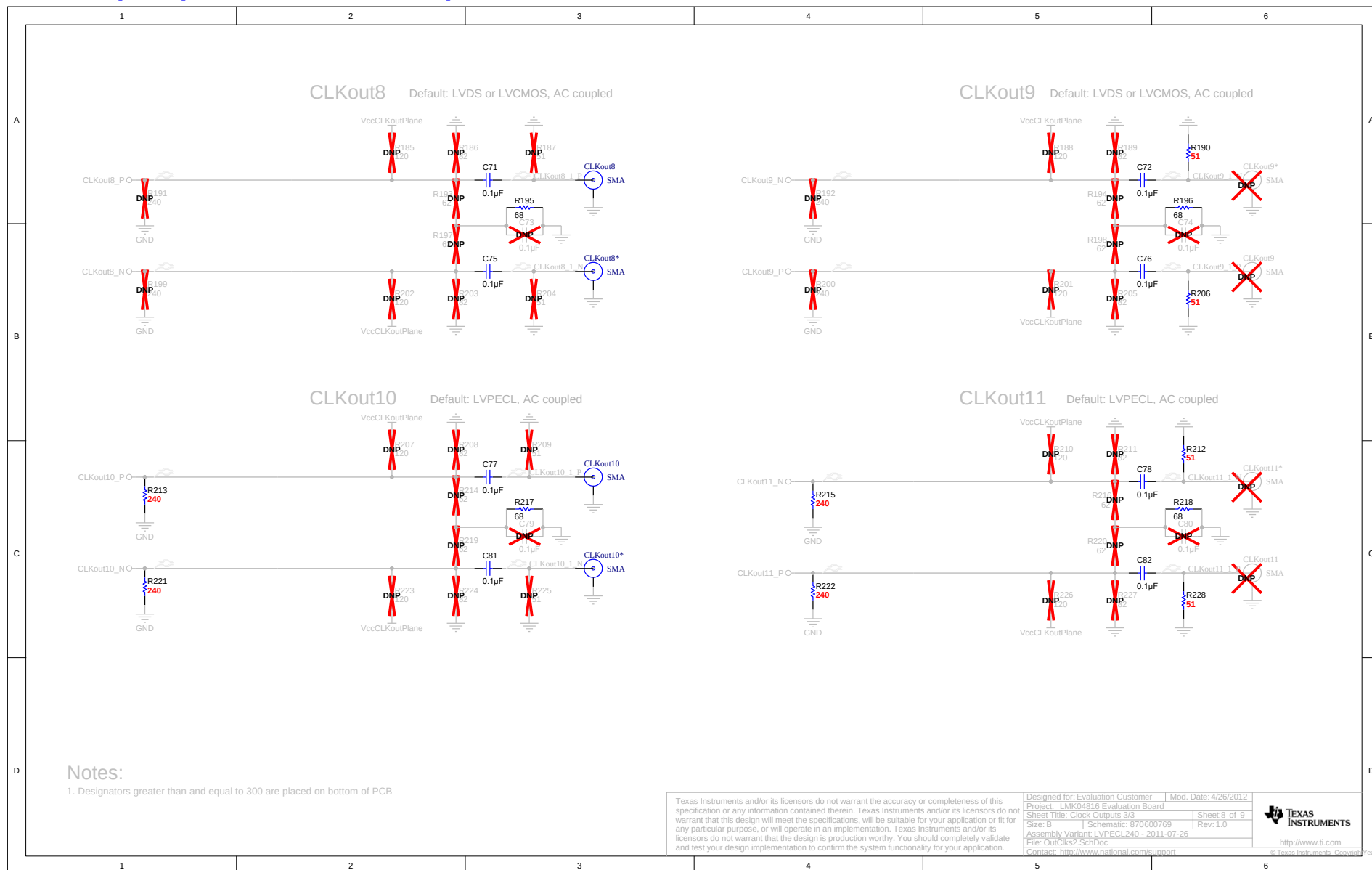


## Clock Outputs (CLKout4 to CLKout7)

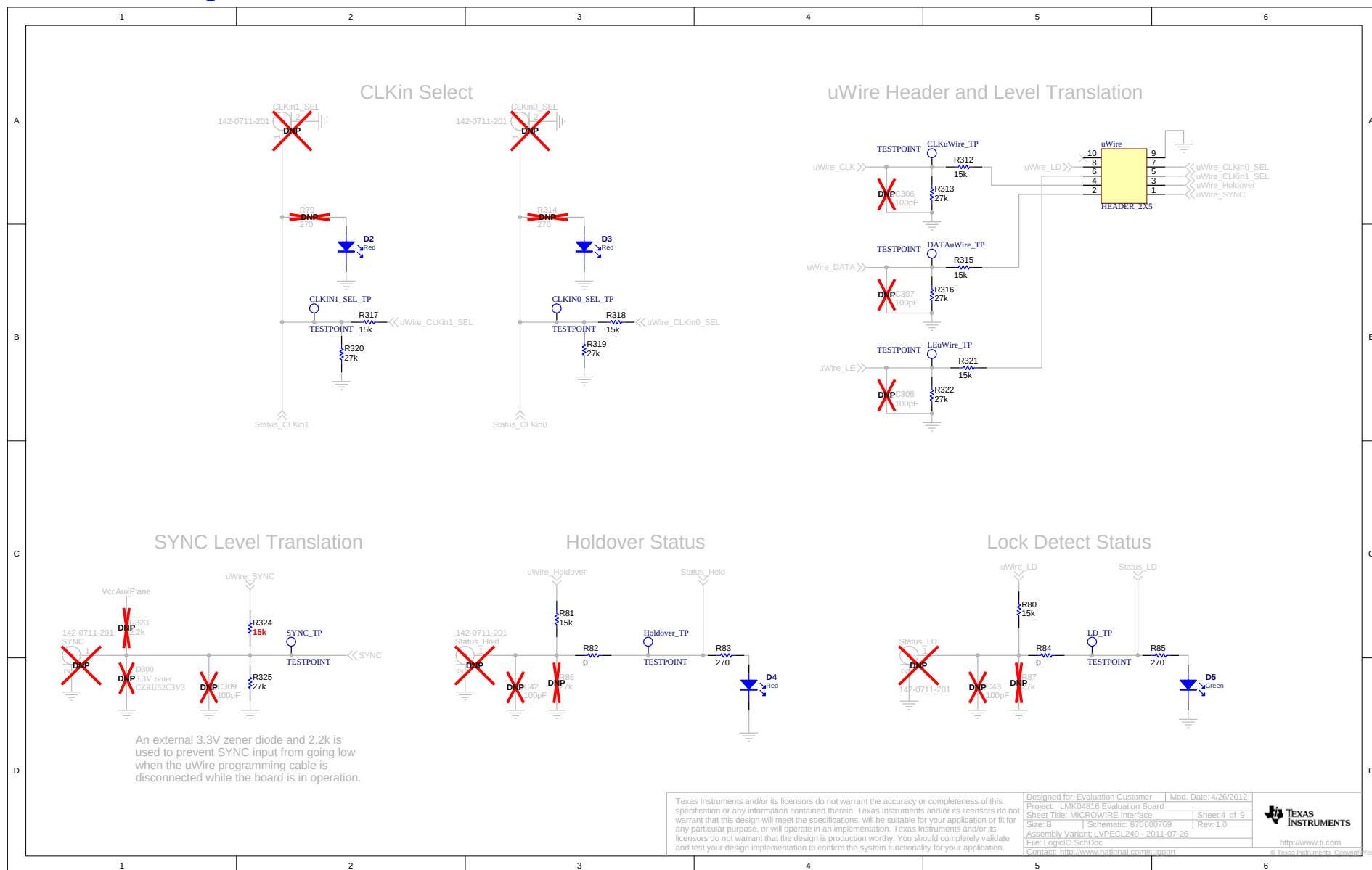




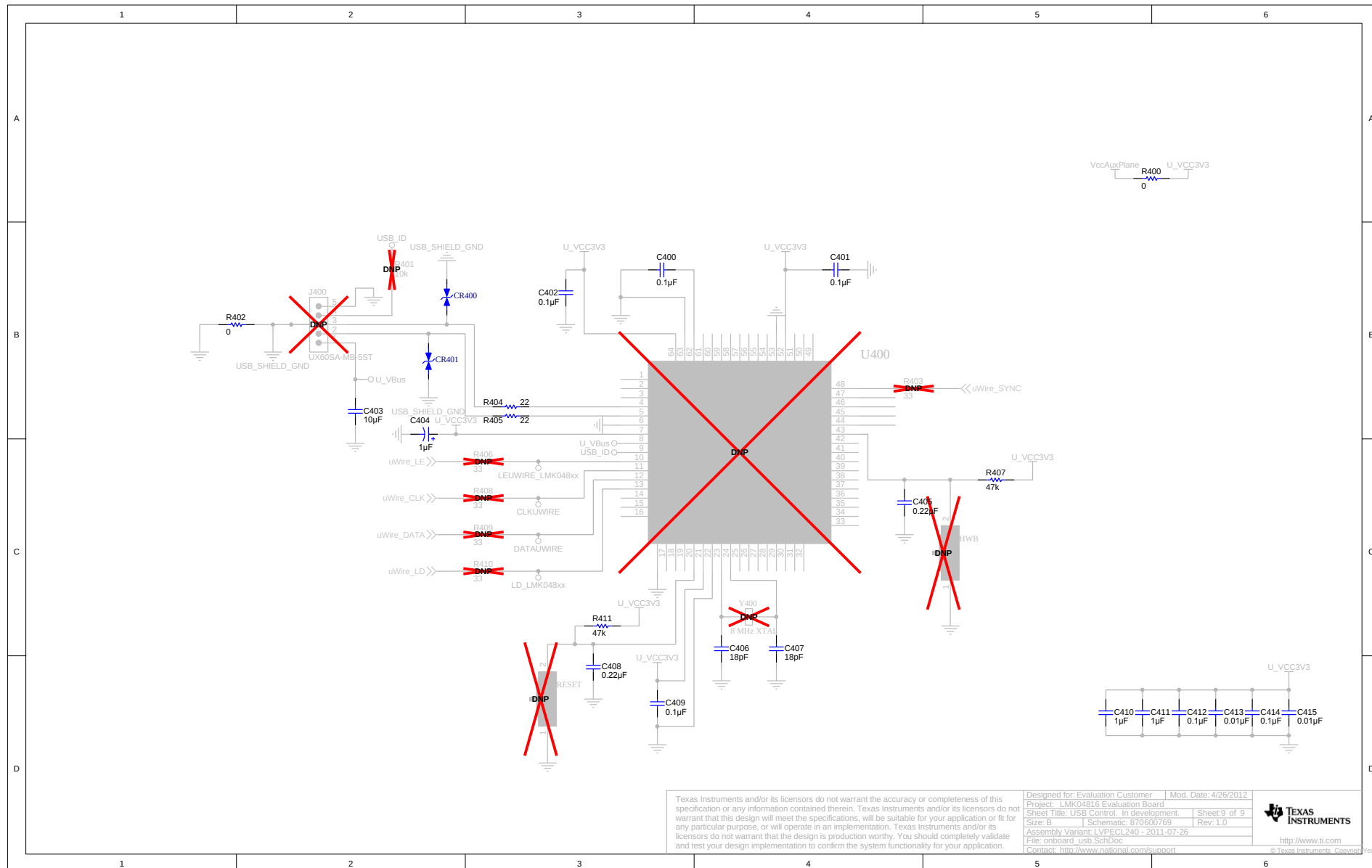
## Clock Outputs (CLKout8 to CLKout11)



## uWire Header, Logic I/O Ports and Status LEDs



## USB Interface



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Designed for: Evaluation Customer Mod. Date: 4/26/2012  
 Project: LMK04816 Evaluation Board  
 Sheet Title: USB Control, in development. Sheet: 9 of 9  
 Size: B Schematic: 870600769 Rev: 1.0  
 Assembly Variant: LVPECL240 - 2011-07-26  
 File: onboard\_usb.SchDoc  
 Contact: <http://www.national.com/support>



<http://www.ti.com>  
 © Texas Instruments. Copyright Year

## Appendix D: Bill of Materials

Table 17: Bill of Materials for LMK04816 Evaluation Boards

| Item | Designator                                                                                                                                                                                                                                     | Description                                 | Manufacturer             | PartNumber       | Quantity |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|--------------------------|------------------|----------|
| 1    | B2                                                                                                                                                                                                                                             | ADT2-1T Balun                               | MiniCircuits             | ADT2-1T+         | 1        |
| 2    | C1, C5, C13, C20, C22, C25, C300, R3, R11, R12, R19, R21, R22, R29, R30, R37, R46, R55, R73, R74, R82, R84, R229, R304, R327, R329, R333, R337, R340, R346, R347, R349, R353, R354, R358, R361, R364, R365, R368, R371, R373, R375, R400, R402 | RES, 0 ohm, 5%, 0.1W, 0603                  | Vishay-Dale, Vishey/Dale | CRCW06030000Z0EA | 44       |
| 3    | C1_A1, C6, C14, C19, C21, C24, C27, C37, C38, C44, C46, C47, C48, C51, C52, C53, C54, C57, C58, C59, C60, C63, C64, C65, C66, C70, C71, C72, C75, C76, C77, C78, C81, C82, C312, C319, C329, C361                                              | CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603     | Kemet                    | C0603C104J3RACTU | 38       |
| 4    | C1_A2                                                                                                                                                                                                                                          | CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603  | Kemet                    | C0603C470J5GACTU | 1        |
| 5    | C1_B2                                                                                                                                                                                                                                          | CAP, CERM, 150pF, 50V, +/-5%, C0G/NP0, 0603 | Kemet                    | C0603C151J5GACTU | 1        |

|    |                                                                                        |                                                                                    |                |                    |    |
|----|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|----------------|--------------------|----|
| 6  | C2, C12, C41, C302, C330, C346                                                         | CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603                                           | Kemet          | C0603C104K4RACTU   | 6  |
| 7  | C2pB2                                                                                  | CAP, CERM, 0.12uF, 50V, +/-10%, X7R, 0805                                          | Kemet          | C0805C124K5RACTU   | 1  |
| 8  | C2_A1                                                                                  | CAP, CERM, 0.68uF, 10V, +/-10%, X5R, 0603                                          | Kemet          | C0603C684K8PAC     | 1  |
| 9  | C2_A2                                                                                  | CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0603                                          | MuRata         | GRM188R71H392KA01D | 1  |
| 10 | C4, C69, C314, C322, C326, C367, C400, C401, C402, C409, C412, C414                    | CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603, CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603 | Kemet          | C0603C104K3RACTU   | 12 |
| 11 | C9                                                                                     | CAP, CERM, 82pF, 50V, +/-10%, C0G/NP0, 0603                                        | Kemet          | C0603C820K5GACTU   | 1  |
| 12 | C10, C29, C32, C341                                                                    | CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603                                          | Kemet          | C0603C222K5RACTU   | 4  |
| 13 | C11                                                                                    | CAP, CERM, 10uF, 10V, +/-20%, X5R, 0805                                            | Kemet          | C0805C106M8PACTU   | 1  |
| 14 | C23, C26, R104, R112, R125, R126, R133, R134, R213, R215, R221, R222, R231, R232, R338 | RES, 240 ohm, 5%, 0.1W, 0603                                                       | Vishay-Dale    | CRCW0603240RJNEA   | 15 |
| 15 | C28, C34                                                                               | CAP, CERM, 2pF, 50V, +/-12.5%, C0G/NP0, 0603                                       | Kemet          | C0603C209C5GACTU   | 2  |
| 16 | C35, C310, C317, C324, Cb2pB1                                                          | CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805                                            | Kemet          | C0805C106K8PACTU   | 5  |
| 17 | C304                                                                                   | CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603                                       | Kemet          | C0603C102J5GACTU   | 1  |
| 18 | C311, C313, C318, C321, C325, C331, C342                                               | CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603                                             | Kemet          | C0603C105K8PACTU   | 7  |
| 19 | C315, C323                                                                             | CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603                                         | Kemet          | C0603C103K1RACTU   | 2  |
| 20 | C340                                                                                   | CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603                                           | Kemet          | C0603C475K8PACTU   | 1  |
| 21 | C350, C351, C359, C360                                                                 | CAP, CERM, 0.47uF, 16V, +/-10%, X7R, 0603                                          | Kemet          | C0603C474K4RACTU   | 4  |
| 22 | C368                                                                                   | CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603                                        | Kemet          | C0603C101J5GACTU   | 1  |
| 23 | C403                                                                                   | CAP, CERM, 10uF, 6.3V, +/-10%, X5R, 0805                                           | Kemet          | C0805C106K9PAC     | 1  |
| 24 | C404                                                                                   | CAP, TANT, 1uF, 20V, +/-10%, 8.4 ohm, 3216-18 SMD                                  | Vishay-Sprague | 293D105X9020A2TE3  | 1  |
| 25 | C405, C408                                                                             | CAP, CERM, 0.22uF, 16V, +/-10%, X7R, 0603                                          | Kemet          | C0603C224K4RACTU   | 2  |
| 26 | C406, C407                                                                             | CAP, CERM, 18pF, 50V, +/-5%, C0G/NP0, 0603                                         | Kemet          | C0603C180J5GACTU   | 2  |
| 27 | C410, C411                                                                             | CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603                                             | Kemet          | C0603C105K4PACTU   | 2  |
| 28 | C413, C415                                                                             | CAP, CERM, 0.01uF, 50V, +/-5%, X7R, 0603                                           | Kemet          | C0603C103J5RACTU   | 2  |

|    |                                                                                                                                                                                                                                           |                                           |                               |                  |    |
|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------------------|------------------|----|
| 29 | Cb1_B1                                                                                                                                                                                                                                    | CAP, CERM, 0.33uF, 16V, +/-10%, X7R, 0603 | Kemet                         | C0603C334K4RACTU | 1  |
| 30 | CLKin0, CLKin0*,<br>CLKin2, CLKin2*,<br>CLKout0,<br>CLKout0*,<br>CLKout2,<br>CLKout2*,<br>CLKout4,<br>CLKout4*,<br>CLKout6,<br>CLKout6*,<br>CLKout8,<br>CLKout8*,<br>CLKout10,<br>CLKout10*,<br>FBCLKin*/CLKin1*,<br>OScout0,<br>OScout0* | Connector, SMT, End launch SMA 50 Ohm     | Emerson Network<br>Power      | 142-0701-851     | 19 |
| 31 | CR400, CR401                                                                                                                                                                                                                              | ESD suppressor                            | Littelfuse Inc                | PGB1010603MR     | 2  |
| 32 | D1                                                                                                                                                                                                                                        | Common Cathode Tuning Varactor            | Skyworks                      | SMV1249-074LF    | 0  |
| 33 | D2, D3, D4                                                                                                                                                                                                                                | LED 2.8X3.2MM 565NM RED CLR SMD           | Lumex<br>Opto/Components Inc. | SML-LX2832IC     | 3  |
| 34 | D5                                                                                                                                                                                                                                        | LED 2.8X3.2MM 565NM GRN CLR SMD           | Lumex<br>Opto/Components Inc. | SML-LX2832GC     | 1  |
| 35 | J1                                                                                                                                                                                                                                        | CONN TERM BLK PCB 5.08MM 2POS OR          | Weidmuller                    | 1594540000       | 1  |
| 36 | R2, R13, R59,<br>R70, R332                                                                                                                                                                                                                | RES, 0 ohm, 5%, 0.125W, 0805              | Vishay-Dale                   | CRCW08050000Z0EA | 5  |
| 37 | R2_A1                                                                                                                                                                                                                                     | RES, 39k ohm, 5%, 0.1W, 0603              | Vishay-Dale                   | CRCW060339K0JNEA | 1  |
| 38 | R2_A2                                                                                                                                                                                                                                     | RES, 620 ohm, 5%, 0.1W, 0603              | Vishay-Dale                   | CRCW0603620RJNEA | 1  |
| 39 | R2_B2                                                                                                                                                                                                                                     | RES, 470 ohm, 5%, 0.1W, 0603              | Vishay-Dale                   | CRCW0603470RJNEA | 1  |
| 40 | R4, R9                                                                                                                                                                                                                                    | RES, 100 ohm, 5%, 0.1W, 0603              | Vishay-Dale                   | CRCW0603100RJNEA | 2  |
| 41 | R18, R336, R342,<br>R343, R374                                                                                                                                                                                                            | FB, 1000 ohm, 600 mA, 0603, Ferrite       | Murata                        | BLM18HE102SN1D   | 5  |
| 42 | R24                                                                                                                                                                                                                                       | RES, 18 ohm, 5%, 0.1W, 0603               | Vishay-Dale                   | CRCW060318R0JNEA | 1  |
| 43 | R26, R27, R83,<br>R85                                                                                                                                                                                                                     | RES, 270 ohm, 5%, 0.1W, 0603              | Vishay-Dale                   | CRCW0603270RJNEA | 4  |

|    |                                                                                                      |                                                   |                   |                  |    |
|----|------------------------------------------------------------------------------------------------------|---------------------------------------------------|-------------------|------------------|----|
| 44 | R35, R38, R41, R43, R44, R61, R102, R117, R124, R138, R142, R158, R164, R182, R190, R206, R212, R228 | RES, 51 ohm, 5%, 0.1W, 0603                       | Vishay-Dale       | CRCW060351R0JNEA | 18 |
| 45 | R62, R67                                                                                             | RES, 4.7k ohm, 5%, 0.1W, 0603                     | Vishay-Dale       | CRCW06034K70JNEA | 2  |
| 46 | R80, R81, R312, R315, R317, R318, R321, R324                                                         | RES, 15k ohm, 5%, 0.1W, 0603                      | Vishay-Dale       | CRCW060315K0JNEA | 8  |
| 47 | R107, R108, R129, R130, R151, R152, R173, R174, R195, R196, R217, R218                               | RES, 68 ohm, 5%, 0.1W, 0603                       | Vishay-Dale       | CRCW060368R0JNEA | 12 |
| 48 | R233, R234                                                                                           | RES, 33 ohm, 5%, 0.1W, 0603                       | Vishay-Dale       | CRCW060333R0JNEA | 2  |
| 49 | R307                                                                                                 | RES, 10k ohm, 5%, 0.1W, 0603                      | Vishay-Dale       | CRCW060310K0JNEA | 1  |
| 50 | R313, R316, R319, R320, R322, R325                                                                   | RES, 27k ohm, 5%, 0.1W, 0603                      | Vishay-Dale       | CRCW060327K0JNEA | 6  |
| 51 | R331, R341, R345, R348, R355, R359, R362, R366, R372                                                 | FB, 120 ohm, 500 mA, 0603                         | Murata            | BLM18AG121SN1D   | 9  |
| 52 | R344                                                                                                 | RES, 392 ohm, 1%, 0.1W, 0603                      | Vishay-Dale       | CRCW0603392RFKEA | 1  |
| 53 | R350, R369                                                                                           | RES, 51k ohm, 5%, 0.1W, 0603                      | Vishay-Dale       | CRCW060351K0JNEA | 2  |
| 54 | R351                                                                                                 | RES, 2.00k ohm, 1%, 0.1W, 0603                    | Vishay-Dale       | CRCW06032K00FKEA | 1  |
| 55 | R356                                                                                                 | RES, 866 ohm, 1%, 0.1W, 0603                      | Vishay-Dale       | CRCW0603866RFKEA | 1  |
| 56 | R404, R405                                                                                           | RES, 22 ohm, 5%, 0.125W, 0805                     | Vishay-Dale       | CRCW080522R0JNEA | 2  |
| 57 | R407, R411                                                                                           | RES, 47k ohm, 5%, 0.1W, 0603                      | Vishay-Dale       | CRCW060347K0JNEA | 2  |
| 58 | Rb2_B1                                                                                               | RES, 3.9k ohm, 5%, 0.1W, 0603                     | Vishay-Dale       | CRCW06033K90JNEA | 1  |
| 59 | S1, S2, S3, S4, S5, S6                                                                               | 0.875" Standoff                                   | VOLTRIX           | SPCS-14          | 6  |
| 60 | U1                                                                                                   | LMK04816                                          | Texas Instruments | LMK04816BISQ     | 1  |
| 61 | U2                                                                                                   | 122.88 MHz VCXO                                   | Crystek           | CVHD-950-122.88  | 1  |
| 62 | U4, U300                                                                                             | Precision Single Low Noise, Low 1/F corner Op Amp | National          | LMP7731MF        | 2  |

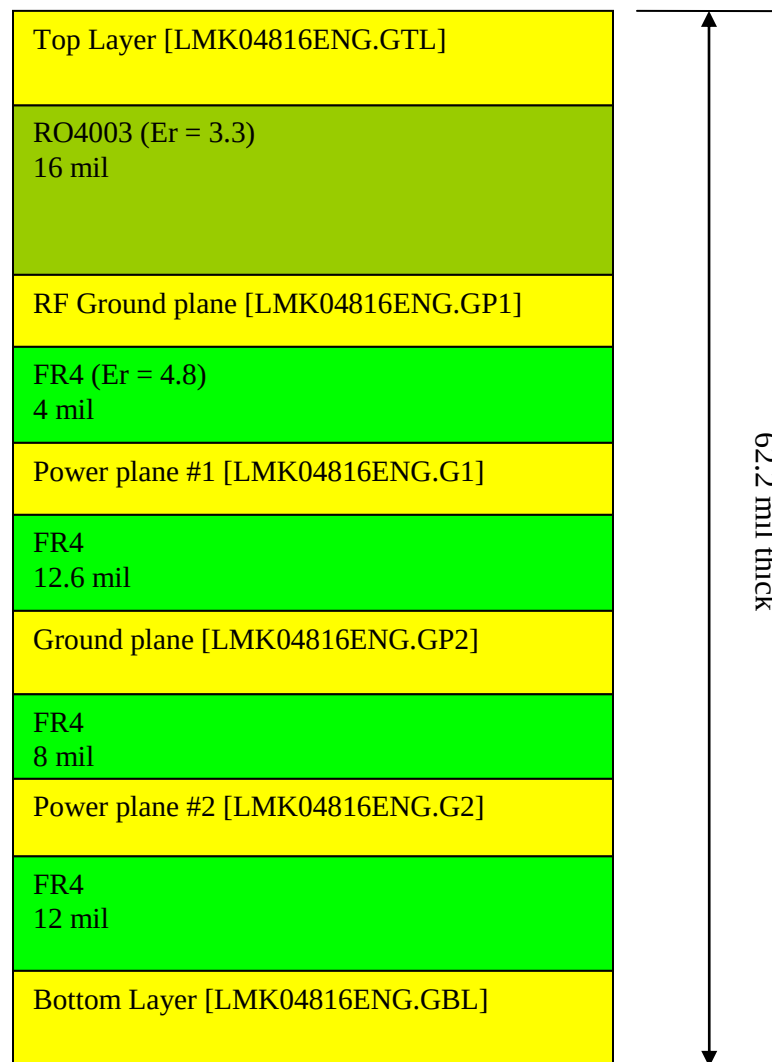
|    |                            |                                                                                                    |                                    |               |   |
|----|----------------------------|----------------------------------------------------------------------------------------------------|------------------------------------|---------------|---|
|    |                            |                                                                                                    | Semiconductor                      |               |   |
| 63 | U302                       | Micropower 800mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1V to 5V Applications | National Semiconductor             | LP3878SD-ADJ  | 1 |
| 64 | U303, U305                 | Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor        | National Semiconductor             | LP5900SD-3.3  | 2 |
| 65 | uWire                      | Low Profile Vertical Header 2x5 0.100"                                                             | FCI                                | 52601-G10-8LF | 1 |
| 66 | Vcc                        | Connector, TH, SMA                                                                                 | Emerson Network Power              | 142-0701-201  | 1 |
| 67 | VccVCO/Aux,<br>VccVCXO/Aux | Connector, SMA Jack, Vertical, Gold, SMD                                                           | Emerson Network Power Connectivity | 142-0711-201  | 2 |



## Appendix E: PCB Layers Stackup

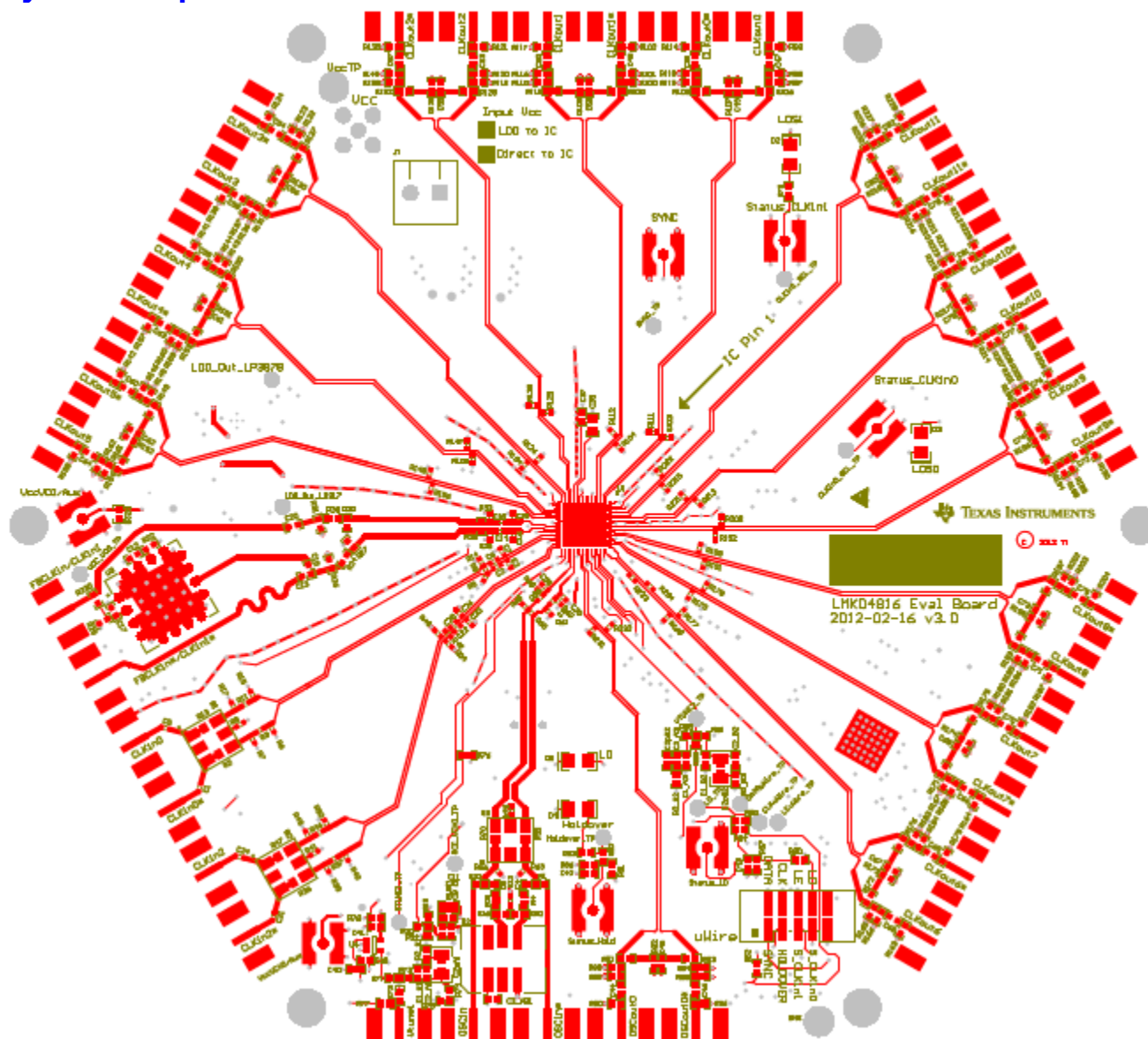
6-layer PCB Stackup includes:

- Top Layer for high-priority high-frequency signals (2 oz.)
- RO4003 Dielectric, 16 mils
- RF Ground plane (1 oz.)
- FR4, 4 mils
- Power plane #1 (1 oz.)
- FR4, 12.6 mils
- Ground plane (1 oz.)
- FR4, 8 mils
- Power Plane #2 (1 oz.)
- FR4, 12 mils
- Bottom Layer copper clad for thermal relief (2 oz.)

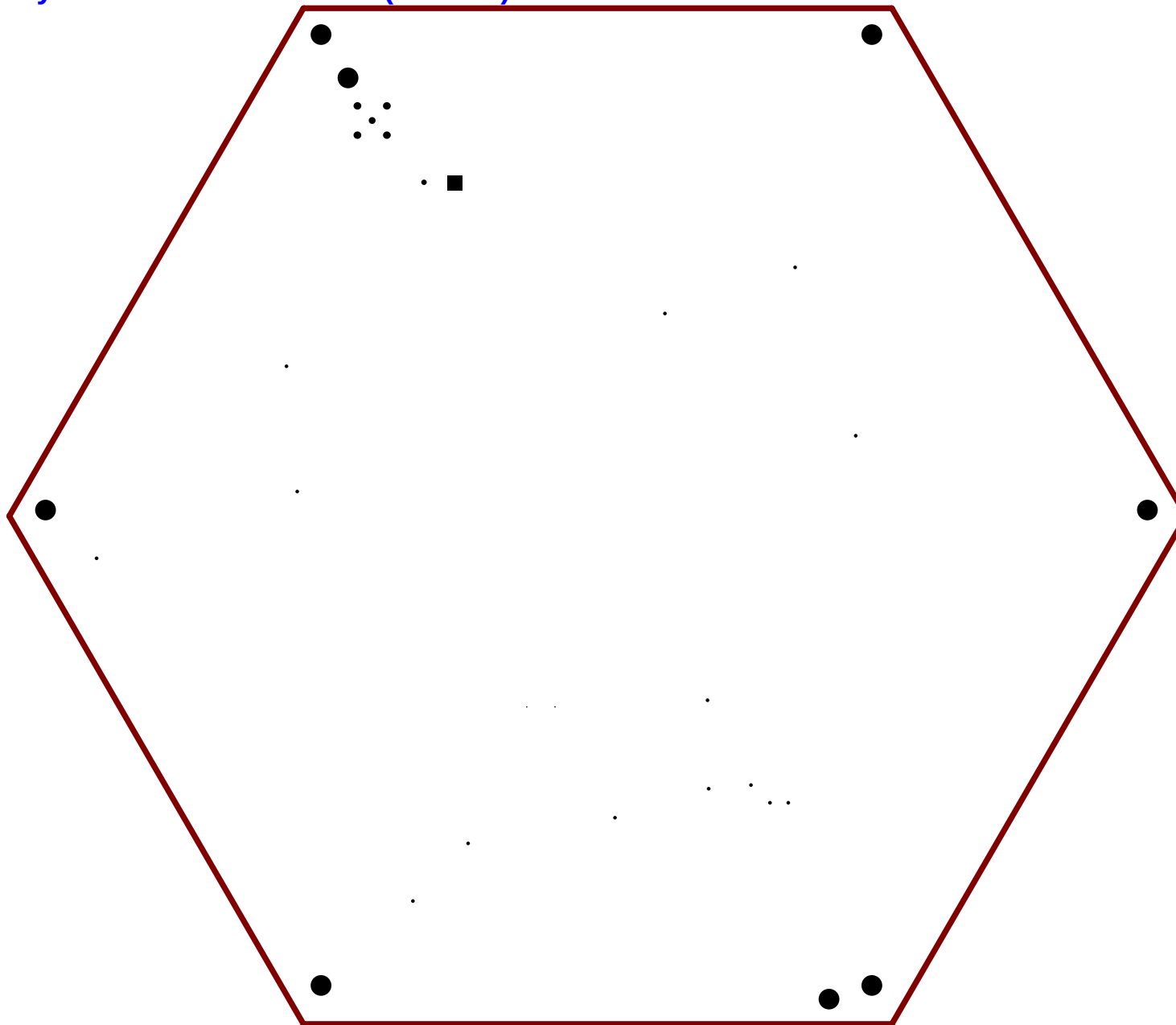


## Appendix F: PCB Layout

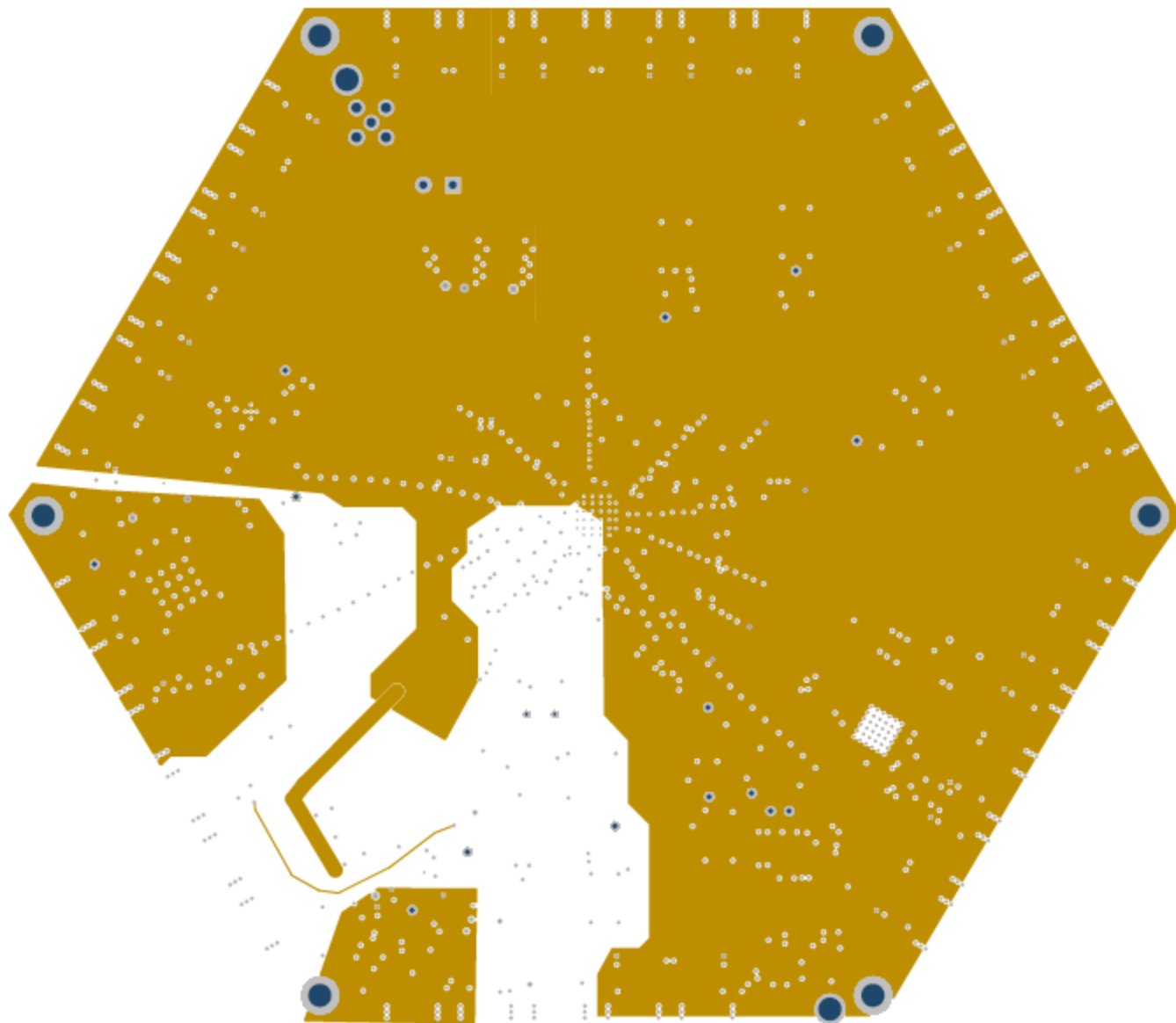
### Layer #1 – Top



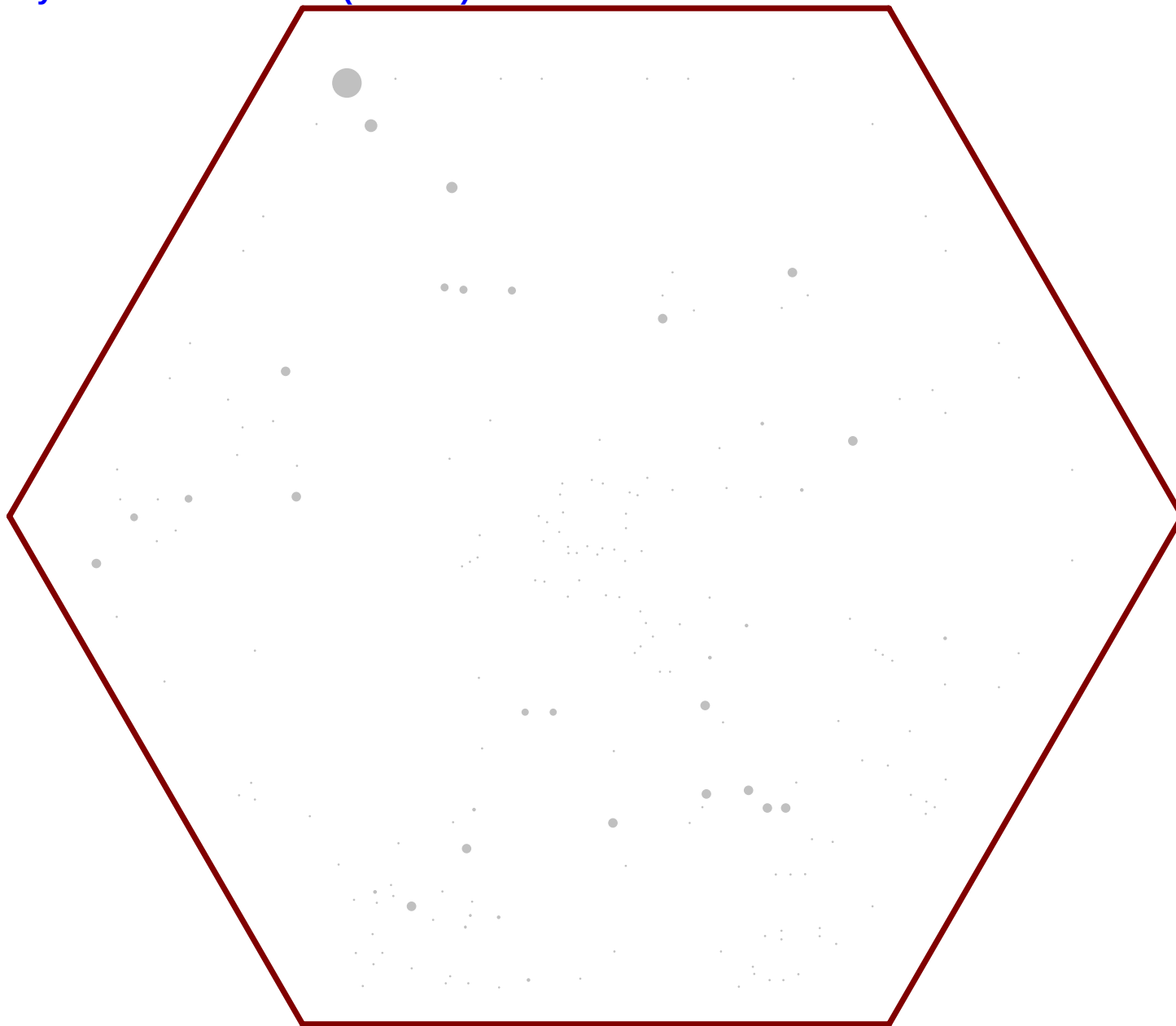
## Layer #2 – RF Ground Plane (Inverted)



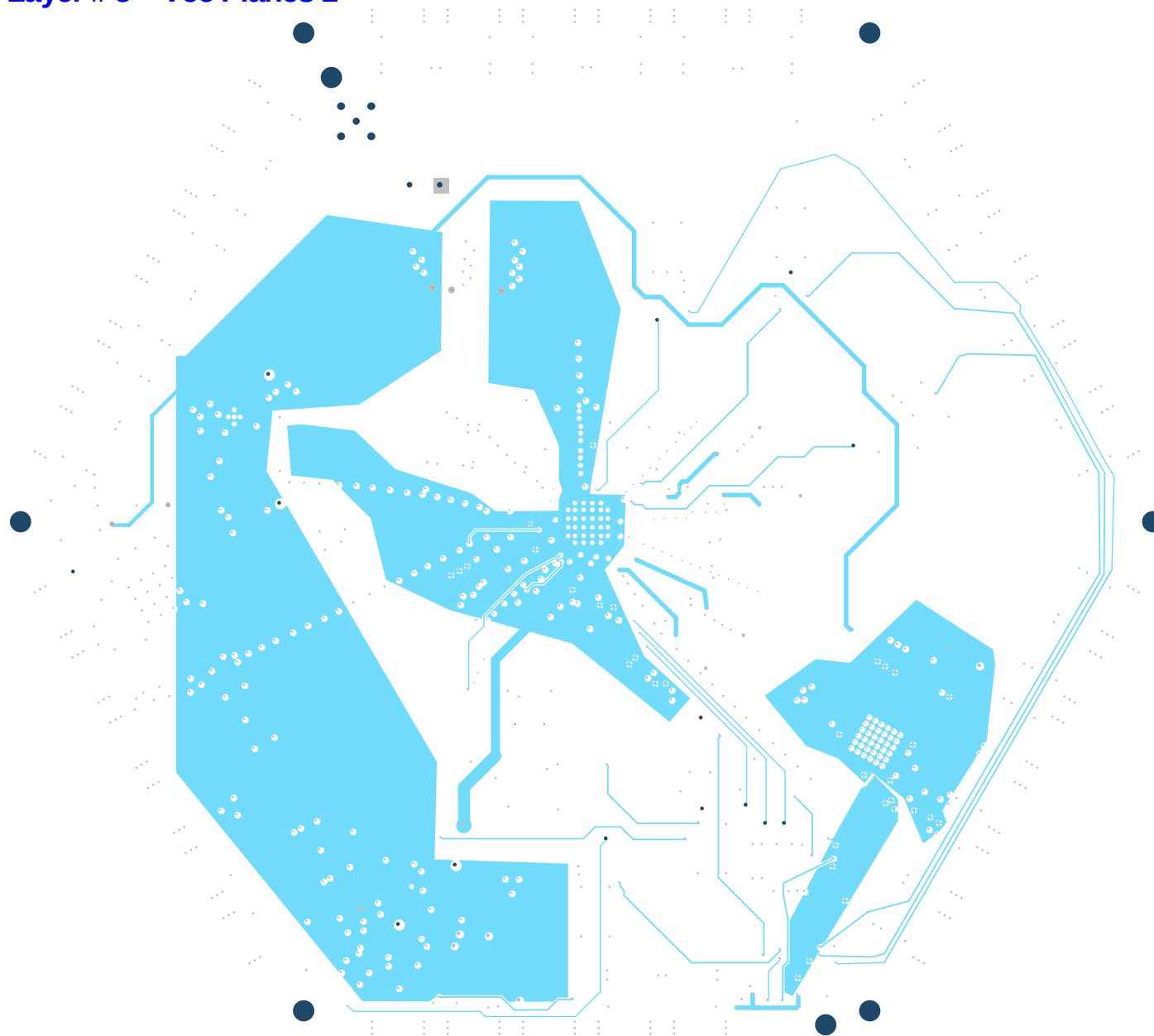
## Layer #3 – Vcc Planes



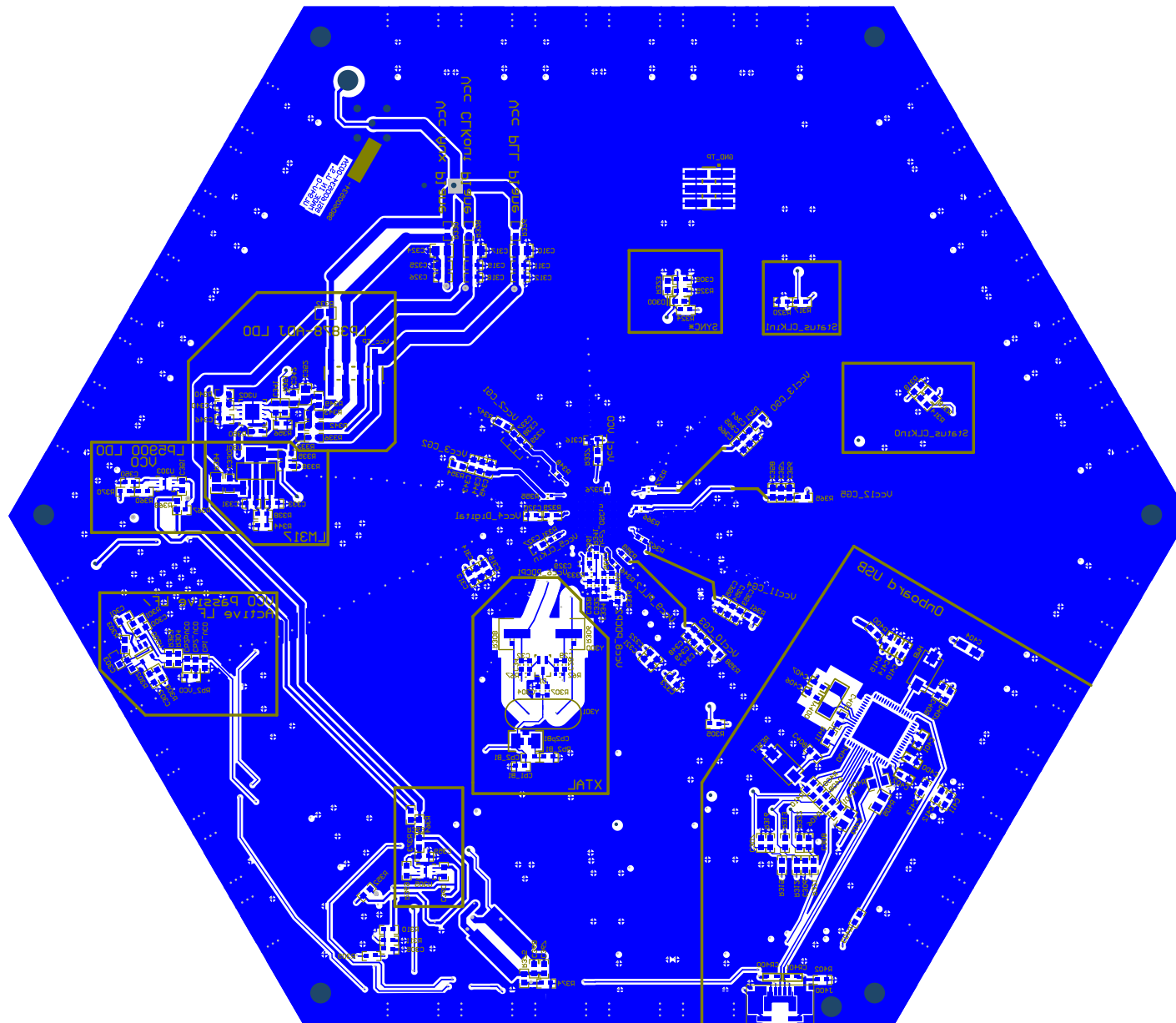
## Layer #4 – Ground Plane (Inverted)



## Layer # 5 – Vcc Planes 2

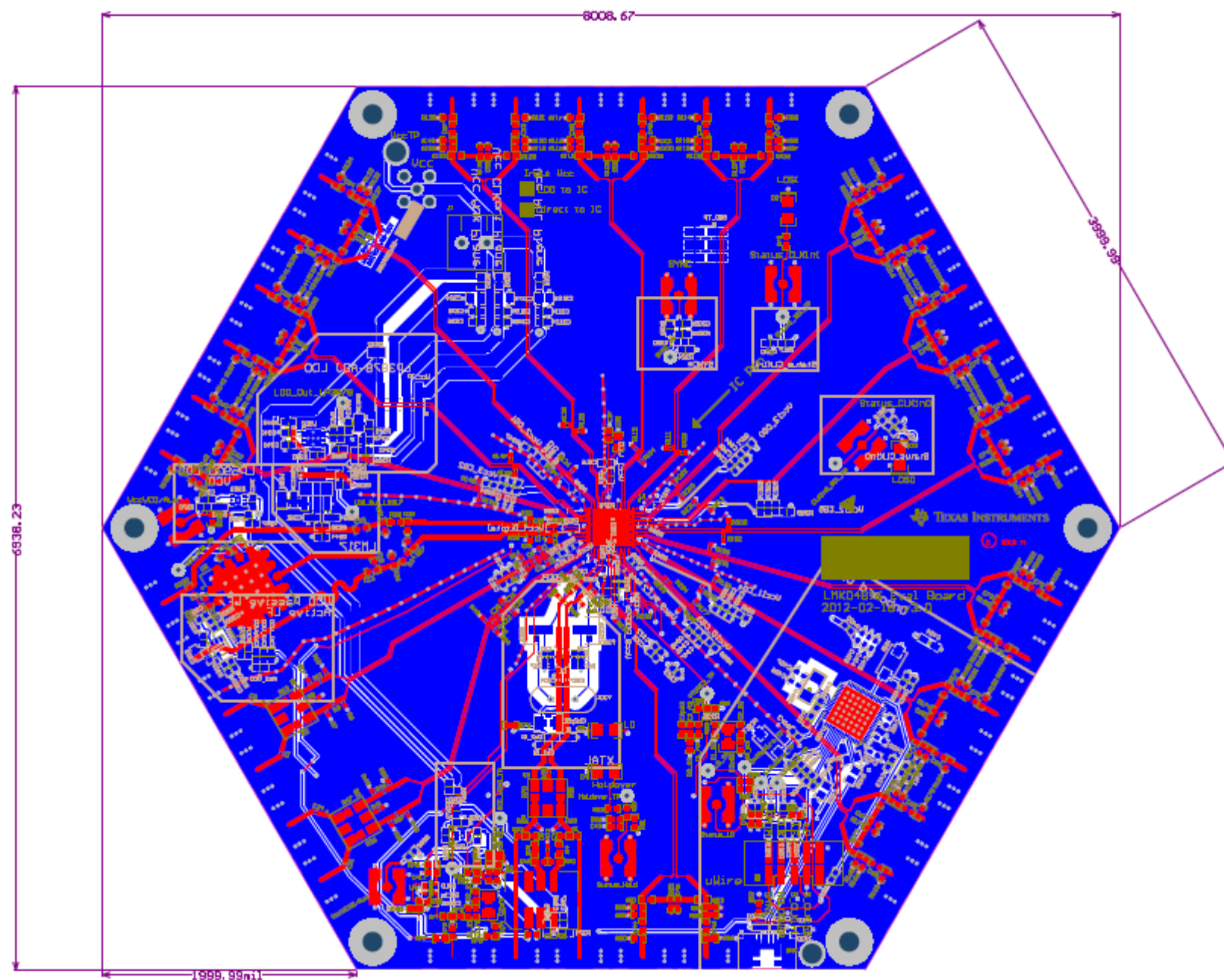


## Layer #6 – Bottom



## Layers #1 and 6 – Top and Bottom (Composite)



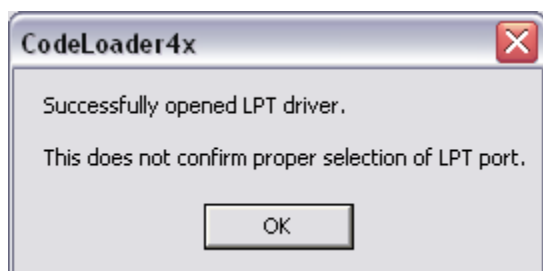


## Appendix G: Properly Configuring LPT Port

When trying to solve any communications issue, it is most convenient to verify communication by programming the POWERDOWN bit to confirm normal or low supply current consumption of the evaluation board.

### LPT Driver Loading

The parallel port must be configured for proper operation. To confirm that the LPT port driver is successfully loading click “LPT/USB” → “Check LPT.” If the driver properly loads then the following message is displayed:



**Figure 18: Successfully Opened LPT Driver**

*Successful loading of LPT driver does not mean LPT communications in CodeLoader are setup properly. The proper LPT port must be selected and the LPT port must not be in an improper mode.*

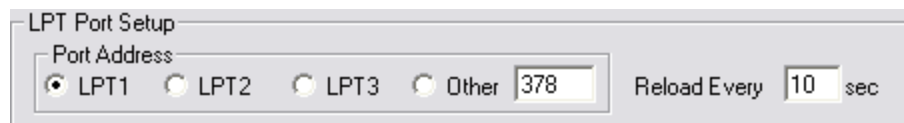
The PC must be rebooted after install for LPT support to work properly.

### Correct LPT Port/Address

To determine the correct LPT port in Windows, open the device manager (On Windows XP, Start → Settings → Control Panel → System → Hardware tab → Device Manager) and check the LPT port under the Ports (COM & LPT) node of the tree. It can be helpful to confirm that the LPT port is mapped to the expected port address, for instance to confirm that LPT1 is really mapped to address 0x378. This can be checked by viewing the Properties of the LPT1 port and viewing Resources tab to verify that the I/O Range starts at 0x378. CodeLoader expects the traditional port mapping:

| Port | Address |
|------|---------|
| LPT1 | 0x378   |
| LPT2 | 0x278   |
| LPT3 | 0x3BC   |

If a non-standard address is used, use the “Other” port address in CodeLoader and type in the port address in hexadecimal. It is possible to change the port address in the computer’s BIOS settings. The port address can be set in CodeLoader in the Port Setup tab as shown in Figure 19.



**Figure 19: Selecting the LPT Port Address**

## Correct LPT Mode

If communications are not working, then it is possible the LPT port mode is set improperly. It is recommended to use the simple, Output-only mode of the LPT port. This can be set in the BIOS of the computer. Common terms for this desired parallel port mode are “Normal,” “Output,” or “AT.” It is possible to enter BIOS setup during the initial boot up sequence of the computer.

## Appendix H: Troubleshooting Information

If the evaluation board is not behaving as expected, the most likely issues are...

- 1) Board communication issue
- 2) Incorrect Programming of the device
- 3) Setup Error

Refer to this checklist for a practical guide on identifying/exposing possible issues.

### 1) Confirm Communications

Refer to Appendix G: Properly Configuring LPT Port to troubleshoot this item.

Remember to load device with Ctrl+L.

### 2) Confirm PLL1 operation/locking

- 1) Program LD\_MUX = "PLL1\_R/2"
- 2) Confirm that LD pin output is half the expected phase detector frequency of PLL1.
  - i. If not, examine CLKIn\_SEL programming.
  - ii. If not, examine CLKIn0\_BUFTYPE / CLKIn1\_BUFTYPE.
  - iii. If not, examine PLL1 register R programming.
  - iv. If not, examine physical CLKIn input.
- 3) Program LD\_MUX = "PLL1\_N/2"
- 4) Confirm that LD pin output is half the expected phase detector frequency of PLL1.
  - i. If not, examine PLL1 register N programming.
  - ii. If not, examine physical OSCin input.

Naturally, the output frequency of the above two items, PLL 1 R Divider/2 and PLL 1 N Divider /2, on LD pin should be the same frequency.

- 5) Program LD\_MUX = "PLL1\_DLD"
- 6) Confirm the LD pin output is high.
  - i. If high, then PLL1 is locked, continue to PLL2 operation/locking.
- 7) If LD pin output is low, but the frequencies are the same, it is possible that excessive leakage on Vtune pin is causing the digital lock detect to not activate. By default PLL2 waits for the digital lock detect to go high before allowing PLL2 and the integrated VCO to lock. Different VCXO models have different input leakage specifications. High leakage, low PLL1 phase detector frequencies, and low PLL1 charge pump current settings can cause the PLL1 charge pump to operate longer than the digital lock detect timeout which allows the device to lock, but prevents the digital lock detect from activating.
  - i. Redesign PLL1 loop filter with higher phase detector frequency
  - ii. Redesign PLL1 loop filter with higher charge pump current
  - iii. Isolate VCXO tuning input from PLL1 charge pump with an op amp.

### 3) Confirm PLL2 operation/locking

- 1) Program LD\_MUX = "PLL2\_R/2"
- 2) Confirm that LD pin output is half the expected phase detector frequency of PLL2.
  - i. If not, examine PLL2\_R programming.
  - ii. If not, examine physical OSCin input.
- 3) Program LD\_MUX = "PLL2\_N/2"
- 4) Confirm that LD pin output is half the expected phase detector frequency of PLL2.
  - i. If not, confirm OSCin\_FREQ is programmed to OSCin frequency.
  - ii. If not, examine PLL2\_N programming.

Naturally, the output frequency of the above two items should be the same frequency.

- 5) Program LD\_MUX = "PLL2 DLD"
- 6) Confirm the LD pin output is high.
- 7) Program LD\_MUX = "PLL1 & PLL2 DLD"
- 8) Confirm the LD pin output is high.

## EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/ kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit [www.ti.com/esh](http://www.ti.com/esh) or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

Mailing Address: Texas Instruments Post Office Box 655303 Dallas, Texas 75265

Copyright 2012, Texas Instruments Incorporated

## REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

### General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this

is strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

### **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

#### **Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

#### **FCC Interference Statement for Class B EVM devices**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### **For EVMs annotated as IC – INDUSTRY CANADA Compliant**

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **Concerning EVMs including radio transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

### **Concerning EVMs including detachable antennas**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

~

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

### **Concernant les EVMs avec appareils radio**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

### **Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## **Important Notice for Users of this Product in Japan]**

### **This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan!**

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

(1) Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,



(2) Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or

(3) Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product.

Also, please do not transfer this product, unless you give the same notice above to the transferee.

Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

**Texas Instruments Japan Limited**

**(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan**

<http://www.tij.co.jp>

## 【ご使用にあたっての注意】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

(1) 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。

(2) 実験局の免許を取得後ご使用いただく。

(3) 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿6丁目24番1号

西新宿三井ビル

<http://www.tij.co.jp>



# EVALUATION BOARD/KIT/MODULE (EVM)

## WARNINGS, RESTRICTIONS AND DISCLAIMERS

**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

**Your Sole Responsibility and Risk.** You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

**Certain Instructions.** It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI. Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices.

Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

**Products**  
Amplifiers  
Audio

**Applications**  
[amplifier.ti.com](http://amplifier.ti.com)  
[www.ti.com/audio](http://www.ti.com/audio)

|                    |                                                                          |
|--------------------|--------------------------------------------------------------------------|
| Data Converters    | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>           |
| Automotive         | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| DSP                | <a href="http://dsp.ti.com">dsp.ti.com</a>                               |
| Broadband          | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Interface          | <a href="http://interface.ti.com">interface.ti.com</a>                   |
| Digital Control    | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Logic              | <a href="http://logic.ti.com">logic.ti.com</a>                           |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Power Mgmt         | <a href="http://power.ti.com">power.ti.com</a>                           |
| Optical Networking | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Microcontrollers   | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>       |
| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
| RFID               | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                     |
| Telephony          | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
| Low Power          | <a href="http://www.ti.com/lpw">www.ti.com/lpw</a>                       |
| Video & Imaging    | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
| Wireless           | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2007, Texas Instruments Incorporated