life.augmented

STM32L100x6/8/B-A

Ultra-low-power 32-bit MCU ARM[®]-based Cortex[®]-M3, 128KB Flash, 16KB SRAM, 2KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.8 V to 3.6 V power supply
 - -40°C to 85°C temperature range
 - 0.28 μA Standby mode (2 wakeup pins)
 - 1.11 µA Standby mode + RTC
 - 0.44 μA Stop mode (16 wakeup lines)
 - 1.38 µA Stop mode + RTC
 - 10.9 μA Low-power Run mode
 - 185 µA/MHz Run mode
 - 10 nA ultra-low I/O leakage
 - < 8 µs wakeup time</p>
- Core: ARM[®] Cortex[®]-M3 32-bit CPU
 - From 32 kHz up to 32 MHz max
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - Memory protection unit
- · Reset and supply management
 - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 24 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High Speed Internal 16 MHz
 - Internal low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz
 - PLL for CPU clock and USB (48 MHz)
- · Pre-programmed bootloader
 - USART supported
- Development support
 - Serial wire debug supported
 - JTAG and trace supported
- Up to 51 fast I/Os (42 I/Os 5V tolerant), all mappable on 16 external interrupt vectors





- Memories
 - Up to 128 Kbytes of Flash memory with ECC
 - Up to 16 Kbytes of RAM
 - Up to 2 Kbytes of true EEPROM with ECC
 - 20-byte backup register
- LCD Driver for up to 8x28 segments
 - Support contrast adjustment
 - Support blinking mode
 - Step-up converter on board
- Rich analog peripherals (down to 1.8 V)
 - 12-bit ADC 1 Msps up to 24 channels
 - 12-bit DAC 2 channels with output buffers
 - 2x ultra-low-power comparators (window mode and wakeup capability)
- DMA controller 7x channels
- 8x peripheral communication interfaces
 - 1x USB 2.0 (internal 48 MHz PLL)
 - 3x USART (ISO 7816, IrDA)
 - 2x SPI 16 Mbit/s
 - 2x I2C (SMBus/PMBus)
- 10x timers: 6x 16-bit with up to 4 IC/OC/PWM channels, 2x 16-bit basic timers, 2x watchdog timers (independent and window)
- · CRC calculation unit

Table 1. Device summary

Reference	Part number
STM32L100C6-A, STM32L100R8-A, STM32L100RB-A	STM32L100C6xxA, STM32L100R8xxA, STM32L100RBxxA

Contents STM32L100x6/8/B-A

Contents

1	Intro	duction	1	. 8
2	Desc	ription		. 9
	2.1	Device	overview	10
	2.2	Ultra-lo	ow-power device continuum	.11
		2.2.1	Performance	. 11
		2.2.2	Shared peripherals	. 11
		2.2.3	Common system strategy	. 11
		2.2.4	Features	. 11
3	Fund	ctional c	overview	12
	3.1	Low-po	ower modes	13
	3.2	$ARM^{ exttt{@}}$	Cortex®-M3 core with MPU	17
	3.3	Reset	and supply management	18
		3.3.1	Power supply schemes	. 18
		3.3.2	Power supply supervisor	. 18
		3.3.3	Voltage regulator	. 19
		3.3.4	Boot modes	. 19
	3.4	Clock r	management	20
	3.5	Low-po	ower real-time clock and backup registers	22
	3.6	GPIOs	(general-purpose inputs/outputs)	22
	3.7	Memor	ries	23
	3.8	DMA (d	direct memory access)	23
	3.9	LCD (li	iquid crystal display)	24
	3.10	ADC (a	analog-to-digital converter)	24
		3.10.1	Internal voltage reference (V _{REFINT})	. 24
	3.11	DAC (d	digital-to-analog converter)	25
	3.12	Ultra-lo	ow-power comparators and reference voltage	25
	3.13	Routing	g interface	25
	3.14	·	and watchdogs	
	3	3.14.1	General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)	
		3.14.2	Basic timers (TIM6 and TIM7)	
		3.14.3	SysTick timer	
			•	



		3.14.4	Independent watchdog (IWDG)
		3.14.5	Window watchdog (WWDG)28
	3.15	Commi	unication interfaces
		3.15.1	I ² C bus
		3.15.2	Universal synchronous/asynchronous receiver transmitter (USART) 28
		3.15.3	Serial peripheral interface (SPI)
		3.15.4	Universal serial bus (USB)
	3.16	CRC (d	cyclic redundancy check) calculation unit
	3.17	Develo	pment support
4	Pin d	lescript	ions
5	Mam	ori mai	oning 40
3	MEIII	ory map	oping
6	Elect	trical ch	aracteristics41
	6.1	Parame	eter conditions41
		6.1.1	Minimum and maximum values
		6.1.2	Typical values41
		6.1.3	Typical curves41
		6.1.4	Loading capacitor41
		6.1.5	Pin input voltage41
		6.1.6	Power supply scheme42
		6.1.7	Optional LCD power supply scheme43
		6.1.8	Current consumption measurement43
	6.2	Absolu	te maximum ratings
	6.3	Operat	ing conditions45
		6.3.1	General operating conditions
		6.3.2	Embedded reset and power control block characteristics 46
		6.3.3	Embedded internal reference voltage
		6.3.4	Supply current characteristics
		6.3.5	Wakeup time from Low-power mode
		6.3.6	External clock source characteristics 60
		6.3.7	Internal clock source characteristics
		6.3.8	PLL characteristics
		6.3.9	Memory characteristics
		6.3.10	EMC characteristics
		6.3.11	Electrical sensitivity characteristics

		6.3.12	I/O current injection characteristics
		6.3.13	I/O port characteristics
		6.3.14	NRST pin characteristics
		6.3.15	TIM timer characteristics
		6.3.16	Communication interfaces
		6.3.17	12-bit ADC characteristics
		6.3.18	DAC electrical specifications
		6.3.19	Comparator
		6.3.20	LCD controller
7	Pack	age info	ormation
	7.1	LQFP6	4 10 x 10 mm, 64-pin low-profile quad flat package information 92
	7.2	UFQFF	PN48 7 x 7 mm, 0.5 mm pitch, package information 95
	7.3	Therma	al characteristics
		7.3.1	Reference document
8	Orde	ring info	ormation 100
9	Revi	sion his	tory

STM32L100x6/8/B-A List of tables

List of tables

Table 1.	Device summary	1
Table 2.	Ultra-low-power STM32L100x6/8/B-A device features and peripheral counts	10
Table 3.	Functionalities depending on the operating power supply range	14
Table 4.	CPU frequency range depending on dynamic voltage scaling	
Table 5.	Working mode-dependent functionalities (from Run/active down to standby)	
Table 6.	VLCD rail decoupling	
Table 7.	Timer feature comparison	
Table 8.	Legend/abbreviations used in the pinout table	
Table 9.	STM32L100x6/8/B-A pin definitions	
Table 10.	Alternate function input/output	
Table 11.	Voltage characteristics	
Table 12.	Current characteristics	
Table 13.	Thermal characteristics.	
Table 14.	General operating conditions	
Table 15.	Embedded reset and power control block characteristics.	
Table 16.	Embedded internal reference voltage calibration values	
Table 10.	Embedded internal reference voltage Calibration values	
Table 17.	Current consumption in Run mode, code with data processing running from Flash	
Table 16.		
	Current consumption in Run mode, code with data processing running from RAM	
Table 20.	Current consumption in Sleep mode	
Table 21.	Current consumption in Low power run mode	
Table 22.	Current consumption in Low power sleep mode	
Table 23.	Typical and maximum current consumptions in Stop mode	
Table 24.	Typical and maximum current consumptions in Standby mode	
Table 25.	Peripheral current consumption	
Table 26.	Low-power mode wakeup timings	
Table 27.	High-speed external user clock characteristics	
Table 28.	Low-speed external user clock characteristics	
Table 29.	HSE oscillator characteristics	
Table 30.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	
Table 31.	HSI oscillator characteristics	
Table 32.	LSI oscillator characteristics	
Table 33.	MSI oscillator characteristics	66
Table 34.	PLL characteristics	67
Table 35.	RAM and hardware registers	68
Table 36.	Flash memory and data EEPROM characteristics	68
Table 37.	Flash memory, data EEPROM endurance and data retention	68
Table 38.	EMS characteristics	69
Table 39.	EMI characteristics	70
Table 40.	ESD absolute maximum ratings	70
Table 41.	Electrical sensitivities	
Table 42.	I/O current injection susceptibility	71
Table 43.	I/O static characteristics	
Table 44.	Output voltage characteristics	
Table 45.	I/O AC characteristics	
Table 46.	NRST pin characteristics	
Table 47.	TIMx characteristics	
Table 48.	I ² C characteristics.	
· · · ·		



List of tables STM32L100x6/8/B-A

Table 49.	SCL frequency (f _{PCLK1} = 32 MHz, V _{DD} = VDD_I2C = 3.3 V)	78
Table 50.	SPI characteristics	79
Table 51.	USB startup time	81
Table 52.	USB DC electrical characteristics	
Table 53.	USB: full speed electrical characteristics	82
Table 54.	ADC clock frequency	83
Table 55.	ADC characteristics	
Table 56.	ADC accuracy	84
Table 57.	Maximum source impedance R _{AIN} max	
Table 58.	DAC characteristics	
Table 59.	Comparator 1 characteristics	89
Table 60.	Comparator 2 characteristics	90
Table 61.	LCD controller characteristics	91
Table 62.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data	92
Table 63.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data	96
Table 64.	Thermal characteristics	98
Table 65.	Ordering information scheme	100
Table 66.	Document revision history	



STM32L100x6/8/B-A List of figures

List of figures

Figure 1.	Ultra-low-power STM32L100x6/8/B-A block diagram	12
Figure 2.	Clock tree	
Figure 3.	STM32L100RxxxA LQFP64 pinout	30
Figure 4.	STM32L100C6xxA UFQFPN48 pinout	31
Figure 5.	Memory map	40
Figure 6.	Pin loading conditions	41
Figure 7.	Pin input voltage	41
Figure 8.	Power supply scheme	42
Figure 9.	Optional LCD power supply scheme	43
Figure 10.	Current consumption measurement scheme	43
Figure 11.	High-speed external clock source AC timing diagram	60
Figure 12.	Low-speed external clock source AC timing diagram	61
Figure 13.	HSE oscillator circuit diagram	63
Figure 14.	Typical application with a 32.768 kHz crystal	64
Figure 15.	I/O AC characteristics definition	
Figure 16.	Recommended NRST pin protection	76
Figure 17.	I ² C bus AC waveforms and measurement circuit	
Figure 18.	SPI timing diagram - slave mode and CPHA = 0	80
Figure 19.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	
Figure 20.	SPI timing diagram - master mode ⁽¹⁾	
Figure 21.	USB timings: definition of data signal rise and fall time	
Figure 22.	ADC accuracy characteristics	
Figure 23.	Typical connection diagram using the ADC	85
Figure 24.	Maximum dynamic current consumption on V _{DDA} supply pin during ADC	
	conversion	
Figure 25.	12-bit buffered /non-buffered DAC	
Figure 26.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline	
Figure 27.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint	
Figure 28.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example	
Figure 29.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline	
Figure 30.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint	
Figure 31.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example	
Figure 32.	Thermal resistance	98



Introduction STM32L100x6/8/B-A

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L100x6/8/B-A ultra-low-power ARM[®] Cortex[®]-M3 based microcontrollers product line.

The ultra-low-power STM32L100x6/8/B-A microcontroller family includes devices in 2 different package types: 48 or 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L100x6/8/B-A microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- · PC peripherals, gaming, GPS and sport equipment
- · Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L100x6/8/B-A datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview.

Both documents are available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M3 core please refer to the Cortex[®]-M3 Technical Reference Manual, available from the ARM website.

Figure 1 shows the general block diagram of the device family.

Caution:

This datasheet does not apply to:

- STM32L100x6/8/B

covered by a separate datasheet.

STM32L100x6/8/B-A Description

2 Description

The ultra-low-power STM32L100x6/8/B-A devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L100x6/8/B-A devices contain standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs and a USB.

They also include a real-time clock with sub-second counting and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L100x6/8/B-A devices operate from a 1.8 to 3.6 V power supply. They are available in the -40 to +85 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.





Description STM32L100x6/8/B-A

2.1 Device overview

Table 2. Ultra-low-power STM32L100x6/8/B-A device features and peripheral counts

Peripheral		STM32L100C6xxA	STM32L100R8/BxxA				
Flash (Kbytes)		32	64	128			
Data EEPROM (K	(bytes)		2				
RAM (Kbytes)		4	8	16			
Timers	General- purpose		6				
	Basic		2				
	SPI		2				
Communication	I ² C		2				
interfaces	USART	3					
	USB	1					
GPIOs		37 51					
12-bit synchroniz Number of chann		1 1 1 1 1 1 1 1 1 20 channels					
12-bit DAC Number of chann	nels		2 2				
LCD COM x SEG		4x16	4x32 8x28				
Comparator		2					
Max. CPU frequency		32 MHz					
Operating voltage		1.8 V to 3.6 V					
Operating temperatures		Ambient temperatures: -40 to +85 °C Junction temperature: -40 to +105°C					
Packages		UFQFPN48	QFPN48 LQFP64				

STM32L100x6/8/B-A Description

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From a proprietary 8-bit core up to the Cortex-M3, including the Cortex-M0+, the STM8Lx and STM32Lx series offer the best range of choices to meet your requirements in terms of ultra-low-power features. The STM32 Ultra-low-power series is an ideal fit for applications like gas/water meters, keyboard/mouse, or wearable devices for fitness and healthcare. Numerous built-in features like LCD drivers, dual-bank memory, low-power Run mode, op-amp, AES-128bit, DAC, crystal-less USB and many others, allow to build highly cost-optimized applications by reducing the BOM.

Note:

STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lx and STM32Lx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your existing applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-Low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xxx and STM32L1xxxx families use a common architecture:

- Common power supply range from 1.8 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 512 Kbytes

Functional overview 3

Figure 1 shows the block diagram.

@V DD JTAG & SW POWER pbus V_{DD} = 1.8 V to 3.6 V VOLT. REG. NJTRST Cortex-M3 CPU JTDI JTCK / SWCLK JTMS / SWDAT 128 KB Flash F_{max}: 32 MHz 2 KB data EEPROM JTDO MPU NVIC 16 KB @VDDA GPDMA AHBPCLK APBPCLK HCLK FCLK OSC_IN OSC_OUT XTAL OSC 7 channels 1-24 MHz clock NRST Supply RC MS IWDG VREF OUTPUT BOR/V_{REFIN} Standby interface OSC32_IN XTAL32 kHz Comp1 OSC32_OUT COMP2_IN-/IN+ Comp2 — RTC_AFIN RTC_OUT, RTC_TS, RTC_TAMP RTC AWU Power-down PA[15:0] < GPIOA Backup interface GPIOB PB[15:0] LCD step-up _ V_{LCD} = 2.5 V to 3.6 V PC[15:0] > 4 Channels PD[2] GPIOD TIM3 4 Channels PH[1:0] GPIOH TIM4 4 Channels RX. TX. CTS. RTS. AHB/ AHB/ APB1 USART 2 RX, TX, CTS, RTS, EXT. IT 51 AF USART 3 MOSI, MISO, SCK, NSS SPI2 SPI1 SCK. NSS as AF SCL, SDA RX, TX, CTS, RTS, SmartCard as AF I2C1 USART 1 as AF SCL, SDA, SMBus, PMBus as AF @VDDA I2C2 12-bit ADC 20 AF USB RAM 512B USB 2.0 FS devi USB_DM WWDG LCD 8x28 (4x32) BASIC TIMERS 2 Channels TIM9 DAC_OUT1 as TIM6 12-bit DAC1 1 Channel TIM10 DAC_OUT2 as AF TIM7 12-bit DAC2 1 Channel TIM11 MSv32067V3

Figure 1. Ultra-low-power STM32L100x6/8/B-A block diagram

1. AF = alternate function on I/O port pin.



3.1 Low-power modes

The ultra-low-power STM32L100x6/8/B-A devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 2.0-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 18* for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to Table 18 for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 18* for consumption.

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

• Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Sleep mode power consumption: refer to Table 20.

• Low-power Run mode

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the MSI range 0 or MSI range 1 clock range (maximum 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In the low-power Run mode, the clock frequency and the number of enabled peripherals are both limited.

Low-power Run mode consumption: refer to *Table 21*.

• Low-power Sleep mode

This mode is achieved by entering the Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In the low-power Sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

Low-power Sleep mode consumption: refer to Table 22.

• Stop mode with RTC

Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

Stop mode without RTC

Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI



line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to Table 23.

Standby mode with RTC

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the two WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

• Standby mode without RTC

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC CSR).

The device exits Standby mode in $60 \mu s$ when an external reset (NRST pin) or a rising edge on one of the two WKUP pin occurs.

Standby mode consumption: refer to *Table 24*.

The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range ⁽¹⁾					
Operating power supply range	DAC and ADC operation USB		Dynamic voltage scaling range			
V_{DD} = 1.8 to 2.0 $V^{(2)}$	Conversion time up to 500 Ksps	Not functional	Range 2 or Range 3			
V _{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional ⁽³⁾	Range 1, Range 2 or Range 3			
V _{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional ⁽³⁾	Range 1, Range 2 or Range 3			

The GPIO speed also depends from VDD voltage and the user has to refer to Table 45: I/O AC characteristics for more information about I/O speed.

DocID025966 Rev 6

Note:

14/103

The CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.

^{3.} Should be USB-compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Table 5. Working mode-dependent functionalities (from Run/active down to standby)

	mode dep		Low-	Low-		Stop	Standby	
lps	Run/Active	Sleep	power Run	power Sleep		Wakeup capability		Wakeup capability
CPU	Υ	-	Y	-	-	-	-	-
Flash	Υ	Y	Y	-	-	-	-	-
RAM	Υ	Y	Y	Υ	Υ	-	-	-
Backup Registers	Y	Y	Y	Y	Υ	-	Υ	-
EEPROM	Υ	Y	Υ	Υ	Υ	-	-	-
Brown-out reset (BOR)	Υ	Υ	Y	Y	Y	Y	Y	-
DMA	Υ	Y	Y	Y	-	-	-	-
Programmable Voltage Detector (PVD)	Υ	Υ	Y	Y	Υ	Y	Y	-
Power On Reset (POR)	Υ	Y	Y	Y	Y	Υ	Υ	-
Power Down Rest (PDR)	Y	Y	Y	Y	Y	-	Υ	-
High Speed Internal (HSI)	Y	Υ	-	-	-	-	-	-
High Speed External (HSE)	Y	Y	-	-	-	-	-	-
Low Speed Internal (LSI)	Υ	Y	Y	Y	Y	-	Υ	-
Low Speed External (LSE)	Υ	Y	Y	Y	Y	-	Υ	-
Multi-Speed Internal (MSI)	Υ	Y	Y	Y	-	-	-	-
Inter-Connect Controller	Υ	Y	Y	Y	-	-	-	-
RTC	Y	Y	Y	Y	Υ	Y	Υ	-
RTC Tamper	Υ	Y	Y	Y	Υ	Y	Υ	Y
Auto Wakeup (AWU)	Υ	Υ	Y	Υ	Y	Υ	Υ	Y
LCD	Υ	Y	Y	Y	Υ	-	ı	-
USB	Y	Y	-	-	-	Y	-	-
USART	Y	Y	Y	Y	Υ	(1)	-	-
SPI	Υ	Y	Y	Y	-	-	-	-
I2C	Y	Y	-	-	-	(1)	-	-
ADC	Υ	Y	-	-	-	-	-	-

16/103

Table 5. Working mode-dependent functionalities (from Run/active down to standby) (continued)

			Low-	Low-	Stop		Standby		
lps	Run/Active	Sleep	power Run	power Sleep		Wakeup capability		Wakeup capability	
DAC	Υ	Y	Υ	Υ	Υ	-	-	-	
Comparators	Y	Y	Y	Y	Υ	Y	-	-	
16-bit Timers	Y	Y	Y	Y	-	-	-	-	
IWDG	Y	Y	Y	Y	Υ	Y	Υ	Y	
WWDG	Y	Y	Y	Y	-	-	-	-	
Systick Timer	Y	Y	Y	Y	-	-	-	-	
GPIOs	Y	Y	Y	Y	Υ	Y	-	2 pins	
Wakeup time to Run mode	0 μs	0.4 μs	3 µs	46 µs		< 8 µs		58 µs	
						43 μΑ (No) V _{DD} =1.8 V	0.27 μA (No RTC) V _{DD} =1.8 V		
Consumption	185 μA/MHz 36.9 μ <i>A</i>	Down to	Down to	Down to	1.13 μA (with RTC) V _{DD} =1.8 V		0.87 μA (with RTC) V _{DD} =1.8 V		
V _{DD} =1.8V to 3.6V (Typ)		(from Flash)	10.9 µA	5.5 μA	0.44 μA (No RTC) V _{DD} =3.0 V		0.28 μA (No RTC) V _{DD} =3.0 V		
						8 μA (with) V _{DD} =3.0 V		1 μA (with) V _{DD} =3.0 V	

The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L100x6/8/B-A devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L100x6/8/B-A devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator.
 Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL.

 V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

After the V_{DD} threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently.

BOR ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V.

18/103 DocID025966 Rev 6

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See the application note "STM32 microcontroller system memory boot mode" (AN2606) for details.

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- Master clock source: three different clock sources can be used to drive the master clock:
 - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
 The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- RTC and LCD clock sources: the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- Clock security system (CSS): this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- Clock-out capability (MCO: microcontroller clock output): it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

20/103 DocID025966 Rev 6



MSI RC MSI ADCCLK to ADC Peripheral clock enable 16 MHz HSI RC HSI USBCI K PLLVCO/2 PLLSRC PLLMUL to USB interface SW PLLDIV x3,x4,x6,x8 HSI SYSCLK 32 MHz max /2,/3,/4 x12,x16,x24 OSC_OUT PLLCLK x32,x48 1-24 MHz HSE HSE OSC OSC_IN CSS HCLK to AHB bus, core, memory and DMA 32 MHz max Clock Enable → to Cortex System timer /8 ▶ FCLK Cortex free running clock AHB APB1 PCLK1 to APB1 32 MHz max Prescale Prescaler /1, 2..512 /1, 2, 4, 8, 16 Peripheral Clock peripherals Enable If (APB1 prescaler =1) x1 to TIM2,3,4,6 and 7 else x2 Peripheral Clock APB2 32 MHz max PCLK2 Prescaler peripherals to APB2 /1, 2, 4, 8, 16 Peripheral Clock Enable to TIM9, 10, and 11 If (APB2 prescaler =1) x else x2 TIMxCLK TIMx0 Peripheral Clock Enable Timer 9, 10, 11 ETR OSC32_IN to RTC LSE OSC RTCCLK 32.768 kHz OSC32_OUT to LCD RTCSEL[1:0] to Independent Watchdog (IWDG) LSI RC **IWDGCLK** Legend: HSE = High-speed external clock signal SYSCLK HSI = High-speed internal clock signalHSI /1,2,4, LSI = Low-speed internal clock signal MCO 8,16 LSE = Low-speed external clock signal PLLCLK LSI LSE MSI = Multispeed internal clock signal MCOSEL ai17212c

Figure 2. Clock tree

3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation. The RTC can also be automatically corrected with a 50/60Hz stable power line.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization. A time stamp can record an external event occurrence, and generates an interrupt.

There are five 32-bit backup registers provided to store 20 bytes of user application data. They are cleared in case of tamper detection. Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 **GPIOs** (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.

22/103 DocID025966 Rev 6

3.7 Memories

The STM32L100x6/8/B-A devices have the following features:

Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).

- The non-volatile memory is divided into three arrays:
 - 32, 64 or 128 Kbytes of embedded Flash program memory
 - 2 Kbytes of data EEPROM
 - Options bytes

The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C , USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 32 segment terminals to drive up to 224 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{I CD} rail decoupling capability

		LOD		
		Pin		
	1/2	1/3	1/4	Pill
V _{LCDrail1}	1/2 V _{LCD}	2/3 V _{LCD}	1/2 V _{LCD}	PB2
V _{LCDrail2}	NA	1/3 V _{LCD}	1/4 V _{LCD}	PB12
V _{LCDrail3}	NA	NA	3/4 V _{LCD}	PB0

Table 6. V_{I CD} rail decoupling

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L100x6/8/B-A devices with up to 20 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It

24/103 DocID025966 Rev 6

enables accurate monitoring of the V_{DD} value. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode see *Table 17: Embedded internal reference voltage*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion

Eight DAC trigger inputs are used in the STM32L100x6/8/B-A devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L100x6/8/B-A devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
 - DAC output
 - External I/O
 - Internal reference voltage (V_{RFFINT}) or V_{RFFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of $1 \mu A$ typical).

3.13 Routing interface

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}



3.14 Timers and watchdogs

The ultra-low-power STM32L100x6/8/B-A devices include six general-purpose timers, two basic timers and two watchdog timers.

Table 7 compares the features of the general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.14.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L100x6/8/B-A devices (see *Table 7* for differences).

TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/down-counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.14.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit down-counter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I2C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.15.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.15.4 Universal serial bus (USB)

The STM32L100x6/8/B-A devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

28/103 DocID025966 Rev 6

3.16 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.17 Development support

Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Pin descriptions STM32L100x6/8/B-A

4 Pin descriptions

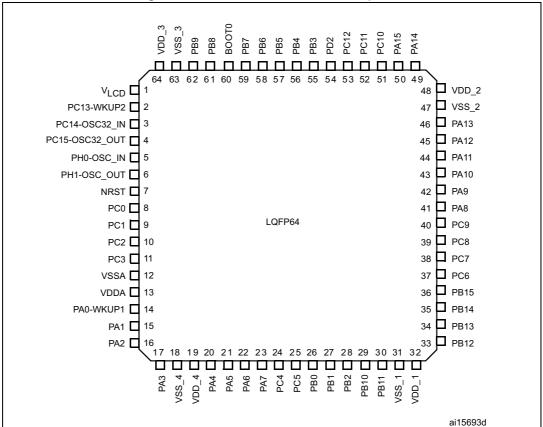


Figure 3. STM32L100RxxxA LQFP64 pinout

1. This figure shows the package top view.

STM32L100x6/8/B-A Pin descriptions

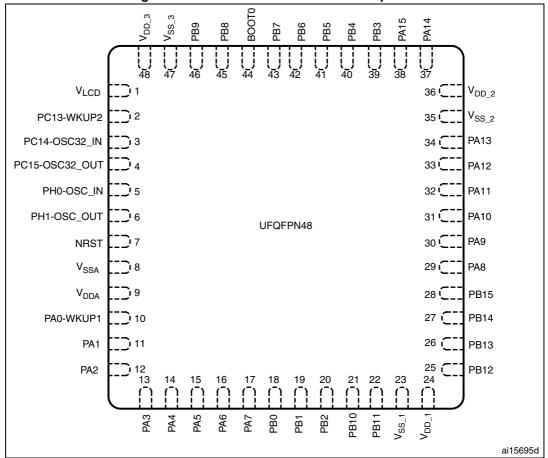


Figure 4. STM32L100C6xxA UFQFPN48 pinout

1. This figure shows the package top view.

Pin descriptions STM32L100x6/8/B-A

Table 8. Legend/abbreviations used in the pinout table

Na	me	Abbreviation	Definition					
Pin r	name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name						
		S	Supply pin					
Pin	type	I	Input only pin					
		I/O	Input / output pin					
		FT	5 V tolerant I/O					
I/O str	uoturo	TC	Standard 3.3 V I/O					
1/0 50	ucture	B Dedicated BOOT0 pin						
		RST Bidirectional reset pin with embedded weak pull-up resist						
No	tes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset						
	Alternate functions	Functions selected through GPIOx_AFR registers						
Pin functions	Additional functions	Functions direct	Functions directly selected/enabled through peripheral registers					

STM32L100x6/8/B-A Pin descriptions

Table 9. STM32L100x6/8/B-A pin definitions

Pi	ins							Pin function	s
LQFP64	UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions		
1	1	V_{LCD}	S	-	V_{LCD}	-	-		
2	2	PC13-WKUP2	I/O	FT	PC13	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/WKUP2		
3	3	PC14- OSC32_IN ⁽³⁾	I/O	TC	PC14	-	OSC32_IN		
4	4	PC15- OSC32_OUT	I/O	TC	PC15	-	OSC32_OUT		
5	5	PH0-OSC_IN ⁽⁴⁾	I/O	TC	PH0	-	OSC_IN		
6	6	PH1-OSC_OUT	I/O	TC	PH1	-	OSC_OUT		
7	7	NRST	I/O	RST	NRST	-	-		
8	ı	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP		
9	i	PC1	1/0	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP		
10	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP		
11	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP		
12	8	V _{SSA}	S	-	V _{SSA}	-	-		
13	9	V_{DDA}	S	-	V_{DDA}	-	-		
14	10	PA0-WKUP1	I/O	FT	PA0	USART2_CTS/ TIM2_CH1_ETR	WKUP1/ADC_IN0/ COMP1_INP		
15	11	PA1	I/O	FT	PA1	USART2_RTS/TIM2_CH2/ LCD_SEG0	ADC_IN1/ COMP1_INP		
16	12	PA2	I/O	FT	PA2	USART2_TX/TIM2_CH3/ TIM9_CH1/LCD_SEG1	ADC_IN2/ COMP1_INP		
17	13	PA3	I/O	TC	PA3	USART2_RX/TIM2_CH4/ TIM9_CH2/LCD_SEG2	ADC_IN3/ COMP1_INP		
18	ı	V _{SS_4}	S	ı	V _{SS_4}	-	-		
19	-	V _{DD_4}	S	-	V_{DD_4}	-	-		

Pin descriptions STM32L100x6/8/B-A

Table 9. STM32L100x6/8/B-A pin definitions (continued)

Pi	ins					Pin functions	S
LQFP64	UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
20	14	PA4	I/O	TC	PA4	SPI1_NSS/USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
21	15	PA5	I/O	TC	PA5	SPI1_SCK/TIM2_CH1_ETR	ADC_IN5/ DAC_OUT2/ COMP1_INP
22	16	PA6	I/O	FT	PA6	SPI1_MISO/TIM3_CH1/ LCD_SEG3/TIM10_CH1	ADC_IN6/ COMP1_INP
23	17	PA7	I/O	FT	PA7	SPI1_MOSI/TIM3_CH2/ LCD_SEG4/TIM11_CH1	ADC_IN7/ COMP1_INP
24	1	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
25	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
26	18	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ VREF_OUT
27	19	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
28	20	PB2	I/O	FT	PB2/BOOT1	BOOT1	-
29	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/ TIM2_CH3/ LCD_SEG10	-
30	22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX /TIM2_CH4/LCD_SEG11	-
31	23	V _{SS_1}	S	-	V _{SS_1}	-	-
32	24	V _{DD_1}	S	-	V _{DD_1}	-	-
33	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/ TIM10_CH1	ADC_IN18/ COMP1_INP/
34	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ LCD_SEG13/TIM9_CH1	ADC_IN19/ COMP1_INP

STM32L100x6/8/B-A Pin descriptions

Table 9. STM32L100x6/8/B-A pin definitions (continued)

Pi	ins				Pin functions	s	
LQFP64	UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
35	27	PB14	I/O	FT	PB14	SPI2_MISO/USART3_RTS/ LCD_SEG14/TIM9_CH2	ADC_IN20/ COMP1_INP
36	28	PB15	I/O	FT	PB15	SPI2_MOSI/LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
37	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
38	1	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
39	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
40	1	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
41	29	PA8	I/O	FT	PA8	USART1_CK/MCO/LCD_COM0	-
42	30	PA9	I/O	FT	PA9	USART1_TX/LCD_COM1	-
43	31	PA10	I/O	FT	PA10	USART1_RX/LCD_COM2	-
44	32	PA11	I/O	FT	PA11	USART1_CTS/SPI1_MISO	USB_DM
45	33	PA12	I/O	FT	PA12	USART1_RTS/SPI1_MOSI	USB_DP
46	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
47	35	V _{SS_2}	S	-	V _{SS_2}	-	-
48	36	V _{DD_2}	S	-	V _{DD_2}	-	-
49	37	PA14	I/O	FT	JTCK-SWCLK	JCTK-SWCLK	-
50	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17/JTDI	-
51	-	PC10	I/O	FT	PC10	USART3_TX/LCD_SEG28/ LCD_SEG40/ LCD_COM4	-
52	1	PC11	I/O	FT	PC11	USART3_RX/LCD_SEG29/ LCD_SEG41/ LCD_COM5	-
53	1	PC12	I/O	FT	PC12	USART3_CK/LCD_SEG30/ LCD_SEG42/ LCD_COM6	-
54	-	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31/ LCD_SEG43/ LCD_COM7	-

Pin descriptions STM32L100x6/8/B-A

Table 9. STM32L100x6/8/B-A pin definitions (continued)

Р	ins						Pin functions	s
LQFP64	UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions	
55	39	PB3	I/O	FT	JTDO	TIM2_CH2/PB3/SPI1_SCK/ LCD_SEG7/JTDO	COMP2_INM	
56	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/SPI1_MISO/ LCD_SEG8/NJTRST	COMP2_INP	
57	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP	
58	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	-	
59	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2 /USART1_RX	PVD_IN	
60	44	BOOT0	I	В	воото	-	-	
61	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/ TIM10_CH1	-	
62	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/ TIM11_CH1	-	
63	47	V _{SS_3}	S	-	V _{SS_3}	-	-	
64	48	V_{DD_3}	S	-	V _{DD_3}	-	-	

^{1.} I = input, O = output, S = supply.

36/103 DocID025966 Rev 6

Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 10*.

^{3.} The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).

^{4.} The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.



Table 10. Alternate function input/output

						Digital alterna	te function	number							
Dord name	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFI O8	AFI O9	AFIO11	AFIO 12	AFIO 13	AFIO14	AFIO15
Port name			•			Altern	ate functio	n	•	•		•			
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
воото	воото	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS- SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK- SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-	-	-	[SEG7]	-	-	-	EVENTOUT

Table 10. Alternate	function i	input/outpu	t (continued)
---------------------	------------	-------------	---------------

						Digital alterna	te function	number							
Post some	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFI O8	AFI O9	AFIO11	AFIO 12	AFIO 13	AFIO14	AFIO15
Port name						Altern	ate functio	n	•	•					
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PB4	NJTRST	=	TIM3_CH1	-	-	SPI1_MISO	-	-	-	-	[SEG8]	-	-	-	EVENTOUT
PB5	-	-	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI	-	-	-	-	[SEG9]	-	-	-	EVENTOUT
PB6	=	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	EVENTOUT
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	-	EVENTOUT
PB8	-	-	TIM4_CH3	TIM10_CH1*	I2C1_SCL	-	-	-	-	-	SEG16	-	-	-	EVENTOUT
PB9	-	-	TIM4_CH4	TIM11_CH1*	I2C1_SDA	-	-	-	-	-	[COM3]	-	-	-	EVENTOUT
PB10	=	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	-	EVENTOUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	-	EVENTOUT
PB12	-	-	-	TIM10_CH1	I2C2_ SMBA	SPI2_NSS	-	USART3_CK	-	-	SEG12	-	-	-	EVENTOUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK	-	USART3_CTS	-	-	SEG13	-	-	-	EVENTOUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	-	EVENTOUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI	-	-	-	-	SEG15	-	-	-	EVENTOUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	-	TIMx_IC1	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	-	TIMx_IC2	EVENTOUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	-	TIMx_IC3	EVENTOUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	-	TIMx_IC4	EVENTOUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	-	TIMx_IC1	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	-	TIMx_IC2	EVENTOUT
PC6	=	-	TIM3_CH1	-	-	-	-	-	-	-	SEG24	-	-	TIMx_IC3	EVENTOUT
PC7	-	-	TIM3_CH2	-	-	-	-	-	-	-	SEG25	-	-	TIMx_IC4	EVENTOUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	-	TIMx_IC1	EVENTOUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	-	TIMx_IC2	EVENTOUT





Table 10. Alternate function input/output (continued)

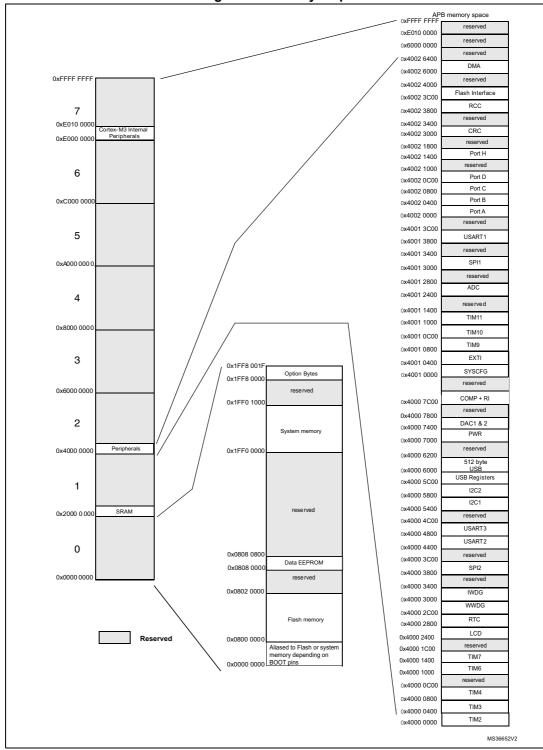
		Digital alternate function number													
Port name	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFI O8	AFI O9	AFIO11	AFIO 12	AFIO 13	AFIO14	AFIO15
Port name						Alterr	ate functio	n							
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT
PC11	-	-	-	-	-	-	-	USART3_RX	-	-	COM5 / SEG29 / SEG41	-	-	TIMx_IC4	EVENTOUT
PC12	-	-	-	-	1	-	-	USART3_CK	-	-	COM6 / SEG30 / SEG42	-	-	TIMx_IC1	EVENTOUT
PC13- WKUP2	-	-		-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PC14- OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PC15- OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	COM7 / SEG31 / SEG43	-	-	TIMx_IC3	EVENTOUT
PH0- OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH1- OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Memory mapping STM32L100x6/8/B-A

5 Memory mapping

The memory map is shown in the following figure.

Figure 5. Memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_A$ max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.0 V (for the 1.8 V \leq V_{DD} \leq 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

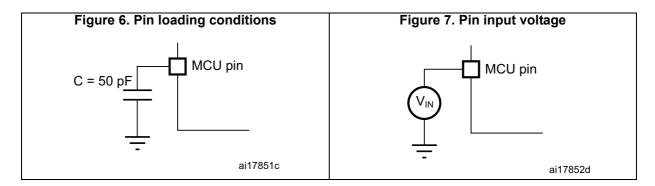
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 6.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.



6.1.6 Power supply scheme

Standby-power circuitry (OSC32K,RTC, Wake-up logic RTC backup registers) Ю Kernel GP I/Os logic (CPU, Logic Digital & Memories) Regulator N x 100 nF + 1 x 10 µF V_{SS1/2/.../N} V_{DDA} Analog: V_{REF+} RCs, PLL ADC/ 100 nF COMP, V_{REF} + 1 µF DAC MS32484V1

Figure 8. Power supply scheme

6.1.7 Optional LCD power supply scheme

Option 1

Option 2

Craits

PB0

VLCDrails

PB12

VLCDrail1

VSEL

Step-up

Converter

Converter

VLCD

PB0

VLCDrail2

VLCDrail1

MS32485V2

Figure 9. Optional LCD power supply scheme

- 1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
- 2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

N x 100 nF +1 x 10 µF N x V_{DD} V_{DDA} V_{REF}-V_{SSA} MS33028V1

Figure 10. Current consumption measurement scheme

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table	11.	Voltage	characteristic	S

Symbol	Ratings	Min	Max	Unit
V _{DD} -V _{SS}	V _{DD} -V _{SS} External main supply voltage (including V _{DDA} and V _{DD}) ⁽¹⁾		4.0	
V _{IN} ⁽²⁾	Input voltage on five-volt tolerant pin	V _{SS} -0.3	V _{DD} +4.0	V
VIN.	Input voltage on any other pin	V _{SS} -0.3	4.0	
∆V _{DDx}	Variations between different V _{DD} power pins	-	50	mV
V _{SSX} -V _{SS}	Variations between all different ground pins ⁽³⁾	-	50	IIIV
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	see Section 6.3.11		-

All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI _{VDD}	Total current into sum of all V _{DD_x} power lines (source) ⁽¹⁾	100	
ΣI _{VSS} ⁽²⁾	Total current out of sum of all V _{SS_x} ground lines (sink) ⁽¹⁾	100	
I _{VDD(PIN)}	Maximum current into each V _{DD_x} power pin (source) ⁽¹⁾	70	
I _{VSS(PIN)}	Maximum current out of each V _{SS_x} ground pin (sink) ⁽¹⁾	-70	mA
1.	Output current sunk by any I/O and control pin	25	
I _{IO}	Output current sourced by any I/O and control pin	- 25	
71	Total output current sunk by sum of all IOs and control pins ⁽²⁾	60	
ΣΙ _{ΙΟ(PIN)}	Total output current sourced by sum of all IOs and control pins ⁽²⁾	-60	
(3)	Injected current on five-volt tolerant I/O(4) RST and B pins	-5/+0	
I _{INJ(PIN)} (3)	Injected current on any other pin ⁽⁵⁾	± 5	
ΣΙ _{ΙΝJ(PIN)}	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

577

44/103 DocID025966 Rev 6

^{2.} V_{IN} maximum must always be respected. Refer to *Table 12* for maximum allowed injected current values.

^{3.} Include VREF- pin.

This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

^{3.} Negative injection disturbs the analog performance of the device. See note in Section 6.3.17.

- Positive current injection is not possible on these I/Os. A negative injection is induced by V_{IN}<V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to Table 11 for maximum allowed input voltage values.
- A positive injection is induced by V_{IN} > V_{DD} while a negative injection is induced by V_{IN} < V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to *Table 11: Voltage characteristics* for the maximum allowed input voltage values.
- When several inputs are submitted to a current injection, the maximum ΣI_{INJ(PIN)} is the absolute sum of the
 positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
T _J	Maximum junction temperature	105	°C
T _{LEAD}	Maximum lead temperature during soldering	see note (1)	°C

Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK[®]
7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS
directive 2011/65/EU, July 2011).

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f _{HCLK}	Internal AHB clock frequency	-	0	32	
f _{PCLK1}	Internal APB1 clock frequency	-	0	32	MHz
f _{PCLK2}	Internal APB2 clock frequency	-	0	32	
V _{DD}	Standard operating voltage	BOR detector enabled, at power on	1.8	3.6	V
V _{DDA} ⁽¹⁾	Analog operating voltage (ADC and DAC used)	Must be the same voltage as $V_{DD}^{(2)}$	1.8	3.6	V
		FT pins: 2.0 V ≤V _{DD}	-0.3	5.5 ⁽³⁾	
\ \ <u>\</u>	I/O input voltage	FT pins: V _{DD} < 2.0 V	-0.3	5.25 ⁽³⁾	V
V _{IN}	ino input voltage	ВООТ0	0	5.5	V
		Any other pin	-0.3	V _{DD} +0.3	
P _D	Power dissipation at TA = 85 °C ⁽⁴⁾	LQFP64 package	-	444	mW
r _D	Fower dissipation at TA = 65° CC7	UFQFPN48 package	-	606	IIIVV
TA	Ambient temperature range	Maximum power dissipation	-40	85	
TJ	Junction temperature range	-40 °C ≤ T _A ≤ 85°C	-40	105	°C

^{1.} When the ADC is used, refer to Table 55: ADC characteristics.

^{3.} To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.



It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see Table 64: Thermal characteristics on page 98).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in the following table.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	V _{DD} rise time rate	BOR detector enabled	0	-	∞	
$t_{VDD}^{(1)}$	\/ fall time rate	BOR detector enabled	20	-	∞	μs/V
	V _{DD} fall time rate	BOR detector disabled	0	-	1000	
T _{RSTTEMPO} ⁽¹⁾	Reset temporization	V _{DD} rising, BOR enabled	-	2	3.3	ms
V	Power on/power down reset	Falling edge	1	1.5	1.65	V
V _{POR/PDR}	threshold	Rising edge	1.3	1.5	1.65	V
\/	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
V_{BOR0}	Brown-out reset threshold o	Rising edge	1.69	1.76	1.8	
\/	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
V_{BOR1}	Brown-out reset threshold i	Rising edge	1.96	2.03	2.07	
M	Drawn aut was at three hald O	Falling edge	2.22	2.30	2.35	.,
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.31	2.41	2.44	V
M	Drawn aut was at three hald 2	Falling edge	2.45	2.55	2.60	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.54	2.66	2.7	
	Drawn and reach threehold 4	Falling edge	2.68	2.8	2.85	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.78	2.9	2.95	

Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V	Programmable voltage detector	Falling edge	1.8	1.85	1.88	
V_{PVD0}	threshold 0	Rising edge	1.88	1.94	1.99	
V	PVD threshold 1	Falling edge	1.98	2.04	2.09	
V_{PVD1}	PVD (IIIeSHOID I	Rising edge	2.08	2.14	2.18	
V	PVD threshold 2	Falling edge	2.20	2.24	2.28	
V_{PVD2}	PVD tilleshold 2	Rising edge	2.28	2.34	2.38	
V	PVD threshold 3	Falling edge	2.39	2.44	2.48	V
V_{PVD3}	PVD threshold 5	Rising edge	2.47	2.54	2.58	V
V	PVD threshold 4	Falling edge	2.57	2.64	2.69	
V_{PVD4}	PVD threshold 4	Rising edge	2.68	2.74	2.79	
V	DVD throughold E	Falling edge	2.77	2.83	2.88	
V_{PVD5}	PVD threshold 5	Rising edge	2.87	2.94	2.99	
M	DVD throughold C	Falling edge	2.97	3.05	3.09	
V_{PVD6}	PVD threshold 6	Rising edge	3.08	3.15	3.20	
		BOR0 threshold	-	40	-	
V_{hyst}	Hysteresis voltage	All BOR and PVD thresholds excepting BOR0	-	100	-	mV

^{1.} Guaranteed by characterization results.

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 16. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C, V _{DDA} = 3 V ±10 mV	0x1FF8 0078-0x1FF8 0079

Table 17. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{REFINT out} ⁽¹⁾	Internal reference voltage	– 40 °C < T _J < +85 °C	1.202	1.224	1.242	V
I _{REFINT}	Internal reference current consumption	-	-	1.4	2.3	μΑ
T _{VREFINT}	Internal reference startup time	-	-	2	3	ms
V _{VREF_MEAS}	V _{DDA} voltage during V _{REFINT} factory measure	-	2.99	3	3.01	V
A _{VREF_MEAS}	Accuracy of factory-measured V _{REF} value ⁽²⁾	Including uncertainties due to ADC and V _{DDA} values	-	-	±5	mV
T _{Coeff} ⁽³⁾	Temperature coefficient	-40 °C < T _J < +85 °C	-	25	100	ppm/°C
A _{Coeff} ⁽³⁾	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
V _{DDCoeff} ⁽³⁾⁽⁴⁾	Voltage coefficient	3.0 V < V _{DDA} < 3.6 V	-	-	2000	ppm/V
T _{S_vrefint} ⁽³⁾	ADC sampling time when reading the internal reference voltage	-	4	-	-	μs
T _{ADC_BUF} ⁽³⁾	Startup time of reference voltage buffer for ADC	-	-	-	10	μs
I _{BUF_ADC} (3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	μΑ
I _{VREF_OUT} (3)	VREF_OUT output current ⁽⁵⁾	-	-	-	1	μΑ
C _{VREF_OUT} ⁽³⁾	VREF_OUT output load	-	-	-	50	pF
I _{LPBUF} ⁽³⁾	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V _{REFINT_DIV1} (3)	1/4 reference voltage	-	24	25	26	
V _{REFINT_DIV2} (3)	1/2 reference voltage	-	49	50	51	% V _{REFINT}
V _{REFINT_DIV3} (3)	3/4 reference voltage	-	74	75	76	

^{1.} Guaranteed by test in production.

 $^{2. \}quad \text{The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes. } \\$

^{3.} Guaranteed by characterization results.

^{4.} Shortest sampling time can be determined in the application by multiple interactions.

^{5.} To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code, unless otherwise specified.

The current consumption values are derived from the tests performed under ambient temperature T_A=25°C and V_{DD} supply voltage conditions summarized in *Table 14: General operating conditions*, unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled f_{APB1} = f_{APB2} = f_{AHB}.
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSC_IN input follows the characteristics specified in Table 27: High-speed external user clock characteristics.
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6 \text{ V}$ is applied to all supply pins.
- For typical current consumption V_{DD} = V_{DDA} = 3.0 V is applied to all supply pins if not specified otherwise.

Table 18. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Cond	litions	f _{HCLK}	Тур	Max ⁽¹⁾	Unit
			D 0.1/ 4.01/	1 MHz	215	285	
			Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	2 MHz	400	490	μΑ
				4 MHz	725	1000	
Supply current in		f _{HSE} = f _{HCLK} up to 16 MHz, included		4 MHz	0.915	1.3	
	$f_{HSE} = f_{HCLK}/2$ above	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	8 MHz	1.75	2.15		
	16 MHz (PLL ON) ⁽²⁾		16 MHz	3.4	4		
		(== 1.1)	Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	8 MHz	2.1	2.9	
I _{DD (Run}	Run mode, code			16 MHz	4.2	5.2	
from Flash)	executed			32 MHz	8.25	9.6	
	from Flash	HSI clock source (16 MHz)	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	3.5	4.4	mA
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	8.2	10.2	
		MSI clock, 65 kHz		65 kHz	0.041	0.085	
		MSI clock, 524 kHz	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	524 kHz	0.125	0.180	
		MSI clock, 4.2 MHz		4.2 MHz	0.775	0.935	

^{1.} Guaranteed by characterization results, unless otherwise specified.

^{2.} Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conc	litions	f _{HCLK}	Тур	Max ⁽¹⁾	Unit
			Range 3,	1 MHz	185	255	
			V _{CORE} =1.2 V	2 MHz	345	435	μA
		f _{HSE} = f _{HCLK}	VOS[1:0] = 11	4 MHz	645	930	
Supply current in Run mode, code		up to 16 MHz,	Range 2,	4 MHz	0.755	1.5	
	included f _{HSE} = f _{HCLK} /2 above	V _{CORE} =1.5 V	8 MHz	1.5	2.2		
	16 MHz (PLL ON) ⁽²⁾	VOS[1:0] = 10	16 MHz	3.0	3.6		
		Range 1,	8 MHz	1.8	2.9		
	Run mode, code		V _{CORE} =1.8 V	16 MHz	3.6	4.3	
I _{DD} (Run from RAM)	executed from		VOS[1:0] = 01	32 MHz	7.15	8.5	mA
RAM, Flash switched off		HSI clock source (16 MHz)	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	2.95	3.7	
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	7.15	8.7	
		MSI clock, 65 kHz	Range 3,	65 kHz	39	115	
		MSI clock, 524 kHz	V _{CORE} =1.2 V	524 kHz	110	205	μΑ
		MSI clock, 4.2 MHz	VOS[1:0] = 11	4.2 MHz	690	870	

^{1.} Guaranteed by characterization results, unless otherwise specified.

^{2.} Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 20. Current consumption in Sleep mode

Symbol	Parameter	I	litions	f _{HCLK}	Тур	Max ⁽¹⁾	Unit
			Range 3,	1 MHz	50	155	
			V _{CORE} =1.2 V	2 MHz	78.5	235	
			VOS[1:0] = 11	4 MHz	140	370 ⁽³⁾	
		f _{HSE} = f _{HCLK} up to 16 MHz included,	Range 2,	4 MHz	165	375	
		$f_{HSE} = f_{HCLK}/2$	V _{CORE} =1.5 V	8 MHz	310	530	
		above 16 MHz (PLL ON) ⁽²⁾	VOS[1:0] = 10	16 MHz	590	1000	
	Cupply	014)	Range 1,	8 MHz	350	615	
	Supply current in		V _{CORE} =1.8 V	16 MHz	680	1200	
Sleep mode, Flash OFF			VOS[1:0] = 01	32 MHz	1600	2350	μΑ
		HSI clock source	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	640	970	
	(16 MHz)	Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	1600	2350		
		MSI clock, 65 kHz	Range 3,	65 kHz	19	60	
		MSI clock, 524 kHz	V _{CORE} =1.2 V	524 kHz	33	90	
I _{DD}		MSI clock, 4.2 MHz	VOS[1:0] = 11	4.2 MHz	145	210	
(Sleep)		f _{HSE} = f _{HCLK} up to 16 MHz included,	Range 3,	1 MHz	60.5	145	
			V _{CORE} =1.2 V	2 MHz	89.5	225	
			VOS[1:0] = 11	4 MHz	150	360	
			Range 2,	4 MHz	180	370	
		$f_{HSE} = f_{HCLK}/2$	V _{CORE} =1.5 V	8 MHz	320	490	
		above 16 MHz (PLL ON) ⁽²⁾	VOS[1:0] = 10	16 MHz	605	895	
	Supply	J,	Range 1,	8 MHz	380	565	
	current in		V _{CORE} =1.8 V	16 MHz	695	1070	
	Sleep		VOS[1:0] = 01	32 MHz	1600	2200	μΑ
	mode, Flash ON	HSI clock source	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	650	970	
		(16 MHz)	Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	1600	2320	
		MSI clock, 65 kHz	Range 3,	65 kHz	29.5	65	
		MSI clock, 524 kHz	V _{CORE} =1.2V	524 kHz	44	80	
	-	MSI clock, 4.2 MHz	VOS[1:0] = 11	4.2 MHz	155	220	

^{1.} Guaranteed by characterization results, unless otherwise specified.

^{2.} Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

^{3.} Guaranteed by test in production.

Table 21. Current consumption in Low power run mode

Symbol	Parameter		Conditions		Тур	Max ⁽¹⁾	Unit
		All	MSI clock, 65 kHz	T _A = -40 °C to 25 °C	10.9	12	
		peripherals OFF, code	f _{HCLK} = 32 kHz	T _A = 85 °C	16.5	23	
		executed	MSI clock, 65 kHz	T _A = -40 °C to 25 °C	15	16	
		from RAM, Flash	f _{HCLK} = 65 kHz	T _A = 85 °C	22	29	
		switched		T _A = -40 °C to 25 °C	29	37	
	Cupply	OFF, V _{DD} from 1.8 V	MSI clock, 131 kHz f _{HCLK} = 131 kHz	T _A = 55 °C	32.5	40	
Supply to 3.6 \	to 3.6 V		T _A = 85 °C	35.5	54		
Run)	Low power	MSI clock, 65 kHz	T _A = -40 °C to 25 °C	23	24		
	Turrinoue	All peripherals	f _{HCLK} = 32 kHz	T _A = 85 °C	31	34	μΑ
		OFF, code	MSI clock, 65 kHz f _{HCLK} = 65 kHz	T _A = -40 °C to 25 °C	29	31	
		executed from Flash,		T _A = 85 °C	38	41	
		V _{DD} from		T _A = -40 °C to 25 °C	46	55	
		1.8 V to 3.6 V	MSI clock, 131 kHz f _{HCLK} = 131 kHz	T _A = 55 °C	48	59	
		HOLK 101 MIL	T _A = 85 °C	53.5	72		
I _{DD} Max (LP Run) ⁽²⁾	Max allowed current in Low power run mode	V _{DD} from 1.8 V to 3.6 V	-	-	-	200	

^{1.} Guaranteed by characterization results, unless otherwise specified.

^{2.} This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 22. Current consumption in Low power sleep mode

Symbol	Parameter		Conditions		Тур	Max ⁽¹⁾	Unit
			MSI clock, 65 kHz f _{HCLK} = 32 kHz Flash OFF	T _A = -40 °C to 25 °C	5.5	-	
			MSI clock, 65 kHz	T_A = -40 °C to 25 °C	15	16	
		All peripherals	f _{HCLK} = 32 kHz Flash ON	T _A = 85 °C	20	23	
Supply current in Low power sleep		OFF, V _{DD} from 1.8 V	MSI clock, 65 kHz	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	15	16	
	Supply	to 3.6 V	f _{HCLK} = 65 kHz, Flash ON	T _A = 85 °C	20.5	23	
		MSI clock,	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	18	20		
		131 kHz f _{HCLK} = 131 kHz,	T _A = 55 °C	21	22		
	mode		Flash ON	T _A = 85 °C	23	27	μΑ
		TIM9 and	MSI clock, 65 kHz	T_A = -40 °C to 25 °C	15	16	
			f _{HCLK} = 32 kHz	T _A = 85 °C	20	22	
		USART1 enabled.	MSI clock, 65 kHz	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	15	16	
		Flash ON,	f _{HCLK} = 65 kHz	T _A = 85 °C	20.5	23	
		V _{DD} from 1.8 V to	MSI clock,	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	18	20	
		3.6 V	131 kHz	T _A = 55 °C	21	22	
			f _{HCLK} = 131 kHz	T _A = 85 °C	23	27	
I _{DD} Max (LP Sleep)	Max allowed current in Low power Sleep mode	V _{DD} from 1.8 V to 3.6 V	-	-	-	200	

^{1.} Guaranteed by characterization results, unless otherwise specified.

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	C	onditions		Typ ⁽¹⁾	Max (1)(2)	Unit
				$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$ $V_{DD} = 1.8 \text{ V}$	1.13	-	
			LCD OFF	$T_A = -40^{\circ}C$ to 25°C	1.38	4	
				T _A = 55°C	1.70	6	
		RTC clocked by LSI,		T _A = 85°C	3.30	10	
		regulator in LP mode, HSI and HSE OFF	LCD ON	$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	1.50	6	
		(no independent watchdog)	(static	T _A = 55°C	1.80	7	
			duty) ⁽³⁾	T _A = 85°C	3.45	12	
			LCD ON	$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	3.80	10	
			(1/8	T _A = 55°C	4.30	11	
			duty) ⁽⁴⁾	T _A = 85°C	6.10	16	
	Cumply ourrant in			$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	1.50	-	
I _{DD} (Stop with RTC) Supply current in Stop mode with RTC enabled		LCD OFF	T _A = 55°C	1.90	-		
	RTC enabled	RTC clocked by LSE		T _A = 85°C	3.65	-	μΑ
		external clock (32.768	LCD ON	$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	1.60	-	
		kHz), regulator in LP mode, HSI and HSE OFF	(static	T _A = 55°C	2.05	-	
		(no independent	duty) ⁽³⁾	T _A = 85°C	3.75	-	
		watchdog)	LCD ON	$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	3.90	-	
			(1/8	T _A = 55°C	4.55	-	
			duty) ⁽¹⁾	T _A = 85°C	6.35	-	
			LCD OFF	$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$ $V_{DD} = 1.8 \text{ V}$	1.23	-	
		RTC clocked by LSE (no independent watchdog) ⁽⁵⁾		$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$ $V_{DD} = 3.0 \text{ V}$	1.50	-	
				$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$ $V_{DD} = 3.6 \text{ V}$	1.75	-	
	Supply current in	Regulator in LP mode, HSI OFF, independent watchdo enabled		T _A = -40°C to 25°C	1.80	2.2	
I _{DD (Stop)}	Stop mode ($T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	0.434	1	
	RTC disabled)	Regulator in LP mode, LSI HSE OFF (no independent		T _A = 55°C	0.735	3	1
		THOE OF T (NO INdependent	wateridog)	T _A = 85°C	2.350	9	
	RMS (root mean	MSI = 4.2 MHz			2	-	
IDD (MIL	square) supply current during	MSI = 1.05 MHz		V _{DD} = 3.0 V	1.45	-	
	wakeup time when exiting from Stop mode	MSI = 65 kHz ⁽⁶⁾		T _A = -40°C to 25°C	1.45	-	mA



- 1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
- 2. Guaranteed by characterization results, unless otherwise specified.
- 3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
- 4. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
- Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
- When MSI = 64 kHz, the RMS current is measured over the first 15 μs following the wakeup event. For the remaining time
 of the wakeup period, the current is similar to the Run mode current.

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ ⁽¹⁾	Max (1)(2)	Unit
			T _A = -40 °C to 25 °C V _{DD} = 1.8 V	0.865	-	
		RTC clocked by LSI (no	T _A = -40 °C to 25 °C	1.11	1.9	
		independent watchdog)	T _A = 55 °C	1.15	2.2	
I _{DD}	Supply current in Standby		T _A = 85 °C	1.35	4	
(Standby with RTC)	mode with RTC enabled		T _A = -40 °C to 25 °C V _{DD} = 1.8 V	0.97	-	
		RTC clocked by LSE (no independent watchdog) ⁽³⁾	T_A = -40 °C to 25 °C	1.28	-	μA
		independent watchdog).	T _A = 55 °C	1.4	-	
			T _A = 85 °C	1.7	-	
		Independent watchdog and LSI enabled	T _A = -40 °C to 25 °C	1.0	1.7	
I_{DD}	Supply current in Standby mode with RTC disabled		T _A = -40 °C to 25 °C	0.277	0.6	
(Standby)	mode with KTC disabled	Independent watchdog and LSI OFF	T _A = 55 °C	0.31	0.9	
			T _A = 85 °C	0.52	2.75	
I _{DD (WU} from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V _{DD} = 3.0 V T _A = -40 °C to 25 °C	1	-	mA

^{1.} The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.

56/103 DocID025966 Rev 6

^{2.} Guaranteed by characterization results, unless otherwise specified.

Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- \bullet $\,$ all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on

Table 25. Peripheral current consumption⁽¹⁾

		Typica	I consumption,	V _{DD} = 3.0 V, T _A	= 25 °C	
Peripheral		Range 1, V _{CORE} = 1.8 V VOS[1:0] = 01	Range 2, V _{CORE} = 1.5 V VOS[1:0] = 10	Range 3, V _{CORE} = 1.2 V VOS[1:0] = 11	Low-power sleep and run	Unit
	TIM2	11.3	9.0	7.3	9.0	
	TIM3	11.4	9.1	7.1	9.1	
	TIM4	11.3	9.0	7.3	9.0	
	TIM6	3.9	3.1	2.5	3.1	
	TIM7	4.2	3.3	2.6	3.3	
	LCD	4.7	3.6	2.9	3.6	
	WWDG	3.7	2.9	2.4	2.9	
	SPI2	5.9	4.8	3.9	4.8	
APB1	USART2	8.1	6.6	5.1	6.6	μΑ/MHz (f _{HCLK})
	USART3	7.9	6.4	5.0	6.4	('HCLK)
	I2C1	7.8	6.1	4.9	6.1	
	I2C2	7.2	5.7	4.6	5.7	
	USB	12.7	10.3	8.1	10.3	
	PWR	3.1	2.4	2.0	2.4	
	DAC	6.6	5.3	4.3	5.3	
	COMP	5.3	4.3	3.4	4.3	

Table 25. Peripheral current consumption⁽¹⁾ (continued)

		Typica	l consumption,				
Periț	bheral	Range 1, V _{CORE} = 1.8 V VOS[1:0] = 01	Range 2, V _{CORE} = 1.5 V VOS[1:0] = 10	Range 3, V _{CORE} = 1.2 V VOS[1:0] = 11	Low-power sleep and run	Unit	
	SYSCFG & RI	2.2	1.9	1.6	1.9		
	TIM9	9.1	7.3	5.9	7.3		
	TIM10	6.0	4.9	3.9	4.9		
APB2	TIM11	5.8	4.6	3.8	4.6		
	ADC ⁽²⁾	8.7	7.0	5.6	7.0		
	SPI1	4.4	3.4	2.8	3.4		
	USART1	8.1	6.5	5.2	6.5		
	GPIOA	4.4	3.5	2.9	3.5		
	GPIOB	4.4	3.5	2.9	3.5	μΑ/MHz	
	GPIOC	3.7	3.0	2.5	3.0	(f _{HCLK})	
	GPIOD	3.6	2.8	2.4	2.8		
AHB	GPIOH	3.7	2.9	2.4	2.9		
ALID	CRC	0.6	0.4	0.4	0.4		
	FLASH	12.2	10.2	7.8	_(3)		
	DMA1	12.4	10.1	8.2	10.1		
All enabled		160	135	103	124.8		
I _{DD (RTC)}			0	.4			
I _{DD (LCD)}			3	.1			
I _{DD (ADC)} ⁽⁴⁾			14	50			
I _{DD (DAC)} ⁽⁵⁾			34	40			
I _{DD (COMP1)}			0.	16		μΑ	
lan (anna)	Slow mode			2			
I _{DD} (COMP2)	Fast mode		!	5			
I _{DD (PVD / BOR)} (6	3)		2.6				
I _{DD (IWDG)}			0.	25			

Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (Range 1), f_{HCLK} = 16 MHz (Range 2), f_{HCLK} = 4 MHz (Range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.

6. Including supply current of internal reference voltage.

^{2.} HSI oscillator is OFF for this measure

^{3.} In low-power sleep and run mode, the Flash memory must always be in power-down mode.

^{4.} Data based on a differential IDD measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).

Data based on a differential IDD measurement between DAC in reset configuration and continuous DAC conversion of VDD/2. DAC is in buffered mode, output is left floating.

6.3.5 Wakeup time from Low-power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Тур	Max ⁽¹⁾	Unit	
t _{WUSLEEP}	Wakeup from Sleep mode	f _{HCLK} = 32 MHz	0.4	-		
	Wakeup from Low-power sleep mode	f _{HCLK} = 262 kHz Flash enabled	46	-		
twusleep_lp	f _{HCLK} = 262 kHz	f _{HCLK} = 262 kHz Flash switched OFF	46	-		
	Wakeup from Stop mode, regulator in Run mode	f _{HCLK} = f _{MSI} = 4.2 MHz	8.2	-		
		f _{HCLK} = f _{MSI} = 4.2 MHz Voltage Ranges 1 and 2	7.7	8.9		
	Wakeup from Stop mode, regulator in low-power mode	f _{HCLK} = f _{MSI} = 4.2 MHz Voltage Range 3	8.2	13.1	μs	
t _{WUSTOP}		f _{HCLK} = f _{MSI} = 2.1 MHz	10.2	13.4		
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	16	20		
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	31	37		
		f _{HCLK} = f _{MSI} = 262 kHz	57	66		
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	112	123		
		f _{HCLK} = MSI = 65 kHz	221	236		
t.,,,,	Wakeup from Standby mode FWU bit = 1	f _{HCLK} = MSI = 2.1 MHz	58	104		
t _{wustdby}	Wakeup from Standby mode FWU bit = 0	f _{HCLK} = MSI = 2.1 MHz	2.6	3.25	ms	

^{1.} Guaranteed by characterization results, unless otherwise specified

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

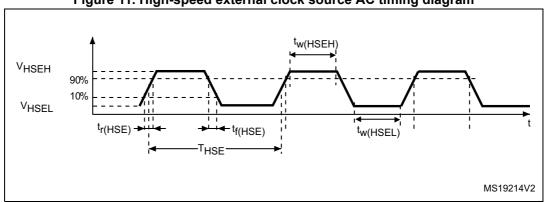
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 11*.

Table 27. High-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f	User external clock source	CSS is on or PLL is used	1	8	32	MHz
f _{HSE_ext}	OSC IN input pin high level voltage	CSS is off, PLL not used	0	0	32	IVII IZ
V _{HSEH}	OSC_IN input pin high level voltage		0.7V _{DD}	-	V_{DD}	
V _{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3V _{DD}	
$t_{w(HSEH)} \ t_{w(HSEL)}$	OSC_IN high or low time	-	12	ı	-	ns
t _{r(HSE)}	OSC_IN rise or fall time		-	-	20	10
C _{in(HSE)}	OSC_IN input capacitance	-	-	2.6	-	pF

^{1.} Guaranteed by design.

Figure 11. High-speed external clock source AC timing diagram



60/103 DocID025966 Rev 6

Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

	•				
Symbol	Parameter	Min	Тур	Max	Unit
f _{LSE_ext}	User external clock source frequency	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7V _{DD}	-	V_{DD}	-
V_{LSEL}	OSC32_IN input pin low level voltage	V _{SS}	-	0.3V _{DD}	-
$t_{w(LSEH)} \ t_{w(LSEL)}$	OSC32_IN high or low time	465	-	-	ns
$t_{r(LSE)} \ t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	10	115
C _{IN(LSE)}	OSC32_IN input capacitance	-	0.6	-	pF

Table 28. Low-speed external user clock characteristics⁽¹⁾

^{1.} Guaranteed by design.

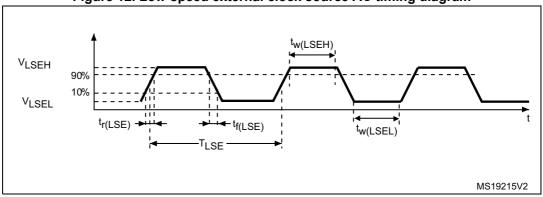


Figure 12. Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol Parameter Conditions Min Тур Max Unit Oscillator frequency 1 24 MHz tosc_in 200 R_{F} Feedback resistor $k\Omega$

Table 29. HSE oscillator characteristics⁽¹⁾⁽²⁾

Table 29. HSE oscillator	r characteristics ⁽¹⁾⁽²⁾ ((continued))
--------------------------	---------------------------------------	-------------	---

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
С	Recommended load capacitance versus equivalent serial resistance of the crystal (R _S) ⁽³⁾	R _S = 30 Ω	-	20	-	pF
I _{HSE}	HSE driving current	V _{DD} = 3.3 V, V _{IN} = V _{SS} with 30 pF load	-	-	3	mA
1	HSE oscillator power consumption	C = 20 pF $f_{OSC} = 16 \text{ MHz}$	ı	i	2.5 (startup) 0.7 (stabilized)	mA
IDD(HSE)		C = 10 pF f _{OSC} = 16 MHz	ı	i	2.5 (startup) 0.46 (stabilized)	IIIA
9 _m	Oscillator transconductance	Startup	3.5	ı	-	mA /V
t _{SU(HSE)}	Startup time	V _{DD} is stabilized	-	1	-	ms

- 1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
- 2. Guaranteed by characterization results.
- 3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
- 4. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 13*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website *www.st.com*.

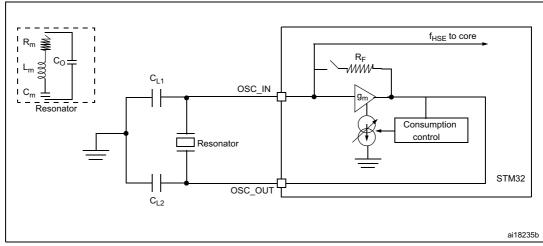


Figure 13. HSE oscillator circuit diagram

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 14*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

	idade del 202 decimates cital determination (i.ESE deliver in i.e.)						
Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
f _{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz	
R _F	Feedback resistor	-	-	1.2	-	ΜΩ	
C ⁽²⁾	Recommended load capacitance versus equivalent serial resistance of the crystal (R _S) ⁽³⁾	R _S = 30 kΩ	-	8	-	pF	
I _{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.1	μA	
		V _{DD} = 1.8 V	-	450	-		
I _{DD (LSE)}	LSE oscillator current consumption	V _{DD} = 3.0 V	-	600	-	nA	
	,	V _{DD} = 3.6V	-	750	-		
9 _m	Oscillator transconductance	-	3	-	-	μA/V	
t _{SU(LSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized	-	1	-	S	

Table 30. LSE oscillator characteristics $(f_{LSE} = 32.768 \text{ kHz})^{(1)}$

- Guaranteed by characterization results.
- Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
- 3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.
- t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note:

For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 14). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula: $CL = CL1 \times CL2 / (CL1 + CL2) + Cstray$ where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution:

To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL \leq 7 pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if the user chooses a resonator with a load capacitance of CL = 6 pF and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

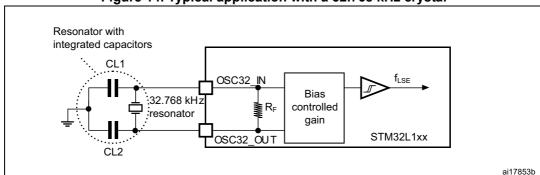


Figure 14. Typical application with a 32.768 kHz crystal

6.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 31. HSI oscillator characteristics

Symbol	Parameter	er Conditions		Тур	Max	Unit
f _{HSI}	Frequency	V _{DD} = 3.0 V	-	16	-	MHz
TRIM ⁽¹⁾⁽²⁾	HSI user-trimmed	Trimming code is not a multiple of 16	-	±0.4	0.7	%
TRIM	resolution	Trimming code is a multiple of 16	-	-	±1.5	%
ACC _{HSI} ⁽²⁾	-	V _{DDA} = 1.8 V to 3.6 V T _A = -40 to 85 °C	-10	-	+10	%
t _{SU(HSI)} ⁽²⁾	HSI oscillator startup time	-	1	3.7	6	μs
I _{DD(HSI)} ⁽²⁾	HSI oscillator power consumption	-	1	100	140	μΑ

The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

Low-speed internal (LSI) RC oscillator

Table 32. LSI oscillator characteristics

Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI} ⁽¹⁾	LSI frequency	26	38	56	kHz
D _{LSI} ⁽²⁾	LSI oscillator frequency drift 0°C ≤T _A ≤85°C	-10	-	4	%
t _{su(LSI)} ⁽³⁾	LSI oscillator startup time	-	-	200	μs
I _{DD(LSI)} ⁽³⁾	LSI oscillator power consumption	-	400	510	nA

^{1.} Guaranteed by test in production.

- 2. This is a deviation for an individual part, once the initial frequency has been measured.
- 3. Guaranteed by design.

^{2.} Guaranteed by characterization results.

Multi-speed internal (MSI) RC oscillator

Table 33. MSI oscillator characteristics

Symbol	Parameter	Condition	Тур	Max	Unit
		MSI range 0	65.5	-	
		MSI range 1	131	-	kHz
		MSI range 2	262	-	KΠZ
f _{MSI}	Frequency after factory calibration, done at V_{DD} = 3.3 V and T_A = 25 °C	MSI range 3	524	-	
	LOD ore carre of	MSI range 4	1.05	-	
ACCura		MSI range 5	2.1	-	MHz
		MSI range 6	4.2	-	
ACC _{MSI}	Frequency error after factory calibration	-	±0.5	-	%
D _{TEMP(MSI)} ⁽¹⁾	MSI oscillator frequency drift 0 °C ≤T _A ≤85 °C	-	±10	-	%
D _{VOLT(MSI)} ⁽¹⁾	MSI oscillator frequency drift 1.8 V ≤V _{DD} ≤3.6 V, T _A = 25 °C	-	-	2.5	%/V
		MSI range 0	0.75	-	
	MSI oscillator power consumption	MSI range 1	1	-	
		MSI range 2	1.5	-	
I _{DD(MSI)} ⁽²⁾		MSI range 3	2.5	-	μΑ
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
		MSI range 0	30	-	
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
t	MSI oscillator startup time	MSI range 4	6	-	116
t _{SU(MSI)}	ino oscillator startup time	MSI range 5	5	-	μs
		MSI range 6, Voltage range 1 and 2	3.5	1	
		MSI range 6, Voltage range 3	5	-	

Symbol	Parameter	Condition	Тур	Max	Unit
		MSI range 0	-	40	
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
+ (2)	MSI oscillator stabilization time	MSI range 4	-	2.5	μs
t _{STAB(MSI)} ⁽²⁾		MSI range 5	-	2	μο
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage Range 3	ı	3	
formus	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
f _{OVER(MSI)}	INOT OSCINATOR ITEQUETICS OVERSHOOT	Any range to range 6	ı	6	IVII IZ

Table 33. MSI oscillator characteristics (continued)

6.3.8 PLL characteristics

I_{DD}(PLL)

The parameters given in *Table 34* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Value **Symbol Parameter** Unit Max⁽¹⁾ Min Typ PLL input clock⁽²⁾ 2 MHz 24 f_{PLL IN} PLL input clock duty cycle 45 % 55 2 32 MHz PLL output clock f_{PLL_OUT} PLL lock time PLL input = 16 MHz 115 160 μs t_{LOCK} PLL VCO = 96 MHz Jitter Cycle-to-cycle jitter ± 600 ps I_{DDA}(PLL) Current consumption on V_{DDA} 220 450 μΑ

Table 34. PLL characteristics

Current consumption on V_{DD}

120

150

^{1.} This is a deviation for an individual part, once the initial frequency has been measured.

^{2.} Guaranteed by characterization results.

^{1.} Guaranteed by characterization results.

^{2.} Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 85 °C unless otherwise specified.

RAM memory

Table 35. RAM and hardware registers

Symbol	mbol Parameter Conditions		Min	Тур	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.8	-	-	V

Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 36. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
V _{DD}	Operating voltage Read / Write / Erase	-	1.8	-	3.6	V
	Programming / erasing time for	Erasing	ı	3.28	3.94	
t _{prog}	byte / word / double word / half- page	Programming	-	3.28	3.94	ms
I _{DD}	Average current during whole program/erase operation	T - 25 °C V - 3 6 V	-	300	-	μΑ
	Maximum current (peak) during program/erase operation	$T_A = 25 ^{\circ}\text{C}, V_{DD} = 3.6 ^{\circ}\text{V}$	-	1.5	2.5	mA

^{1.} Guaranteed by design.

Table 37. Flash memory, data EEPROM endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
Syllibol	raiametei	Conditions	Min ⁽¹⁾	Тур	Max	Oilit
N _{CYC} ⁽²⁾	Cycling (erase / write) Program memory $T_{A} = -40^{\circ}\text{C to}$		1	-	-	kcycles
INCYC.	Cycling (erase / write) EEPROM data memory	85 °C	100	-	-	KCycles
t(2)	Data retention (program memory) after 1 kcycle at T _A = 85 °C	T _{RET} = +85 °C	10	ı	ı	veare
t _{RET} ⁽²⁾	Data retention (EEPROM data memory) after 100 kcycles at T _A = 85 °C	RET - 100 C	10	ı		years

^{1.} Guaranteed by characterization results.

^{2.} Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during the device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Level/ **Symbol Parameter Conditions** Class $V_{DD} = 3.3 \text{ V, LQFP100, } T_A = +25 \text{ °C,}$ Voltage limits to be applied on any I/O pin V_{FESD} $f_{HCLK} = 32 \text{ MHz}$ 3B to induce a functional disturbance conforms to IEC 61000-4-2 $V_{DD} = 3.3 \text{ V, LQFP100, } T_A = +25 \text{ °C,}$ Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} $f_{HCLK} = 32 \text{ MHz}$ V_{EFTB} 4A pins to induce a functional disturbance conforms to IEC 61000-4-4

Table 38. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pregualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

				Max vs	s. frequency	range	
Symbol	Parameter	Conditions	Monitored frequency band	4 MHz voltage Range 3	16 MHz voltage Range 2	32 MHz voltage Range 1	Unit
		$\begin{array}{c} V_{DD} = 3.3 \text{ V,} \\ T_{A} = 25 ^{\circ}\text{C,} \\ \text{LQFP100 package} \\ \text{compliant with IEC} \\ 61967-2 \end{array}$	0.1 to 30 MHz	-16	-7	-3	
e	Poak lovol		30 to 130 MHz	-12	2	12	dΒμV
S _{EMI}	reak level		130 MHz to 1GHz	-11	0	8	
			SAE EMI Level	1	1.5	2	-

Table 39. EMI characteristics

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1 standard.

	<u> </u>					
Symbol	Ratings	Conditions	Packages	s Class Maximum value ⁽¹⁾		Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C4	500	V

Table 40. ESD absolute maximum ratings



^{1.} Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class	
LU	Static latch-up class	T _A = +85 °C conforming to JESD78A	II level A	

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5~\mu\text{A}/+0~\mu\text{A}$ range), or other functional failure (for example reset occurrence, oscillator frequency deviation, LCD levels).

The test results are given in Table 42.

Table 42. I/O current injection susceptibility

		Functional s			
Symbol	Description	Negative injection	Positive injection	Unit	
	Injected current on all 5 V tolerant (FT) pins	-5	NA ⁽¹⁾		
I _{INJ}	Injected current on BOOT0	-0	NA ⁽¹⁾	mA	
	Injected current on any other pin	-5	+5		

^{1.} Injection is not possible.

Note:

It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V _{DD} ⁽¹⁾⁽²⁾	V
		BOOT0	-		0.14 V _{DD} ⁽²⁾	
V _{IH}	Input high level voltage	TC I/O	0.45 V _{DD} +0.38 ⁽²⁾	-	-	
		FT I/O	0.39 V _{DD} +0.59 ⁽²⁾	-	-	
		BOOT0	0.15 V _{DD} +0.56 ⁽²⁾	-	-	
	I/O Schmitt trigger voltage hysteresis ⁽²⁾	TC and FT I/O	-	10% V _{DD} ⁽³⁾	-	
V _{hys}		BOOT0	-	0.01	-	
I _{lkg}	Input leakage current ⁽⁴⁾	V _{SS} ≤V _{IN} ≤V _{DD} I/Os with LCD	-	-	±50	
		V _{SS} ≤V _{IN} ≤V _{DD} I/Os with analog switches	-	-	±50	
		V _{SS} ≤V _{IN} ≤V _{DD} I/Os with analog switches and LCD	-	-	±50	nA
		V _{SS} ≤V _{IN} ≤V _{DD} I/Os with USB	-	-	±250	
		V _{SS} ≤V _{IN} ≤V _{DD} TC and FT I/O	-	-	±50	
		FT I/O V _{DD} ≤V _{IN} ≤5V	-	-	±10	uA
R _{PU}	Weak pull-up equivalent resistor ⁽⁵⁾⁽¹⁾	$V_{IN} = V_{SS}$	25	45	65	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	25	45	65	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

^{1.} Guaranteed by test in production.

72/103 DocID025966 Rev 6

^{2.} Guaranteed by design.

^{3.} With a minimum of 200 mV.

^{4.} The max. value may be exceeded if negative current is injected on adjacent pins.

Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with the non-standard V_{OL}/V_{OH} specifications given in *Table 44*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL} ⁽¹⁾⁽²⁾	Output low level voltage for an I/O pin	I _{IO} = 8 mA	-	0.4	
V _{OH} ⁽³⁾⁽²⁾	Output high level voltage for an I/O pin	2.7 V < V _{DD} < 3.6 V	V _{DD} -0.4	-	
V _{OL} (1)(4)	Output low level voltage for an I/O pin	I _{IO} = 4 mA	-	0.45	V
V _{OH} (3)(4)	Output high level voltage for an I/O pin	1.8 V < V _{DD} < 2.7 V	V _{DD} -0.45	-	ľ
V _{OL} ⁽¹⁾⁽⁴⁾	Output low level voltage for an I/O pin	I _{IO} = 20 mA	-	1.3	
V _{OH} ⁽³⁾⁽⁴⁾	Output high level voltage for an I/O pin	2.7 V < V _{DD} < 3.6 V	V _{DD} -1.3	-	

The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

^{2.} Guaranteed by test in production.

The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

^{4.} Guaranteed by characterization results.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 15* and *Table 45*, respectively.

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 45. I/O AC characteristics⁽¹⁾

OSPEEDRx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
	f	Maximum frequency ⁽³⁾	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	400	kHz
00	f _{max(IO)} out	Maximum nequency.	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	400	KIIZ
00	t _{f(IO)out}	Output rise and fall time	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	625	20
	t _{r(IO)out}	Output rise and fail time	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	625	ns
	£	Maximum frequency ⁽³⁾	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	2	MHz
0.4	f _{max(IO)} out	(IO)out Maximum frequency(*)	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	1	IVIIIZ
01	t _{f(IO)out}	Output rise and fall time	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	125	20
	t _{r(IO)out}	Output rise and fail time	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	250	ns
	Е	رار المراميل I Maximum frequency المراميل الم	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	10	MHz
10	F _{max(IO)out}		C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	2	IVIITZ
10	t _{f(IO)out}	Output rice and fall time	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	25	20
	t _{r(IO)out}	Output rise and fall time	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	125	ns
	Г	Maximum frequency ⁽³⁾	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	50	MHz
11	F _{max(IO)out}	waximum frequency.	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	8	IVITZ
11	t _{f(IO)out}	Output vice and fall times	C _L = 30 pF, V _{DD} = 2.7 V to 3.6 V	-	5	
	t _{r(IO)out}	Output rise and fall time	C _L = 50 pF, V _{DD} = 1.8 V to 2.7 V	-	30	
-	t _{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0038 reference manual for a description of GPIO Port configuration register.

^{2.} Guaranteed by design.

^{3.} The maximum frequency is defined in *Figure 15*.

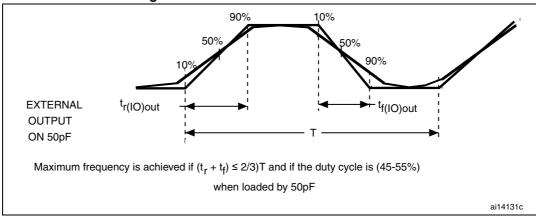


Figure 15. I/O AC characteristics definition

6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU (see *Table 46*).

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL(NRST)} ⁽¹⁾	NRST input low level voltage	-	-	-	0.3 V _{DD}	
V _{IH(NRST)} ⁽¹⁾	NRST input high level voltage	-	0.39 V _{DD} +0.59	-		
V . (1)		I _{OL} = 2 mA 2.7 V < V _{DD} < 3.6 V	-	-	0.4	V
V _{OL(NRST)} ⁽¹⁾		I _{OL} = 1.5 mA 1.8 V < V _{DD} < 2.7 V	-	-	0.4	
V _{hys(NRST)} ⁽¹⁾	NRST Schmitt trigger voltage hysteresis	-	-	10%V _{DD} ⁽²⁾		mV
R _{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	25	45	65	kΩ
V _{F(NRST)} ⁽¹⁾	NRST input filtered pulse	-	-	-	50	ns
V _{NF(NRST)} ⁽¹⁾	NRST input not filtered pulse	-	350	-	-	ns

Table 46. NRST pin characteristics

^{1.} Guaranteed by design.

^{2. 200} mV minimum value.

^{3.} The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

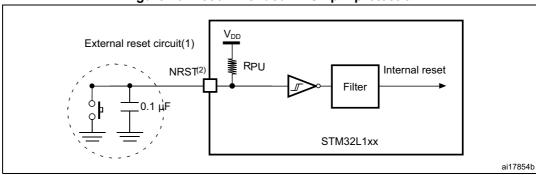


Figure 16. Recommended NRST pin protection

- The reset network protects the device against parasitic resets. 0.1 uF capacitor must be placed as close as
 possible to the chip.
- The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 46. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 47* are guaranteed by design.

Refer to Section 6.3.13: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Tubio III I IIIX							
Symbol	Parameter	Conditions	Min	Max	Unit		
	Timer resolution time	-	1	-	t _{TIMxCLK}		
^t res(TIM)	Timer resolution time	f _{TIMxCLK} = 32 MHz	31.25	-	ns		
f	Timer external clock	-	0	f _{TIMxCLK} /2	MHz		
f _{EXT}	frequency on CH1 to CH4	f _{TIMxCLK} = 32 MHz	0	16	MHz		
Res _{TIM}	Timer resolution	-	-	16	bit		
^t COUNTER	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	t _{TIMxCLK}		
		f _{TIMxCLK} = 32 MHz	0.0312	2048	μs		
+	Maximum possible sount	-	-	65536 × 65536	t _{TIMxCLK}		
t _{MAX_COUNT}	Maximum possible count	f _{TIMxCLK} = 32 MHz	-	134.2	S		

Table 47. TIMx⁽¹⁾ characteristics

^{1.} TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

6.3.16 Communication interfaces

I²C interface characteristics

The STM32L100x6/8/B-A product line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: SDA and SCL are not "true" open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 48*. Refer also to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 48. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾⁽²⁾		Fast mode	Unit		
		Min	Max	Min	Max		
t _{w(SCLL)}	SCL clock low time	4.7	-	1.3	-	ше	
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6	-	μs	
t _{su(SDA)}	SDA setup time	250	-	100	-		
t _{h(SDA)}	SDA data hold time	-	3450 ⁽³⁾	-	900 ⁽³⁾		
t _{r(SDA)}	SDA and SCL rise time	-	1000	-	300		
t _{f(SDA)}	SDA and SCL fall time	-	300	-	300		
t _{h(STA)}	Start condition hold time	4.0	-	0.6	-		
t _{su(STA)}	Repeated Start condition setup time	4.7	-	0.6	-	μs	
t _{su(STO)}	Stop condition setup time	4.0	-	0.6	-	μs	
t _{w(STO:STA)}	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs	
C _b	Capacitive load for each bus line	-	400	-	400	pF	
t _{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50 ⁽⁴⁾	0	50 ⁽⁴⁾	ns	

^{1.} Guaranteed by design.

4. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$.

f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to
achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast
mode clock

The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

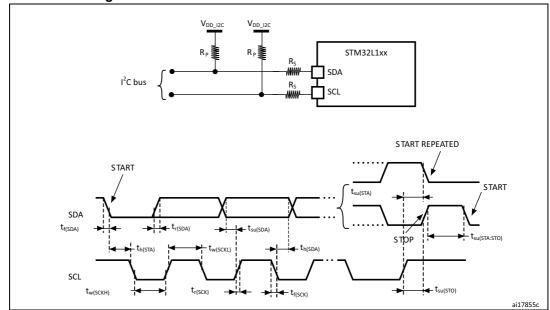


Figure 17. I²C bus AC waveforms and measurement circuit

- 1. R_S = series protection resistors
- 2. R_P = pull-up resistors
- 3. V_{DD_I2C} = I2C bus supply
- Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Table 49. SCL frequency (f_{PCLK1} = 32 MHz, $V_{DD} = V_{DD_I2C} = 3.3 V$)⁽¹⁾⁽²⁾

f //LU-\	I2C_CCR value
f _{SCL} (kHz)	$R_P = 4.7 \text{ k}\Omega$
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

- 1. R_P = External pull-up resistance, f_{SCL} = I^2C speed.
- 2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

Refer to Section 6.3.12: I/O current injection characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 50. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
_		Master mode	-	16	
f _{SCK} 1/t _{c(SCK)}	SPI clock frequency	Slave mode	-	16	MHz
(SCK)		Slave transmitter	-	12 ⁽³⁾	
$t_{r(SCK)}^{(2)} \\ t_{f(SCK)}^{(2)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
t _{su(NSS)}	NSS setup time	Slave mode	4t _{HCLK}	-	
t _{h(NSS)}	NSS hold time	Slave mode	2t _{HCLK}	-	
$t_{\text{w(SCKH)}^{(2)}}$	SCK high and low time	Master mode	t _{SCK} /2-5	t _{SCK} /2+3	
t _{su(MI)} ⁽²⁾	Data input setup time	Master mode	5	-	
t _{su(SI)} ⁽²⁾	Data input setup time	Slave mode	6	-	
t _{h(MI)} ⁽²⁾	Data input hold time	Master mode	5	-	ns
t _{h(SI)} (2)	Data input hold time	Slave mode	5	-	
t _{a(SO)} ⁽⁴⁾	Data output access time	Slave mode	0	3t _{HCLK}	
t _{v(SO)} (2)	Data output valid time	Slave mode	-	33	
t _{v(MO)} ⁽²⁾	Data output valid time	Master mode	-	6.5	
t _{h(SO)} (2)	Data output hold time	Slave mode	17	-	
t _{h(MO)} ⁽²⁾	Data output noid time	Master mode	0.5	-	

^{1.} The characteristics above are given for voltage Range 1.

^{2.} Guaranteed by characterization results.

^{3.} The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.

^{4.} Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

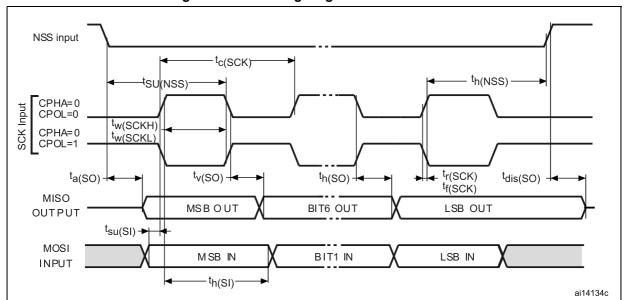
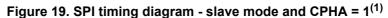
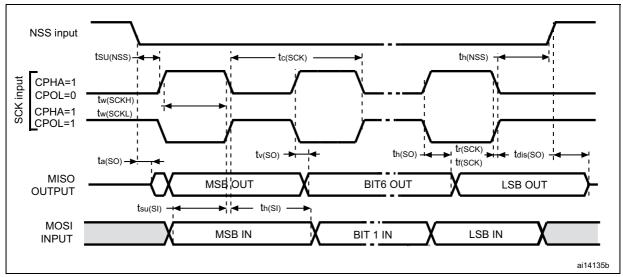


Figure 18. SPI timing diagram - slave mode and CPHA = 0





^{1.} Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

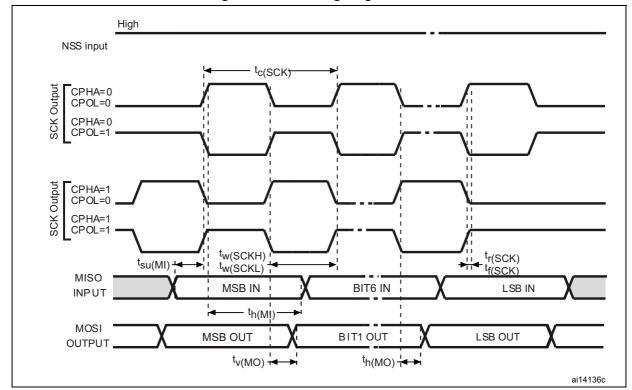


Figure 20. SPI timing diagram - master mode⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 51. USB startup time

Symbol	Parameter	Max	Unit
t _{STARTUP} ⁽¹⁾	USB transceiver startup time	1	μs

1. Guaranteed by design.

Table 52	. USB DC	: electrical	characteristics

. 42.15 12. 102 20 5.05tiloui oliuluotoliotio								
Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit			
Input levels								
V_{DD}	USB operating voltage ⁽²⁾	-	3.0	3.6	V			
V _{DI} ⁽³⁾	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-				
V _{CM} ⁽³⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	V			
V _{SE} ⁽³⁾	Single ended receiver threshold	-	1.3	2.0				
Output levels								
V _{OL} ⁽⁴⁾	Static output level low	R_L of 1.5 kΩ to 3.6 $V^{(5)}$	-	0.3	V			
V _{OH} ⁽⁴⁾	Static output level high	R_L of 15 k Ω to $V_{SS}^{(5)}$	2.8	3.6] '			

- 1. All the voltages are measured from the local ground potential.
- 2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 k Ω resistor to a 3.0-to-3.6 V voltage range.
- 3. Guaranteed by characterization results.
- 4. Guaranteed by test in production.
- 5. R_L is the load connected on the USB drivers.

Figure 21. USB timings: definition of data signal rise and fall time

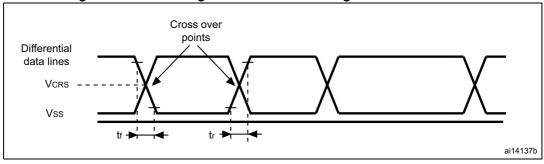


Table 53. USB: full speed electrical characteristics

	Driver characteristics ⁽¹⁾								
Symbol	Parameter	Conditions	Min	Max	Unit				
t _r	Rise time ⁽²⁾	C _L = 50 pF	4	20	ns				
t _f	Fall Time ⁽²⁾	C _L = 50 pF	4	20	ns				
t _{rfm}	Rise/ fall time matching	t _r /t _f	90	110	%				
V _{CRS}	Output signal crossover voltage	-	1.3	2.0	V				

^{1.} Guaranteed by design.

82/103

DocID025966 Rev 6

Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification section 7 (version 2.0).

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 55* are guaranteed by design.

Table 54. ADC clock frequency

Symbol	Parameter	Conditions		Min	Max	Unit
		Voltage	2.4 V ≤V _{DDA} ≤3.6 V		16	
IADC I	ADC clock frequency Range 1 & 2	1.8 V ≤V _{DDA} ≤2.4 V	0.480	8	MHz	
			Voltage Range 3		4	

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
V_{DDA}	Power supply	-	1.8	-	3.6	V	
	Current on the V _{DDA} input	Peak	-	1400	2150		
I _{VDDA}	pin	Average	-	1400	1900	μA	
V _{AIN}	Conversion voltage range	-	0 ⁽¹⁾	-	V_{DDA}	V	
	12 hit compling rate	Direct channels	-	-	1	Mono	
	12-bit sampling rate	Multiplexed channels	-	-	0.76	Msps	
	10 hit compling rate	Direct channels	-	-	1.07	Mono	
_	10-bit sampling rate	Multiplexed channels	-	-	0.8	Msps	
f _S	O hit compling yets	Direct channels	-	-	1.23	Mana	
	8-bit sampling rate	Multiplexed channels	-	-	0.89	Msps	
	C hit compline vote	Direct channels	-	-	1.45	Mana	
	6-bit sampling rate	Multiplexed channels	-	-	1	Msps	
		Direct channels 2.4 V ≤V _{DDA} ≤3.6 V	0.25	-	-		
		Multiplexed channels 2.4 V ≤V _{DDA} ≤3.6 V	0.56	-	-		
t _S	Sampling time ⁽²⁾	Direct channels 1.8 V ≤V _{DDA} ≤2.4 V	0.56	-	-	μs	
		Multiplexed channels 1.8 V ≤V _{DDA} ≤2.4 V	1	-	-		
		-	4	-	384	1/f _{ADC}	
		f _{ADC} = 16 MHz	1	-	24.75	μs	
t _{CONV}	Total conversion time (including sampling time)	-	4 to 384 (sampling phase) +12 (successi approximation)			1/f _{ADC}	
	Internal sample and hold	Direct channels	-	10	-		
C _{ADC}	capacitor	Multiplexed channels	-	- 16		- pF	

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f	External trigger frequency	12-bit conversions	-	-	Tconv+1	1/f _{ADC}
f _{TRIG}	Regular sequencer	6/8/10-bit conversions	-	-	Tconv	1/f _{ADC}
f	External trigger frequency	12-bit conversions	-	-	Tconv+2	1/f _{ADC}
f _{TRIG}	Injected sequencer	6/8/10-bit conversions	-	-	Tconv+1	1/f _{ADC}
R _{AIN}	Signal source impedance ⁽²⁾	-	ı	-	50	κΩ
+	Injection trigger conversion	f _{ADC} = 16 MHz	219	-	281	ns
t _{lat}	latency	-	3.5	-	4.5	1/f _{ADC}
t. .	Regular trigger conversion latency	f _{ADC} = 16 MHz	156	-	219	ns
t _{latr}		-	2.5	-	3.5	1/f _{ADC}
t _{STAB}	Power-up time	-	-	-	3.5	μs

^{1.} V_{SSA} must be tied to ground.

Table 56. ADC accuracy⁽¹⁾⁽²⁾

Symbol	Parameter	Test conditions	Min ⁽³⁾	Тур	Max ⁽³⁾	Unit
ET	Total unadjusted error		-	2.5	4	
EO	Offset error	2.4 V ≤ V _{DDA} ≤ 3.6 V	-	1	2	
EG	Gain error	f_{ADC} = 8 MHz, R_{AIN} = 50 Ω	-	1.5	3.5	LSB
ED	Differential linearity error	$T_A = -40 \text{ to } 85 ^{\circ}\text{C}$	-	1	2	
EL	Integral linearity error		-	2	3	
ENOB	Effective number of bits		9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio	$72.4 \text{ V} \leq \text{V}_{DDA} \leq 3.6 \text{ V}$ $72.4 \text{ V} \leq \text{V}_{DDA} \leq 3.6 \text{ V}$ $72.4 \text{ OF } \Omega = 16 \text{ MHz}, R_{AIN} = 50 \Omega$	59	62	-	
SNR	Signal-to-noise ratio	─ T _A = -40 to 85 ° C _ F _{input} =10 kHz	60	62	-	dB
THD	Total harmonic distortion	- Input 19 ta ta	-	-72	-69	
ENOB	Effective number of bits	1.8 V ≤ V _{DDA} ≤ 2.4 V	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio	$f_{ADC} = 8 \text{ MHz or 4 MHz},$ $R_{AIN} = 50 \Omega$	59	62	-	
SNR	Signal-to-noise ratio	T _A = -40 to 85 ° C	60	62	-	dB
THD	Total harmonic distortion	F _{input} =10 kHz	-	-72	-69	
ET	Total unadjusted error		-	2	3	
EO	Offset error	1.8 V ≤ V_{DDA} ≤ 2.4 V f_{ADC} = 4 MHz, R_{AIN} = 50 Ω T_{A} = -40 to 85 °C	-	1	1.5	
EG	Gain error		-	1.5	2.5	LSB
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-		3	

^{1.} ADC DC accuracy values are measured after internal calibration.

^{2.} See Table 57: Maximum source impedance RAIN max for $R_{\mbox{\scriptsize AIN}}$ limitations

- ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents. Any positive injection current within the limits specified for $I_{\text{INJ}(\text{PIN})}$ and $\Sigma I_{\text{INJ}(\text{PIN})}$ in Section 6.3.12 does not affect the ADC
- 3. Guaranteed by characterization results.

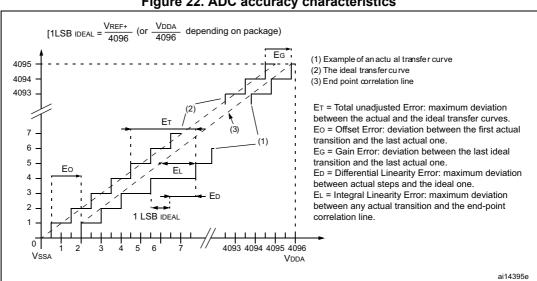
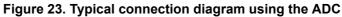
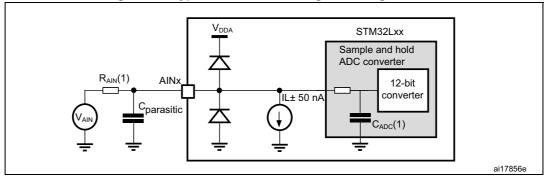


Figure 22. ADC accuracy characteristics





- Refer to *Table 57: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 55: ADC characteristics* for the value of CADC
- $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

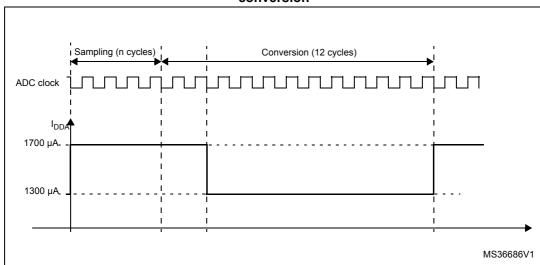


Figure 24. Maximum dynamic current consumption on V_{DDA} supply pin during ADC conversion

Table 57. Maximum source impedance R_{AIN} max⁽¹⁾

Ts (µs)	Multiplexed channels		Multiplexed channels Direct channels		tiplexed channels Direct channels			
	2.4 V < V _{DDA} < 3.6 V 1.8 V < V _{DDA} < 2.4 V 2.4 V < V _{DD}		2.4 V < V _{DDA} < 3.3 V	< V _{DDA} < 3.3 V 1.8 V < V _{DDA} < 2.4 V				
0.25	Not allowed	Not allowed	0.7	Not allowed	4			
0.5625	0.8	Not allowed	2.0	1.0	9			
1	2.0	0.8	4.0	3.0	16			
1.5	3.0	1.8	6.0	4.5	24			
3	6.8	4.0	15.0	10.0	48			
6	15.0	10.0	30.0	20.0	96			
12	32.0	25.0	50.0	40.0	192			
24	50.0	50.0	50.0	50.0	384			

^{1.} Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 8*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Number of samples calculated for f_{ADC} = 16 MHz. For f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).

6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 58. DAC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
(4)	Current consumption on	No load, middle code (0x800)	-	330	540	μA
I _{DDA} ⁽¹⁾	V _{DDA} supply V _{DDA} = 3.3 V	No load, worst code (0xF1C)	-	540	870	μΑ
R_L	Resistive load	DAC output buffer ON Connected to V _{SSA}	-	-	-	kΩ
C _L	Capacitive load	DAC output buffer ON	-	-	50	pF
R _O	Output impedance	DAC output buffer OFF	12	16	20	kΩ
V	Voltage on DAC_OUT	DAC output buffer ON	0.2	-	V _{DDA} – 0.2	V
V _{DAC_OUT}	output	DAC output buffer OFF	0.5	-	V _{DDA} - 1LSB	mV
DNL ⁽¹⁾	Differential non linearity ⁽²⁾	$C_L \le 50$ pF, $R_L \ge 5$ k Ω DAC output buffer ON	-	1.5	3	
		No R _L , C _L \leq 50 pF DAC output buffer OFF	-	1.5	3	
INL ⁽¹⁾	Integral non linearity ⁽³⁾	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$ DAC output buffer ON	-	2	4	
INC	integral non intearity (No R _L , C _L \leq 50 pF DAC output buffer OFF	-	2	4	LSB
Offset ⁽¹⁾	Offset error at code 0x800 ⁽⁴⁾	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$ DAC output buffer ON	-	±10	±25	
Oliset	Offset effor at code 0x000	No R_L , $C_L \le 50 pF$ DAC output buffer OFF	-	±5	±8	
Offset1 ⁽¹⁾	Offset error at code 0x001 ⁽⁵⁾	No R _L , C _L \leq 50 pF DAC output buffer OFF	-	±1.5	±5	
(4)	Offset error temperature	V _{DDA} = 3.3V,T _A = 0 to 50 ° C DAC output buffer OFF	-20	-10	0	\//90
dOffset/dT ⁽¹⁾	coefficient (code 0x800)	V _{DDA} = 3.3V, T _A = 0 to 50 °C DAC output buffer ON	0	20	50	- μV/°C
Gain ⁽¹⁾	Gain error ⁽⁶⁾	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / - 0.5%	0/
Gainer	Gaill elloix	No R _L , C _L \leq 50 pF DAC output buffer OFF	-	+0 / - 0.2%	+0 / - 0.4%	- %



Table 58. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
dGain/dT ⁽¹⁾	Gain error temperature	V _{DDA} = 3.3V, T _A = 0 to 50 ° C DAC output buffer OFF	-10	-2	0	μV/°C
uGaiii/u1 v	coefficient	V _{DDA} = 3.3V, T _A = 0 to 50 °C DAC output buffer ON	-40	-8	0	μν/ Ο
TUE ⁽¹⁾	Total unadjusted error	$C_L \le 50$ pF, $R_L \ge 5$ k Ω DAC output buffer ON	-	12	30	LSB
TOE	Total unadjusted error	No R _L , C _L \leq 50 pF DAC output buffer OFF	-	8	12	LOB
tsettling	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$	-	7	12	μs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$	-	-	1	Msps
t _{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register) ⁽⁷⁾	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$	-	9	15	μs
PSRR+	V _{DDA} supply rejection ratio (static DC measurement)	$C_L \le 50 \text{ pF}, R_L \ge 5 \text{ k}\Omega$	-	-60	-35	dB

^{1.} Guaranteed by characterization results.

^{2.} Difference between two consecutive codes - 1 LSB.

^{3.} Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.

^{4.} Difference between the value measured at Code (0x800) and the ideal value = $V_{DDA}/2$.

^{5.} Difference between the value measured at Code (0x001) and the ideal value.

^{6.} Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and $(V_{DDA} - 0.2)$ V when buffer is ON.

^{7.} In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Buffered/Non-buffered DAC

Buffer(1)

12-bit digital to analog converter

C L

ai17157V3

Figure 25. 12-bit buffered /non-buffered DAC

 The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Comparator

Table 59. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.8		3.6	V
R _{400K}	R _{400K} value	-	-	400	-	kΩ
R _{10K}	R _{10K} value	-	-	10	-	K22
V _{IN}	Comparator 1 input voltage range	-	0.6	1	V_{DDA}	V
t _{START}	Comparator startup time	-	-	7	10	ue
td	Propagation delay ⁽²⁾	-	-	3	10	μs
Voffset	Comparator offset	-	-	£3	±10	mV
d _{Voffset} /dt	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6 \text{ V}$ $V_{IN+} = 0 \text{ V}$ $V_{IN-} = V_{REFINT}$ $T_A = 25 ^{\circ}\text{ C}$	0	1.5	10	mV/1000 h
I _{COMP1}	Current consumption ⁽³⁾	-	-	160	260	nA

^{1.} Guaranteed by characterization results.

^{2.} The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

^{3.} Comparator consumption only. Internal reference voltage not included.

Table 60. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V _{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
+ .	Comparator startup time	Fast mode	-	15	20	
t _{START}	Comparator startup time	Slow mode	-	20	25	
+	Propagation delay ⁽²⁾ in slow mode	1.8 V ≤V _{DDA} ≤2.7 V	-	1.8	3.5	
t _{d slow}	Propagation delay. 7 in Slow mode	2.7 V ≤V _{DDA} ≤3.6 V	-	2.5	6	μs
+	Propagation delay ⁽²⁾ in fast mode	1.8 V ≤V _{DDA} ≤2.7 V	-	0.8	2	
t _{d fast}	Propagation delay. 7 in last mode	2.7 V ≤V _{DDA} ≤3.6 V	-	1.2	4	
V _{offset}	Comparator offset error	-	-	±4	±20	mV
dThreshold/ Threshold voltage temperature coefficient		$V_{DDA} = 3.3V$ $T_A = 0$ to $50 ^{\circ}$ C $V_{-} = V_{REFINT}$, $3/4 ^{\circ}$ V_{REFINT} , $1/2 ^{\circ}$ V_{REFINT} , $1/4 ^{\circ}$ V_{REFINT}	-	15	100	ppm /°C
1	Current consumption ⁽³⁾	Fast mode	-	3.5	5	
I _{COMP2}	Carrent consumptions	Slow mode	-	0.5	2	μA

^{1.} Guaranteed by characterization results.

^{2.} The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.20 LCD controller

The STM32L100x6/8/B-A devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 61. LCD controller characteristics

Symbol	Parameter	Min	Тур	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	
V _{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V _{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V _{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V _{LCD3}	LCD internal reference voltage 3	-	2.98	-	V
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V _{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V _{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V _{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C _{ext}	V _{LCD} external capacitance	0.1	-	2	μF
ı (1)	Supply current at V _{DD} = 2.2 V	-	3.3	-	
I _{LCD} ⁽¹⁾	Supply current at V _{DD} = 3.0 V	-	3.1	-	μA
R _{Htot} ⁽²⁾	Low drive resistive network overall value	5.28	6.6	7.92	МΩ
R _L ⁽²⁾	High drive resistive network total value	192	240	288	kΩ
V ₄₄	Segment/Common highest level voltage	-	-	V_{LCD}	V
V ₃₄	Segment/Common 3/4 level voltage	-	3/4 V _{LCD}	-	
V ₂₃	Segment/Common 2/3 level voltage	-	2/3 V _{LCD}	-	
V ₁₂	Segment/Common 1/2 level voltage	-	1/2 V _{LCD}	-	V
V ₁₃	V ₁₃ Segment/Common 1/3 level voltage		1/3 V _{LCD}	-	, v
V ₁₄	V ₁₄ Segment/Common 1/4 level voltage		1/4 V _{LCD}	-	İ
V ₀	Segment/Common lowest level voltage		-	-	İ
$\Delta Vxx^{(2)}$	Segment/Common level voltage error T _A = -40 to 85 ° C	-	-	±50	mV

LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected

^{2.} Guaranteed by characterization results.

Package information STM32L100x6/8/B-A

Package information 7

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

LQFP64 10 x 10 mm, 64-pin low-profile quad flat package 7.1 information

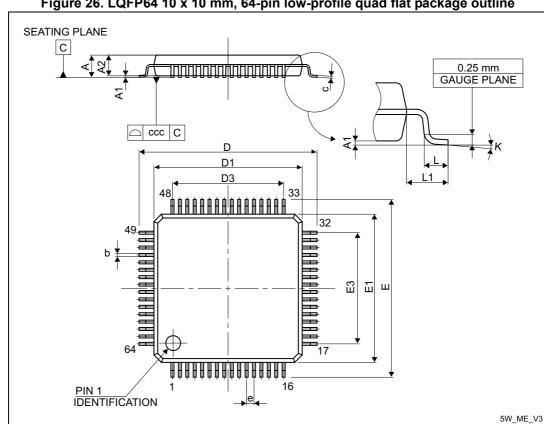


Figure 26. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline

1. Drawing is not to scale.

Table 62. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical

Symbol	Symbol millimeters				inches ⁽¹⁾	
Symbol	Min	Тур	Max	Тур	Min	Max
Α	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571



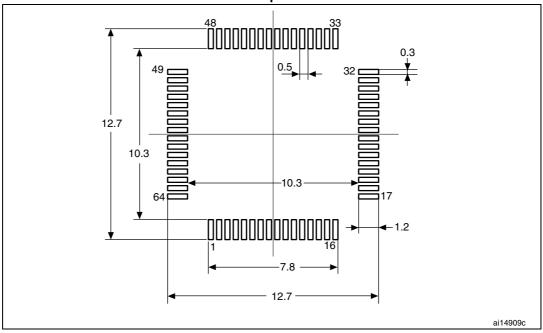
STM32L100x6/8/B-A Package information

Table 62. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data (continued)

	data (continued)									
Symbol		millimeters			inches ⁽¹⁾					
Symbol	Min	Тур	Max	Тур	Min	Max				
b	0.170	0.220	0.270	0.0067	0.0087	0.0106				
С	0.090	-	0.200	0.0035	-	0.0079				
D	-	12.000	-	-	0.4724	-				
D1	-	10.000	-	-	0.3937	-				
D3	-	7.500	-	-	0.2953	-				
Е	-	12.000	-	-	0.4724	-				
E1	-	10.000	-	-	0.3937	-				
E3	-	7.500	-	-	0.2953	-				
е	-	0.500	-	-	0.0197	-				
K	0°	3.5°	7°	0°	3.5°	7°				
L	0.450	0.600	0.750	0.0177	0.0236	0.0295				
L1	-	1.000	-	-	0.0394	-				
ccc	-	-	0.080	-	-	0.0031				

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

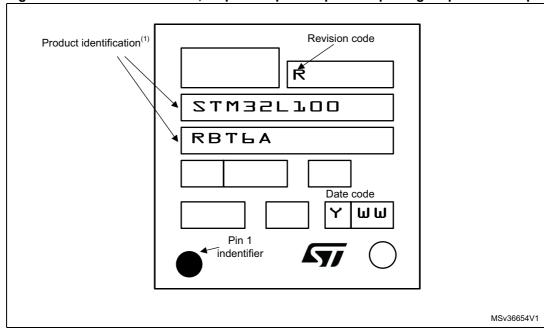
Package information STM32L100x6/8/B-A

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 28. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified
and therefore not approved for use in production. ST is not responsible for any consequences resulting
from such use. In no event will ST be liable for the customer using any of these engineering samples in
production. ST's Quality department must be contacted prior to any decision to use these engineering
samples to run a qualification activity.

57

7.2 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Pin 1 identifier laser marking area D Seating b Detail Y D Exposed pad D2 area C 0.500x45° R 0.125 typ Detail Z E2 A0B9 ME V3

Figure 29. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline

- 1. Drawing is not to scale.
- 2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
- 3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

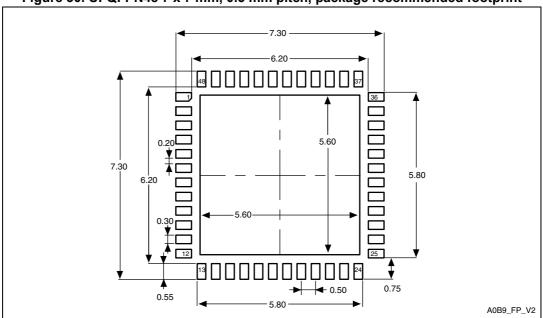
Package information STM32L100x6/8/B-A

Table 63. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
Α	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
Т	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
е	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 30. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



1. Dimensions are in millimeters.

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

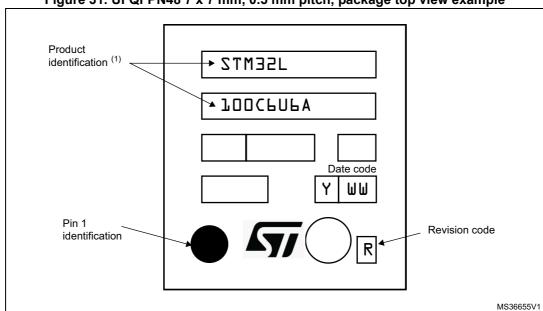


Figure 31. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example

^{1.} Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Package information STM32L100x6/8/B-A

7.3 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

 $T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

P_{I/O} max represents the maximum power dissipation on output pins where:

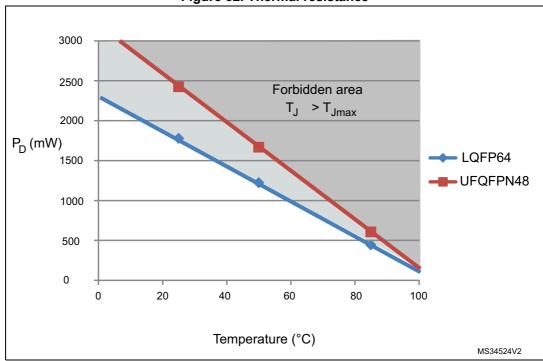
$$\mathsf{P}_\mathsf{I/O} \; \mathsf{max} = \Sigma \; (\mathsf{V}_\mathsf{OL} \times \mathsf{I}_\mathsf{OL}) + \Sigma ((\mathsf{V}_\mathsf{DD} - \mathsf{V}_\mathsf{OH}) \times \mathsf{I}_\mathsf{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 64. Thermal characteristics

Symbol	Parameter	Value	Unit	
Α	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W	
Θ_{JA}	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	33	- C/VV	

Figure 32. Thermal resistance



7.3.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.



8 Ordering information

Table 65. Ordering information scheme STM32 L 100 R B A TR **Example:** Т **Device family** STM32 = ARM-based 32-bit microcontroller **Product type** L = Low power Device subfamily 100 Pin count C = 48 pinsR = 64 pinsFlash memory size 6 = 32 Kbytes of Flash memory 8 = 64 Kbytes of Flash memory B = 128 Kbytes of Flash memory **Package** T = LQFP U = UFQFPN Temperature range 6 = Industrial temperature range, -40 to 85 °C **Options** A = Device generation A

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



STM32L100x6/8/B-A Revision history

9 Revision history

Table 66. Document revision history

Date	Revision	Changes	
25-Mar-2014	1	Initial release.	
27-Oct-2014	2	Updated DMIPS features in cover page and Section 2: Description Updated current consumption in Table 20: Current consumption in Sleep mode. Updated Table 25: Peripheral current consumption with new measured values. Updated Table 57: Maximum source impedance RAIN max adding note 2.	
03-Feb-2015	3	Updated Section 7: Package information with new package device markings. Updated Figure 5: Memory map.	
30-Apr-2015	4	Updated Section 7: Package information structure: Paragraph titles and paragraph heading level. Updated Table 62: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data. Updated Section 7: Package information for LQFP64 and UFQFPN48 package device markings, adding text for device orientation versus pin 1 identifier. Updated Table 17: Embedded internal reference voltage temperature coefficient at 100ppm/°C and table footnote 3: "guaranteed by design" changed by "guaranteed by characterization results". Updated Table 60: Comparator 2 characteristics new maximum threshold voltage temperature coefficient at 100ppm/°C.	
25-Apr-2016	5	Updated <i>Table 40: ESD absolute maximum ratings</i> CDM class. Updated all the notes, removing 'not tested in production'. Updated <i>Table 11: Voltage characteristics</i> adding note about V _{REF-pin} . Updated <i>Table 3: Functionalities depending on the operating power supply range</i> LSI and LSE functionalities putting "Y" in Standby mode. Removed note 1 below <i>Figure 2: Clock tree</i> . Updated <i>Section 7: Package information</i> replacing "Marking of engineering samples" by "device marking". Updated <i>Table 58: DAC characteristics</i> resistive load.	

Revision history STM32L100x6/8/B-A

Table 66. Document revision history (continued)

Date	Revision	Changes
		Updated Table 43: I/O static characteristics pull-up and pull-down values.
		Updated Table 46: NRST pin characteristics pull-up values.
		Updated Section 7: Package information adding information about other optional marking or inset/upset marks.
		Updated note 1 below all the package device marking figures.
		Updated Nested vectored interrupt controller (NVIC) in Section 3.2: ARM® Cortex®-M3 core with MPU about process state automatically saved.
28-Aug-2017	6	Updated <i>Table 3: Functionalities depending on the operating power supply range</i> removing I/O operation column and adding note about GPIO speed.
		Updated <i>Table 42: I/O current injection susceptibility</i> note by 'injection is not possible'.
		Updated <i>Figure 16: Recommended NRST pin protection</i> note about the 0.1uF capacitor.
		Updated Section 3.1: Low-power modes Low-power run mode (MSI) RC oscillator clock.
		Updated <i>Table 5: Working mode-dependent functionalities (from Run/active down to standby)</i> disabling I2C functionality in Lowpower Run and Low-power Sleep modes.

IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics - All rights reserved

