REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV																						
PAGE																						
REV STATUS OF PAGES	**REV**																					
	PAGE	1	2	3	4	5	6	7	8	9	10											

PMIC N/A

PREPARED BY
Phu H. Nguyen

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

Original date of drawing
YY MM DD

18-08-09

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

TITLE

MICROCIRCUIT, DIGITAL, 3-AXIS, ±200 *g*, DIGITAL MEMS ACCELEROMETER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**
A	**16236**

DWG NO.
V62/18612

REV

PAGE 1 **OF** 10

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

AMSC N/A

5962-V100-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3-Axis, ±200 g Digital MEMS Accelerometer microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/18612	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADXL375 –EP	3-Axis, ±200 *g* Digital MEMS Accelerometer

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	14	Land Grid Array (LGA) Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Acceleration, Any Axis :
- Unpowered ..... 10000 *g*
- Powered ..... 10000 *g*

V_S ..... -0.3 V to 3.9 V
$V_{DD\ I/O}$ ..... -0.3 V to 3.9 V
Digital Pins ..... -0.3 V to $V_{DD\ I/O}$ + 0.3 V or 3.9 V whichever is less
Output Short-Circuit Duration (Any Pin to Ground) ..... Indedfinite
Temperature Range:
- Powered ..... -55°C to 105°C
- Storage ..... -65°C to 150°C

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JC}	Unit
Case X 2/	150	85	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ 3/	Max	
SENSOR INPUT (Each Axis)					
Measurement Range 4/		±180	±200		*g*
Nonlinearity	Percentage of full scale		±0.25		%
Cross-Axis Sensitivity 5/			±2.5		%
SENSITIVITY (Each Axis)					
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT} 4/ 6/	ODR ≤ 800 Hz	18.4	20.5	22.6	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT} 4/ 6/	ODR ≤ 800 Hz	44	49	54	m*g*/LSB
Sensitivity Change Due to Temperature			±0.02		%/°C
0 *g* OFFSET (Each Axis)					
0 *g* Output for X_{OUT}, Y_{OUT}, Z_{OUT}		-6000	±400	+6000	m*g*
0 *g* Offset vs. Temperature			±10		m*g*/°C
NOISE					
Noise	X-, y-, and z-axes		5		mg/√Hz
OUTPUT DATA RATE AND BANDWIDTH (User selectable) 7/					
Output Data Rate (ODR) 6/ 8/		0.1		3200	Hz
SELF-TEST					
Output Change in Z-Axis			6.4		*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		2.0	2.5	3.6	V
Interface Voltage Range ($V_{DD\ I/O}$)		1.7	1.8	V_S	V
Supply Current					
Measurement Mode	ODR ≥ 100 Hz		145		µA
	ODR ≤ 3 Hz		35		µA
Standby Mode			0.1		µA
Turn-On and Wake-Up Time 10/	ODR = 3200 Hz		1.4		ms
TEMPERATURE					
Operating Temperature Range		-55		+105	°C
WEIGHT					
Device Weight			30		mg

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 2.5 V, acceleration = 0 *g*, C_S = 10 µF tantalum, $C_{I/O}$ = 0.1 µF, and output data rate (ODR) = 800 Hz, unless otherwise noted.

3/ Typical specifications are for at least 68% of the population of devices and are based on the worst case of mean ± 1 σ distribution, except for sensitivity, which represents the target value.

4/ Minimum and maximum specifications represent the worst case of mean ± 3 σ distribution and are not guaranteed in production.

5/ Cross axis sensitivity is defined as coupling between any two axes.

6/ The output format for the 1600 Hz and 3200 Hz output data rates is different from the output format for the other output data rates. For more information, see manufacturer data sheet.

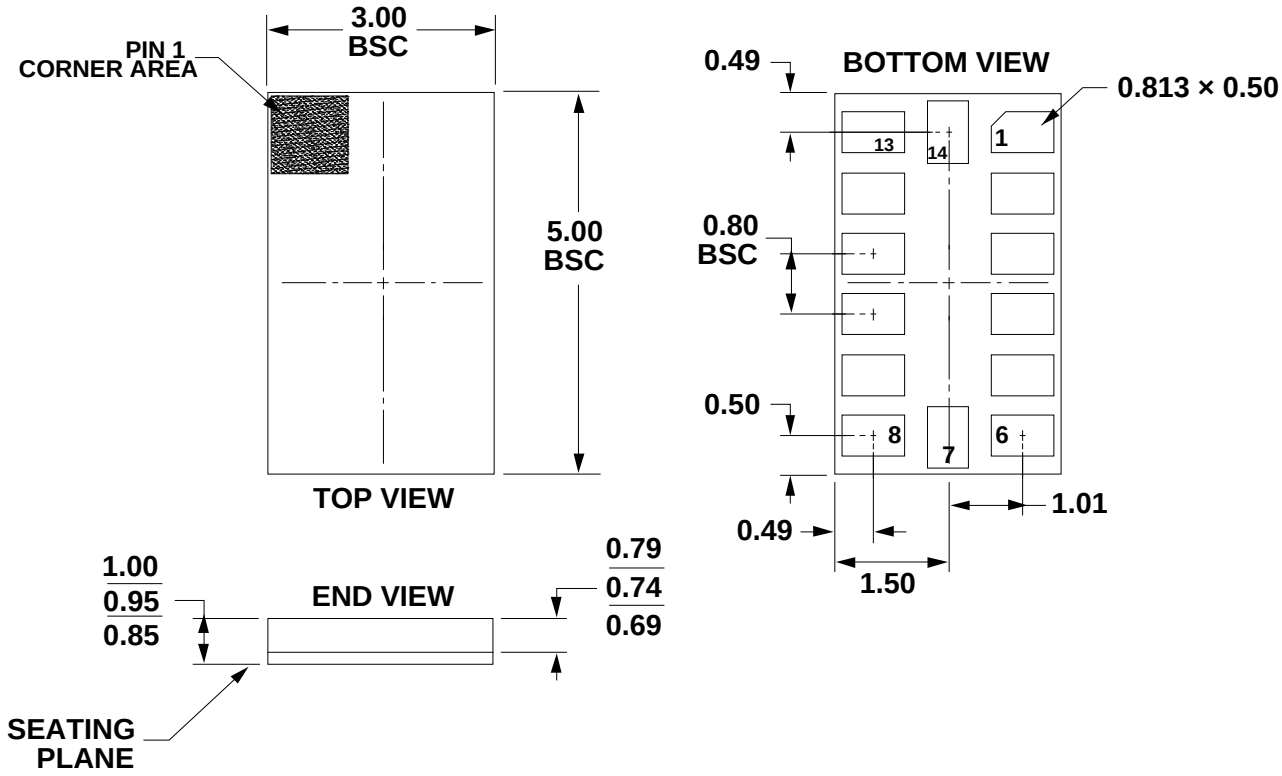
7/ Bandwidth is the −3 dB frequency and is half the output data rate: bandwidth = ODR/2.

8/ Output data rates < 6.25 Hz exhibit additional offset shift with increased temperature.

9/ Self test change is defined as the output (*g*) when the SELF_TEST bit = 1 (DATA_FORMAT register, Address 0x31) minus the output (*g*) when the SELF_TEST bit = 0. Due to device filtering, the output reaches its final value after 4 × τ when enabling or disabling self test, where τ = 1/(data rate). For the self test to operate correctly, the part must be in normal power operation (LOW_POWER bit = 0 in the BW_RATE register, Address 0x2C).

10/ Turn on and wake-up times are determined by the user defined bandwidth. At a 100 Hz data rate, the turn on and wake-up times are each approximately 11.1 ms. For other data rates, the turn on and wake-up times are each approximately τ + 1.1 ms, where τ = 1/(data rate).

Case X



NOTES:

1. All linear dimensions are in millimeters.

FIGURE 1. Case outline.

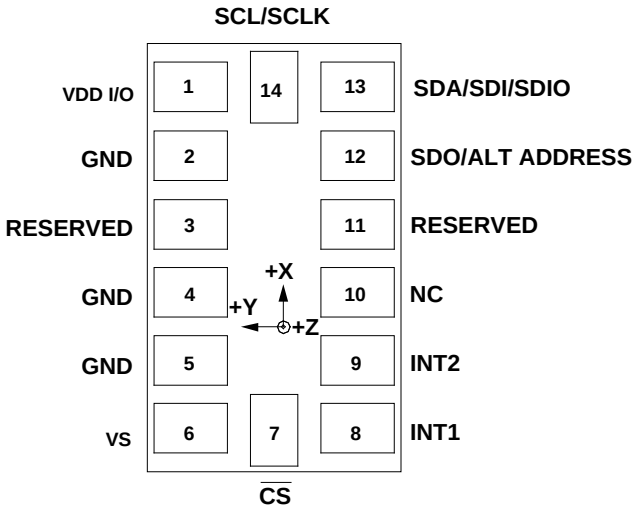


FIGURE 2. Terminal connections.

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
2	GND	Ground. This pin must be connected to ground.
3	RESERVED	Reserved. This pin must be connected to V_S or left open.
4	GND	Ground. This pin must be connected to ground.
5	GND	Ground. This pin must be connected to ground.
6	V_S	Supply Voltage.
7	$\overline{CS}$	Chip Select.
8	INT1	Interrupt 1 Output.
9	INT2	Interrupt 2 Output.
10	NC	Not Internally Connected.
11	RESERVED	Reserved. This pin must be connected to ground or left open.
12	SDO/ALT ADDRESS	SPI 4-Wire Serial Data Output (SDO)/I_2C Alternate Address Select (ALT ADDRESS).
13	SDA/SDI/SDIO	I^2C Serial Data (SDA)/SPI 4-Wire Serial Data Input (SDI)/SPI 3-Wire Serial Data Input and Output (SDIO).
14	SCL/SCLK	I^2C Serial Communications Clock (SCL)/SPI Serial Communications Clock (SCLK).

FIGURE 3. Terminal function.

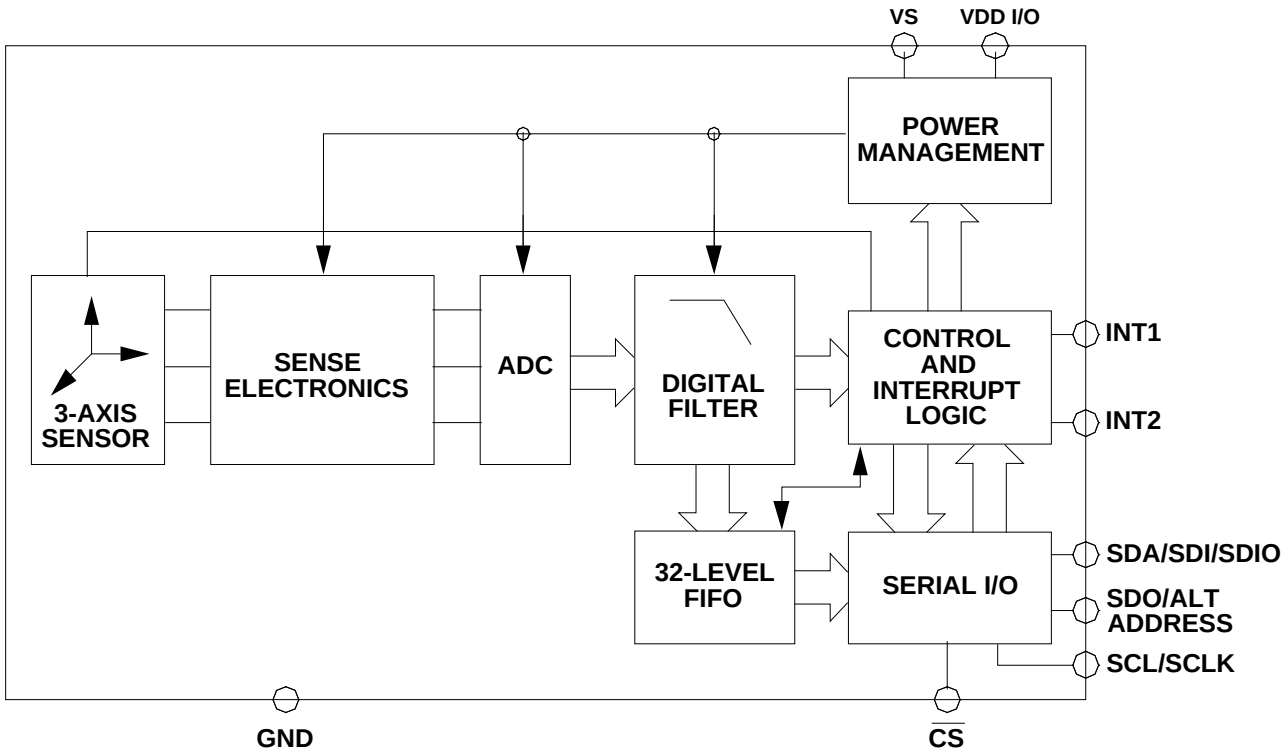


FIGURE 4. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Order Quantity	Vendor part number
V62/18612-01XE	24355	Tray = 490	ADXL375SCCZ-EP
		RL7 quantity = 1500	ADXL375SCCZ-EP -RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106