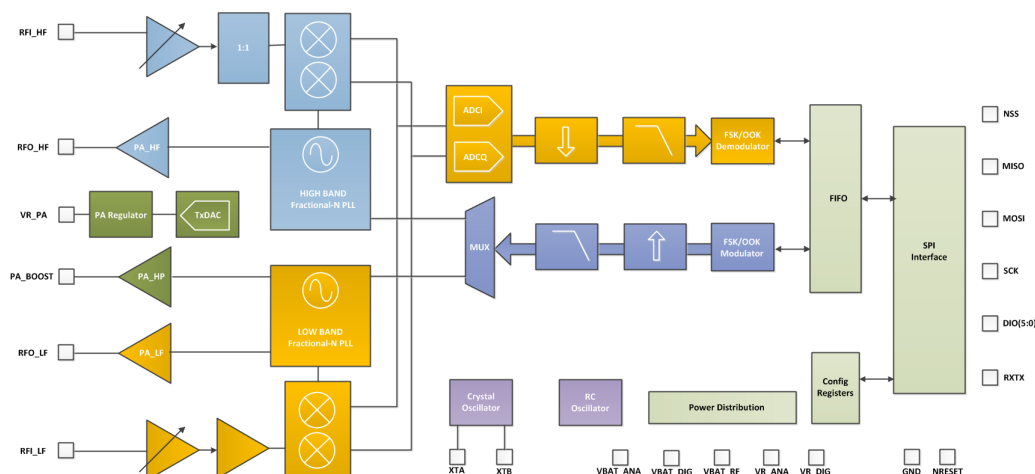


SX1236 - 137 MHz to 1020 MHz Low Power Bi-Band Transceiver

GENERAL DESCRIPTION

The SX1236 is a fully integrated ISM band transceiver capable of bi-band operation in most un-licensed bands in the sub-GHz space with a minimum of external components. It offers a combination of high link budget and low current consumption in all operating modes. The 143 dB link budget is achieved by a low noise CMOS receiver front end and up to +20 dBm of transmit output power. A set of internal power amplifiers are provided permitting either fully regulated - for constant RF performance, or direct supply connection - for optimal efficiency. This makes SX1236 ideal for either M2M applications powered by alkaline battery chemistries or long battery life metering applications using Lithium battery chemistries.

The Low-IF architecture of the SX1236 sees fast transceiver start times and demodulation predicated towards low modulation index and gaussian filtered spectrally efficient modulation formats.

This device also support high performance (G)FSK modes for systems including WMBus, IEEE802.15.4g. The SX1236 delivers exceptional phase noise, selectivity, receiver linearity and IIP3 for significantly lower current consumption than competing devices.

ORDERING INFORMATION

| Part Number | Delivery | MOQ / Multiple |
|--------------|----------|----------------|
| SX1236IMLTRT | T&R | 3000 pieces |

- ◆ QFN 28 Package - Operating Range [-40;+85°C]
- ◆ Pb-free, Halogen free, RoHS/WEEE compliant product

KEY PRODUCT FEATURES

- ◆ 143 dB maximum link budget
- ◆ +20 dBm - 100 mW constant RF output vs. V supply
- ◆ +14 dBm high efficiency PA
- ◆ Programmable bit rate up to 300 kbps
- ◆ High sensitivity: down to -123 dBm
- ◆ Bullet-proof front end: IIP3 = -11 dBm
- ◆ Excellent blocking immunity
- ◆ Low RX current of 10.8 mA, 200 nA register retention
- ◆ Fully integrated synthesizer with a resolution of 61 Hz
- ◆ FSK, GFSK, MSK, GMSK and OOK modulation
- ◆ Built-in bit synchronizer for clock recovery
- ◆ Preamble detection
- ◆ 127 dB Dynamic Range RSSI
- ◆ Ultra-fast AFC
- ◆ Packet engine up to 256 bytes with CRC
- ◆ Built-in temperature sensor and low battery indicator

APPLICATIONS

- ◆ Automated Meter Reading.
- ◆ Home and Building Automation.
- ◆ Wireless Alarm and Security Systems.
- ◆ Industrial Monitoring and Control
- ◆ Long range Irrigation Systems

Table of contents

| Section | Page |
|--|-------------|
| 1. General Description | 8 |
| 1.1. Simplified Block Diagram | 8 |
| 1.2. Pin Diagram | 9 |
| 1.3. Pin Description | 10 |
| 1.4. Package Marking | 11 |
| 2. Electrical Characteristics | 12 |
| 2.1. ESD Notice | 12 |
| 2.2. Absolute Maximum Ratings | 12 |
| 2.3. Operating Range | 12 |
| 2.4. Thermal Properties | 12 |
| 2.5. Chip Specification | 13 |
| 2.5.1. Power Consumption | 13 |
| 2.5.2. Frequency Synthesis | 13 |
| 2.5.3. FSK/OOK Mode Receiver | 15 |
| 2.5.4. FSK/OOK Mode Transmitter | 16 |
| 2.5.5. Digital Specification | 18 |
| 3. SX1236 Features | 19 |
| 4. SX1236 Digital Electronics | 21 |
| 4.1. FSK/OOK Modem | 21 |
| 4.1.1. Bit Rate Setting | 21 |
| 4.1.2. FSK/OOK Transmission | 22 |
| 4.1.3. FSK/OOK Reception | 23 |
| 4.1.4. Operating Modes in FSK/OOK Mode | 28 |
| 4.1.5. Startup Times | 29 |
| 4.1.6. Receiver Startup Options | 32 |
| 4.1.7. Receiver Restart Methods | 33 |
| 4.1.8. Top Level Sequencer | 34 |
| 4.1.9. Data Processing in FSK/OOK Mode | 39 |
| 4.1.10. FIFO | 40 |
| 4.1.11. Digital IO Pins Mapping | 43 |
| 4.1.12. Continuous Mode | 44 |
| 4.1.13. Packet Mode | 45 |
| 4.1.14. io-homecontrol® Compatibility Mode | 53 |
| 4.2. SPI Interface | 54 |
| 5. SX1236 Analog & RF Frontend Electronics | 55 |
| 5.1. Power Supply Strategy | 55 |
| 5.2. Low Battery Detector | 55 |
| 5.3. Frequency Synthesis | 55 |
| 5.3.1. Crystal Oscillator | 55 |

Table of contents

| Section | Page |
|--|-------------|
| 5.3.2. CLKOUT Output | 56 |
| 5.3.3. PLL | 56 |
| 5.3.4. RC Oscillator | 56 |
| 5.4. Transmitter Description | 57 |
| 5.4.1. Architecture Description | 57 |
| 5.4.2. RF Power Amplifiers | 57 |
| 5.4.3. High Power +20 dBm Operation | 58 |
| 5.4.4. Over Current Protection | 59 |
| 5.5. Receiver Description | 59 |
| 5.5.1. Overview | 59 |
| 5.5.2. Receiver Enabled and Receiver Active States | 59 |
| 5.5.3. Automatic Gain Control | 59 |
| 5.5.4. RSSI | 60 |
| 5.5.5. Channel Filter | 61 |
| 5.5.6. Temperature Measurement | 62 |
| 6. Description of the Registers | 63 |
| 6.1. Register Table Summary | 63 |
| 6.2. Register Map | 65 |
| 6.3. Band Specific Additional Registers | 78 |
| 7. Application Information | 80 |
| 7.1. Crystal Resonator Specification | 80 |
| 7.2. Reset of the Chip | 80 |
| 7.2.1. POR | 80 |
| 7.2.2. Manual Reset | 81 |
| 7.3. Top Sequencer: Listen Mode Examples | 81 |
| 7.3.1. Wake on Preamble Interrupt | 81 |
| 7.3.2. Wake on SyncAddress Interrupt | 84 |
| 7.4. Top Sequencer: Beacon Mode | 87 |
| 7.4.1. Timing diagram | 87 |
| 7.4.2. Sequencer Configuration | 87 |
| 7.5. Example CRC Calculation | 89 |
| 7.6. Example Temperature Reading | 90 |
| 8. Packaging Information | 92 |
| 8.1. Package Outline Drawing | 92 |
| 8.2. Recommended Land Pattern | 93 |
| 8.3. Tape & Reel Information | 94 |
| 9. Revision History | 95 |

Table of contents

| Section | Page |
|---|-------------|
| Table 1. Pin Description | 10 |
| Table 2. Absolute Maximum Ratings | 12 |
| Table 3. Operating Range | 12 |
| Table 4. Thermal Properties | 12 |
| Table 5. Power Consumption Specification | 13 |
| Table 6. Frequency Synthesizer Specification | 13 |
| Table 7. FSK/OOK Receiver Specification | 15 |
| Table 8. Transmitter Specification | 16 |
| Table 9. Digital Specification | 18 |
| Table 10. Bit Rate Examples | 21 |
| Table 11. Preamble Detector Settings | 27 |
| Table 12. RxTrigger Settings to Enable Timeout Interrupts | 28 |
| Table 13. Basic Transceiver Modes | 28 |
| Table 14. Receiver Startup Time Summary | 30 |
| Table 15. Receiver Startup Options | 33 |
| Table 16. Sequencer States | 34 |
| Table 17. Sequencer Transition Options | 35 |
| Table 18. Sequencer Timer Settings | 37 |
| Table 19. Status of FIFO when Switching Between Different Modes of the Chip | 41 |
| Table 20. DIO Mapping, Continuous Mode | 43 |
| Table 21. DIO Mapping, Packet Mode | 43 |
| Table 22. CRC Description | 51 |
| Table 23. Frequency Bands | 56 |
| Table 24. Power Amplifier Mode Selection Truth Table | 57 |
| Table 25. High Power Settings | 58 |
| Table 26. Operating Range, +20dBm Operation | 58 |
| Table 27. Operating Range, +20dBm Operation | 58 |
| Table 28. Trimming of the OCP Current | 59 |
| Table 29. LNA Gain Control and Performances | 60 |
| Table 30. RssiSmoothing Options | 60 |
| Table 31. Available RxBw Settings | 61 |
| Table 32. Registers Summary | 63 |
| Table 33. Register Map | 65 |
| Table 34. Low Frequency Additional Registers | 78 |
| Table 35. High Frequency Additional Registers | 79 |
| Table 36. Crystal Specification | 80 |
| Table 37. Listen Mode with PreambleDetect Condition Settings | 83 |
| Table 38. Listen Mode with PreambleDetect Condition Recommended DIO Mapping | 83 |
| Table 39. Listen Mode with SyncAddress Condition Settings | 86 |

Table of contents

| Section | Page |
|---|-------------|
| Table 40. Listen Mode with PreambleDetect Condition Recommended DIO Mapping | 86 |
| Table 41. Beacon Mode Settings | 88 |
| Table 42. Revision History | 95 |

Table of contents

| Section | Page |
|--|-------------|
| Figure 1. Block Diagram | 8 |
| Figure 2. Pin Diagram | 9 |
| Figure 3. Marking Diagram | 11 |
| Figure 4. SX1236 Block Schematic Diagram | 19 |
| Figure 5. OOK Peak Demodulator Description | 23 |
| Figure 6. Floor Threshold Optimization | 24 |
| Figure 7. Bit Synchronizer Description | 25 |
| Figure 8. Startup Process | 29 |
| Figure 9. Time to RSSI Sample | 30 |
| Figure 10. Tx to Rx Turnaround | 31 |
| Figure 11. Rx to Tx Turnaround | 31 |
| Figure 12. Receiver Hopping | 32 |
| Figure 13. Transmitter Hopping | 32 |
| Figure 14. Timer1 and Timer2 Mechanism | 36 |
| Figure 15. Sequencer State Machine | 38 |
| Figure 16. SX1236 Data Processing Conceptual View | 39 |
| Figure 17. FIFO and Shift Register (SR) | 40 |
| Figure 18. FifoLevel IRQ Source Behavior | 41 |
| Figure 19. Sync Word Recognition | 42 |
| Figure 20. Continuous Mode Conceptual View | 44 |
| Figure 21. Tx Processing in Continuous Mode | 44 |
| Figure 22. Rx Processing in Continuous Mode | 45 |
| Figure 23. Packet Mode Conceptual View | 46 |
| Figure 24. Fixed Length Packet Format | 47 |
| Figure 25. Variable Length Packet Format | 48 |
| Figure 26. Unlimited Length Packet Format | 48 |
| Figure 27. Manchester Encoding/Decoding | 52 |
| Figure 28. Data Whitening Polynomial | 53 |
| Figure 29. SPI Timing Diagram (single access) | 54 |
| Figure 30. TCXO Connection | 55 |
| Figure 31. RF Front-end Architecture Shows the Internal PA Configuration. | 57 |
| Figure 32. Temperature Sensor Response | 62 |
| Figure 33. POR Timing Diagram | 80 |
| Figure 34. Manual Reset Timing Diagram | 81 |
| Figure 35. Listen Mode: Principle | 81 |
| Figure 36. Listen Mode with No Preamble Received | 82 |
| Figure 37. Listen Mode with Preamble Received | 82 |
| Figure 38. Wake On PreambleDetect State Machine | 83 |
| Figure 39. Listen Mode with no SyncAddress Detected | 84 |

Table of contents

| Section | Page |
|---|-------------|
| Figure 40. Listen Mode with Preamble Received and no SyncAddress | 84 |
| Figure 41. Listen Mode with Preamble Received & Valid SyncAddress | 85 |
| Figure 42. Wake On SyncAddress State Machine | 85 |
| Figure 43. Beacon Mode Timing Diagram | 87 |
| Figure 44. Beacon Mode State Machine | 87 |
| Figure 45. Example CRC Code | 89 |
| Figure 46. Example Temperature Reading | 90 |
| Figure 47. Example Temperature Reading (continued) | 91 |
| Figure 48. Package Outline Drawing | 92 |
| Figure 49. Recommended Land Pattern | 93 |
| Figure 50. Tape and Reel Information | 94 |

1. General Description

The SX1236 is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. The SX1236's advanced feature set includes a state-of-the-art packet engine and top level sequencer. In conjunction with a 64 byte FIFO, these automate the entire process of packet transmission, reception and acknowledgment without incurring the consumption penalty common to many transceivers that feature an on-chip MCU. Being easily configurable, it greatly simplifies system design and reduces external MCU workload to an absolute minimum. The high level of integration reduces the external BOM to passive decoupling and impedance matching components. It is intended for use as a high performance, low-cost FSK and OOK RF transceiver for robust, frequency-agile, half-duplex, bi-directional RF links. Where stable and constant RF performance is required over the full operating range of the device down to 1.8V the receiver and PA are fully regulated. For transmit intensive applications - a high efficiency PA can be selected to optimize the current consumption.

The SX1236 is intended for applications requiring high sensitivity and low receive current. Coupling the digital state machine with an RF front end capable of delivering a link budget of 143dB (-123dBm sensitivity in conjunction with +20dBm Pout). The SX1236 complies with both ETSI and FCC regulatory requirements and is available in a 6 x 6 mm QFN 28 lead package. The low-IF architecture of the SX1236 is well suited for low modulation index and narrow band operation.

1.1. Simplified Block Diagram

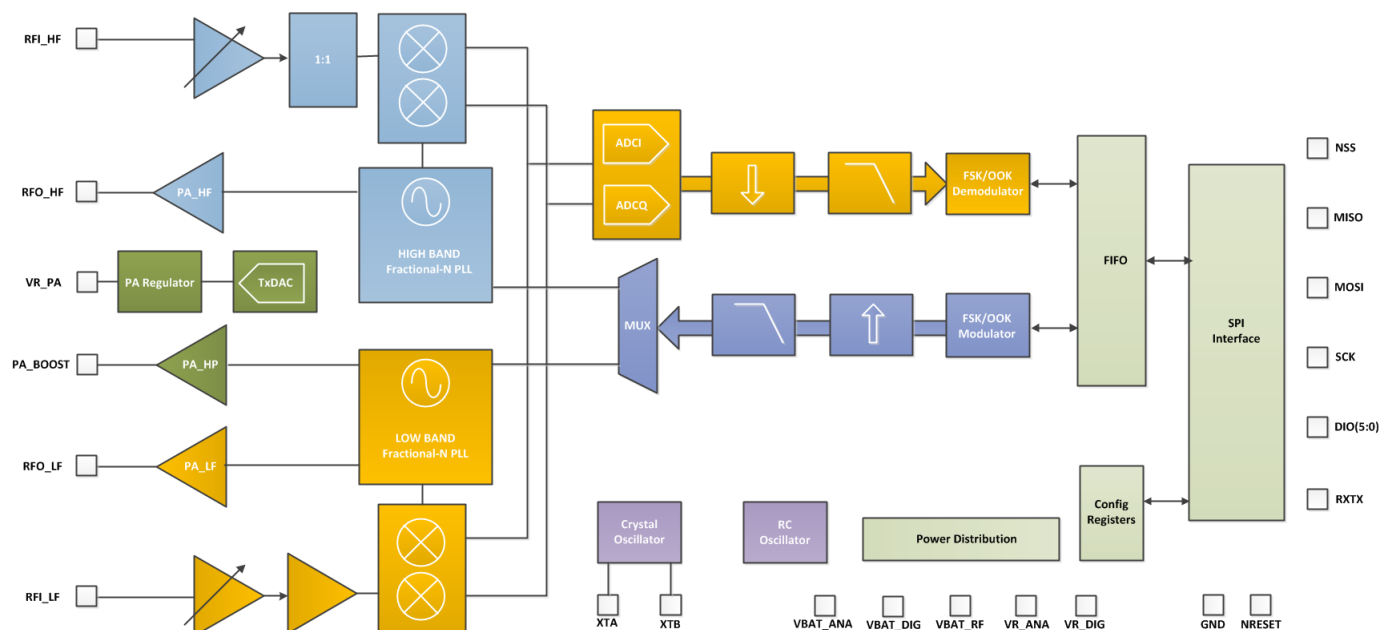


Figure 1. Block Diagram

1.2. Pin Diagram

The following diagram shows the pin arrangement of the QFN package, top view.

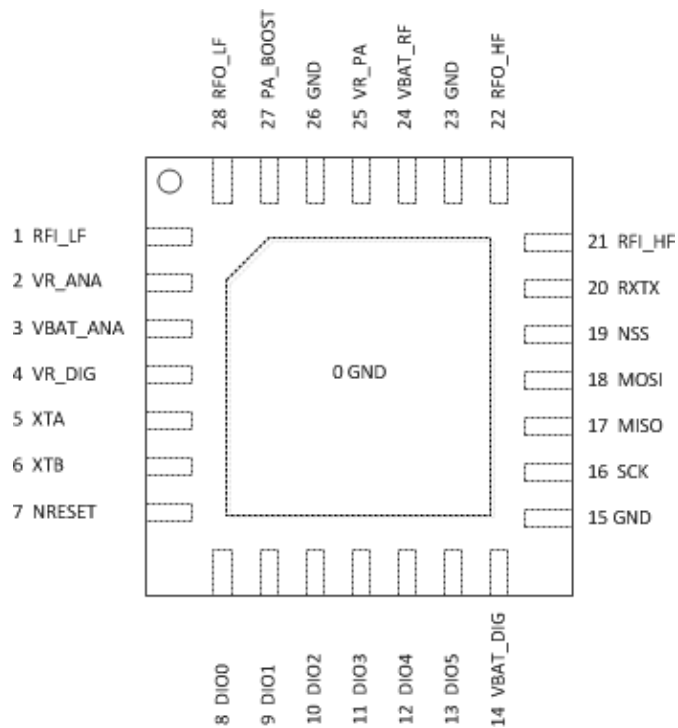


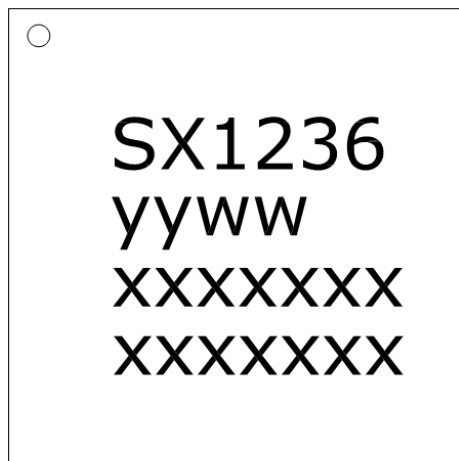
Figure 2. Pin Diagram

1.3. Pin Description

Table 43 Pin Description

| Number | Name | Type | Description |
|--------|-----------|------|--|
| 0 | GROUND | - | Exposed ground pad. |
| 1 | RFI_LF | I | RF input for bands 2&3 |
| 2 | VR_ANA | - | Regulated supply voltage for analogue circuitry |
| 3 | VBAT_ANA | - | Supply voltage for analogue circuitry |
| 4 | VR_DIG | - | Regulated supply voltage for digital blocks |
| 5 | XTA | I/O | XTAL connection or TCXO input |
| 6 | XTB | I/O | XTAL connection. |
| 7 | NRESET | I/O | Reset trigger input. |
| 8 | DIO0 | I/O | Digital I/O, software configured. |
| 9 | DIO1/DCLK | I/O | Digital I/O, software configured. |
| 10 | DIO2/DATA | I/O | Digital I/O, software configured. |
| 11 | DIO3 | I/O | Digital I/O, software configured. |
| 12 | DIO4 | I/O | Digital I/O, software configured. |
| 13 | DIO5 | I/O | Digital I/O, software configured. |
| 14 | VBAT_DIG | - | Supply voltage for digital blocks |
| 15 | GND | - | Ground |
| 16 | SCK | I | SPI Clock input |
| 17 | MISO | O | SPI Data output |
| 18 | MOSI | I | SPI Data input |
| 19 | NSS | I | SPI Chip select input |
| 20 | RXTX | O | Rx/Tx switch control: high in Tx |
| 21 | RFI_HF | I | RF input for band 1 |
| 22 | RFO_HF | O | RF output for band 1 |
| 23 | GND | - | Ground |
| 24 | VBAT_RF | - | Supply voltage for RF blocks |
| 25 | VR_PA | - | Regulated supply for the PA |
| 26 | GND | - | Ground |
| 27 | PA_BOOST | O | Optional high-power PA output, all frequency bands |
| 28 | RFO_LF | O | RF output for bands 2&3 |

1.4. Package Marking



| TOP MARK | |
|-----------|------|
| CHAR | ROWS |
| 7/7/7/7/7 | 5 |

Marking for the 6 x 6 mm MLPQ 28ld Lead package:

nnnnnn = Part Number (Example: SX1236)
 yyww = Date Code (Example: 1352)
 xxxxxx = Semtech Lot No. (Example: EA90101)
 xxxxxx 0101-10)

Figure 3. Marking Diagram

2. Electrical Characteristics

2.1. ESD Notice

The SX1236 is a high performance radio frequency device. It satisfies:

- ◆ Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model) on all pins.
- ◆ Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins



It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 44 Absolute Maximum Ratings

| Symbol | Description | Min | Max | Unit |
|--------|----------------------|------|------|------|
| VDDmr | Supply Voltage | -0.5 | 3.9 | V |
| Tmr | Temperature | -55 | +115 | ° C |
| Tj | Junction temperature | - | +125 | ° C |
| Pmr | RF Input Level | - | +10 | dBm |

Note Specific ratings apply to +20 dBm operation (see Section 5.4.3).

2.3. Operating Range

Table 1 Operating Range

| Symbol | Description | Min | Max | Unit |
|--------|-----------------------------------|-----|-----|------|
| VDDop | Supply voltage | 1.8 | 3.7 | V |
| Top | Operational temperature range | -40 | +85 | °C |
| Clop | Load capacitance on digital ports | - | 25 | pF |
| ML | RF Input Level | - | +10 | dBm |

Note A specific supply voltage range applies to +20 dBm operation (see Section 5.4.3).

2.4. Thermal Properties

Table 2 Thermal Properties

| Symbol | Description | Min | Typ | Max | Unit |
|----------|--|-----|--------|-----|------|
| THETA_JA | Package θ_{ja} (Junction to ambient) | - | 22.185 | - | °C/W |
| THETA_JC | Package θ_{jc} (Junction to case ground paddle) | - | 0.757 | - | °C/W |

2.5. Chip Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VDD=3.3 V, temperature = 25 °C, FXOSC = 32 MHz, F_{RF} = 169/434/868/915 MHz (see specific indication), Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, shared Rx and Tx path matching, unless otherwise specified.

Note Specification whose symbol is appended with “_LF” corresponds to the performance in Band 2 and/or Band 3, as described in section 5.3.3. “_HF” refers to the upper Band 1

2.5.1. Power Consumption

Table 3 Power Consumption Specification

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---------|---|--|------------------|-----------------------|------------------|----------------------|
| IDDSL | Supply current in Sleep mode | | - | 0.2 | 1 | uA |
| IDDIDLE | Supply current in Idle mode | RC oscillator enabled | - | 1.5 | - | uA |
| IDDST | Supply current in Standby mode | Crystal oscillator enabled | - | 1.6 | 1.8 | mA |
| IDDFS | Supply current in Synthesizer mode | FSRx | - | 5.8 | - | mA |
| IDDR | Supply current in Receive mode | LnaBoost Off, band 1 LnaBoost On, band 1 Bands 2&3 | - - - | 10.8 11.5 12.0 | - - - | mA |
| IDDT | Supply current in Transmit mode with impedance matching | RFOP = +20 dBm, on PA_BOOST RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFO_LF/HF pin RFOP = + 7 dBm, on RFO_LF/HF pin | - - - - | 120 87 29 20 | - - - - | mA mA mA mA |

2.5.2. Frequency Synthesis

Table 4 Frequency Synthesizer Specification

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|--------|--|--|-------------------|-------------|--------------------|------|
| FR | Synthesizer frequency range | Programmable Band 1 Band 2 Band 3 | 137 410 862 | - - - | 175 525 1020 | MHz |
| FXOSC | Crystal oscillator frequency | | - | 32 | - | MHz |
| TS_OSC | Crystal oscillator wake-up time | | - | 250 | - | us |
| TS_FS | Frequency synthesizer wake-up time to PllLock signal | From Standby mode | - | 60 | - | us |

| | | | | | | |
|--------|--|--|-----|------|--------|------|
| TS_HOP | Frequency synthesizer hop time at most 10 kHz away from the target frequency | 200 kHz step | - | 20 | - | us |
| | | 1 MHz step | - | 20 | - | us |
| | | 5 MHz step | - | 50 | - | us |
| | | 7 MHz step | - | 50 | - | us |
| | | 12 MHz step | - | 50 | - | us |
| | | 20 MHz step | - | 50 | - | us |
| | | 25 MHz step | - | 50 | - | us |
| FSTEP | Frequency synthesizer step | $FSTEP = FXOSC/2^{19}$ | - | 61.0 | - | Hz |
| FRC | RC Oscillator frequency | After calibration | - | 62.5 | - | kHz |
| BRF | Bit rate, FSK | Programmable values (1) | 1.2 | - | 300 | kbps |
| BRA | Bit rate Accuracy, FSK | ABS(wanted BR - available BR) | - | - | 250 | ppm |
| BRO | Bit rate, OOK | Programmable | 1.2 | - | 32.768 | kbps |
| FDA | Frequency deviation, FSK (1) | Programmable $FDA + BRF/2 \leq 250 \text{ kHz}$ | 0.6 | - | 200 | kHz |

Note For Maximum Bit rate the maximum modulation index is 0.5.

2.5.3. FSK/OOK Mode Receiver

All receiver tests are performed with $RxBw = 10$ kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence. Sensitivities are reported for a 0.1% BER (with Bit Synchronizer enabled), unless otherwise specified. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the receiver sensitivity level.

Table 5 FSK/OOK Receiver Specification

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|---|---|--------|--------------|--------|------------|
| RFS_F_LF | Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitivity, highest LNA gain. Bands 2&3 | FDA = 5 kHz, BR = 1.2 kb/s | - | -121 | - | dBm |
| | | FDA = 5 kHz, BR = 4.8 kb/s | - | -117 | - | dBm |
| | | FDA = 40 kHz, BR = 38.4 kb/s* | - | -107 | - | dBm |
| | | FDA = 20 kHz, BR = 38.4 kb/s** | - | -108 | - | dBm |
| | | FDA = 62.5 kHz, BR = 250 kb/s*** | - | -95 | - | dBm |
| | Split RF paths, the RF switch insertion loss is not accounted for. Bands 2&3 | FDA = 5 kHz, BR = 1.2 kb/s | - | -123 | - | dBm |
| | | FDA = 5 kHz, BR = 4.8 kb/s | - | -119 | - | dBm |
| | | FDA = 40 kHz, BR = 38.4 kb/s* | - | -109 | - | dBm |
| | | FDA = 20 kHz, BR = 38.4 kb/s** | - | -110 | - | dBm |
| | | FDA = 62.5 kHz, BR = 250 kb/s*** | - | -97 | - | dBm |
| RFS_F_HF | Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitivity, highest LNA gain. Band 1 | FDA = 5 kHz, BR = 1.2 kb/s | - | -119 | - | dBm |
| | | FDA = 5 kHz, BR = 4.8 kb/s | - | -115 | - | dBm |
| | | FDA = 40 kHz, BR = 38.4 kb/s* | - | -105 | - | dBm |
| | | FDA = 20 kHz, BR = 38.4 kb/s** | - | -105 | - | dBm |
| | | FDA = 62.5 kHz, BR = 250 kb/s*** | - | -92 | - | dBm |
| | Split RF paths, <i>LnaBoost</i> is turned on, the RF switch insertion loss is not accounted for. Band 1 | FDA = 5 kHz, BR = 1.2 kb/s | - | -123 | - | dBm |
| | | FDA = 5 kHz, BR = 4.8 kb/s | - | -119 | - | dBm |
| | | FDA = 40 kHz, BR = 38.4 kb/s* | - | -109 | - | dBm |
| | | FDA = 20 kHz, BR = 38.4 kb/s** | - | -109 | - | dBm |
| | | FDA = 62.5 kHz, BR = 250 kb/s*** | - | -96 | - | dBm |
| RFS_O | OOK sensitivity, highest LNA gain shared Rx, Tx paths | BR = 4.8 kb/s BR = 32 kb/s | - - | -117 -108 | - - | dBm dBm |
| CCR | Co-Channel Rejection, FSK | | - | -9 | - | dB |
| ACR | Adjacent Channel Rejection | FDA = 5 kHz, BR=4.8kb/s Offset = +/- 25 kHz or +/- 50kHz | | | | |
| | | Band 3 | - | 60 | - | dB |
| | | Band 2 | - | 56 | - | dB |
| | | Band 1 | - | 50 | - | dB |
| BI_HF | Blocking Immunity, Band 1 | Offset = +/- 1 MHz | - | 71 | - | dB |
| | | Offset = +/- 2 MHz | - | 76 | - | dB |
| | | Offset = +/- 10 MHz | - | 84 | - | dB |
| BI_LF | Blocking Immunity, Bands 2&3 | Offset = +/- 1 MHz | - | 71 | - | dB |
| | | Offset = +/- 2 MHz | - | 72 | - | dB |
| | | Offset = +/- 10 MHz | - | 78 | - | dB |

| | | | | | | |
|---------|---|---|------------|------------|-----------|------------|
| IIP2 | 2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO | Highest LNA gain | - | +55 | - | dBm |
| IIP3_HF | 3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO | Band 1 Highest LNA gain G1 LNA gain G2, 5dB sensitivity hit | - - | -11 -6 | - - | dBm dBm |
| IIP3_LF | 3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO | Band 2 Highest LNA gain G1 LNA gain G2, 2.5dB sensitivity hit | - - | -22 -15 | - - | dBm dBm |
| | | Band 3 Highest LNA gain G1 LNA gain G2, 2.5dB sensitivity hit | - - | -15 -11 | - - | dBm dBm |
| BW_SSB | Single Side channel filter BW | Programmable | 2.7 | - | 250 | kHz |
| IMR | Image Rejection | Wanted signal 3dB over sensitivity BER=0.1% | - | 50 | - | dB |
| IMA | Image Attenuation | | - | 57 | - | dB |
| DR_RSSI | RSSI Dynamic Range | AGC enabled | Min Max | - - | -127 0 | dBm dBm |

* $RxBw = 83 \text{ kHz}$ (Single Side Bandwidth)

** $RxBw = 50 \text{ kHz}$ (Single Side Bandwidth)

*** $RxBw = 250 \text{ kHz}$ (Single Side Bandwidth)

2.5.4. FSK/OOK Mode Transmitter

Table 6 Transmitter Specification

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---------------------|--|--|--------|-----------|--------|------------|
| RF_OP | RF output power in 50 ohms on RFO pin (High efficiency PA). | Programmable with steps Max Min | - - | +14 -1 | - - | dBm dBm |
| ΔRF_OP_V | RF output power stability on RFO pin versus voltage supply. | VDD = 2.5 V to 3.3 V VDD = 1.8 V to 3.7 V | - - | 3 8 | - - | dB dB |
| RF_OPH | RF output power in 50 ohms, on PA_BOOST pin (Regulated PA). | Programmable with 1dB steps Max Min | - - | +17 +2 | - - | dBm dBm |
| RF_OPH_MAX | Max RF output power, on PA_BOOST pin | High power mode | - | +20 | - | dBm |
| ΔRF_OPH_V | RF output power stability on PA_BOOST pin versus voltage supply. | VDD = 2.4 V to 3.7 V | - | +/-1 | - | dB |
| ΔRF_T | RF output power stability versus temperature on PA_BOOST pin. | From T = -40 °C to +85 °C | - | +/-1 | - | dB |

| | | | | | | |
|-------|--|---|---|------|-----|------------|
| PHN | Transmitter Phase Noise | 169 MHz, Band 3 | | | | |
| | | 10kHz Offset | - | -118 | - | dBc/ Hz |
| | | 50kHz Offset | - | -118 | - | |
| | | 400kHz Offset | - | -128 | - | |
| | | 1MHz Offset | - | -134 | - | |
| | | 433 MHz, Band 2 | | | | |
| | | 10kHz Offset | - | -110 | - | dBc/ Hz |
| | | 50kHz Offset | - | -110 | - | |
| | | 400kHz Offset | - | -122 | - | |
| | | 1MHz Offset | - | -129 | - | |
| | | 868/915 MHz, Band 1 | | | | |
| | | 10kHz Offset | - | -103 | - | dBc/ Hz |
| | | 50kHz Offset | - | -103 | - | |
| | | 400kHz Offset | - | -115 | - | |
| | | 1MHz Offset | - | -122 | - | |
| ACP | Transmitter adjacent channel power (measured at 25 kHz offset) | BT=1. Measurement conditions as defined by EN 300 220-1 V2.3.1 | - | - | -37 | dBm |
| TS_TR | Transmitter wake up time, to the first rising edge of DCLK | Frequency Synthesizer enabled, <i>PaR-amp</i> = 10us, BR = 4.8 kb/s | - | 120 | - | us |

2.5.5. Digital Specification

Conditions: Temp = 25° C, VDD = 3.3 V, FXOSC = 32 MHz, unless otherwise specified.

Table 7 Digital Specification

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---------------------|------------------------------------|--|-----|-----|-----|------|
| V _{IH} | Digital input level high | | 0.8 | - | - | VDD |
| V _{IL} | Digital input level low | | - | - | 0.2 | VDD |
| V _{OH} | Digital output level high | I _{max} = 1 mA | 0.9 | - | - | VDD |
| V _{OL} | Digital output level low | I _{max} = -1 mA | - | - | 0.1 | VDD |
| F _{SCK} | SCK frequency | | - | - | 10 | MHz |
| t _{ch} | SCK high time | | 50 | - | - | ns |
| t _{cl} | SCK low time | | 50 | - | - | ns |
| t _{rise} | SCK rise time | | - | 5 | - | ns |
| t _{fall} | SCK fall time | | - | 5 | - | ns |
| t _{setup} | MOSI setup time | From MOSI change to SCK rising edge. | 30 | - | - | ns |
| t _{hold} | MOSI hold time | From SCK rising edge to MOSI change. | 20 | - | - | ns |
| t _{nsetup} | NSS setup time | From NSS falling edge to SCK rising edge. | 30 | - | - | ns |
| t _{nhold} | NSS hold time | From SCK falling edge to NSS rising edge, normal mode. | 100 | - | - | ns |
| t _{nhigh} | NSS high time between SPI accesses | | 20 | - | - | ns |
| T_DATA | DATA hold and setup time | | 250 | - | - | ns |

3. SX1236 Features

This section gives a high-level overview of the functionality of the SX1236 low-power, highly integrated transceiver. The following figure shows a simplified block diagram of the SX1236.

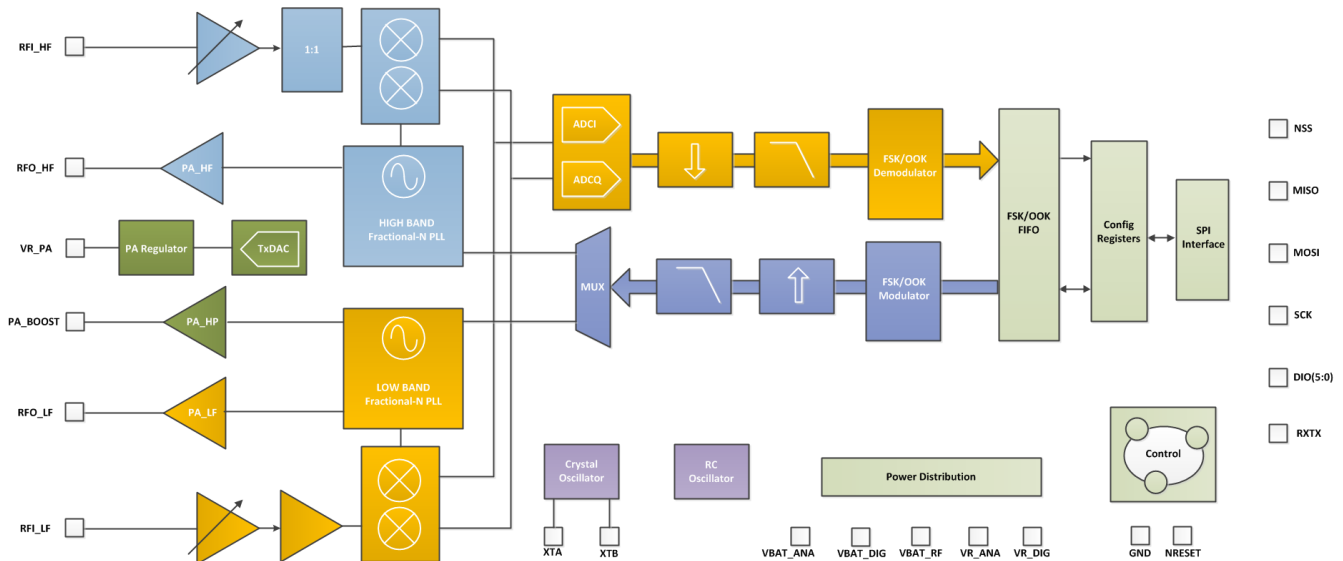


Figure 4. SX1236 Block Schematic Diagram

SX1236 is a half-duplex, low-IF transceiver. Here the received RF signal is first amplified by the LNA. The LNA inputs are single ended to minimize the external BoM and for ease of design. Following the LNA inputs, the conversion to differential is made to improve the second order linearity and harmonic rejection. The signal is then down-converted to in-phase and quadrature (I&Q) components at the intermediate frequency (IF) by the mixer stage. A pair of sigma delta ADCs then perform data conversion, with all subsequent signal processing and demodulation performed in the digital domain. The digital state machine also controls the automatic frequency correction (AFC), received signal strength indicator (RSSI) and automatic gain control (AGC). It also features the higher-level packet and protocol level functionality of the top level sequencer (TLS).

The frequency synthesizers generate the local oscillator (LO) frequency for both receiver and transmitter, one covering the lower UHF bands (up to 525 MHz), and the other one covering the upper UHF bands (from 860 MHz). The PLLs are optimized for user-transparent low lock time and fast auto-calibrating operation. In transmission, frequency modulation is performed digitally within the PLL bandwidth. The PLL also features optional pre-filtering of the bit stream to improve spectral purity.

SX1236 features three distinct RF power amplifiers. Two of those, connected to RFO_LF and RFO_HF, can deliver up to +14 dBm, are unregulated for high power efficiency and can be connected directly to their respective RF receiver inputs via a pair of passive components to form a single antenna port high efficiency transceiver. The third PA, connected to the PA_BOOST pin, can deliver up to +20 dBm via a dedicated matching network. Unlike the high efficiency PAs, this high-stability PA covers all frequency bands that the frequency synthesizer addresses.

SX1236 also include two timing references, an RC oscillator and a 32 MHz crystal oscillator.

All major parameters of the RF front end and digital state machine are fully configurable via an SPI interface which gives access to SX1236's configuration registers. This includes a mode auto sequencer that oversees the transition and calibration of the SX1236 between intermediate modes of operation in the fastest time possible.

The SX1236 supports standard modulation techniques including OOK, FSK, GFSK, MSK and GMSK. The SX1236 is especially suited to narrow band communication thanks the low-IF architecture employed and the built-in AFC functionality. For full information on the FSK/OOK modem please consult Section 4.1 of this document.

4. SX1236 Digital Electronics

4.1. FSK/OOK Modem

4.1.1. Bit Rate Setting

The bitrate setting is referenced to the crystal oscillator and provides a precise means of setting the bit rate (or equivalently chip) rate of the radio. In continuous transmit mode (Section 4.1.12.) the data stream to be transmitted can be inputted directly to the modulator via pin 9 (DIO2/DATA) in an asynchronous manner, unless Gaussian filtering is used, in which case the DCLK signal on pin 10 (DIO1/DCLK) is used to synchronize the data stream. See section 4.1.2.3 for details on the Gaussian filter.

In Packet mode or in Continuous mode with Gaussian filtering enabled, the Bit Rate (BR) is controlled by bits *Bitrate* in *RegBitrateMsb* and *RegBitrateLsb*

$$BitRate = \frac{FXOSC}{BitRate(15:0) + \frac{BitrateFrac}{16}}$$

*Note: BitrateFrac bits have **no effect** (i.e may be considered equal to 0) in OOK modulation mode.*

The quantity *BitrateFrac* is hence designed to allow very high precision (max. 250 ppm programing resolution) for any bitrate in the programmable range. Table 8 below shows a range of standard bitrates and the accuracy to within which they may be reached.

Table 8 Bit Rate Examples

| Type | BitRate (15:8) | BitRate (7:0) | (G)FSK (G)MSK | OOK | Actual BR (b/s) |
|---|-------------------|------------------|------------------|-----------|--------------------|
| Classical modem baud rates (multiples of 1.2 kbps) | 0x68 | 0x2B | 1.2 kbps | 1.2 kbps | 1200.015 |
| | 0x34 | 0x15 | 2.4 kbps | 2.4 kbps | 2400.060 |
| | 0x1A | 0x0B | 4.8 kbps | 4.8 kbps | 4799.760 |
| | 0x0D | 0x05 | 9.6 kbps | 9.6 kbps | 9600.960 |
| | 0x06 | 0x83 | 19.2 kbps | 19.2 kbps | 19196.16 |
| | 0x03 | 0x41 | 38.4 kbps | | 38415.36 |
| | 0x01 | 0xA1 | 76.8 kbps | | 76738.60 |
| | 0x00 | 0xD0 | 153.6 kbps | | 153846.1 |
| Classical modem baud rates (multiples of 0.9 kbps) | 0x02 | 0x2C | 57.6 kbps | | 57553.95 |
| | 0x01 | 0x16 | 115.2 kbps | | 115107.9 |

| Type | BitRate (15:8) | BitRate (7:0) | (G)FSK (G)MSK | OOK | Actual BR (b/s) |
|---|-------------------|------------------|------------------|-------------|--------------------|
| Round bit rates (multiples of 12.5, 25 and 50 kbps) | 0x0A | 0x00 | 12.5 kbps | 12.5 kbps | 12500.00 |
| | 0x05 | 0x00 | 25 kbps | 25 kbps | 25000.00 |
| | 0x80 | 0x00 | 50 kbps | | 50000.00 |
| | 0x01 | 0x40 | 100 kbps | | 100000.0 |
| | 0x00 | 0xD5 | 150 kbps | | 150234.7 |
| | 0x00 | 0xA0 | 200 kbps | | 200000.0 |
| | 0x00 | 0x80 | 250 kbps | | 250000.0 |
| | 0x00 | 0x6B | 300 kbps | | 299065.4 |
| Watch Xtal frequency | 0x03 | 0xD1 | 32.768 kbps | 32.768 kbps | 32753.32 |

4.1.2. FSK/OOK Transmission

4.1.2.1. FSK Modulation

FSK modulation is performed inside the PLL bandwidth, by changing the fractional divider ratio in the feedback loop of the PLL. The high resolution of the sigma-delta modulator, allows for very narrow frequency deviation. The frequency deviation F_{DEV} is given by:

$$F_{DEV} = F_{STEP} \times F_{dev}(13,0)$$

To ensure correct modulation, the following limit applies:

$$F_{DEV} + \frac{BR}{2} \leq (250)kHz$$

Note No constraint applies to the modulation index of the transmitter, but the frequency deviation must be set between 600 Hz and 200 kHz.

4.1.2.2. OOK Modulation

OOK modulation is applied by switching on and off the power amplifier. Digital control and ramping are available to improve the transient power response of the OOK transmitter.

4.1.2.3. Modulation Shaping

Modulation shaping can be applied in both OOK and FSK modulation modes, to improve the narrow band response of the transmitter. Both shaping features are controlled with *PaRamp* bits in *RegPaRamp*.

- ◆ In FSK mode, a Gaussian filter with $BT = 0.5$ or 1 is used to filter the modulation stream, at the input of the sigma-delta modulator. If the Gaussian filter is enabled when the SX1236 is in Continuous mode, DCLK signal on pin 10 (DIO1/ DCLK) will trigger an interrupt on the uC each time a new bit has to be transmitted. Please refer to section 4.1.12.2 for details.
- ◆ When OOK modulation is used, the PA bias voltages are ramped up and down smoothly when the PA is turned on and off, to reduce spectral splatter.

Note The transmitter must be restarted if the *ModulationShaping* setting is changed, in order to recalibrate the built-in filter.

4.1.3. FSK/OOK Reception

4.1.3.1. FSK Demodulator

The FSK demodulator of the SX1236 is designed to demodulate FSK, GFSK, MSK and GMSK modulated signals. It is most efficient when the modulation index of the signal is greater than 0.5 and below 10:

$$0.5 \leq \beta = \frac{2 \times F_{DEV}}{BR} \leq 10$$

The output of the FSK demodulator can be fed to the Bit Synchronizer to provide the companion processor with a synchronous data stream in Continuous mode.

4.1.3.2. OOK Demodulator

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, configured through bits *OokThreshType* in *RegOokPeak*.

The recommended mode of operation is the “Peak” threshold mode, illustrated in Figure 5:

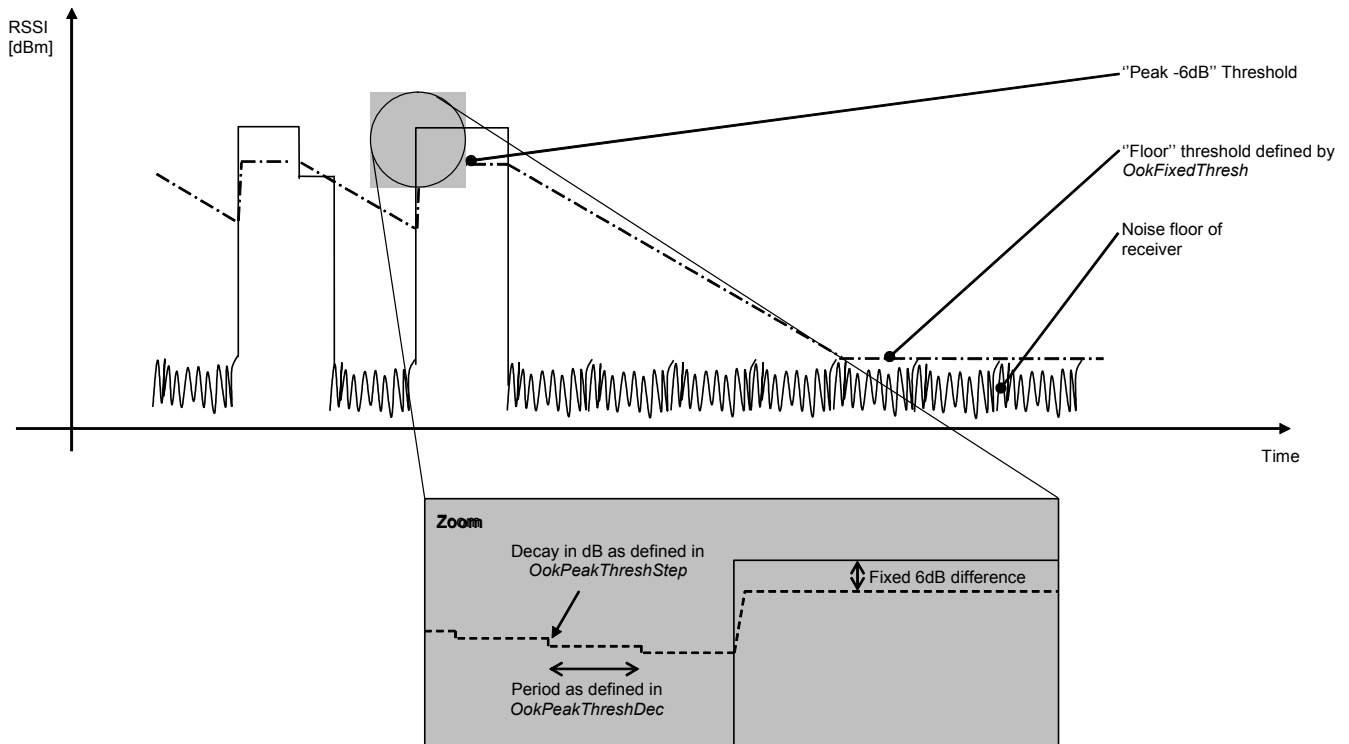


Figure 5. OOK Peak Demodulator Description

In peak threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6dB. In the absence of an input signal, or during the reception of a logical ‘0’, the acquired peak value is decremented by one *OokPeakThreshStep* every *OokPeakThreshDec* period.

When the RSSI output is null for a long time (for instance after a long string of “0” received, or if no transmitter is present), the peak threshold level will continue falling until it reaches the “Floor Threshold”, programmed in *OokFixedThresh*.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters should be optimized accordingly.

Optimizing the Floor Threshold

OokFixedThresh determines the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (i.e. those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

- ◆ The noise figure of the receiver
- ◆ The gain of the receive chain from antenna to base band
- ◆ The matching - including SAW filter if any
- ◆ The bandwidth of the channel filters

It is therefore important to note that the setting of *OokFixedThresh* will be application dependant. The following procedure is recommended to optimize *OokFixedThresh*.

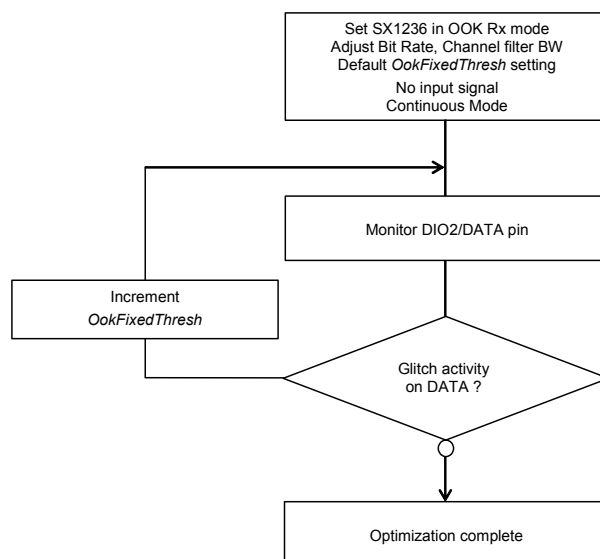


Figure 6. Floor Threshold Optimization

The new floor threshold value found during this test should be used for OOK reception with those receiver settings.

Optimizing OOK Demodulator for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated, the following OOK demodulator parameters *OokPeakThreshStep* and *OokPeakThreshDec* can be optimized as described below for a given number of threshold decrements per bit. Refer to *RegOokPeak* to access those settings.

Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK threshold mode, the user can alternatively select two other types of threshold detectors:

- ◆ Fixed Threshold: The value is selected through *OokFixedThresh*
- ◆ Average Threshold: Data supplied by the RSSI block is averaged, and this operation mode should only be used with DC-free encoded data.

4.1.3.3. Bit Synchronizer

The bit synchronizer provides a clean and synchronized digital output based upon timing recovery information gleaned from the received data edge transitions. Its output is made available on pin DIO1/DCLK in Continuous mode and can be disabled through register settings. However, for optimum receiver performance, especially in Continuous receive mode, its use is strongly advised.

The Bit Synchronizer is automatically activated in Packet mode. Its bit rate is controlled by *BitRateMsb* and *BitRateLsb* in *RegBitrate*.

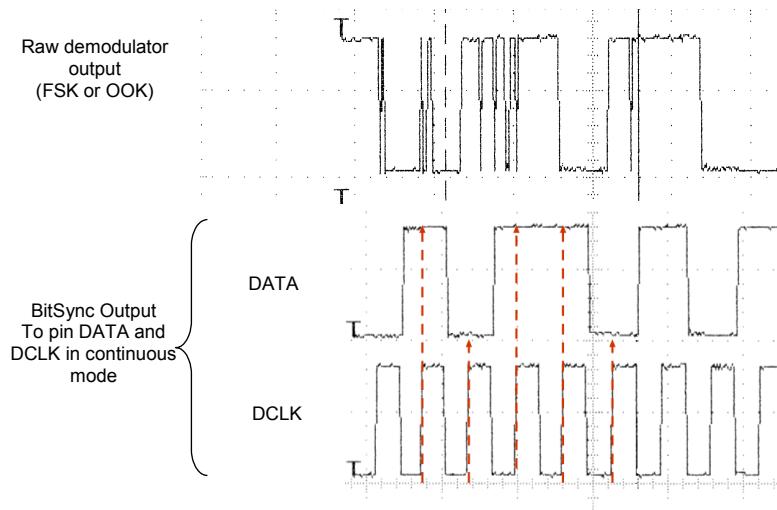


Figure 7. Bit Synchronizer Description

To ensure correct operation of the Bit Synchronizer, the following conditions have to be satisfied:

- ◆ A preamble (0x55 or 0xAA) of at least 12 bits is required for synchronization, the longer the synchronization phase is the better the ensuing packet detection rate will be
- ◆ The subsequent payload bit stream must have at least one edge transition (either rising or falling) every 16 bits during data transmission
- ◆ The absolute error between transmitted and received bit rate must not exceed 6.5%

4.1.3.4. Frequency Error Indicator

This frequency error indicator measures the frequency error between the programmed RF center frequency and the carrier frequency of the modulated input signal to the receiver. When the FEI is performed, the frequency error is measured and the signed result is loaded in *FeiValue* in *RegFei*, in 2's complement format. The time required for an FEI evaluation is 4 bit periods.

To ensure correct operation of the FEI:

- ◆ The measurement must be launched during the reception of preamble.
- ◆ The sum of the frequency offset and the 20 dB signal bandwidth must be lower than the base band filter bandwidth, i.e. the whole modulated spectrum must be received.

The 20 dB bandwidth of the signal can be evaluated as follows (double-side bandwidth):

$$BW_{20dB} = 2 \times \left(F_{DEV} + \frac{BR}{2} \right)$$

The frequency error, in Hz, can be calculated with the following formula:

$$FEI = F_{STEP} \times FeiValue$$

The FEI is enabled automatically upon the transition to receive mode and automatically updated every 4 bits.

4.1.3.5. AFC

The AFC is based on the FEI measurement, therefore the same input signal and receiver setting conditions apply. When the AFC procedure is performed the *AfcValue* is directly subtracted from the register that defines the frequency of operation of the chip, F_{RF} . The AFC is executed every time the receiver is enabled, if *AfcAutoOn* = 1.

When the AFC is enabled (*AfcAutoOn* = 1), the user has the option to:

- ◆ Clear the former AFC correction value, if *AfcAutoClearOn* = 1, allowing the next frequency correction to be performed from the initial center frequency.
- ◆ Start the AFC evaluation from the previously corrected frequency. This may be useful in systems in which the center frequency experiences cumulative drift - such as the ageing of a crystal reference.

The SX1236 offers an alternate receiver bandwidth setting during the AFC phase allowing the accommodation of larger frequency errors. The setting *RegAfcBw* sets the receive bandwidth during the AFC process. In a typical receiver application, once the AFC is performed, the radio will revert to the receiver communication or channel bandwidth (*RegRxBw*) for the ensuing communication phase.

Note that the FEI measurement is valid only during the reception of preamble. The provision of the *PreambleDetect* flag can hence be used to detect this condition and allow a reliable AFC or FEI operation to be triggered. This process can be performed automatically by using the appropriate options in *StartDemodOnPreamble* found in the *RegRxConfig* register.

A detailed description of the receiver setup to enable the AFC is provided in section 4.1.6.

4.1.3.6. Preamble Detector

The Preamble Detector indicates the reception of a carrier modulated with a 0101...sequence. It is insensitive to the frequency offset, as long as the receiver bandwidth is large enough. The size of detection can be programmed from 1 to 3 bytes with *PreambleDetectorSize* in *RegPreambleDetect* as defined in the next table.

Table 9 *Preamble Detector Settings*

| <i>PreambleDetectorSize</i> | # of Bytes |
|-----------------------------|-----------------|
| 00 | 1 |
| 01 | 2 (recommended) |
| 10 | 3 |
| 11 | reserved |

For normal operation, *PreambleDetectTol* should be set to be set to 10 (0x0A), with a qualifying preamble size of 2 bytes.

The *PreambleDetect* interrupt (either in *RegIrqFlags1* or mapped to a specific DIO) then goes high every time a valid preamble is detected, assuming *PreambleDetectorOn*=1.

The preamble detector can also be used as a gate to ensure that AFC and AGC are performed on valid preamble. See section 4.1.6. for details.

4.1.3.7. Image Rejection Mixer

The SX1236 employs an image rejection mixer (IRM) which, uncalibrated, 35 dB image rejection. A low phase noise PLL is used to perform calibration of the receiver chain. This increases the typical image rejection to 48 dB.

4.1.3.8. Image and RSSI Calibration

An automatic calibration process is used to calibrate the phase and gain of both I and Q receive paths. This calibration allows enhanced image frequency rejection and improves the RSSI precision. This Calibration process is launched under the following circumstances:

- ◆ Automatically at Power On Reset or after a Manual Reset of the chip (refer to section 7.2). For applications where the temperature remains stable, or if the Image Rejection is not a major concern, this single calibration will suffice.
- ◆ Automatically when a pre-defined temperature change is observed.
- ◆ Upon User request, by setting bit *ImageCalStart* in *RegImageCal*, when the device is in Standby mode.

A selectable temperature change, set with *TempThreshold* (5, 10, 15 or 20°C), is detected and reported in *TempChange*, if the temperature monitoring is turned On with *TempMonitorOff*=0.

This interrupt flag can be used by the application to launch a new image calibration at a convenient time if *AutoImageCalOn*=0, or immediately when this temperature variation is detected, if *AutoImageCalOn*=1.

The calibration process takes approximately 10ms.

4.1.3.9. Timeout Function

The SX1236 includes a Timeout function, which allows it to automatically shut-down the receiver after a receive sequence and therefore save energy.

- ◆ Timeout interrupt is generated $TimeoutRxRssi \times 16 \times Tbit$ after switching to Rx mode if the *Rssi* flag does not raise within this time frame ($RssiValue > RssiThreshold$)
- ◆ Timeout interrupt is generated $TimeoutRxPreamble \times 16 \times Tbit$ after switching to Rx mode if the *PreambleDetect* flag does not raise within this time frame
- ◆ Timeout interrupt is generated $TimeoutSignalSync \times 16 \times Tbit$ after switching to Rx mode if the *SyncAddress* flag does not raise within this time frame

This timeout interrupt can be used to warn the companion processor to shut down the receiver and return to a lower power mode. To become active, these timeouts must also be enabled by setting the correct *RxTrigger* parameters in *RegRxConfig*:

Table 10 *RxTrigger Settings to Enable Timeout Interrupts*

| Receiver Triggering Event | RxTrigger (2:0) | Timeout on Rssi | Timeout on Preamble | Timeout on SyncAddress |
|---------------------------------|-----------------|-----------------|---------------------|------------------------|
| None | 000 | Off | Off | Active |
| Rssi Interrupt | 001 | Active | Off | |
| PreambleDetect | 110 | Off | Active | |
| Rssi Interrupt & PreambleDetect | 111 | Active | Active | |

4.1.4. Operating Modes in FSK/OOK Mode

The SX1236 has several working modes, manually programmed in *RegOpMode*. Fully automated mode selection, packet transmission and reception is also possible using the Top Level Sequencer described in Section 4.1.8.

Table 11 *Basic Transceiver Modes*

| Mode | Selected mode | Symbol | Enabled blocks |
|------|---------------------------------------|--------|---|
| 000 | Sleep mode | Sleep | None |
| 001 | Standby mode | Stdby | Top regulator and crystal oscillator |
| 010 | Frequency synthesiser to Tx frequency | FSTx | Frequency synthesizer at Tx frequency (Frf) |
| 011 | Transmit mode | Tx | Frequency synthesizer and transmitter |
| 100 | Frequency synthesiser to Rx frequency | FSRx | Frequency synthesizer at frequency for reception (Frf-IF) |
| 101 | Receive mode | Rx | Frequency synthesizer and receiver |

When switching from a mode to another, the sub-blocks are woken up according to a pre-defined optimized sequence.

4.1.5. Startup Times

The startup time of the transmitter or the receiver is dependent upon which mode the transceiver was in at the beginning. For a complete description, Figure 8 below shows a complete startup process, from the lower power mode “Sleep”.

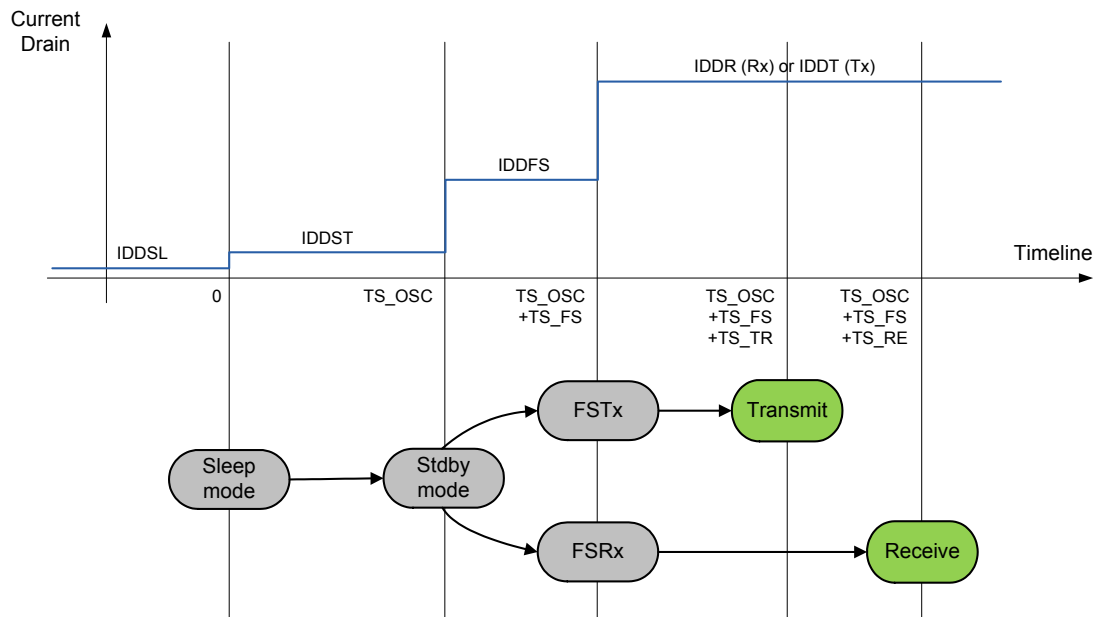


Figure 8. Startup Process

TS_OSC is the startup time of the crystal oscillator which depends on the electrical characteristics of the crystal. TS_FS is the startup time of the PLL including systematic calibration of the VCO.

Typical values of TS_OSC and TS_FS are given in Section 2.5.

4.1.5.1. Transmitter Startup Time

The transmitter startup time, TS_TR, is calculated as follows in FSK mode:

$$TS_TR = 5\mu s + 1.25 \times PaRamp + \frac{1}{2} \times Tbit$$

where *PaRamp* is the ramp-up time programmed in *RegPaRamp* and *Tbit* is the bit time.

In OOK mode, this equation can be simplified to the following:

$$TS_TR = 5\mu s + \frac{1}{2} \times Tbit$$

4.1.5.2. Receiver Startup Time

The receiver startup time, TS_RE, only depends upon the receiver bandwidth effective at the time of startup. When AFC is enabled (*AfcAutoOn*=1), *AfcBw* should be used instead of *RxBw* to extract the receiver startup time:

Table 12 Receiver Startup Time Summary

| <i>RxBw if AfcAutoOn=0 RxBwAfc if AfcAutoOn=1</i> | <i>TS_RE (+/-5%)</i> |
|---|--------------------------|
| 2.6 kHz | 2.33 ms |
| 3.1 kHz | 1.94 ms |
| 3.9 kHz | 1.56 ms |
| 5.2 kHz | 1.18 ms |
| 6.3 kHz | 984 us |
| 7.8 kHz | 791 us |
| 10.4 kHz | 601 us |
| 12.5 kHz | 504 us |
| 15.6 kHz | 407 us |
| 20.8 kHz | 313 us |
| 25.0 kHz | 264 us |
| 31.3 kHz | 215 us |
| 41.7 kHz | 169 us |
| 50.0 kHz | 144 us |
| 62.5 kHz | 119 us |
| 83.3 kHz | 97 us |
| 100.0 kHz | 84 us |
| 125.0 kHz | 71 us |
| 166.7 kHz | 85 us |
| 200.0 kHz | 74 us |
| 250.0 kHz | 63 us |

TS_RE or later after setting the device in Receive mode, any incoming packet will be detected and demodulated by the transceiver.

4.1.5.3. Time to RSSI Evaluation

The first RSSI sample will be available TS_RSSI after the receiver is ready, in other words TS_RE + TS_RSSI after the receiver was requested to turn on.

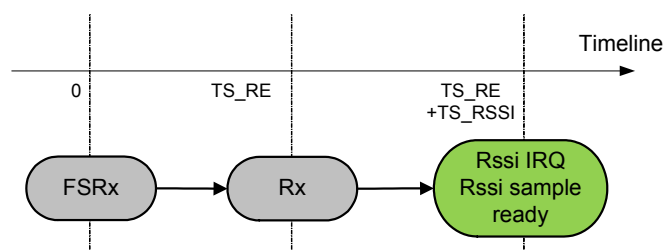


Figure 9. Time to RSSI Sample

TS_RSSI depends on the receiver bandwidth, as well as the *RssiSmoothing* option that was selected. The formula used to calculate TS_RSSI is provided in section 5.5.4.

4.1.5.4. Tx to Rx Turnaround Time

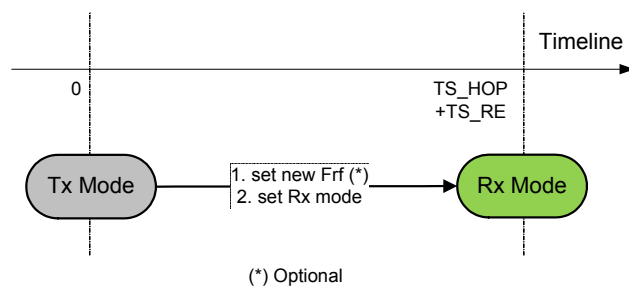


Figure 10. Tx to Rx Turnaround

Note The SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock).

4.1.5.5. Rx to Tx

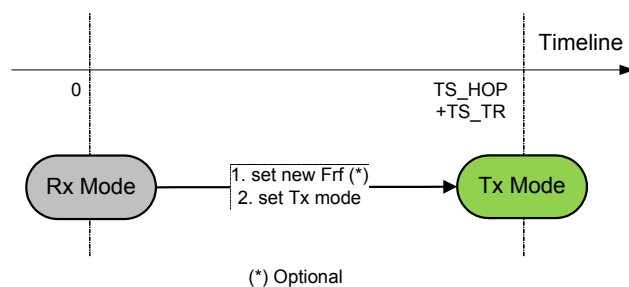


Figure 11. Rx to Tx Turnaround

4.1.5.6. Receiver Hopping, Rx to Rx

Two methods are possible:

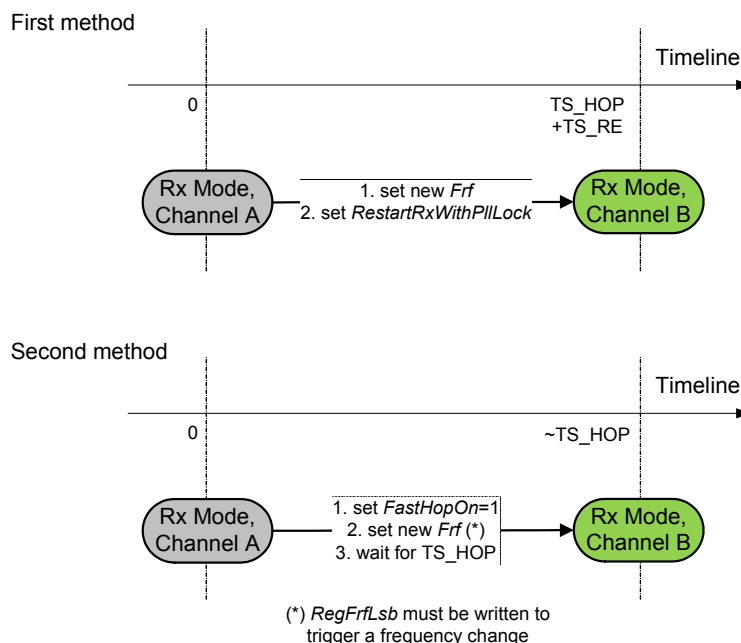


Figure 12. Receiver Hopping

The second method is quicker, and should be used if a very quick RF sniffing mechanism is to be implemented.

4.1.5.7. Tx to Tx

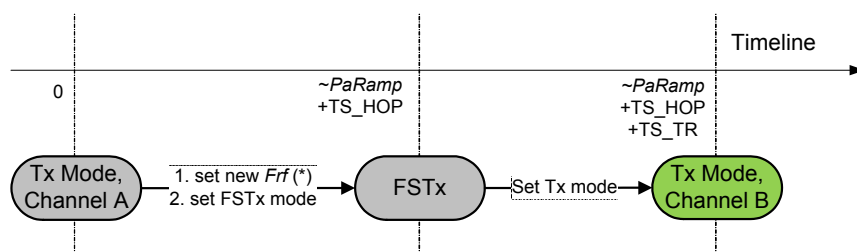


Figure 13. Transmitter Hopping

4.1.6. Receiver Startup Options

The SX1236 receiver can automatically control the gain of the receiving chain (AGC) and adjust the receiver LO frequency (AFC). Those processes are carried out on a packet-by-packet basis. They occur:

- ◆ When the receiver is turned On.
- ◆ When the Receiver is restarted upon user request, through the use of trigger bits *RestartRxWithoutPllLock* or *RestartRxWithPllLock*, in *RegRxConfig*.
- ◆ When the receiver is automatically restarted after the reception of a valid packet, or after a packet collision.

Automatic restart capabilities are detailed in Section 4.1.7.

The receiver startup options available in SX1236 are described in Table 13.

Table 13 Receiver Startup Options

| Triggering Event | Realized Function | AgcAutoOn | AfcAutoOn | RxTrigger (2:0) |
|---------------------------------|-------------------|-----------|-----------|-----------------|
| None | None | 0 | 0 | 000 |
| Rssi Interrupt | AGC | 1 | 0 | 001 |
| | AGC & AFC | 1 | 1 | 001 |
| PreambleDetect | AGC | 1 | 0 | 110 |
| | AGC & AFC | 1 | 1 | 110 |
| Rssi Interrupt & PreambleDetect | AGC | 1 | 0 | 111 |
| | AGC & AFC | 1 | 1 | 111 |

When *AgcAutoOn*=0, the LNA gain is manually selected by choosing *LnaGain* bits in *RegLna*.

4.1.7. Receiver Restart Methods

The options for restart of the receiver are covered below. This is typically of use to prepare for the reception of a new signal whose strength or carrier frequency is different from the preceding packet to allow the AGC or AFC to be re-evaluated.

4.1.7.1. Restart Upon User Request

In Receive mode the user can request a receiver restart. This can be useful in conjunction with the use of a Timeout interrupt following a period of inactivity in the channel of interest. Two options are available:

- ◆ No change in the Local Oscillator upon restart: the AFC is disabled, and the *Frf* register has not been changed through SPI before the restart instruction: set bit *RestartRxWithoutPllLock* in *RegRxConfig* to 1.
- ◆ Local Oscillator change upon restart: if AFC is enabled (*AfcAutoOn*=1), and/or the *Frf* register had been changed during the last Rx period: set bit *RestartRxWithPllLock* in *RegRxConfig* to 1.

Note *ModeReady* must be at logic level 1 for a new *RestartRx* command to be taken into account.

4.1.7.2. Automatic Restart after valid Packet Reception

The bits *AutoRestartRxMode* in *RegSyncConfig* control the automatic restart feature of the SX1236 receiver, when a valid packet has been received:

- ◆ If *AutoRestartRxMode* = 00, the function is off, and the user should manually restart the receiver upon valid packet reception (see section 4.1.7.1).
- ◆ If *AutoRestartRxMode* = 01, after the user has emptied the FIFO following a *PayloadReady* interrupt, the receiver will automatically restart itself after a delay of *InterPacketRxDelay*, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection on the 'tail' of the previous packet.
- ◆ If *AutoRestartRxMode* = 10 should be used if the next reception is expected on a new frequency, i.e. *Frf* is changed after the reception of the previous packet. An additional delay is systematically added, in order for the PLL to lock at a new frequency.

4.1.7.3. Automatic Restart when Packet Collision is Detected

In receive mode the SX1236 is able to detect packet collision and restart the receiver. Collisions are detected by a sudden rise in received signal strength, detected by the RSSI. This functionality can be useful in network configurations where many asynchronous slaves attempt periodic communication with a single a master node.

The collision detector is enabled by setting bit *RestartRxOnCollision* to 1.

The decision to restart the receiver is based on the detection of RSSI change. The sensitivity of the system can be adjusted in 1 dB steps by using register *RssiCollisionThreshold* in *RegRxConfig*.

4.1.8. Top Level Sequencer

Depending on the application, it is desirable to be able to change the mode of the circuit according to a predefined sequence without access to the serial interface. In order to define different sequences or scenarios, a user-programmable state machine, called Top Level Sequencer (Sequencer in short), can automatically control the chip modes.

The Sequencer is activated by setting the *SequencerStart* bit in *RegSeqConfig1* to 1 in Sleep or Standby mode (called initial mode).

It is also possible to force the Sequencer off by setting the *Stop* bit in *RegSeqConfig1* to 1 at any time.

Note *SequencerStart* and *Stop* bit must never be set at the same time.

4.1.8.1. Sequencer States

As shown in the table below, with the aid of a pair of interrupt timers (T1 and T2), the sequencer can take control of the chip operation in all modes.

Table 14 Sequencer States

| Sequencer State | Description |
|---------------------------|---|
| SequencerOff State | The Sequencer is not activated. Sending a <i>SequencerStart</i> command will launch it. When coming from LowPowerSelection state, the Sequencer will be Off, whilst the chip will return to its initial mode (either Sleep or Standby mode). |
| Idle State | The chip is in low-power mode, either <i>Standby</i> or <i>Sleep</i> , as defined by <i>IdleMode</i> in <i>RegSeqConfig1</i> . The Sequencer waits only for the <i>T1</i> interrupt. |
| Transmit State | The transmitter in On. |
| Receive State | The receiver in On. |
| PacketReceived | The receiver is On and a packet has been received. It is stored in the FIFO. |
| LowPowerSelection | Selects low power state (SequencerOff or Idle State) |
| RxTimeout | Defines the action to be taken on a RxTimeout interrupt. RxTimeout interrupt can be a <i>TimeoutRxRssi</i> , <i>TimeoutRxPreamble</i> or <i>TimeoutSignalSync</i> interrupt. |

4.1.8.2. Sequencer Transitions

The transitions between sequencer states are listed in the forthcoming table:

Table 15 Sequencer Transition Options

| Variable | Transition |
|---------------------------|--|
| <i>IdleMode</i> | Selects the chip mode during Idle state: 0: <i>Standby</i> mode 1: <i>Sleep</i> mode |
| <i>FromStart</i> | Controls the Sequencer transition when the <i>SequencerStart</i> bit is set to 1 in <i>Sleep</i> or <i>Standby</i> mode: 00: to LowPowerSelection 01: to Receive state 10: to Transmit state 11: to Transmit state on a <i>FifoThreshold</i> interrupt |
| <i>LowPowerSelection</i> | Selects Sequencer LowPower state after a <i>to LowPowerSelection</i> transition 0: SequencerOff state with chip on Initial mode 1: Idle state with chip on <i>Standby</i> or <i>Sleep</i> mode depending on <i>IdleMode</i> Note: Initial mode is the chip LowPower mode at Sequencer start. |
| <i>FromIdle</i> | Controls the Sequencer transition from the Idle state on a <i>T1</i> interrupt: 0: to Transmit state 1: to Receive state |
| <i>FromTransmit</i> | Controls the Sequencer transition from the Transmit state: 0: to LowPowerSelection on a <i>PacketSent</i> interrupt 1: to Receive state on a <i>PacketSent</i> interrupt |
| <i>FromReceive</i> | Controls the Sequencer transition from the Receive state: 000 and 111: unused 001: to PacketReceived state on a <i>PayloadReady</i> interrupt 010: to LowPowerSelection on a <i>PayloadReady</i> interrupt 011: to PacketReceived state on a <i>CrcOk</i> interrupt. If CRC is wrong (corrupted packet, with CRC on but <i>CrcAutoClearOn</i> is off), the <i>PayloadReady</i> interrupt will drive the sequencer to <i>RxTimeout</i> state. 100: to SequencerOff state on a <i>Rssi</i> interrupt 101: to SequencerOff state on a <i>SyncAddress</i> interrupt 110: to SequencerOff state on a <i>PreambleDetect</i> interrupt Irrespective of this setting, transition to LowPowerSelection on a <i>T2</i> interrupt |
| <i>FromRxTimeout</i> | Controls the state-machine transition from the Receive state on a <i>RxTimeout</i> interrupt (and on <i>PayloadReady</i> if <i>FromReceive</i> = 011): 00: to Receive state via <i>ReceiveRestart</i> 01: to Transmit state 10: to LowPowerSelection 11: to SequencerOff state Note: <i>RxTimeout</i> interrupt is a <i>TimeoutRxRssi</i> , <i>TimeoutRxPreamble</i> or <i>TimeoutSignalSync</i> interrupt. |
| <i>FromPacketReceived</i> | Controls the state-machine transition from the PacketReceived state: 000: to SequencerOff state 001: to Transmit on a <i>FifoEmpty</i> interrupt 010: to LowPowerSelection 011: to Receive via <i>FS</i> mode, if frequency was changed 100: to Receive state (no frequency change) |

4.1.8.3. Timers

Two timers (Timer1 and Timer2) are also available in order to define periodic sequences. These timers are used to generate interrupts, which can trigger transitions of the Sequencer.

T1 interrupt is generated ($\text{Timer1Resolution} * \text{Timer1Coefficient}$) after **T2 interrupt** or **SequencerStart** command.

T2 interrupt is generated ($\text{Timer2Resolution} * \text{Timer2Coefficient}$) after **T1 interrupt**.

The timers' mechanism is summarized on the following diagram.

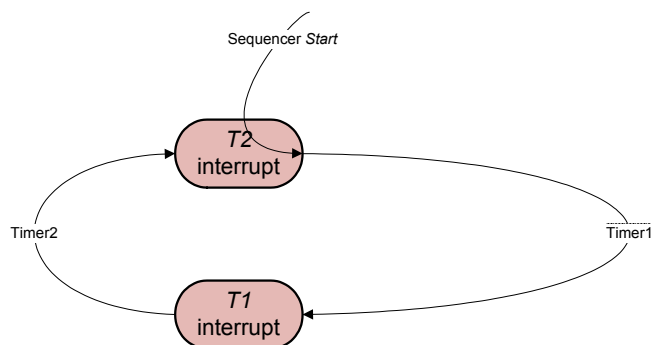


Figure 14. Timer1 and Timer2 Mechanism

Note *The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve periodic cycling.*

Table 16 Sequencer Timer Settings

| <i>Variable</i> | <i>Description</i> |
|-------------------|---|
| Timer1Resolution | Resolution of Timer1 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms |
| Timer2Resolution | Resolution of Timer2 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms |
| Timer1Coefficient | Multiplying coefficient for Timer1 |
| Timer2Coefficient | Multiplying coefficient for Timer2 |

4.1.8.4. Sequencer State Machine

The following graphs summarize every possible transition between each Sequencer state. The Sequencer states are highlighted in grey. The transitions are represented by arrows. The condition activating them is described over the transition arrow. For better readability, the start transitions are separated from the rest of the graph.

Transitory states are highlighted in light grey, and exit states are represented in red. It is also possible to force the Sequencer off by setting the *Stop* bit in *RegSeqConfig1* to 1 at any time.

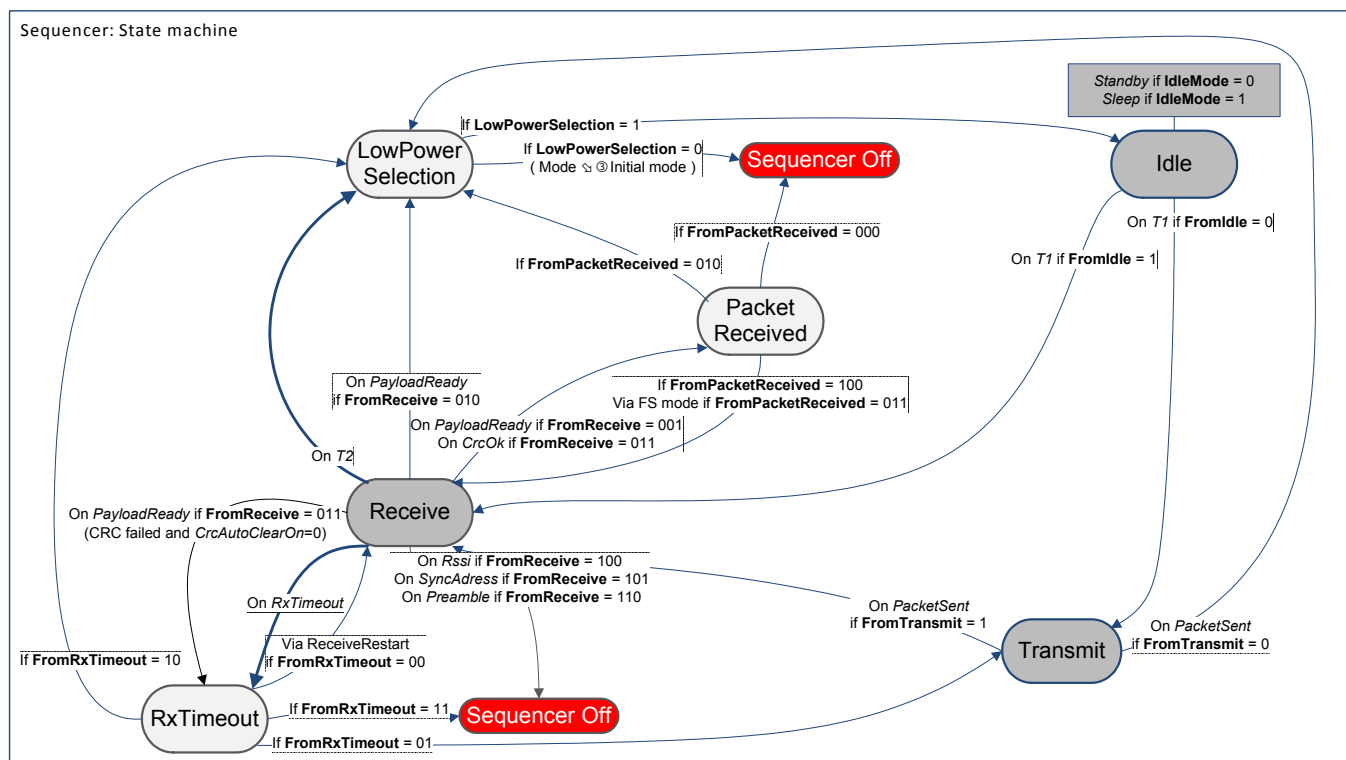
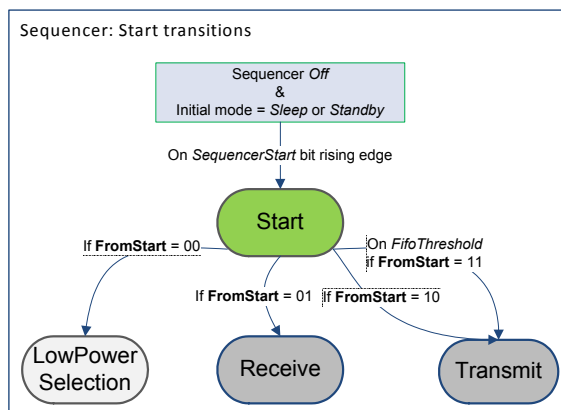


Figure 15. Sequencer State Machine

4.1.9. Data Processing in FSK/OOK Mode

4.1.9.1. Block Diagram

Figure below illustrates the SX1236 data processing circuit. Its role is to interface the data to/from the modulator/demodulator and the uC access points (SPI and DIO pins). It also controls all the configuration registers.

The circuit contains several control blocks which are described in the following paragraphs.

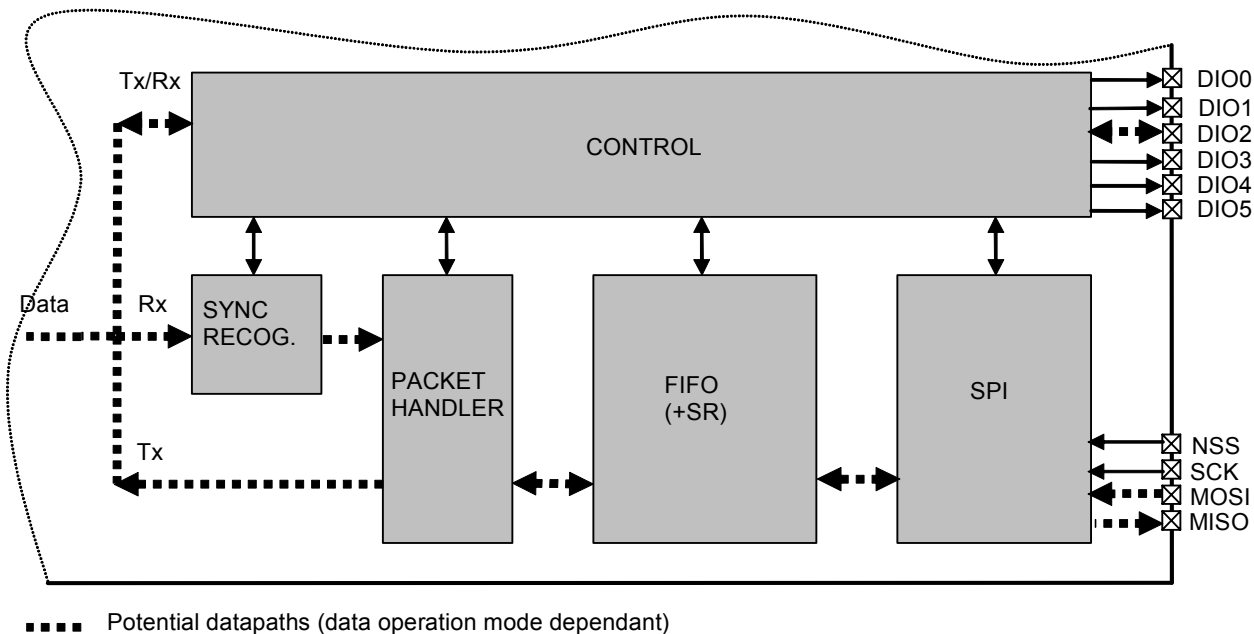


Figure 16. SX1236 Data Processing Conceptual View

The SX1236 implements several data operation modes, each with their own data path through the data processing. Depending on the data operation mode selected, some control blocks are active whilst others remain disabled.

4.1.9.2. Data Operation Modes

The SX1236 has two different data operation modes selectable by the user:

- ◆ **Continuous mode:** each bit transmitted or received is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.
- ◆ **Packet mode (recommended):** user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically built with preamble, Sync word, and optional CRC and DC-free encoding schemes. The reverse operation is performed in reception. The uC processing overhead is hence significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, etc) the maximum payload length is limited to 255, 2047 bytes or unlimited.

Each of these data operation modes is fully described in the following sections.

4.1.10. FIFO

Overview and Shift Register (SR)

In packet mode of operation, both data to be transmitted and that has been received are stored in a configurable FIFO (First In First Out) device. It is accessed via the SPI interface and provides several interrupts for transfer management.

The FIFO is 1 byte wide hence it only performs byte (parallel) operations, whereas the demodulator functions serially. A shift register is therefore employed to interface the two devices. In transmit mode it takes bytes from the FIFO and outputs them serially (MSB first) at the programmed bit rate to the modulator. Similarly in Rx, the shift register gets bit by bit data from the demodulator and writes them byte by byte to the FIFO. This is illustrated in figure below.

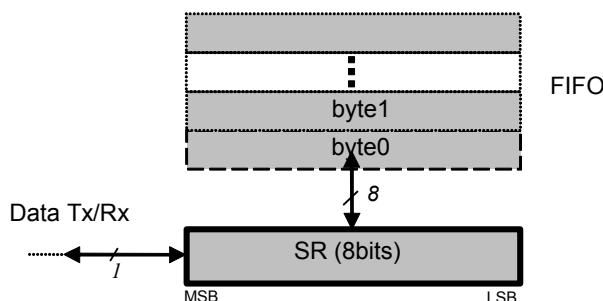


Figure 17. FIFO and Shift Register (SR)

Note When switching to Sleep mode, the FIFO can only be used once the ModeReady flag is set (quasi immediate from all modes except from Tx)

The FIFO size is fixed to 64 bytes.

Interrupt Sources and Flags

- ◆ **FifoEmpty:** *FifoEmpty* interrupt source is high when byte 0, i.e. whole FIFO, is empty. Otherwise it is low. Note that when retrieving data from the FIFO, *FifoEmpty* is updated on NSS falling edge, i.e. when *FifoEmpty* is updated to low state, the currently started read operation must be completed. In other words, *FifoEmpty* state must be checked after each read operation for a decision on the next one (*FifoEmpty* = 0: more byte(s) to read; *FifoEmpty* = 1: no more byte to read).
- ◆ **FifoFull:** *FifoFull* interrupt source is high when the last FIFO byte, i.e. the whole FIFO, is full. Otherwise it is low.
- ◆ **FifoOverrunFlag:** *FifoOverrunFlag* is set when a new byte is written by the user (in Tx or Standby modes) or the SR (in Rx mode) while the FIFO is already full. Data is lost and the flag should be cleared by writing a 1, note that the FIFO will also be cleared.
- ◆ **PacketSent:** *PacketSent* interrupt source goes high when the SR's last bit has been sent.
- ◆ **FifoLevel:** Threshold can be programmed by *FifoThreshold* in *RegFifoThresh*. Its behavior is illustrated in figure below.

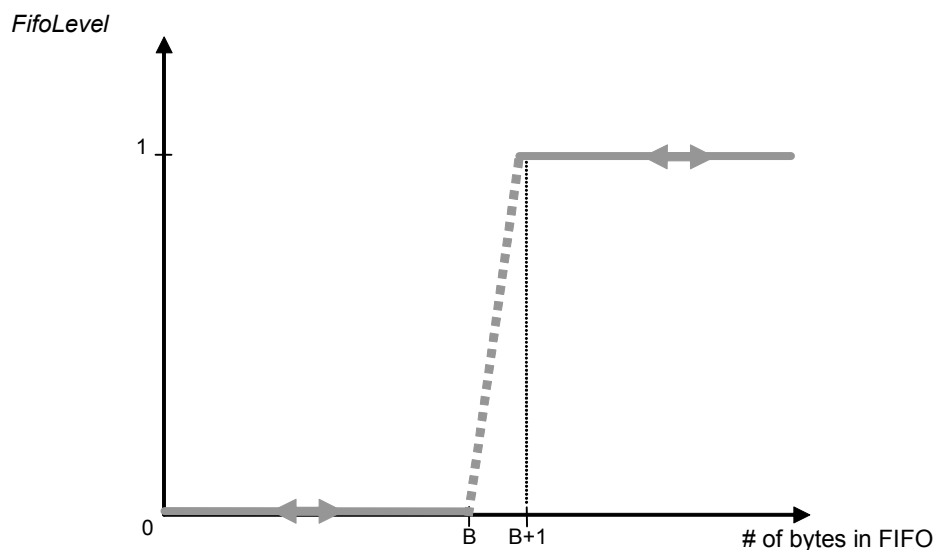


Figure 18. FifoLevel IRQ Source Behavior

- Notes**
- *FifoLevel interrupt is updated only after a read or write operation on the FIFO. Thus the interrupt cannot be dynamically updated by only changing the FifoThreshold parameter*
 - *FifoLevel interrupt is valid as long as FifoFull does not occur. An empty FIFO will restore its normal operation*

FIFO Clearing

Table below summarizes the status of the FIFO when switching between different modes.

Table 17 Status of FIFO when Switching Between Different Modes of the Chip

| From | To | FIFO status | Comments |
|-------------|-------------|-------------|--|
| Stdby | Sleep | Not cleared | |
| Sleep | Stdby | Not cleared | |
| Stdby/Sleep | Tx | Not cleared | To allow the user to write the FIFO in Stdby/Sleep before Tx |
| Stdby/Sleep | Rx | Cleared | |
| Rx | Tx | Cleared | |
| Rx | Stdby/Sleep | Not cleared | To allow the user to read FIFO in Stdby/Sleep mode after Rx |
| Tx | Any | Cleared | |

4.1.10.1. Sync Word Recognition

Overview

Sync word recognition (also called Pattern recognition) is activated by setting *SyncOn* in *RegSyncConfig*. The bit synchronizer must also be activated in Continuous mode (automatically done in Packet mode).

The block behaves like a shift register; it continuously compares the incoming data with its internally programmed Sync word and sets *SyncAddressMatch* when a match is detected. This is illustrated in Figure 19 below.

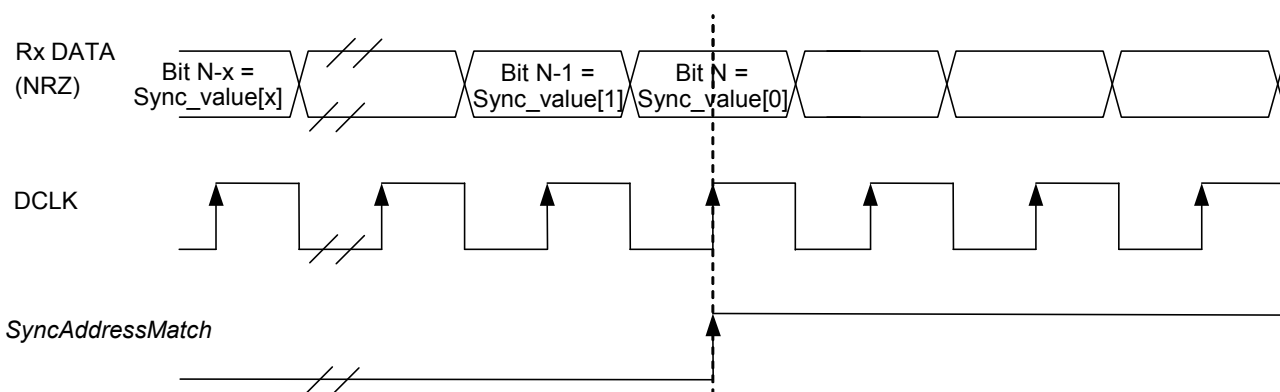


Figure 19. Sync Word Recognition

During the comparison of the demodulated data, the first bit received is compared with bit 7 (MSB) of *RegSyncValue1* and the last bit received is compared with bit 0 (LSB) of the last byte whose address is determined by the length of the Sync word.

When the programmed Sync word is detected, the user can assume that this incoming packet is for the node and can be processed accordingly.

SyncAddressMatch is cleared when leaving Rx or FIFO is emptied.

Configuration

- ◆ Size: Sync word size can be set from 1 to 8 bytes (i.e. 8 to 64 bits) via *SyncSize* in *RegSyncConfig*. In Packet mode this field is also used for Sync word generation in Tx mode.
- ◆ Value: The Sync word value is configured in *SyncValue(63:0)*. In Packet mode this field is also used for Sync word generation in Tx mode.

Note *SyncValue* choices containing 0x00 bytes are not allowed.

Packet Handler

The packet handler is the block used in Packet mode. Its functionality is fully described in Section 4.1.13.

Control

The control block configures and controls the full chip's behavior according to the settings programmed in the configuration registers.

4.1.11. Digital IO Pins Mapping

Six general purpose IO pins are available on the SX1236, and their configuration in Continuous or Packet mode is controlled through *RegDioMapping1* and *RegDioMapping2*.

Table 18 *DIO Mapping, Continuous Mode*

| | DIOx Mapping | Sleep | Standby | FSRx/Tx | Rx | Tx |
|------|--------------|--------------|---------|---------------------|-----------------------|---------|
| DIO0 | 00 | | - | | SyncAddress | TxReady |
| | 01 | | - | | Rssi / PreambleDetect | - |
| | 10 | | - | | RxReady | TxReady |
| | 11 | | - | - | | |
| DIO1 | 00 | | - | | Dclk | |
| | 01 | | - | | Rssi / PreambleDetect | - |
| | 10 | | - | - | | |
| | 11 | | - | - | | |
| DIO2 | 00 | | - | | Data | |
| | 01 | | - | | Data | |
| | 10 | | - | | Data | |
| | 11 | | - | | Data | |
| DIO3 | 00 | | - | | Timeout | - |
| | 01 | | - | | Rssi / PreambleDetect | - |
| | 10 | | - | - | | |
| | 11 | - | | TempChange / LowBat | TempChange / LowBat | |
| DIO4 | 00 | | - | | TempChange / LowBat | |
| | 01 | | - | | PIILock | |
| | 10 | | - | | TimeOut | - |
| | 11 | - | | ModeReady | ModeReady | |
| DIO5 | 00 | ClkOut if RC | | ClkOut | ClkOut | |
| | 01 | | - | | PIILock | |
| | 10 | | - | | Rssi / PreambleDetect | - |
| | 11 | - | | ModeReady | ModeReady | |

Table 19 *DIO Mapping, Packet Mode*

| | DIOx Mapping | Sleep | Standby | FSRx/Tx | Rx | Tx |
|------|--------------|--------------|----------|---------------------|-----------------------|------------|
| DIO0 | 00 | | - | | PayloadReady | PacketSent |
| | 01 | | - | | CrcOk | - |
| | 10 | | - | - | | |
| | 11 | - | | TempChange / LowBat | TempChange / LowBat | |
| DIO1 | 00 | FifoLevel | | FifoLevel | FifoLevel | |
| | 01 | FifoEmpty | | FifoEmpty | FifoEmpty | |
| | 10 | FifoFull | | FifoFull | FifoFull | |
| | 11 | | - | - | | |
| DIO2 | 00 | FifoFull | | FifoFull | FifoFull | |
| | 01 | | - | | RxReady | - |
| | 10 | | FifoFull | | TimeOut | FifoFull |
| | 11 | | FifoFull | | SyncAddress | FifoFull |
| DIO3 | 00 | FifoEmpty | | FifoEmpty | FifoEmpty | |
| | 01 | | - | | | TxReady |
| | 10 | FifoEmpty | | FifoEmpty | FifoEmpty | |
| | 11 | FifoEmpty | | FifoEmpty | FifoEmpty | |
| DIO4 | 00 | - | | TempChange / LowBat | TempChange / LowBat | |
| | 01 | | - | | PIILock | |
| | 10 | | - | | TimeOut | - |
| | 11 | | - | | Rssi / PreambleDetect | - |
| DIO5 | 00 | ClkOut if RC | | ClkOut | ClkOut | |
| | 01 | | - | | PIILock | |
| | 10 | | - | | Data | |
| | 11 | - | | ModeReady | ModeReady | |

4.1.12. Continuous Mode

4.1.12.1. General Description

As illustrated in Figure 20, in Continuous mode, the NRZ data to (from) the (de)modulator is directly accessed by the uC on the bidirectional DIO2/DATA pin. The FIFO and packet handler are thus inactive.

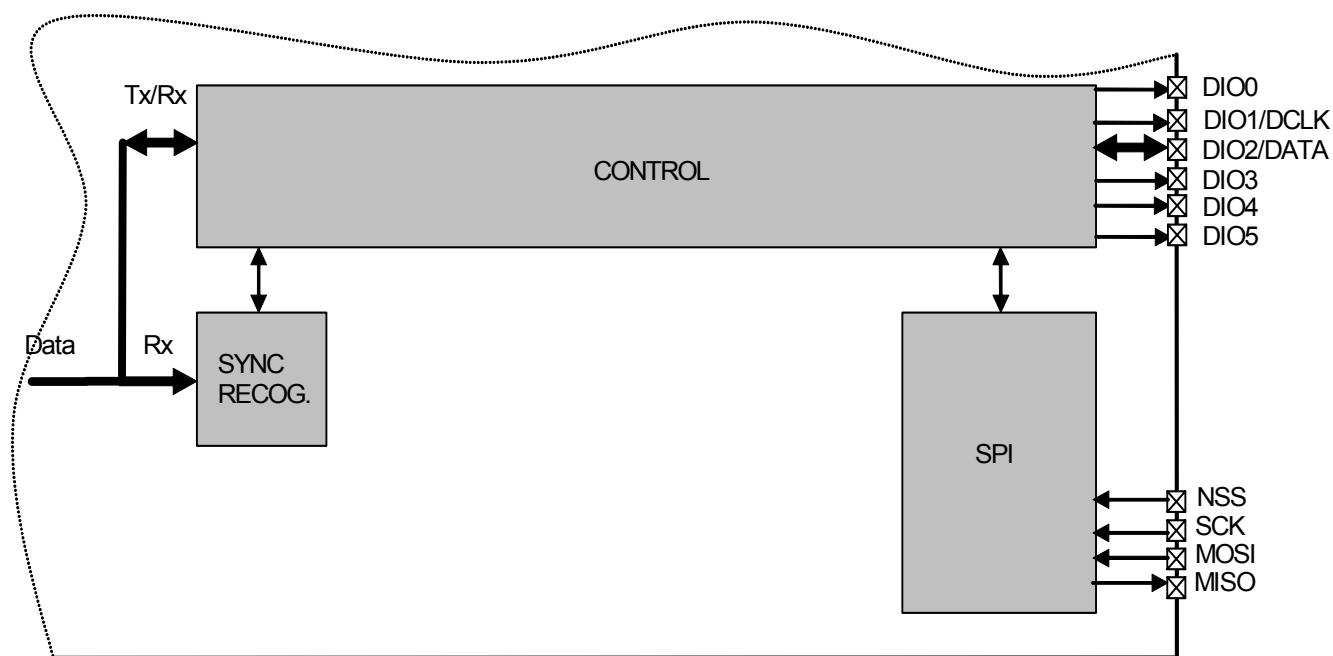


Figure 20. Continuous Mode Conceptual View

4.1.12.2. Tx Processing

In Tx mode, a synchronous data clock for an external uC is provided on DIO1/DCLK pin. Clock timing with respect to the data is illustrated in Figure 21. DATA is internally sampled on the rising edge of DCLK so the uC can change logic state anytime outside the grayed out setup/hold zone.

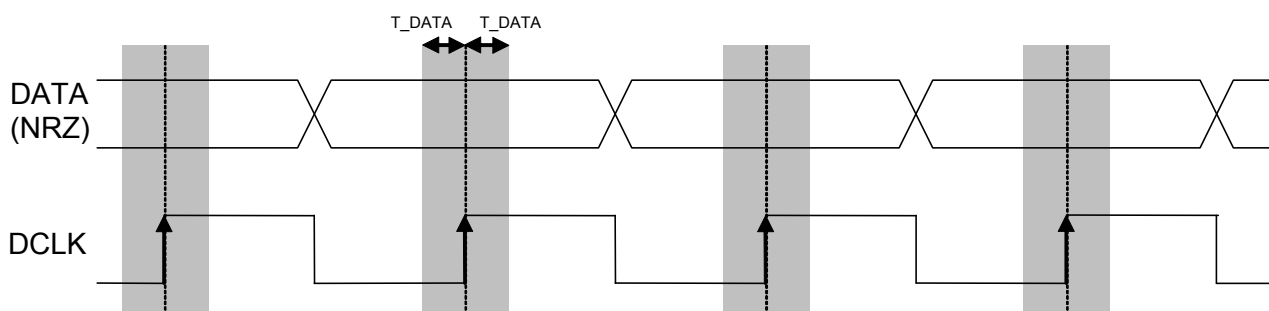


Figure 21. Tx Processing in Continuous Mode

Note The use of DCLK is required when the modulation shaping is enabled.

4.1.12.3. Rx Processing

If the bit synchronizer is disabled, the raw demodulator output is made directly available on DATA pin and no DCLK signal is provided.

Conversely, if the bit synchronizer is enabled, synchronous cleaned data and clock are made available respectively on DIO2/DATA and DIO1/DCLK pins. DATA is sampled on the rising edge of DCLK and updated on the falling edge as illustrated below.

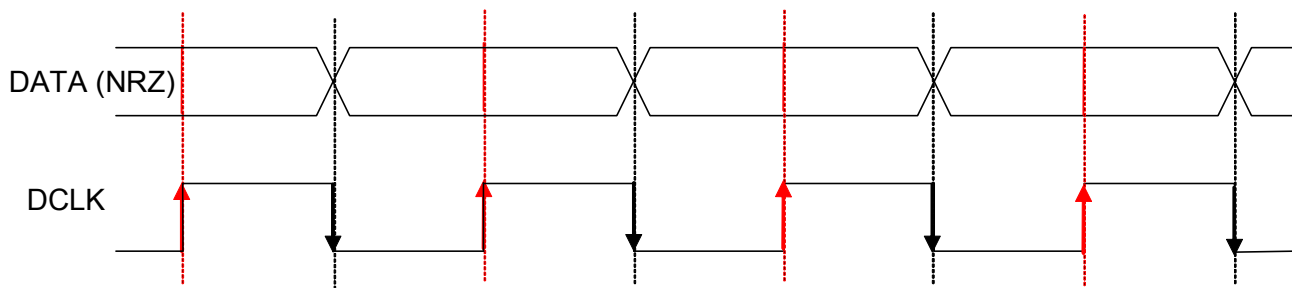


Figure 22. Rx Processing in Continuous Mode

Note In Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC (bit synchronizer is automatically enabled in Packet mode).

4.1.13. Packet Mode

4.1.13.1. General Description

In Packet mode the NRZ data to (from) the (de)modulator is not directly accessed by the uC but stored in the FIFO and accessed via the SPI interface.

In addition, the SX1236 packet handler performs several packet oriented tasks such as Preamble and Sync word generation, CRC calculation/check, whitening/dewhitening of data, Manchester encoding/decoding, address filtering, etc. This simplifies software and reduces uC overhead by performing these repetitive tasks within the RF chip itself.

Another important feature is ability to fill and empty the FIFO in Sleep/Stdby mode, ensuring optimum power consumption and adding more flexibility for the software.

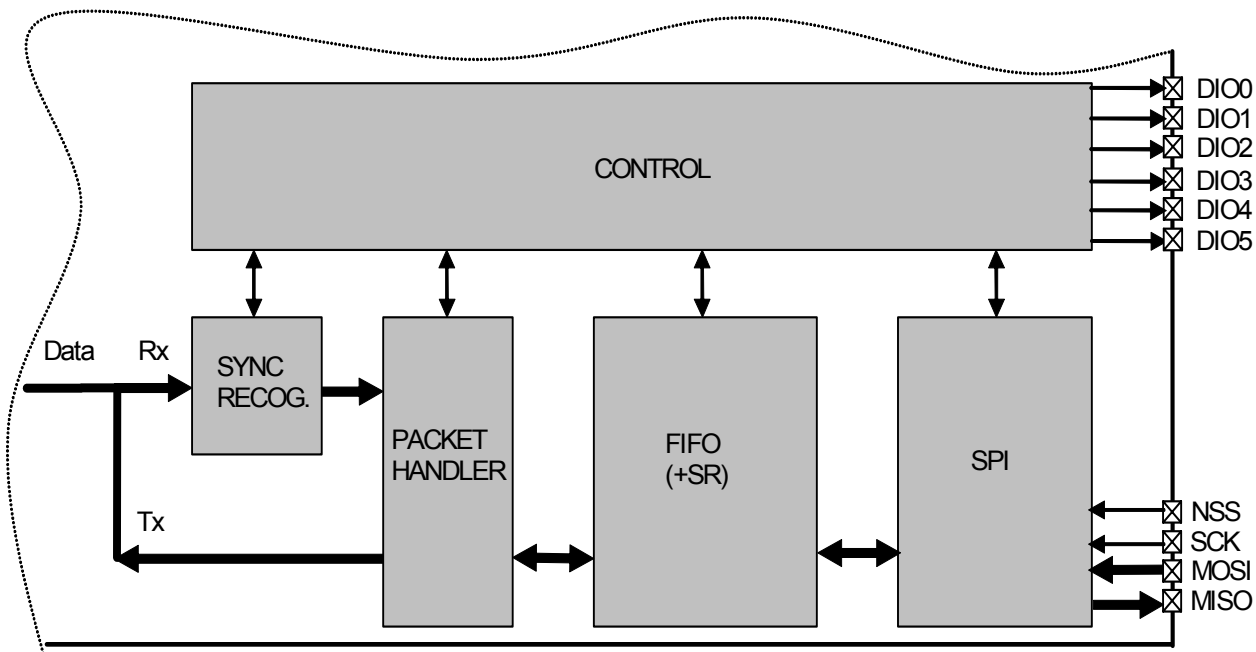


Figure 23. Packet Mode Conceptual View

Note The Bit Synchronizer is automatically enabled in Packet mode.

4.1.13.2. Packet Format

Fixed Length Packet Format

Fixed length packet format is selected when bit *PacketFormat* is set to 0 and *PayloadLength* is set to any value greater than 0.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.

The length of the payload is limited to 2047 bytes.

The length programmed in *PayloadLength* relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown below. It contains the following fields:

- ◆ Preamble (1010...)
- ◆ Sync word (Network ID)
- ◆ Optional Address byte (Node ID)
- ◆ Message data
- ◆ Optional 2-bytes CRC checksum

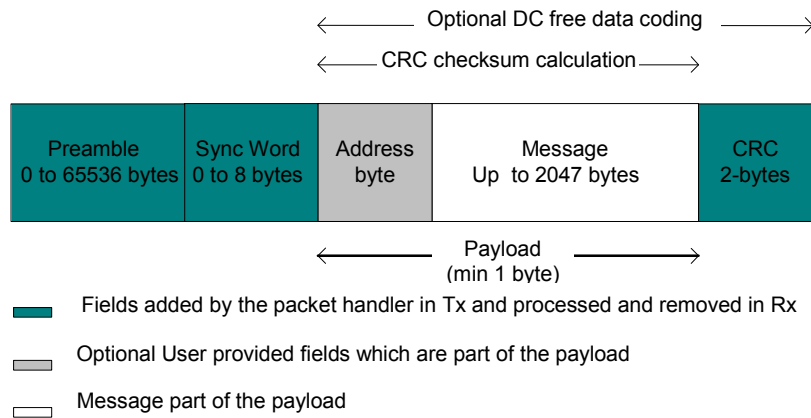


Figure 24. Fixed Length Packet Format

Variable Length Packet Format

Variable length packet format is selected when bit *PacketFormat* is set to 1.

This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte, is given by the first byte of the FIFO and is limited to 255 bytes. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown below. It contains the following fields:

- ◆ Preamble (1010...)
- ◆ Sync word (Network ID)
- ◆ Length byte
- ◆ Optional Address byte (Node ID)
- ◆ Message data

◆ Optional 2-bytes CRC checksum

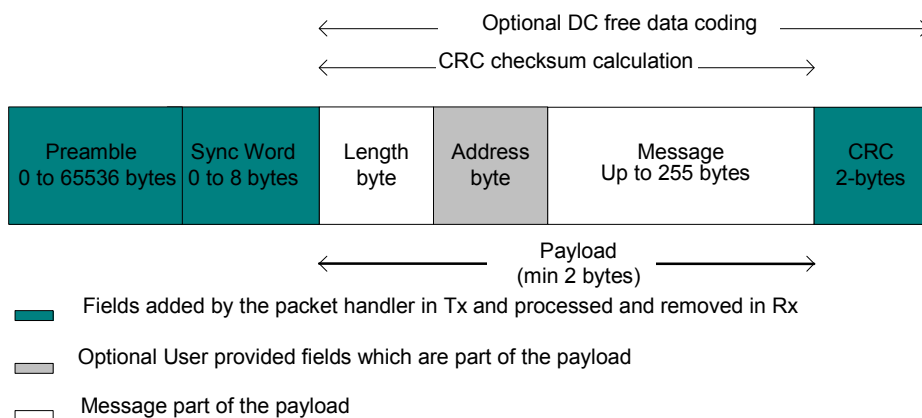


Figure 25. Variable Length Packet Format

Unlimited Length Packet Format

Unlimited length packet format is selected when bit *PacketFormat* is set to 0 and *PayloadLength* is set to 0. The user can then transmit and receive packet of arbitrary length and *PayloadLength* register is not used in Tx/Rx modes for counting the length of the bytes transmitted/received.

In Tx the data is transmitted depending on the *TxStartCondition* bit. On the Rx side the data processing features like Address filtering, Manchester encoding and data whitening are not available if the sync pattern length is set to zero (*SyncOn* = 0). The CRC detection in Rx is also not supported in this mode of the packet handler, however CRC generation in Tx is operational. The interrupts like *CrcOk* & *PayloadReady* are not available either.

An unlimited length packet shown below is made up of the following fields:

- ◆ Preamble (1010...)
- ◆ Sync word (Network ID)
- ◆ Optional Address byte (Node ID)
- ◆ Message data
- ◆ Optional 2-bytes CRC checksum (Tx only)

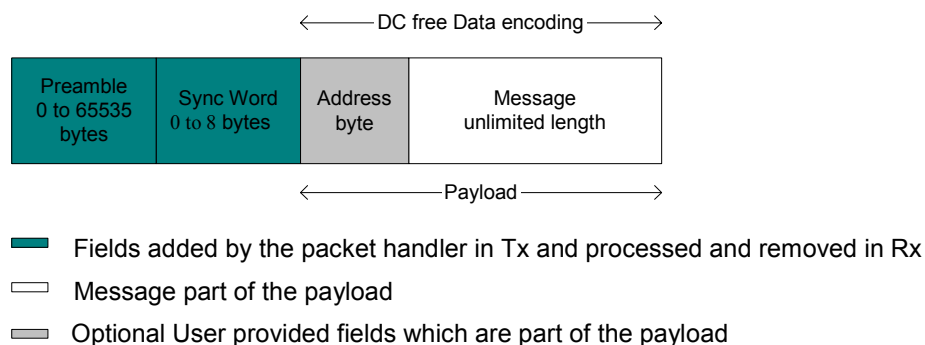


Figure 26. Unlimited Length Packet Format

4.1.13.3. Tx Processing

In Tx mode the packet handler dynamically builds the packet by performing the following operations on the payload available in the FIFO:

- ◆ Add a programmable number of preamble bytes
- ◆ Add a programmable Sync word
- ◆ Optionally calculating CRC over complete payload field (optional length byte + optional address byte + message) and appending the 2 bytes checksum
- ◆ Optional DC-free encoding of the data (Manchester or whitening)

Only the payload (including optional address and length fields) is required to be provided by the user in the FIFO.

The transmission of packet data is initiated by the Packet Handler only if the chip is in Tx mode and the transmission condition defined by *TxStartCondition* is fulfilled. If transmission condition is not fulfilled then the packet handler transmits a preamble sequence until the condition is met. This happens only if the preamble length $\neq 0$, otherwise it transmits a zero or one until the condition is met to transmit the packet data.

The transmission condition itself is defined as:

- ◆ if *TxStartCondition* = 1, the packet handler waits until the first byte is written into the FIFO, then it starts sending the preamble followed by the sync word and user payload
- ◆ If *TxStartCondition* = 0, the packet handler waits until the number of bytes written in the FIFO is equal to the number defined in *RegFifoThresh* + 1
- ◆ If the condition for transmission was already fulfilled i.e. the FIFO was filled in Sleep/Stdby then the transmission of packet starts immediately on enabling Tx

4.1.13.4. Rx Processing

In Rx mode the packet handler extracts the user payload to the FIFO by performing the following operations:

- ◆ Receiving the preamble and stripping it off
- ◆ Detecting the Sync word and stripping it off
- ◆ Optional DC-free decoding of data
- ◆ Optionally checking the address byte
- ◆ Optionally checking CRC and reflecting the result on *CrcOk*.

Only the payload (including optional address and length fields) is made available in the FIFO.

When the Rx mode is enabled the demodulator receives the preamble followed by the detection of sync word. If fixed length packet format is enabled, then the number of bytes received as the payload is given by the *PayloadLength* parameter.

In variable length mode the first byte received after the sync word is interpreted as the length of the received packet. The internal length counter is initialized to this received length. The *PayloadLength* register is set to a value which is greater than the maximum expected length of the received packet. If the received length is greater than the maximum length stored in *PayloadLength* register the packet is discarded otherwise the complete packet is received.

If the address check is enabled, then the second byte received in case of variable length and first byte in case of fixed length is the address byte. If the address matches the one in the *NodeAddress* field, reception of the data continues otherwise it is stopped. The CRC check is performed if *CrcOn* = 1 and the result is available in *CrcOk* indicating that the

CRC was successful. An interrupt (*PayloadReady*) is also generated on DIO0 as soon as the payload is available in the FIFO. The payload available in the FIFO can also be read in Sleep/Standby mode.

If the CRC fails the *PayloadReady* interrupt is not generated and the FIFO is cleared. This function can be overridden by setting *CrcAutoClearOff* = 1, forcing the availability of *PayloadReady* interrupt and the payload in the FIFO even if the CRC fails.

4.1.13.5. Handling Large Packets

When *PayloadLength* exceeds FIFO size (64 bytes) whether in fixed, variable or unlimited length packet format, in addition to *PacketSent* in Tx and *PayloadReady* or *CrcOk* in Rx, the FIFO interrupts/flags can be used as described below:

- ◆ For Tx: FIFO can be prefilled in Sleep/Standby but must be refilled “on-the-fly” during Tx with the rest of the payload.
 - 1) Pre-fill FIFO (in Sleep/Standby first or directly in Tx mode) until *FifoThreshold* or *FifoFull* is set
 - 2) In Tx, wait for *FifoThreshold* or *FifoEmpty* to be set (i.e. FIFO is nearly empty)
 - 3) Write bytes into the FIFO until *FifoThreshold* or *FifoFull* is set
 - 4) Continue to step 2 until the entire message has been written to the FIFO (*PacketSent* will fire when the last bit of the packet has been sent).
- ◆ For Rx: FIFO must be unfilled “on-the-fly” during Rx to prevent FIFO overrun.
 - 1) Start reading bytes from the FIFO when *FifoEmpty* is cleared or *FifoThreshold* becomes set
 - 2) Suspend reading from the FIFO if *FifoEmpty* fires before all bytes of the message have been read
 - 3) Continue to step 1 until *PayloadReady* or *CrcOk* fires
 - 4) Read all remaining bytes from the FIFO either in Rx or Sleep/Standby mode

4.1.13.6. Packet Filtering

The SX1236 packet handler offers several mechanisms for packet filtering, ensuring that only useful packets are made available to the uC, reducing significantly system power consumption and software complexity.

Sync Word Based

Sync word filtering/recognition is used for identifying the start of the payload and also for network identification. As previously described, the Sync word recognition block is configured (size, value) in *RegSyncConfig* and *RegSyncValue(i)* registers. This information is used, both for appending Sync word in Tx, and filtering packets in Rx.

Every received packet which does not start with this locally configured Sync word is automatically discarded and no interrupt is generated.

When the Sync word is detected, payload reception automatically starts and *SyncAddressMatch* is asserted.

Note Sync Word values containing 0x00 byte(s) are forbidden

Address Based

Address filtering can be enabled via the *AddressFiltering* bits. It adds another level of filtering, above Sync word (i.e. Sync must match first), typically useful in a multi-node networks where a network ID is shared between all nodes (Sync word) and each node has its own ID (address).

Two address based filtering options are available:

- ◆ *AddressFiltering* = 01: Received address field is compared with internal register *NodeAddress*. If they match then the packet is accepted and processed, otherwise it is discarded.
- ◆ *AddressFiltering* = 10: Received address field is compared with internal registers *NodeAddress* and *BroadcastAddress*. If either is a match, the received packet is accepted and processed, otherwise it is discarded. This additional check with a constant is useful for implementing broadcast in a multi-node networks

Please note that the received address byte, as part of the payload, is not stripped off the packet and is made available in the FIFO. In addition, *NodeAddress* and *AddressFiltering* only apply to Rx. On Tx side, if address filtering is expected, the address byte should simply be put into the FIFO like any other byte of the payload.

As address filtering requires a Sync word match, both features share the same interrupt flag *SyncAddressMatch*.

Length Based

In variable length Packet mode, *PayloadLength* must be programmed with the maximum payload length permitted. If received length byte is smaller than this maximum, then the packet is accepted and processed, otherwise it is discarded.

Please note that the received length byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

To disable this function, the user should set the value of the *PayloadLength* to 2047.

CRC Based

The CRC check is enabled by setting bit *CrcOn* in *RegPacketConfig1*. It is used for checking the integrity of the message.

- ◆ On Tx side a two byte CRC checksum is calculated on the payload part of the packet and appended to the end of the message
- ◆ On Rx side the checksum is calculated on the received payload and compared with the two checksum bytes received. The result of the comparison is stored in bit *CrcOk*

By default, if the CRC check fails then the FIFO is automatically cleared and no interrupt is generated. This filtering function can be disabled via *CrcAutoClearOff* bit and in this case, even if CRC fails, the FIFO is not cleared and only *PayloadReady* interrupt goes high. Please note that in both cases, the two CRC checksum bytes are stripped off by the packet handler and only the payload is made available in the FIFO. Two CRC implementations are selected with bit *CrcWhiteningType*.

Table 20 CRC Description

| Crc Type | CrcWhiteningType | Polynomial | Seed Value | Complemented |
|--------------|------------------|-----------------------------|------------|--------------|
| CCITT | 0 (default) | $X^{16} + X^{12} + X^5 + 1$ | 0x1D0F | Yes |
| IBM | 1 | $X^{16} + X^{15} + X^2 + 1$ | 0xFFFF | No |

A C code implementation of each CRC type is proposed in Application Section 7.

4.1.13.7. DC-Free Data Mechanisms

The payload to be transmitted may contain long sequences of 1's and 0's, which introduces a DC bias in the transmitted signal. The radio signal thus produced has a non uniform power distribution over the occupied channel bandwidth. It also introduces data dependencies in the normal operation of the demodulator. Thus it is useful if the transmitted data is random and DC free.

For such purposes, two techniques are made available in the packet handler: Manchester encoding and data whitening.

Note Only one of the two methods can be enabled at a time.

Manchester Encoding

Manchester encoding/decoding is enabled if *DcFree* = 01 and can only be used in Packet mode.

The NRZ data is converted to Manchester code by coding '1' as "10" and '0' as "01".

In this case, the maximum chip rate is the maximum bit rate given in the specifications and the actual bit rate is half the chip rate.

Manchester encoding and decoding is only applied to the payload and CRC checksum while preamble and Sync word are kept NRZ. However, the chip rate from preamble to CRC is the same and defined by *BitRate* in *RegBitRate* (Chip Rate = Bit Rate NRZ = 2 x Bit Rate Manchester).

Manchester encoding/decoding is thus made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

| | 1/BR ...Sync | | | | | | | | 1/BR Payload... | | | | | | | | | | |
|---------------------------------|--------------|---|---|---|---|---|---|---|-----------------|---|---|---|---|---|---|---|---|---|-----|
| RF chips @ BR | ... | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | ... |
| User/NRZ bits Manchester OFF | ... | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | ... |
| User/NRZ bits Manchester ON | ... | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | ... |

Figure 27. Manchester Encoding/Decoding

Data Whitening

Another technique called whitening or scrambling is widely used for randomizing the user data before radio transmission. The data is whitened using a random sequence on the Tx side and de-whitened on the Rx side using the same sequence. Comparing to Manchester technique it has the advantage of keeping NRZ data rate i.e. actual bit rate is not halved.

The whitening/de-whitening process is enabled if *DcFree* = 10. A 9-bit LFSR is used to generate a random sequence. The payload and 2-byte CRC checksum is then XORed with this random sequence as shown below. The data is de-whitened on the receiver side by XORing with the same random sequence.

Payload whitening/de-whitening is thus made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

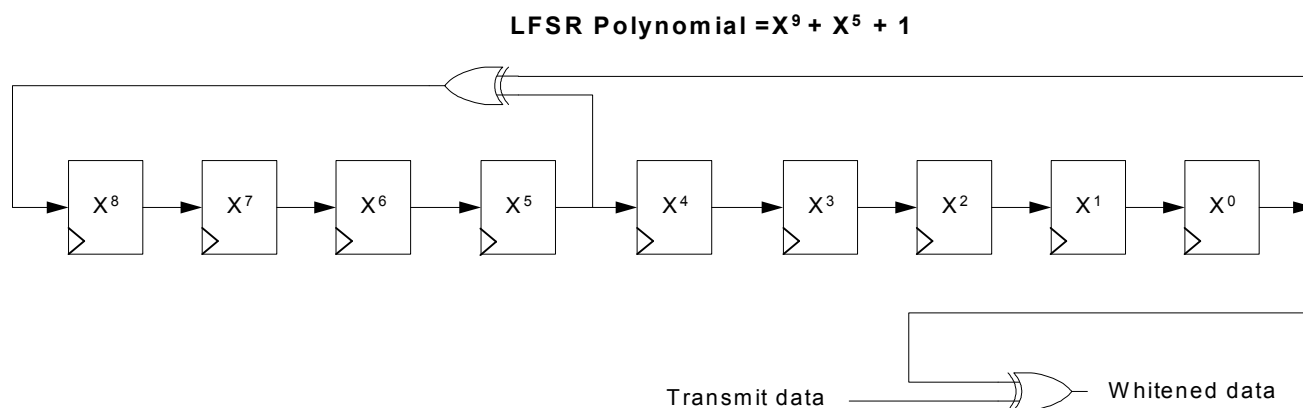


Figure 28. Data Whitening Polynomial

4.1.13.8. Beacon Tx Mode

In some short range wireless network topologies a repetitive message, also known as beacon, is transmitted periodically by a transmitter. The Beacon Tx mode allows for the re-transmission of the same packet without having to fill the FIFO multiple times with the same data.

When *BeaconOn* in *RegPacketConfig2* is set to 1, the FIFO can be filled only once in Sleep or Stdbby mode with the required payload. After a first transmission, *FifoEmpty* will go high as usual, but the FIFO content will be restored when the chip exits Transmit mode. *FifoEmpty*, *FifoFull* and *FifoLevel* flags are also restored.

This feature is only available in Fixed packet format, with the Payload Length smaller than the FIFO size. The control of the chip modes (Tx-Sleep-Tx....) can either be undertaken by the microcontroller, or be automated in the Top Sequencer. See example in Section 4.1.8.

The Beacon Tx mode is exited by setting *BeaconOn* to 0, and clearing the FIFO by setting *FifoOverrun* to 1.

4.1.14. io-homecontrol® Compatibility Mode

The SX1236 features a io-homecontrol® compatibility mode. Please contact your local Semtech representative for details on its implementation.

4.2. SPI Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- ◆ **SINGLE access:** an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.
- ◆ **BURST access:** the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- ◆ **FIFO access:** if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

The figure below shows a typical SPI single access to a register.

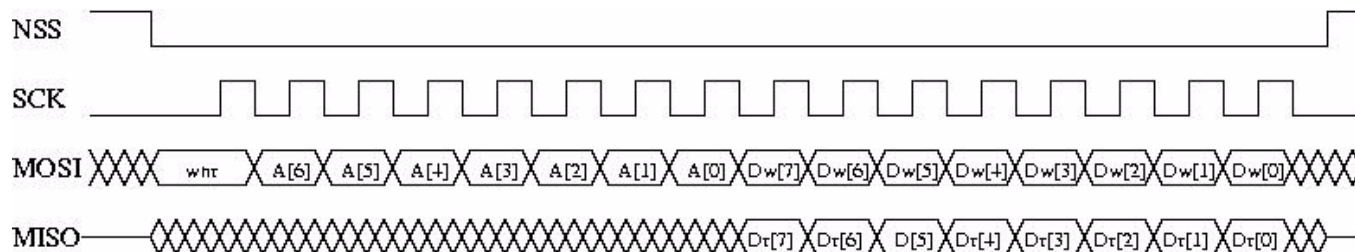


Figure 29. SPI Timing Diagram (single access)

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer is always started by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It comprises:

- ◆ A wnr bit, which is 1 for write access and 0 for read access.
- ◆ Then 7 bits of address, MSB first.

The second byte is a data byte, either sent on MOSI by the master in case of a write access or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

Proceeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without a rising NSS edge and re-sending the address. In FIFO mode, if the address was the FIFO address then the bytes will be written / read at the FIFO address. In Burst mode, if the address was not the FIFO address, then it is automatically incremented for each new byte received.

The frame ends when NSS goes high. The next frame must start with an address byte. The SINGLE access mode is therefore a special case of FIFO / BURST mode with only 1 data byte transferred.

During the write access, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

5. SX1236 Analog & RF Frontend Electronics

5.1. Power Supply Strategy

The SX1236 employs an internal voltage regulation scheme which provides stable operating voltage, and hence device characteristics, over the full industrial temperature and operating voltage range of operation. This includes up to +17 dBm of RF output power which is maintained from 1.8 V to 3.7 V and +20 dBm from 2.4 V to 3.7 V.

The SX1236 can be powered from any low-noise voltage source via pins VBAT_ANA, VBAT_RF and VBAT_DIG. Decoupling capacitors should be connected, as suggested in the reference design of the applications section of this document, on VR_PA, VR_DIG and VR_ANA pins to ensure correct operation of the built-in voltage regulators.

5.2. Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to the supply voltage dropping below a programmable threshold that is adjustable through the register *RegLowBat*. The interrupt signal can be mapped to any of the DIO pins by programming *RegDioMapping*.

5.3. Frequency Synthesis

5.3.1. Crystal Oscillator

The crystal oscillator is the main timing reference of the SX1236. It is used as the reference for the PLL's frequency synthesis and as the clock signal for all digital processing.

The crystal oscillator startup time, TS_OSC, depends on the electrical characteristics of the crystal reference used, for more information on the electrical specification of the crystal see section 7.1. The crystal connects to the Pierce oscillator on pins XTA and XTB. The SX1236 optimizes the startup time and automatically triggers the PLL when the oscillator signal is stable.

Optionally, an external clock can be used to replace the crystal oscillator. This typically takes the form of a tight tolerance temperature compensated crystal oscillator (TCXO). When using an external clock source the bit *TcxoInputOn* of register *RegTcxo* should be set to 1 and the external clock has to be provided on XTA (pin 5). XTB (pin 6) should be left open.

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, C_D .

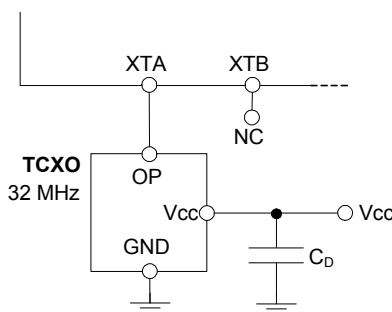


Figure 30. TCXO Connection

5.3.2. CLKOUT Output

The reference frequency, or a fraction of it, can be provided on DIO5 (pin 13) by modifying bits *ClkOut* in *RegDioMapping2*. Two typical applications of the CLKOUT output include:

- ◆ To provide a clock output for a companion processor, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at power on reset.
- ◆ To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note To minimize the current consumption of the SX1236, please ensure that the CLKOUT signal is disabled when not required.

5.3.3. PLL

The local oscillator of the SX1236 is derived from two almost identical fractional-N PLLs that are referenced to the crystal oscillator circuit. Both PLLs feature a programmable bandwidth setting where one of four discrete preset bandwidths may be accessed.

The SX1236 PLL uses a 19-bit sigma-delta modulator whose frequency resolution, constant over the whole frequency range, is given by:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through *RegFrf*, split across addresses 0x06 to 0x08:

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note The *Frf* setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte *FrfLsb* in *RegFrfLsb* is written. This allows the potential for user generation of *m*-ary FSK at very low bit rates. This is possible where frequency modulation is achieved by direct programming of the programmed RF centre frequency. To enable this functionality set the *FastHopOn* bit of register *RegPllHop*.

Three frequency bands are supported, defined as follows:

Table 21 Frequency Bands

| Name | Frequency Limits |
|-------------|------------------|
| Band 1 (HF) | 820-1020 MHz |
| Band 2 (LF) | 410-525 MHz |
| Band 3 (LF) | 137-175 MHz |

5.3.4. RC Oscillator

All timing operations in the low-power Sleep state of the Top Level Sequencer rely on the accuracy of the internal low-power RC oscillator. This oscillator is automatically calibrated at the device power-up not requiring any user input.

5.4. Transmitter Description

The transmitter of SX1236 comprises the frequency synthesizer, modulator, and power amplifier blocks, together with the DC biasing and ramping functionality that is provided through the VR_PA block.

5.4.1. Architecture Description

The architecture of the RF front end is shown in the following diagram:

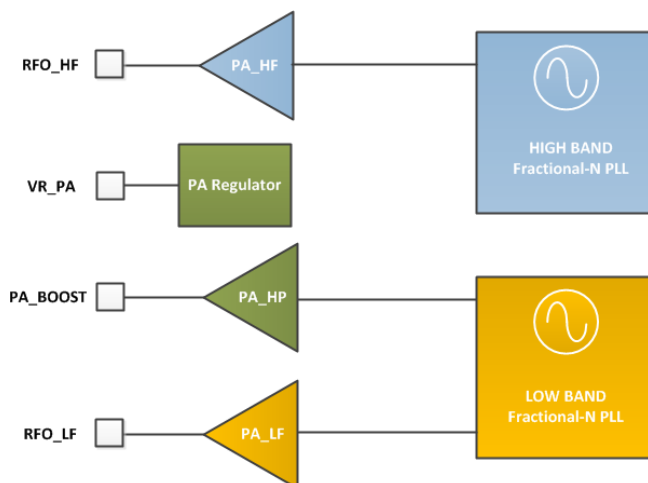


Figure 31. RF Front-end Architecture Shows the Internal PA Configuration.

5.4.2. RF Power Amplifiers

PA_HF and PA_LF are high efficiency amplifiers capable of yielding RF power programmable in 1 dB steps from -4 to +14dBm directly into a 50 ohm load with low current consumption. PA_LF covers the lower bands (up to 525 MHz), whilst PA_HF will cover the upper bands (from 860 MHz). The output power is sensitive to the power supply voltage, and typically their performance is expressed at 3.3V.

PA_HP (High Power), connected to the PA_BOOST pin, covers all frequency bands that the chip addresses. It permits continuous operation at up to +17 dBm and duty cycled operation at up to +20dBm. For full details of operation at +20dBm please consult section 5.4.3

Table 22 Power Amplifier Mode Selection Truth Table

| PaSelect | Mode | Power Range | Pout Formula |
|----------|------------------------------------|--------------|---|
| 0 | PA_HF or PA_LF on RFO_HF or RFO_LF | -4 to +15dBm | $P_{out} = P_{max} - (15 - \text{OutputPower})$ $P_{max} = 10.8 + 0.6 * \text{MaxPower [dBm]}$ |
| 1 | PA_HP on PA_BOOST, any frequency | +2 to +17dBm | $P_{out} = 17 - (15 - \text{OutputPower}) \text{ [dBm]}$ |

Notes - For +20 dBm restrictions on operation please consult the following section.

- To ensure correct operation at the highest power levels ensure that the current limiter OcpTrim is adjusted to permit delivery of the requisite supply current.

- If the PA_BOOST pin is not used, it may be left floating.

5.4.3. High Power +20 dBm Operation

The SX1236 have a high power +20 dBm capability on PA_BOOST pin, with the following settings:

Table 23 High Power Settings

| Register | Address | Value for High Power | Default value PA_HF/LF or +17dBm | Description |
|----------|---------|----------------------|----------------------------------|------------------------------|
| RegPaDac | 0x4d | 0x87 | 0x84 | Set Pmax to +20dBm for PA_HP |

Notes

- High Power settings must be turned off when using PA_LF or PA_HF
- The Over Current Protection limit should be adapted to the actual power level, in RegOcp

Specific Absolute Maximum Ratings and Operating Range restrictions apply to the +20 dBm operation. They are listed in Table 24 and Table 25.

Table 24 Operating Range, +20dBm Operation

| Symbol | Description | Min | Max | Unit |
|------------|--|-----|-----|------|
| DC_20dBm | Duty Cycle of transmission at +20 dBm output | - | 1 | % |
| VSWR_20dBm | Maximum VSWR at antenna port, +20 dBm output | - | 3:1 | - |

Table 25 Operating Range, +20dBm Operation

| Symbol | Description | Min | Max | Unit |
|-------------|--------------------------------|-----|-----|------|
| VDDop_20dBm | Supply voltage, +20 dBm output | 2.4 | 3.7 | V |

The duty cycle of transmission at +20 dBm is limited to 1%, with a maximum VSWR of 3:1 at antenna port, over the standard operating range [-40;+85°C]. For any other operating condition, contact your Semtech representative.

5.4.4. Over Current Protection

The power amplifiers of SX1236 are protected against current over supply in adverse RF load conditions by the over current protection block. This has the added benefit of protecting battery chemistries with limited peak current capability and minimising worst case PA consumption in battery life calculation. The current limiter value is controlled by the *OcpTrim* bits in *RegOcp*, and is calculated according to the following formulae:

Table 26 Trimming of the OCP Current

| <i>OcpTrim</i> | I_{MAX} | <i>I</i> _{max} Formula |
|----------------|---------------|---------------------------------|
| 0 to 15 | 45 to 120 mA | $45 + 5 * OcpTrim$ [mA] |
| 16 to 27 | 130 to 240 mA | $-30 + 10 * OcpTrim$ [mA] |
| 27+ | 240 mA | 240 mA |

Note *I*_{max} sets a limit on the current drain of the Power Amplifier only, hence the maximum current drain of the SX1236 is equal to *I*_{max} + *I*_{FS}.

5.5. Receiver Description

5.5.1. Overview

The SX1236 features a digital receiver with the analog to digital conversion process being performed directly following the LNA-Mixers block. The low-IF receiver is able to demodulate ASK, OOK, (G)FSK and (G)MSK modulation. All filtering, demodulation, gain control, synchronization and packet handling are performed digitally allowing a high degree of programmable flexibility. The receiver also has automatic gain calibration, improving the precision of RSSI measurement and enhancing image rejection.

5.5.2. Receiver Enabled and Receiver Active States

In the receiver operating mode two states of functionality are defined. Upon initial transition to receiver operating mode the receiver is in the 'receiver-enabled' state. In this state the receiver awaits for either the user defined valid preamble or RSSI detection criterion to be fulfilled. Once met the receiver enters 'receiver-active' state. In this second state the received signal is processed by the packet engine and top level sequencer. For a complete description of the digital functions of the SX1236 receiver please see section 4 of the datasheet.

5.5.3. Automatic Gain Control

The AGC feature allows receiver to handle a wide Rx input dynamic range from the sensitivity level up to maximum input level of 0dBm or more, whilst optimizing the system linearity.

The following table shows typical NF and IIP3 performances for the SX1236 LNA gains available.

Table 27 LNA Gain Control and Performances

| <i>RX</i> input level (<i>Pin</i>) | Gain Setting | <i>LnaGain</i> | Relative LNA Gain [dB] | NF Band 3/2/1 [dB] | IIP3 Band 3/2/1 [dBm] |
|---|--------------|----------------|------------------------|--------------------|-----------------------|
| Pin <= AgcThresh1 | G1 | '001' | 0 dB | 4/5.5/7 | -15/-22/-11 |
| AgcThresh1 < Pin <= AgcThresh2 | G2 | '010' | -6 dB | 6.5/8/12 | -11/-15/-6 |
| AgcThresh2 < Pin <= AgcThresh3 | G3 | '011' | -12 dB | 11/12/17 | -11/-12/0 |
| AgcThresh3 < Pin <= AgcThresh4 | G4 | '100' | -24 dB | 20/21/27 | 2/3/9 |
| AgcThresh4 < Pin <= AgcThresh5 | G5 | '110' | -26 dB | 32/33/35 | 10/10/14 |
| AgcThresh5 < Pin | G6 | '111' | -48 dB | 44/45/43 | 11/12/14 |

5.5.4. RSSI

The RSSI provides a measure of the incoming signal power at RF input port, measured within the receiver bandwidth. The signal power is available in *RssiValue*. This value is absolute in units of dBm and with a resolution of 0.5 dB. The formula below relates the register value to the absolute input signal level at the RF input port:

$$RssiValue = -2 \cdot RF \text{ level [dBm]} + RssiOffset \text{ [dB]}$$

The RSSI value can be compensated to take into account the loss in the matching network or even the gain of an additional LNA by using *RssiOffset*. The offset can be chosen in 1 dB steps from -16 to +15 dB. When compensation is applied, the effective signal strength is read as follows:

$$RSSI[dBm] = -\frac{RssiValue}{2}$$

The RSSI value is smoothed on a user defined number of measured RSSI samples. The precision of the RSSI value is related to the number of RSSI samples used. *RssiSmoothing* selects the number of RSSI samples from a minimum of 2 samples up to 256 samples in increments of power of 2. Table 28 gives the estimation of the RSSI accuracy for a 10 dB SNR and response time versus the number of RSSI samples programmed in *RssiSmoothing*.

Table 28 *RssiSmoothing* Options

| <i>RssiSmoothing</i> | Number of Samples | Estimated Accuracy | Response Time |
|----------------------|-------------------|--------------------|--|
| '000' | 2 | ± 6 dB | $\frac{2^{(RssiSmoothing+1)}}{4 \cdot Rx Bw [kHz]} [ms]$ |
| '001' | 4 | ± 5 dB | |
| '010' | 8 | ± 4 dB | |
| '011' | 16 | ± 3 dB | |
| '100' | 32 | ± 2 dB | |
| '101' | 64 | ± 1.5 dB | |
| '110' | 128 | ± 1.2 dB | |
| '111' | 256 | ± 1.1 dB | |

The RSSI is calibrated when the image and RSSI calibration process is launched.

5.5.5. Channel Filter

The role of the channel filter is to reject noise and interference outside of the wanted channel. The SX1236 channel filtering is implemented with a 16-tap finite impulse response (FIR) filter. Rejection of the filter is high enough that the filter stop-band performance is not the dominant influence on adjacent channel rejection performance. This is instead limited by the SX1236 local oscillator phase noise.

Note To respect sampling criterion in the decimation chain of the receiver, the communication bit rate cannot be set higher than twice the single side receiver bandwidth ($BitRate < 2 \times RxBw$).

The single-side channel filter bandwidth $RxBw$ is controlled by the parameters $RxBwMant$ and $RxBwExp$ in $RegRxBw$:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 2}}$$

The following channel filter bandwidths are hence accessible in the case of a 32 MHz reference oscillator:

Table 29 Available $RxBw$ Settings

| $RxBwMant$ (binary/value) | $RxBwExp$ (decimal) | $RxBw$ (kHz) |
|------------------------------|------------------------|--------------|
| | | FSK/OOK |
| 10b / 24 | 7 | 2.6 |
| 01b / 20 | 7 | 3.1 |
| 00b / 16 | 7 | 3.9 |
| 10b / 24 | 6 | 5.2 |
| 01b / 20 | 6 | 6.3 |
| 00b / 16 | 6 | 7.8 |
| 10b / 24 | 5 | 10.4 |
| 01b / 20 | 5 | 12.5 |
| 00b / 16 | 5 | 15.6 |
| 10b / 24 | 4 | 20.8 |
| 01b / 20 | 4 | 25.0 |
| 00b / 16 | 4 | 31.3 |
| 10b / 24 | 3 | 41.7 |
| 01b / 20 | 3 | 50.0 |
| 00b / 16 | 3 | 62.5 |
| 10b / 24 | 2 | 83.3 |
| 01b / 20 | 2 | 100.0 |
| 00b / 16 | 2 | 125.0 |
| 10b / 24 | 1 | 166.7 |
| 01b / 20 | 1 | 200.0 |
| 00b / 16 | 1 | 250.0 |
| Other settings | | reserved |

5.5.6. Temperature Measurement

A stand alone temperature measurement block is used in order to measure the temperature in any mode except Sleep and Standby. It is enabled by default, and can be stopped by setting *TempMonitorOff* to 1. The result of the measurement is stored in *TempValue* in *RegTemp*.

Due to process variations, the absolute accuracy of the result is $\pm 10^{\circ}\text{C}$. Higher precision requires a calibration procedure at a known temperature. The figure below shows the influence of just such a calibration process. For more information, including source code, please consult the applications section of this document.

Example temperature curve, typical device

| Correction Factor 15 | | | |
|-----------------------|---------------|------------------------------|-----------------------------|
| Actual Temp [Celsius] | RegTemp [Dec] | Temp before calibration [°C] | Temp after calibration [°C] |
| 85 | 181 | 74 | 89 |
| 75 | 190 | 65 | 80 |
| 65 | 201 | 54 | 69 |
| 55 | 211 | 44 | 59 |
| 45 | 222 | 33 | 48 |
| 35 | 232 | 23 | 38 |
| 25 | 245 | 10 | 25 |
| 15 | 0 | 0 | 15 |
| 5 | 10 | -10 | 5 |
| -5 | 21 | -21 | -6 |
| -15 | 33 | -33 | -18 |
| -25 | 44 | -44 | -29 |
| -35 | 56 | -56 | -41 |
| -40 | 63 | -63 | -48 |

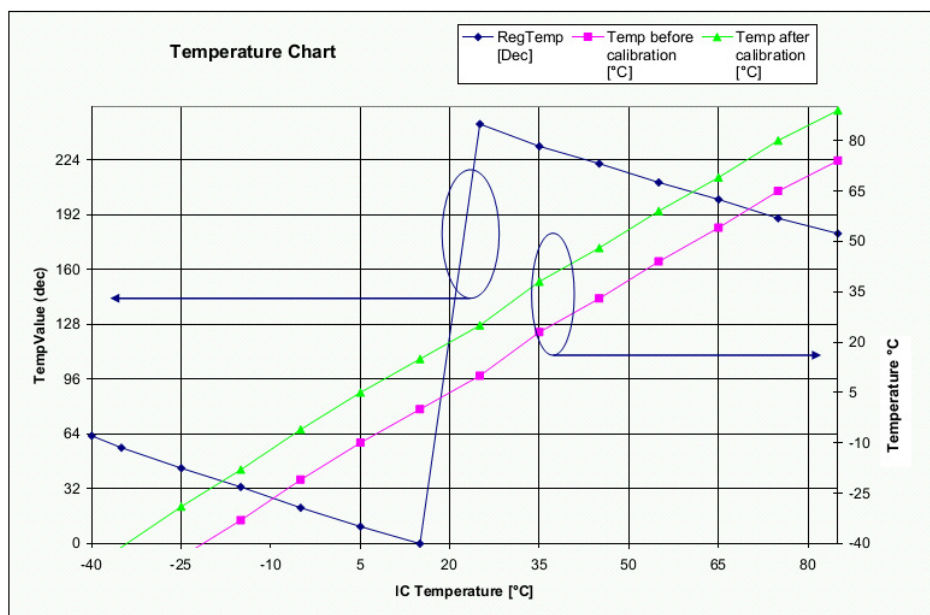


Figure 32. Temperature Sensor Response

When using the temperature sensor in the application, the following sequence should be followed:

- ◆ Set the device to Standby and wait for oscillator startup
- ◆ Set the device to FSRx mode
- ◆ Set *TempMonitorOff* = 0 (enables the sensor). It is not required to wait for the PLL Lock indication
- ◆ Wait for 140 microseconds
- ◆ Set *TempMonitorOff* = 1
- ◆ Set device back to Sleep or Standby mode
- ◆ Access temperature value in *RegTemp*

6. Description of the Registers

The following table summarises the location and function of each register.

6.1. Register Table Summary

Table 30 Registers Summary

| Address | Register Name | Reset (POR) | Description |
|---------|-------------------|-------------|---|
| | FSK/OOK Mode | | FSK Mode |
| 0x00 | RegFifo | 0x00 | FIFO read/write access |
| 0x01 | RegOpMode | 0x01 | Operating mode selection |
| 0x02 | RegBtrateMsb | 0x1A | Bit Rate setting, Most Significant Bits |
| 0x03 | RegBtrateLsb | 0x0B | Bit Rate setting, Least Significant Bits |
| 0x04 | RegFdevMsb | 0x00 | Frequency Deviation setting, Most Significant Bits |
| 0x05 | RegFdevLsb | 0x52 | Frequency Deviation setting, Least Significant Bits |
| 0x06 | RegFrfrMsb | 0x6C | RF Carrier Frequency, Most Significant Bits |
| 0x07 | RegFrfrMid | 0x80 | RF Carrier Frequency, Intermediate Bits |
| 0x08 | RegFrfrLsb | 0x00 | RF Carrier Frequency, Least Significant Bits |
| 0x09 | RegPaConfig | 0x4F | PA selection and Output Power control |
| 0x0A | RegPaRamp | 0x09 | Control of PA ramp time, low phase noise PLL |
| 0x0B | RegOcp | 0x2B | Over Current Protection control |
| 0x0C | RegLna | 0x20 | LNA settings |
| 0x0D | RegRxConfig | 0x08 | AFC, AGC, ctrl |
| 0x0E | RegRssiConfig | 0x02 | RSSI |
| 0x0F | RegRssiCollision | 0x0A | RSSI Collision detector |
| 0x10 | RegRssiThresh | 0xFF | RSSI Threshold control |
| 0x11 | RegRssiValue | n/a | RSSI value in dBm |
| 0x12 | RegRxBw | 0x15 | Channel Filter BW Control |
| 0x13 | RegAfcBw | 0x0B | AFC Channel Filter BW |
| 0x14 | RegOokPeak | 0x28 | OOK demodulator |
| 0x15 | RegOokFix | 0x0C | Threshold of the OOK demod |
| 0x16 | RegOokAvg | 0x12 | Average of the OOK demod |
| 0x17 | Reserved17 | 0x47 | - |
| 0x18 | Reserved18 | 0x32 | - |
| 0x19 | Reserved19 | 0x3E | - |
| 0x1A | RegAfcFei | 0x00 | AFC and FEI control |
| 0x1B | RegAfcMsb | 0x00 | Frequency correction value of the AFC |
| 0x1C | RegAfcLsb | 0x00 | |
| 0x1D | RegFeiMsb | 0x00 | Value of the calculated frequency error |
| 0x1E | RegFeiLsb | 0x00 | |
| 0x1F | RegPreambleDetect | 0x40 | Settings of the Preamble Detector |
| 0x20 | RegRxTimeout1 | 0x00 | Timeout Rx request and RSSI |
| 0x21 | RegRxTimeout2 | 0x00 | Timeout RSSI and <i>PayloadReady</i> |
| 0x22 | RegRxTimeout3 | 0x00 | Timeout RSSI and <i>SyncAddress</i> |
| 0x23 | RegRxDelay | 0x00 | Delay between Rx cycles |
| 0x24 | RegOsc | 0x05 | RC Oscillators Settings, CLKOUT frequency |

| Address | Register Name | Reset (POR) | Description |
|-----------|------------------|-------------|---|
| | FSK/OOK Mode | | FSK Mode |
| 0x25 | RegPreambleMsb | 0x00 | Preamble length, MSB |
| 0x26 | RegPreambleLsb | 0x03 | Preamble length, LSB |
| 0x27 | RegSyncConfig | 0x93 | Sync Word Recognition control |
| 0x28-0x2F | RegSyncValue1-8 | 0x55 | Sync Word bytes, 1 through 8 |
| 0x30 | RegPacketConfig1 | 0x90 | Packet mode settings |
| 0x31 | RegPacketConfig2 | 0x40 | Packet mode settings |
| 0x32 | RegPayloadLength | 0x40 | Payload length setting |
| 0x33 | RegNodeAdrs | 0x00 | Node address |
| 0x34 | RegBroadcastAdrs | 0x00 | Broadcast address |
| 0x35 | RegFifoThresh | 0x0F | Fifo threshold, Tx start condition |
| 0x36 | RegSeqConfig1 | 0x00 | Top level Sequencer settings |
| 0x37 | RegSeqConfig2 | 0x00 | Top level Sequencer settings |
| 0x38 | RegTimerResol | 0x00 | Timer 1 and 2 resolution control |
| 0x39 | RegTimer1Coef | 0xF5 | Timer 1 setting |
| 0x3A | RegTimer2Coef | 0x20 | Timer 2 setting |
| 0x3B | RegImageCal | 0x82 | Image calibration engine control |
| 0x3C | RegTemp | - | Temperature Sensor value |
| 0x3D | RegLowBat | 0x02 | Low Battery Indicator Settings |
| 0x3E | RegIrqFlags1 | 0x80 | Status register: PLL Lock state, Timeout, RSSI |
| 0x3F | RegIrqFlags2 | 0x40 | Status register: FIFO handling flags, Low Battery |
| 0x40 | RegDioMapping1 | 0x00 | Mapping of pins DIO0 to DIO3 |
| 0x41 | RegDioMapping2 | 0x00 | Mapping of pins DIO4 and DIO5, ClkOut frequency |
| 0x42 | RegVersion | 0x12 | Semtech ID relating the silicon revision |
| 0x44 | RegPllHop | 0x2D | Control the fast frequency hopping mode |
| 0x4B | RegTcxo | 0x09 | TCXO or XTAL input setting |
| 0x4D | RegPaDac | 0x84 | Higher power settings of the PA |
| 0x5B | RegFormerTemp | - | Stored temperature during the former IQ Calibration |
| 0x5D | RegBitRateFrac | 0x00 | Fractional part in the Bit Rate division ratio |
| 0x61 | RegAgcRef | 0x13 | Adjustment of the AGC thresholds |
| 0x62 | RegAgcThresh1 | 0x0E | |
| 0x63 | RegAgcThresh2 | 0x5B | |
| 0x64 | RegAgcThresh3 | 0xDB | |
| 0x70 | RegPll | 0xD0 | Control of the PLL bandwidth |
| others | RegTest | - | Internal test registers. Do not overwrite |

Note: Reset values are automatically refreshed in the chip at Power On Reset

6.2. Register Map

This section details the SX1236 register mapping and the precise contents of each register.

Convention: r: read, w: write, t: trigger, c: clear

Table 31 Register Map

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-------------------------------|------|--------------------|------|------------------|--|
| RegFifo (0x00) | 7-0 | Fifo | rw | 0x00 | FIFO data input/output |
| Registers for Common settings | | | | | |
| RegOpMode (0x01) | 7 | reserved | rw | 0x00 | reserved |
| | 6-5 | ModulationType | rw | 0x00 | Modulation scheme: 00 → FSK 01 → OOK 10 → 11 → reserved |
| | 4 | reserved | r | 0x0 | reserved |
| | 3 | LowFrequencyModeOn | rw | 0x01 | Access Low Frequency Mode registers (from address 0x61 on) 0 → High Frequency Mode (access to HF test registers) 1 → Low Frequency Mode (access to LF test registers) |
| | 2-0 | Mode | rw | 0x01 | Transceiver modes 000 → Sleep mode 001 → Stdby mode 010 → FS mode TX (FSTx) 011 → Transmitter mode (Tx) 100 → FS mode RX (FSRx) 101 → Receiver mode (Rx) 110 → reserved 111 → reserved |
| RegBitrateMsb (0x02) | 7-0 | BitRate(15:8) | rw | 0x1a | MSB of Bit Rate (chip rate if Manchester encoding is enabled) |
| RegBitrateLsb (0x03) | 7-0 | BitRate(7:0) | rw | 0x0b | LSB of bit rate (chip rate if Manchester encoding is enabled) $BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$ Default value: 4.8 kb/s |
| RegFdevMsb (0x04) | 7-6 | reserved | rw | 0x00 | reserved |
| | 5-0 | Fdev(13:8) | rw | 0x00 | MSB of the frequency deviation |
| RegFdevLsb (0x05) | 7-0 | Fdev(7:0) | rw | 0x52 | LSB of the frequency deviation $Fdev = Fstep \times Fdev(15,0)$ Default value: 5 kHz |
| RegFrFmsb (0x06) | 7-0 | FrF(23:16) | rw | 0x6c | MSB of the RF carrier frequency |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-------------------------------|------|-------------------|------|------------------|---|
| RegFrfMid (0x07) | 7-0 | Frf(15:8) | rw | 0x80 | MSB of the RF carrier frequency |
| RegFrfLsb (0x08) | 7-0 | Frf(7:0) | rw | 0x00 | LSB of RF carrier frequency $Frf = Fstep \times Frf(23;0)$ Default value: 434.000 MHz The RF frequency is taken into account internally only when: - entering FSRX/FSTX modes - re-starting the receiver |
| Registers for the Transmitter | | | | | |
| RegPaConfig (0x09) | 7 | PaSelect | rw | 0x00 | Selects PA output pin 0 → RFO pin. Maximum power of +14 dBm 1 → PA_BOOST pin. Maximum power of +20 dBm |
| | 6-4 | MaxPower | rw | 0x04 | Select max output power: $P_{max} = 10.8 + 0.6 \times \text{MaxPower}$ [dBm] |
| | 3-0 | OutputPower | rw | 0x0f | $P_{out} = P_{max} - (15 - \text{OutputPower})$ if PaSelect = 0 (RFO pins) $P_{out} = 17 - (15 - \text{OutputPower})$ if PaSelect = 1 (PA_BOOST pin) |
| RegPaRamp (0x0A) | 7 | unused | r | 0x00 | unused |
| | 6-5 | ModulationShaping | rw | 0x00 | Data shaping: In FSK: 00 → no shaping 01 → Gaussian filter BT = 1.0 10 → Gaussian filter BT = 0.5 11 → Gaussian filter BT = 0.3 In OOK: 00 → no shaping 01 → filtering with $f_{cutoff} = \text{bit_rate}$ 10 → filtering with $f_{cutoff} = 2 \times \text{bit_rate}$ (for $\text{bit_rate} < 125 \text{ kb/s}$) 11 → reserved |
| | 4 | reserved | rw | 0x00 | reserved |
| | 3-0 | PaRamp | rw | 0x09 | Rise/Fall time of ramp up/down in FSK 0000 → 3.4 ms 0001 → 2 ms 0010 → 1 ms 0011 → 500 us 0100 → 250 us 0101 → 125 us 0110 → 100 us 0111 → 62 us 1000 → 50 us 1001 → 40 us (d) 1010 → 31 us 1011 → 25 us 1100 → 20 us 1101 → 15 us 1110 → 12 us 1111 → 10 us |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|----------------------------|------|---------------|------|------------------|--|
| RegOcp (0x0B) | 7-6 | unused | r | 0x00 | unused |
| | 5 | OcpOn | rw | 0x01 | Enables overload current protection (OCP) for the PA: 0 → OCP disabled 1 → OCP enabled |
| | 4-0 | OcpTrim | rw | 0x0b | Trimming of OCP current: $I_{max} = 45 + 5 \cdot OcpTrim$ [mA] if $OcpTrim \leq 15$ (120 mA) / $I_{max} = -30 + 10 \cdot OcpTrim$ [mA] if $15 < OcpTrim \leq 27$ (130 to 240 mA) $I_{max} = 240$ mA for higher settings Default $I_{max} = 100$ mA |
| Registers for the Receiver | | | | | |
| RegLna (0x0C) | 7-5 | LnaGain | rw | 0x01 | LNA gain setting: 000 → reserved 001 → G1 = highest gain 010 → G2 = highest gain – 6 dB 011 → G3 = highest gain – 12 dB 100 → G4 = highest gain – 24 dB 101 → G5 = highest gain – 36 dB 110 → G6 = highest gain – 48 dB 111 → reserved Note: Reading this address always returns the current LNA gain (which may be different from what had been previously selected if AGC is enabled). |
| | 4-3 | LnaBoostLf | rw | 0x00 | Low Frequency (RFI_LF) LNA current adjustment 00 → Default LNA current Other → Reserved |
| | 2 | reserved | rw | 0x00 | reserved |
| | 1-0 | LnaBoostHf | rw | 0x00 | High Frequency (RFI_HF) LNA current adjustment 00 → Default LNA current 11 → Boost on, 150% LNA current |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|----------------------------|------|-------------------------|------|------------------|--|
| RegRxConfig (0x0d) | 7 | RestartRxOnCollision | rw | 0x00 | Turns on the mechanism restarting the receiver automatically if it gets saturated or a packet collision is detected 0 → No automatic Restart 1 → Automatic restart On |
| | 6 | RestartRxWithoutPllLock | wt | 0x00 | Triggers a manual Restart of the Receiver chain when set to 1. Use this bit when there is no frequency change, RestartRxWithPllLock otherwise. |
| | 5 | RestartRxWithPllLock | wt | 0x00 | Triggers a manual Restart of the Receiver chain when set to 1. Use this bit when there is a frequency change, requiring some time for the PLL to re-lock. |
| | 4 | AfcAutoOn | rw | 0x00 | 0 → No AFC performed at receiver startup 1 → AFC is performed at each receiver startup |
| | 3 | AgcAutoOn | rw | 0x01 | 0 → LNA gain forced by the LnaGain Setting 1 → LNA gain is controlled by the AGC |
| | 2-0 | RxTrigger | rw | 0x06 * | Selects the event triggering AGC and/or AFC at receiver startup. See Table 18 for a description. |
| RegRssiConfig (0x0e) | 7-3 | RssiOffset | rw | 0x00 | Signed RSSI offset, to compensate for the possible losses/gains in the front-end (LNA, SAW filter...) 1dB / LSB, 2's complement format |
| | 2-0 | RssiSmoothing | rw | 0x02 | Defines the number of samples taken to average the RSSI result: 000 → 2 samples used 001 → 4 samples used 010 → 8 samples used 011 → 16 samples used 100 → 32 samples used 101 → 64 samples used 110 → 128 samples used 111 → 256 samples used |
| RegRssiCollision (0x0f) | 7-0 | RssiCollisionThreshold | rw | 0x0a | Sets the threshold used to consider that an interferer is detected, witnessing a packet collision. 1dB/LSB (only RSSI increase) Default: 10dB |
| RegRssiThresh (0x10) | 7-0 | RssiThreshold | rw | 0xff | RSSI trigger level for the Rssi interrupt: - RssiThreshold / 2 [dBm] |
| RegRssiValue (0x11) | 7-0 | RssiValue | r | - | Absolute value of the RSSI in dBm, 0.5dB steps. RSSI = - RssiValue/2 [dBm] |
| RegRxBw (0x12) | 7 | unused | r | - | unused |
| | 6-5 | reserved | rw | 0x00 | reserved |
| | 4-3 | RxBwMant | rw | 0x02 | Channel filter bandwidth control: 00 → RxBwMant = 16 10 → RxBwMant = 24 01 → RxBwMant = 20 11 → reserved |
| | 2-0 | RxBwExp | rw | 0x05 | Channel filter bandwidth control |
| RegAfcBw (0x13) | 7-5 | reserved | rw | 0x00 | reserved |
| | 4-3 | RxBwMantAfc | rw | 0x01 | RxBwMant parameter used during the AFC |
| | 2-0 | RxBwExpAfc | rw | 0x03 | RxBwExp parameter used during the AFC |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|----------------------------|------|----------------------|------|----------------------|---|
| RegOokPeak (0x14) | 7-6 | reserved | rw | 0x00 | reserved |
| | 5 | BitSyncOn | rw | 0x01 | Enables the Bit Synchronizer. 0 → Bit Sync disabled (not possible in Packet mode) 1 → Bit Sync enabled |
| | 4-3 | OokThreshType | rw | 0x01 | Selects the type of threshold in the OOK data slicer: 00 → fixed threshold 10 → average mode 01 → peak mode (default) 11 → reserved |
| | 2-0 | OokPeakTheshStep | rw | 0x00 | Size of each decrement of the RSSI threshold in the OOK demodulator: 000 → 0.5 dB 001 → 1.0 dB 010 → 1.5 dB 011 → 2.0 dB 100 → 3.0 dB 101 → 4.0 dB 110 → 5.0 dB 111 → 6.0 dB |
| RegOokFix (0x15) | 7-0 | OokFixedThreshold | rw | 0x0C | Fixed threshold for the Data Slicer in OOK mode Floor threshold for the Data Slicer in OOK when Peak mode is used |
| RegOokAvg (0x16) | 7-5 | OokPeakThreshDec | rw | 0x00 | Period of decrement of the RSSI threshold in the OOK demodulator: 000 → once per chip 001 → once every 2 chips 010 → once every 4 chips 011 → once every 8 chips 100 → twice in each chip 101 → 4 times in each chip 110 → 8 times in each chip 111 → 16 times in each chip |
| | 4 | reserved | rw | 0x01 | reserved |
| | 3-2 | OokAverageOffset | rw | 0x00 | Static offset added to the threshold in average mode in order to reduce glitching activity (OOK only): 00 → 0.0 dB 10 → 4.0 dB 01 → 2.0 dB 11 → 6.0 dB |
| | 1-0 | OokAverageThreshFilt | rw | 0x02 | Filter coefficients in average mode of the OOK demodulator: 00 → $f_C \approx \text{chip rate} / 32.\pi$ 01 → $f_C \approx \text{chip rate} / 8.\pi$ 10 → $f_C \approx \text{chip rate} / 4.\pi$ 11 → $f_C \approx \text{chip rate} / 2.\pi$ |
| RegRes17 to RegRes19 | 7-0 | reserved | rw | 0x47 0x32 0x3E | reserved. Keep the Reset values. |
| RegAfcFei (0x1a) | 7-5 | unused | r | - | unused |
| | 4 | AgcStart | wt | 0x00 | Triggers an AGC sequence when set to 1. |
| | 3 | reserved | rw | 0x00 | reserved |
| | 2 | unused | - | - | unused |
| | 1 | AfcClear | wc | 0x00 | Clear AFC register set in Rx mode. Always reads 0. |
| | 0 | AfcAutoClearOn | rw | 0x00 | Only valid if AfcAutoOn is set 0 → AFC register is not cleared at the beginning of the automatic AFC phase 1 → AFC register is cleared at the beginning of the automatic AFC phase |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-----------------------------|------|----------------------|------|------------------|--|
| RegAfcMsb (0x1b) | 7-0 | AfcValue(15:8) | rw | 0x00 | MSB of the AfcValue, 2's complement format. Can be used to overwrite the current AFC value |
| RegAfcLsb (0x1c) | 7-0 | AfcValue(7:0) | rw | 0x00 | LSB of the AfcValue, 2's complement format. Can be used to overwrite the current AFC value |
| RegFeiMsb (0x1d) | 7-0 | FeiValue(15:8) | rw | - | MSB of the measured frequency offset, 2's complement. Must be read before RegFeiLsb. |
| RegFeiLsb (0x1e) | 7-0 | FeiValue(7:0) | rw | - | LSB of the measured frequency offset, 2's complement <i>Frequency error</i> = FeiValue x Fstep |
| RegPreambleDetect (0x1f) | 7 | PreambleDetectorOn | rw | 0x01 * | Enables Preamble detector when set to 1. The AGC settings supersede this bit during the startup / AGC phase. 0 → Turned off 1 → Turned on |
| | 6-5 | PreambleDetectorSize | rw | 0x01 * | Number of Preamble bytes to detect to trigger an interrupt 00 → 1 byte 10 → 3 bytes 01 → 2 bytes 11 → Reserved |
| | 4-0 | PreambleDetectorTol | rw | 0x0A * | Number or chip errors tolerated over PreambleDetectorSize. 4 chips per bit. |
| RegRxTimeout1 (0x20) | 7-0 | TimeoutRxRssi | rw | 0x00 | <i>Timeout</i> interrupt is generated $TimeoutRxRssi * 16 * T_{bit}$ after switching to Rx mode if <i>Rssi</i> interrupt doesn't occur (i.e. $RssiValue > RssiThreshold$) 0x00: <i>TimeoutRxRssi</i> is disabled |
| RegRxTimeout2 (0x21) | 7-0 | TimeoutRxPreamble | rw | 0x00 | <i>Timeout</i> interrupt is generated $TimeoutRxPreamble * 16 * T_{bit}$ after switching to Rx mode if <i>Preamble</i> interrupt doesn't occur 0x00: <i>TimeoutRxPreamble</i> is disabled |
| RegRxTimeout3 (0x22) | 7-0 | TimeoutSignalSync | rw | 0x00 | <i>Timeout</i> interrupt is generated $TimeoutSignalSync * 16 * T_{bit}$ after the Rx mode is programmed, if <i>SyncAddress</i> doesn't occur 0x00: <i>TimeoutSignalSync</i> is disabled |
| RegRxDelay (0x23) | 7-0 | InterPacketRxDelay | rw | 0x00 | Additional delay before an automatic receiver restart is launched: Delay = InterPacketRxDelay * 4 * Tbit |
| RC Oscillator registers | | | | | |
| RegOsc (0x24) | 7-4 | unused | r | - | unused |
| | 3 | RcCalStart | wt | 0x00 | Triggers the calibration of the RC oscillator when set. Always reads 0. RC calibration must be triggered in Standby mode. |
| | 2-0 | ClkOut | rw | 0x07 * | Selects CLKOUT frequency: 000 → FXOSC 001 → FXOSC / 2 010 → FXOSC / 4 011 → FXOSC / 8 100 → FXOSC / 16 101 → FXOSC / 32 110 → RC (automatically enabled) 111 → OFF |
| Packet Handling registers | | | | | |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|--------------------------|------|--------------------|------|------------------|---|
| RegPreambleMsb (0x25) | 7-0 | PreambleSize(15:8) | rw | 0x00 | Size of the preamble to be sent (from <i>TxStartCondition</i> fulfilled). (MSB byte) |
| RegPreambleLsb (0x26) | 7-0 | PreambleSize(7:0) | rw | 0x03 | Size of the preamble to be sent (from <i>TxStartCondition</i> fulfilled). (LSB byte) |
| RegSyncConfig (0x27) | 7-6 | AutoRestartRxMode | rw | 0x02 | Controls the automatic restart of the receiver after the reception of a valid packet (PayloadReady or CrcOk): 00 → Off 01 → On, without waiting for the PLL to re-lock 10 → On, wait for the PLL to lock (frequency changed) 11 → reserved |
| | 5 | PreamblePolarity | rw | 0x00 | Sets the polarity of the Preamble 0 → 0xAA (default) 1 → 0x55 |
| | 4 | SyncOn | rw | 0x01 | Enables the Sync word generation and detection: 0 → Off 1 → On |
| | 3 | reserved | rw | 0x00 | reserved |
| | 2-0 | SyncSize | rw | 0x03 | Size of the Sync word: (SyncSize + 1) bytes, (SyncSize) bytes if <i>ioHomeOn</i> =1 |
| RegSyncValue1 (0x28) | 7-0 | SyncValue(63:56) | rw | 0x01 * | 1 st byte of Sync word. (MSB byte) Used if <i>SyncOn</i> is set. |
| RegSyncValue2 (0x29) | 7-0 | SyncValue(55:48) | rw | 0x01 * | 2 nd byte of Sync word Used if <i>SyncOn</i> is set and (SyncSize + 1) >= 2. |
| RegSyncValue3 (0x2a) | 7-0 | SyncValue(47:40) | rw | 0x01 * | 3 rd byte of Sync word. Used if <i>SyncOn</i> is set and (SyncSize + 1) >= 3. |
| RegSyncValue4 (0x2b) | 7-0 | SyncValue(39:32) | rw | 0x01 * | 4 th byte of Sync word. Used if <i>SyncOn</i> is set and (SyncSize + 1) >= 4. |
| RegSyncValue5 (0x2c) | 7-0 | SyncValue(31:24) | rw | 0x01 * | 5 th byte of Sync word. Used if <i>SyncOn</i> is set and (SyncSize + 1) >= 5. |
| RegSyncValue6 (0x2d) | 7-0 | SyncValue(23:16) | rw | 0x01 * | 6 th byte of Sync word. Used if <i>SyncOn</i> is set and (SyncSize + 1) >= 6. |
| RegSyncValue7 (0x2e) | 7-0 | SyncValue(15:8) | rw | 0x01 * | 7 th byte of Sync word. Used if <i>SyncOn</i> is set and (SyncSize + 1) >= 7. |
| RegSyncValue8 (0x2f) | 7-0 | SyncValue(7:0) | rw | 0x01 * | 8 th byte of Sync word. Used if <i>SyncOn</i> is set and (SyncSize + 1) = 8. |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|----------------------------|------|---------------------|------|------------------|---|
| RegPacketConfig1 (0x30) | 7 | PacketFormat | rw | 0x01 | Defines the packet format used: 0 → Fixed length 1 → Variable length |
| | 6-5 | DcFree | rw | 0x00 | Defines DC-free encoding/decoding performed: 00 → None (Off) 01 → Manchester 10 → Whitening 11 → reserved |
| | 4 | CrcOn | rw | 0x01 | Enables CRC calculation/check (Tx/Rx): 0 → Off 1 → On |
| | 3 | CrcAutoClearOff | rw | 0x00 | Defines the behavior of the packet handler when CRC check fails: 0 → Clear FIFO and restart new packet reception. No <i>PayloadReady</i> interrupt issued. 1 → Do not clear FIFO. <i>PayloadReady</i> interrupt issued. |
| | 2-1 | AddressFiltering | rw | 0x00 | Defines address based filtering in Rx: 00 → None (Off) 01 → Address field must match <i>NodeAddress</i> 10 → Address field must match <i>NodeAddress</i> or <i>BroadcastAddress</i> 11 → reserved |
| | 0 | CrcWhiteningType | rw | 0x00 | Selects the CRC and whitening algorithms: 0 → CCITT CRC implementation with standard whitening 1 → IBM CRC implementation with alternate whitening |
| RegPacketConfig2 (0x31) | 7 | unused | r | - | unused |
| | 6 | DataMode | rw | 0x01 | Data processing mode: 0 → Continuous mode 1 → Packet mode |
| | 5 | IoHomeOn | rw | 0x00 | Enables the io-homecontrol [®] compatibility mode 0 → Disabled 1 → Enabled |
| | 4 | IoHomePowerFrame | rw | 0x00 | reserved - Linked to io-homecontrol [®] compatibility mode |
| | 3 | BeaconOn | rw | 0x00 | Enables the Beacon mode in Fixed packet format |
| | 2-0 | PayloadLength(10:8) | rw | 0x00 | Packet Length Most significant bits |
| RegPayloadLength (0x32) | 7-0 | PayloadLength(7:0) | rw | 0x40 | If PacketFormat = 0 (fixed), payload length. If PacketFormat = 1 (variable), max length in Rx, not used in Tx. |
| RegNodeAdrs (0x33) | 7-0 | NodeAddress | rw | 0x00 | Node address used in address filtering. |
| RegBroadcastAdrs (0x34) | 7-0 | BroadcastAddress | rw | 0x00 | Broadcast address used in address filtering. |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-------------------------|------|-------------------|------|------------------|--|
| RegFifoThresh (0x35) | 7 | TxStartCondition | rw | 0x01 * | Defines the condition to start packet transmission: 0 → <i>FifoLevel</i> (i.e. the number of bytes in the FIFO exceeds <i>FifoThreshold</i>) 1 → <i>FifoEmpty goes low</i> (i.e. at least one byte in the FIFO) |
| | 6 | unused | r | - | unused |
| | 5-0 | FifoThreshold | rw | 0x0f | Used to trigger <i>FifoLevel</i> interrupt, when: number of bytes in FIFO ≥ <i>FifoThreshold</i> + 1 |
| Sequencer registers | | | | | |
| RegSeqConfig1 (0x36) | 7 | SequencerStart | wt | 0x00 | Controls the top level Sequencer When set to '1', executes the "Start" transition. The sequencer can only be enabled when the chip is in Sleep or Standby mode. |
| | 6 | SequencerStop | wt | 0x00 | Forces the Sequencer Off. Always reads '0' |
| | 5 | IdleMode | rw | 0x00 | Selects chip mode during the state: 0: Standby mode 1: Sleep mode |
| | 4-3 | FromStart | rw | 0x00 | Controls the Sequencer transition when <i>SequencerStart</i> is set to 1 in Sleep or Standby mode: 00: to LowPowerSelection 01: to Receive state 10: to Transmit state 11: to Transmit state on a <i>FifoLevel</i> interrupt |
| | 2 | LowPowerSelection | rw | 0x00 | Selects the Sequencer LowPower state after a <i>LowPowerSelection</i> transition: 0: SequencerOff state with chip on Initial mode 1: Idle state with chip on <i>Standby</i> or <i>Sleep</i> mode depending on <i>IdleMode</i> <i>Note: Initial mode is the chip LowPower mode at Sequencer Start.</i> |
| | 1 | FromIdle | rw | 0x00 | Controls the Sequencer transition from the Idle state on a T1 interrupt: 0: to Transmit state 1: to Receive state |
| | 0 | FromTransmit | rw | 0x00 | Controls the Sequencer transition from the Transmit state: 0: to LowPowerSelection on a <i>PacketSent</i> interrupt 1: to Receive state on a <i>PacketSent</i> interrupt |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-------------------------|------|--------------------|------|------------------|---|
| RegSeqConfig2 (0x37) | 7-5 | FromReceive | rw | 0x00 | Controls the Sequencer transition from the Receive state 000 and 111: unused 001: to PacketReceived state on a <i>PayloadReady</i> interrupt 010: to LowPowerSelection on a <i>PayloadReady</i> interrupt 011: to PacketReceived state on a <i>CrcOk</i> interrupt (1) 100: to SequencerOff state on a <i>Rssi</i> interrupt 101: to SequencerOff state on a <i>SyncAddress</i> interrupt 110: to SequencerOff state on a <i>PreambleDetect</i> interrupt Irrespective of this setting, transition to LowPowerSelection on a T2 interrupt (1) If the CRC is wrong (corrupted packet, with CRC on but <i>CrcAutoClearOn</i> =0), the <i>PayloadReady</i> interrupt will drive the sequencer to RxTimeout state. |
| | 4-3 | FromRxTimeout | rw | 0x00 | Controls the state-machine transition from the Receive state on a <i>RxTimeout</i> interrupt (and on <i>PayloadReady</i> if FromReceive = 011): 00: to Receive State, via ReceiveRestart 01: to Transmit state 10: to LowPowerSelection 11: to SequencerOff state <i>Note: RxTimeout interrupt is a TimeoutRxRssi, TimeoutRxPreamble or TimeoutSignalSync interrupt</i> |
| | 2-0 | FromPacketReceived | rw | 0x00 | Controls the state-machine transition from the PacketReceived state: 000: to SequencerOff state 001: to Transmit state on a <i>FifoEmpty</i> interrupt 010: to LowPowerSelection 011: to Receive via FS mode, if frequency was changed 100: to Receive state (no frequency change) |
| RegTimerResol (0x38) | 7-4 | unused | r | - | unused |
| | 3-2 | Timer1Resolution | rw | 0x00 | Resolution of Timer 1 00: Timer1 disabled 01: 64 us 10: 4.1 ms 11: 262 ms |
| | 1-0 | Timer2Resolution | rw | 0x00 | Resolution of Timer 2 00: Timer2 disabled 01: 64 us 10: 4.1 ms 11: 262 ms |
| RegTimer1Coef (0x39) | 7-0 | Timer1Coefficient | rw | 0xf5 | Multiplying coefficient for Timer 1 |
| RegTimer2Coef (0x3a) | 7-0 | Timer2Coefficient | rw | 0x20 | Multiplying coefficient for Timer 2 |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-----------------------|------|-----------------|------|------------------|---|
| Service registers | | | | | |
| RegImageCal (0x3b) | 7 | AutoImageCalOn | rw | 0x00 * | Controls the Image calibration mechanism 0 → Calibration of the receiver depending on the temperature is disabled 1 → Calibration of the receiver depending on the temperature enabled. |
| | 6 | ImageCalStart | wt | - | Triggers the IQ and RSSI calibration when set in Standby mode. |
| | 5 | ImageCalRunning | r | 0x00 | Set to 1 while the Image and RSSI calibration are running. Toggles back to 0 when the process is completed |
| | 4 | unused | r | - | unused |
| | 3 | TempChange | r | 0x00 | IRQ flag witnessing a temperature change exceeding TempThreshold since the last Image and RSSI calibration: 0 → Temperature change lower than TempThreshold 1 → Temperature change greater than TempThreshold |
| | 2-1 | TempThreshold | rw | 0x01 | Temperature change threshold to trigger a new I/Q calibration 00 → 5 °C 01 → 10 °C 10 → 15 °C 11 → 20 °C |
| | 0 | TempMonitorOff | rw | 0x00 | Controls the temperature monitor operation: 0 → Temperature monitoring done in all modes except Sleep and Standby 1 → Temperature monitoring stopped. |
| RegTemp (0x3c) | 7-0 | TempValue | r | - | Measured temperature -1°C per Lsb Needs calibration for absolute accuracy |
| RegLowBat (0x3d) | 7-4 | unused | r | - | unused |
| | 3 | LowBatOn | rw | 0x00 | Low Battery detector enable signal 0 → LowBat detector disabled 1 → LowBat detector enabled |
| | 2-0 | LowBatTrim | rw | 0x02 | Trimming of the LowBat threshold: 000 → 1.695 V 001 → 1.764 V 010 → 1.835 V (d) 011 → 1.905 V 100 → 1.976 V 101 → 2.045 V 110 → 2.116 V 111 → 2.185 V |
| Status registers | | | | | |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|------------------------|------|------------------|------|------------------|---|
| RegIrqFlags1 (0x3e) | 7 | ModeReady | r | - | Set when the operation mode requested in <i>Mode</i> , is ready - Sleep: Entering Sleep mode - Standby: XO is running - FS: PLL is locked - Rx: RSSI sampling starts - Tx: PA ramp-up completed Cleared when changing the operating mode. |
| | 6 | RxReady | r | - | Set in Rx mode, after RSSI, AGC and AFC. Cleared when leaving Rx. |
| | 5 | TxReady | r | - | Set in Tx mode, after PA ramp-up. Cleared when leaving Tx. |
| | 4 | PIILock | r | - | Set (in FS, Rx or Tx) when the PLL is locked. Cleared when it is not. |
| | 3 | Rssi | rwc | - | Set in Rx when the <i>RssiValue</i> exceeds <i>RssiThreshold</i> . Cleared when leaving Rx or setting this bit to 1. |
| | 2 | Timeout | r | - | Set when a timeout occurs Cleared when leaving Rx or FIFO is emptied. |
| | 1 | PreambleDetect | rwc | - | Set when the Preamble Detector has found valid Preamble. bit clear when set to 1 |
| | 0 | SyncAddressMatch | rwc | - | Set when Sync and Address (if enabled) are detected. Cleared when leaving Rx or FIFO is emptied. This bit is read only in Packet mode, rwc in Continuous mode |
| RegIrqFlags2 (0x3f) | 7 | FifoFull | r | - | Set when FIFO is full (i.e. contains 66 bytes), else cleared. |
| | 6 | FifoEmpty | r | - | Set when FIFO is empty, and cleared when there is at least 1 byte in the FIFO. |
| | 5 | FifoLevel | r | - | Set when the number of bytes in the FIFO strictly exceeds <i>FifoThreshold</i> , else cleared. |
| | 4 | FifoOverrun | rwc | - | Set when FIFO overrun occurs. (except in Sleep mode) Flag(s) and FIFO are cleared when this bit is set. The FIFO then becomes immediately available for the next transmission / reception. |
| | 3 | PacketSent | r | - | Set in Tx when the complete packet has been sent. Cleared when exiting Tx |
| | 2 | PayloadReady | r | - | Set in Rx when the payload is ready (i.e. last byte received and CRC, if enabled and <i>CrcAutoClearOff</i> is cleared, is Ok). Cleared when FIFO is empty. |
| | 1 | CrcOk | r | - | Set in Rx when the CRC of the payload is Ok. Cleared when FIFO is empty. |
| | 0 | LowBat | rwc | - | Set when the battery voltage drops below the Low Battery threshold. Cleared only when set to 1 by the user. |
| IO control registers | | | | | |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|--------------------------|------|-------------------|------|------------------|---|
| RegDioMapping1 (0x40) | 7-6 | Dio0Mapping | rw | 0x00 | Mapping of pins DIO0 to DIO5 See Table 27 for mapping in Continuous mode See table 28 for mapping in Packet mode |
| | 5-4 | Dio1Mapping | rw | 0x00 | |
| | 3-2 | Dio2Mapping | rw | 0x00 | |
| | 1-0 | Dio3Mapping | rw | 0x00 | |
| RegDioMapping2 (0x41) | 7-6 | Dio4Mapping | rw | 0x00 | reserved. Retain default value Allows the mapping of either <i>Rssi</i> Or <i>PreambleDetect</i> to the DIO pins, as summarized on Table 27 and Table 28 0 → <i>Rssi</i> interrupt 1 → <i>PreambleDetect</i> interrupt |
| | 5-4 | Dio5Mapping | rw | 0x00 | |
| | 3-1 | reserved | rw | 0x00 | |
| | 0 | MapPreambleDetect | rw | 0x00 | |
| Version register | | | | | |
| RegVersion (0x42) | 7-0 | Version | r | 0x12 | Version code of the chip. Bits 7-4 give the full revision number; bits 3-0 give the metal mask revision number. |
| Additional registers | | | | | |
| RegPllHop (0x44) | 7 | FastHopOn | rw | 0x00 | Bypasses the main state machine for a quick frequency hop. Writing RegFrFlsb will trigger the frequency change. 0 → Frf is validated when FSTx or FSRx is requested 1 → Frf is validated triggered when RegFrFlsb is written |
| | 6-0 | reserved | rw | 0x2d | reserved |
| RegTcxo (0x4b) | 7-5 | reserved | rw | 0x00 | reserved. Retain default value |
| | 4 | TcxoInputOn | rw | 0x00 | Controls the crystal oscillator 0 → Crystal Oscillator with external Crystal 1 → External clipped sine TCXO AC-connected to XTA pin |
| | 3-0 | reserved | rw | 0x09 | Reserved. Retain default value. |
| RegPaDac (0x4d) | 7-3 | reserved | rw | 0x10 | reserved. Retain default value |
| | 2-0 | PaDac | rw | 0x04 | Enables the +20dBm option on PA_BOOST pin 0x04 → Default value 0x07 → +20dBm on PA_BOOST when OutputPower=1111 |
| RegFormerTemp (0x5b) | 7-0 | FormerTemp | rw | - | Temperature saved during the latest IQ (RSSI and Image) calibrated. Same format as <i>TempValue</i> in <i>RegTemp</i> . |
| RegBitrateFrac (0x5d) | 7-4 | unused | r | 0x00 | unused |
| | 3-0 | BitRateFrac | rw | 0x00 | Fractional part of the bit rate divider (Only valid for FSK) If <i>BitRateFrac</i> > 0 then: $BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$ |

| Name (Address) | Bits | Variable Name | Mode | Default value | FSK/OOK Description |
|-------------------------|------|-------------------|------|------------------|---|
| RegAgcRef (0x61) | 7-6 | unused | r | - | unused |
| | 5-0 | AgcReferenceLevel | rw | 0x19 | Sets the floor reference for all AGC thresholds: AGC Reference[dBm]= $-174\text{dBm} + 10 \cdot \log(2 \cdot RxBw) + \text{SNR} + \text{AgcReferenceLevel}$ SNR = 8dB, fixed value |
| RegAgcThresh1 (0x62) | 7-5 | unused | r | - | unused |
| | 4-0 | AgcStep1 | rw | 0x0c | Defines the 1st AGC Threshold |
| RegAgcThresh2 (0x63) | 7-4 | AgcStep2 | rw | 0x04 | Defines the 2nd AGC Threshold: |
| | 3-0 | AgcStep3 | rw | 0x0b | Defines the 3rd AGC Threshold: |
| RegAgcThresh3 (0x64) | 7-4 | AgcStep4 | rw | 0x0c | Defines the 4th AGC Threshold: |
| | 3-0 | AgcStep5 | rw | 0x0c | Defines the 5th AGC Threshold: |

6.3. Band Specific Additional Registers

The registers in the address space from 0x61 to 0x73 are specific for operation in the lower frequency bands (below 525 MHz), or in the upper frequency bands (above 860 MHz). Their programmed value may differ, and are retained when switching from lower to high frequency and vice-versa. The access to the band specific registers is granted by enabling or disabling the bit 3 *LowFrequencyModeOn* of the *RegOpMode* register. By default, the bit *LowFrequencyModeOn* is at '1' indicating that the registers are configured for the low frequency band.

Table 32 Low Frequency Additional Registers

| Name (Address) | Bits | Variable Name | Mode | Default value | Low Frequency Additional Registers |
|---------------------------|------|-------------------|------|------------------|---|
| RegAgcRefLf (0x61) | 7-6 | unused | r | - | unused |
| | 5-0 | AgcReferenceLevel | rw | 0x19 | Sets the floor reference for all AGC thresholds: AGC Reference[dBm]= $-174\text{dBm} + 10 \cdot \log(2 \cdot RxBw) + \text{SNR} + \text{AgcReferenceLevel}$ SNR = 8dB, fixed value |
| RegAgcThresh1Lf (0x62) | 7-5 | unused | r | - | unused |
| | 4-0 | AgcStep1 | rw | 0x0c | Defines the 1st AGC Threshold |
| RegAgcThresh2Lf (0x63) | 7-4 | AgcStep2 | rw | 0x04 | Defines the 2nd AGC Threshold: |
| | 3-0 | AgcStep3 | rw | 0x0b | Defines the 3rd AGC Threshold: |
| RegAgcThresh3Lf (0x64) | 7-4 | AgcStep4 | rw | 0x0c | Defines the 4th AGC Threshold: |
| | 3-0 | AgcStep5 | rw | 0x0c | Defines the 5th AGC Threshold: |
| RegPllLf (0x70) | 7-6 | PllBandwidth | rw | 0x03 | Controls the PLL bandwidth: 00 → 75 kHz 10 → 225 kHz 01 → 150 kHz 11 → 300 kHz |
| | 5-0 | reserved | rw | 0x10 | reserved. Retain default value |

Table 33 High Frequency Additional Registers

| Name (Address) | Bits | Variable Name | Mode | Default value | Low Frequency Additional Registers |
|---------------------------|------|-------------------|------|------------------|---|
| RegAgcRefHf (0x61) | 7-6 | unused | r | - | unused |
| | 5-0 | AgcReferenceLevel | rw | 0x1c | Sets the floor reference for all AGC thresholds: AGC Reference[dBm]= $-174\text{dBm} + 10 \cdot \log(2 \cdot RxBw) + \text{SNR} + \text{AgcReferenceLevel}$ SNR = 8dB, fixed value |
| RegAgcThresh1Hf (0x62) | 7-5 | unused | r | - | unused |
| | 4-0 | AgcStep1 | rw | 0x0e | Defines the 1st AGC Threshold |
| RegAgcThresh2Hf (0x63) | 7-4 | AgcStep2 | rw | 0x05 | Defines the 2nd AGC Threshold: |
| | 3-0 | AgcStep3 | rw | 0x0b | Defines the 3rd AGC Threshold: |
| RegAgcThresh3Hf (0x64) | 7-4 | AgcStep4 | rw | 0x0c | Defines the 4th AGC Threshold: |
| | 3-0 | AgcStep5 | rw | 0x0c | Defines the 5th AGC Threshold: |
| RegPllHf (0x70) | 7-6 | PllBandwidth | rw | 0x03 | Controls the PLL bandwidth: 00 → 75 kHz 10 → 225 kHz 01 → 150 kHz 11 → 300 kHz |
| | 5-0 | reserved | rw | 0x10 | reserved. Retain default value |

7. Application Information

7.1. Crystal Resonator Specification

Table 34 shows the crystal resonator specification for the crystal reference oscillator circuit of the SX1236. This specification covers the full range of operation of the SX1236 and is employed in the reference design.

Table 34 Crystal Specification

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|--------|---------------------------|-------------------------|-----|-----|-----|------|
| FXOSC | XTAL Frequency | | - | 32 | - | MHz |
| RS | XTAL Serial Resistance | | - | 15 | 100 | ohms |
| C0 | XTAL Shunt Capacitance | | - | 1 | 3 | pF |
| CFOOT | External Foot Capacitance | On each pin XTA and XTB | 10 | 15 | 22 | pF |
| CLOAD | Crystal Load Capacitance | | 6 | - | 12 | pF |

- Notes**
- The initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.
 - The loading capacitance should be applied externally, and adapted to the actual Cload specification of the XTAL.

7.2. Reset of the Chip

A power-on reset of the SX1236 is triggered at power up. Additionally, a manual reset can be issued by controlling pin 7.

7.2.1. POR

If the application requires the disconnection of VDD from the SX1236, despite of the extremely low Sleep Mode current, the user should wait for 10 ms from the end of the POR cycle before commencing communications over the SPI bus. Pin 7 (NRESET) should be left floating during the POR sequence.

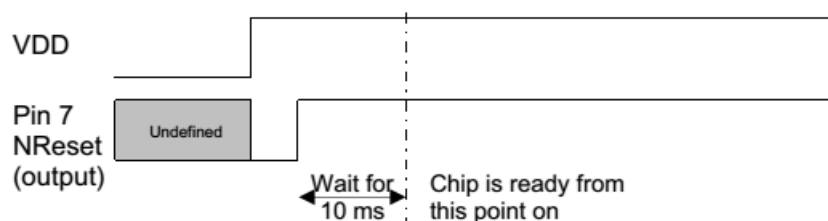


Figure 33. POR Timing Diagram

Please note that any CLKOUT activity can also be used to detect that the chip is ready.

7.2.2. Manual Reset

A manual reset of the SX1236 is possible even for applications in which VDD cannot be physically disconnected. Pin 7 should be pulled low for a hundred microseconds, and then released. The user should then wait for 5 ms before using the chip.

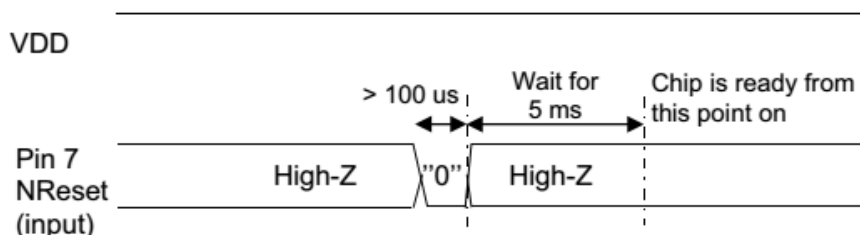


Figure 34. Manual Reset Timing Diagram

Note Whilst pin 7 is driven low, an over current consumption of up to one milliampere can be seen on VDD.

7.3. Top Sequencer: Listen Mode Examples

In this scenario, the circuit spends most of the time in Idle mode, during which only the RC oscillator is on. Periodically the receiver wakes up and looks for incoming signal. If a wanted signal is detected, the receiver is kept on and data are analyzed. Otherwise, if there was no wanted signal for a defined period of time, the receiver is switched off until the next receive period.

During Listen mode, the Radio stays most of the time in a Low Power mode, resulting in very low average power consumption. The general timing diagram of this scenario is given in Figure 35.

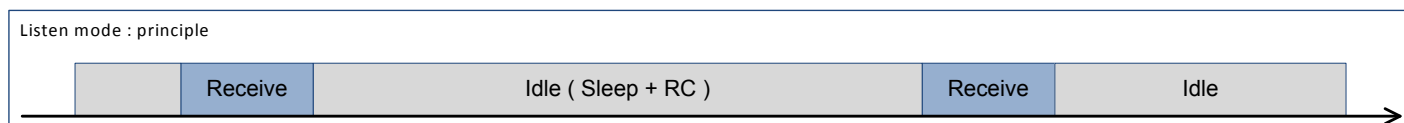


Figure 35. Listen Mode: Principle

An interrupt request is generated on a packet reception. The user can then take appropriate action.

Depending on the application and environment, there are several ways to implement Listen mode:

- ◆ Wake on a *PreambleDetect* interrupt
- ◆ Wake on a *SyncAddress* interrupt
- ◆ Wake on a *PayloadReady* interrupt

7.3.1. Wake on Preamble Interrupt

In one possible scenario, the sequencer polls for a Preamble detection. If a preamble signal is detected, the sequencer is switched off and the circuit stays in Receive mode until the user switches modes. Otherwise, the receiver is switched off until the next Rx period.

7.3.1.1. Timing Diagram

When no signal is received, the circuit wakes every $\text{Timer1} + \text{Timer2}$ and switches to Receive mode for a time defined by Timer2 , as shown on the following diagram. If no Preamble is detected, it then switches back to Idle mode, i.e. Sleep mode with RC oscillator on.

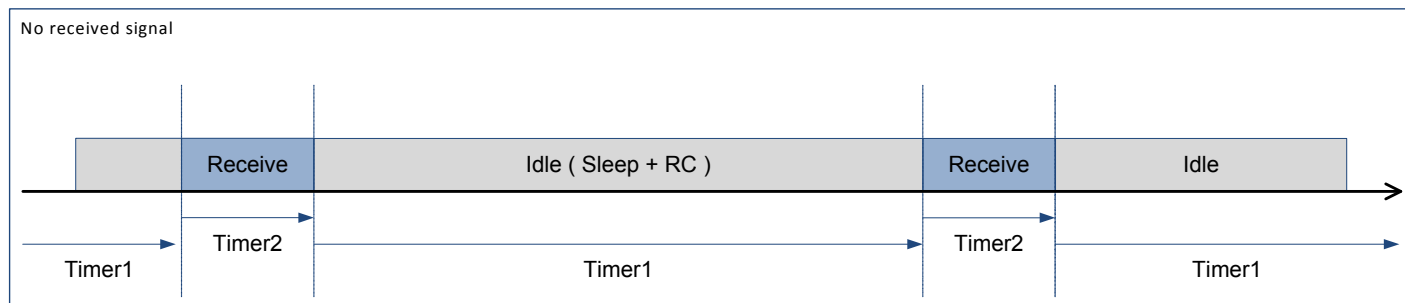


Figure 36. Listen Mode with No Preamble Received

If a Preamble signal is detected, the Sequencer is switched off. The *PreambleDetect* signal can be mapped to DIO4, in order to request the user's attention. The user can then take appropriate action.

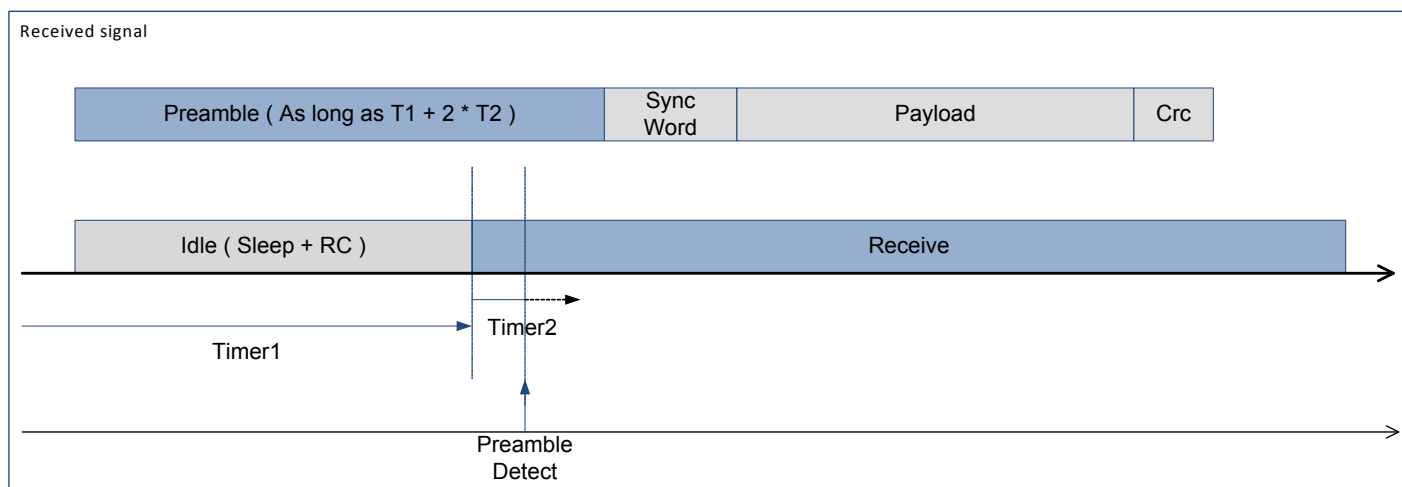


Figure 37. Listen Mode with Preamble Received

7.3.1.2. Sequencer Configuration

The following graph shows Listen mode - Wake on *PreambleDetect* state machine:

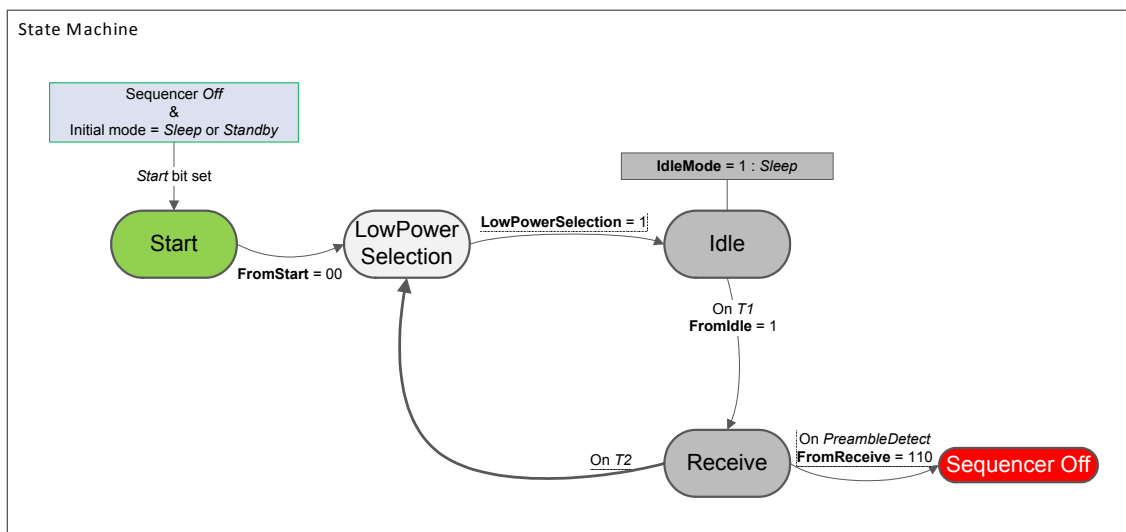


Figure 38. Wake On PreambleDetect State Machine

This example configuration is achieved as follows:

Table 35 Listen Mode with PreambleDetect Condition Settings

| Variable | Effect |
|-------------------|---|
| IdleMode | 1: Sleep mode |
| FromStart | 00: To LowPowerSelection |
| LowPowerSelection | 1: To Idle state |
| FromIdle | 1: To Receive state on <i>T1</i> interrupt |
| FromReceive | 110: To Sequencer Off on <i>PreambleDetect</i> interrupt |

T_{Timer2} defines the maximum duration the chip stays in Receive mode as long as no Preamble is detected. In order to optimize power consumption, Timer2 must be set just long enough for Preamble detection.

$T_{Timer1} + T_{Timer2}$ defines the cycling period, i.e. time between two Preamble polling starts. In order to optimize average power consumption, Timer1 should be relatively long. However, increasing Timer1 also extends packet reception duration.

In order to insure packet detection and optimize the receiver's power consumption, the received packet Preamble should be as long as $T_{Timer1} + 2 \times T_{Timer2}$.

An example of DIO configuration for this mode is described in the following table:

Table 36 Listen Mode with PreambleDetect Condition Recommended DIO Mapping

| DIO | Value | Description |
|-----|-------|--|
| 0 | 01 | CrcOk |
| 1 | 00 | FifoLevel |
| 3 | 00 | FifoEmpty |
| 4 | 11 | PreambleDetect – Note: <i>MapPreambleDetect</i> bit should be set. |

7.3.2. Wake on SyncAddress Interrupt

In another possible scenario, the sequencer polls for a Preamble detection and then for a valid *SyncAddress* interrupt. If events occur, the sequencer is switched off and the circuit stays in Receive mode until the user switches modes. Otherwise, the receiver is switched off until the next Rx period.

7.3.2.1. Timing Diagram

Most of the sequencer running time is spent while no wanted signal is received. As shown by the timing diagram in Figure 39, the circuit wakes periodically for a short time, defined by *RxTimeout*. The circuit is in a Low Power mode for the rest of *Timer1* + *Timer2* (i.e. *Timer1* + *Timer2* - *TrxTimeout*)

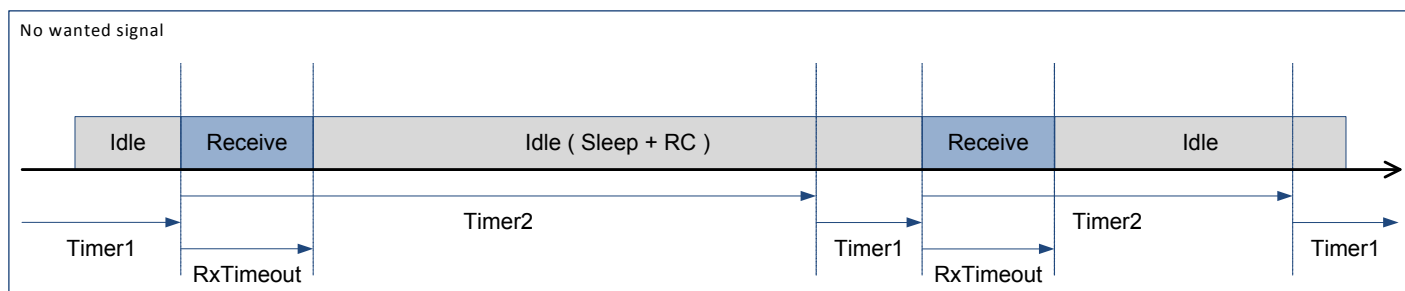


Figure 39. Listen Mode with no SyncAddress Detected

If a preamble is detected before *RxTimeout* timer ends, the circuit stays in Receive mode and waits for a valid *SyncAddress* detection. If none is detected by the end of *Timer2*, Receive mode is deactivated and the polling cycle resumes, without any user intervention.

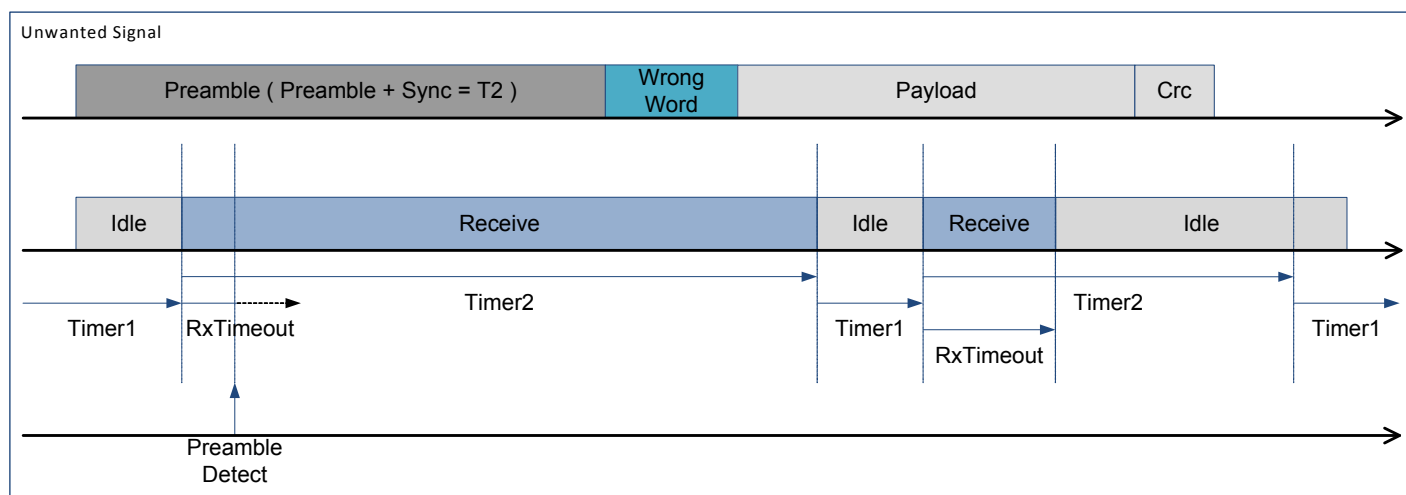


Figure 40. Listen Mode with Preamble Received and no SyncAddress

But if a valid Sync Word is detected, a *SyncAddress* interrupt is fired, the Sequencer is switched off and the circuit stays in Receive mode as long as the user doesn't switch modes.

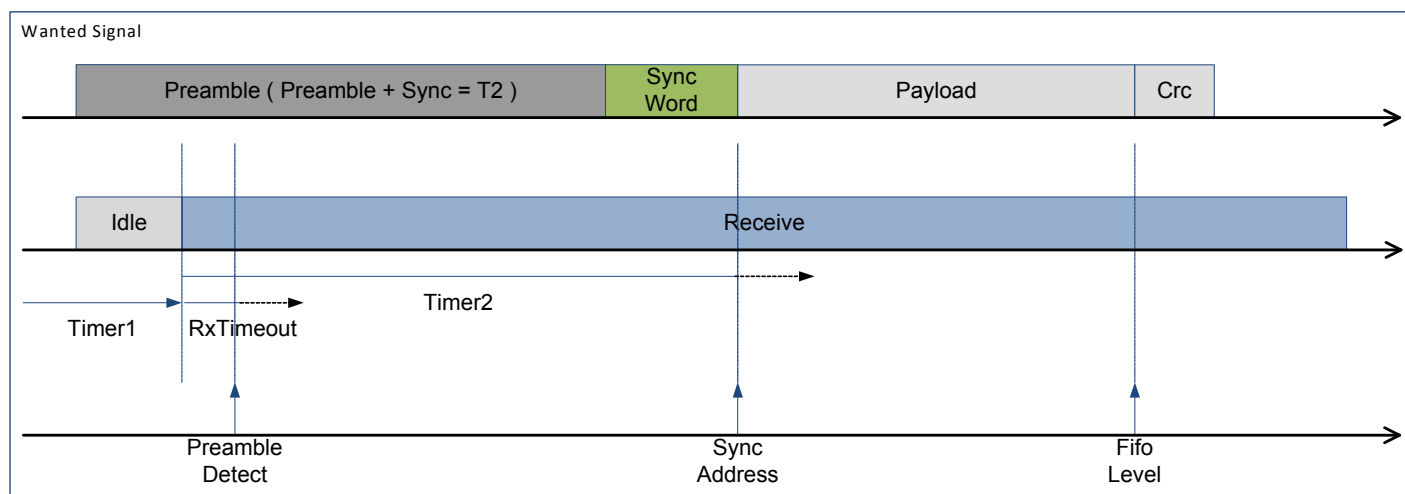


Figure 41. Listen Mode with Preamble Received & Valid SyncAddress

7.3.2.2. Sequencer Configuration

The following graph shows Listen mode - Wake on SyncAddress state machine:

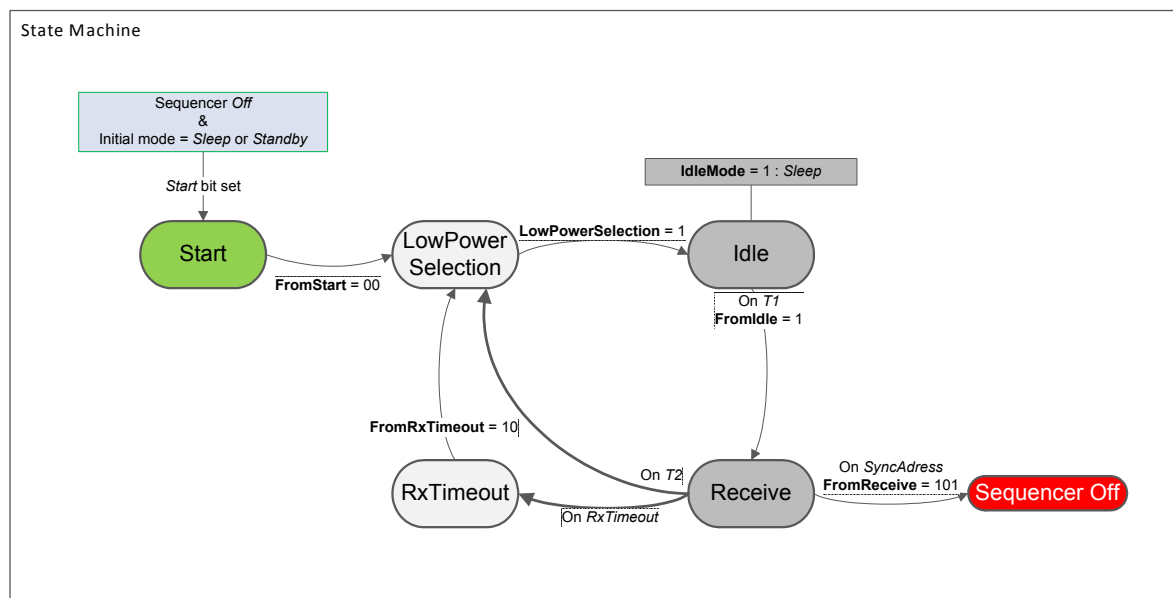


Figure 42. Wake On SyncAddress State Machine

This example configuration is achieved as follows:

Table 37 *Listen Mode with SyncAddress Condition Settings*

| Variable | Effect |
|-------------------|--|
| IdleMode | 1: Sleep mode |
| FromStart | 00: To LowPowerSelection |
| LowPowerSelection | 1: To Idle state |
| FromIdle | 1: To Receive state on <i>T1</i> interrupt |
| FromReceive | 101: To Sequencer off on <i>SyncAddress</i> interrupt |
| FromRxTimeout | 10: To LowPowerSelection |

$T_{\text{TimeoutRxPreamble}}$ should be set to just long enough to catch a preamble (depends on *PreambleDetectSize* and *BitRate*).

T_{Timer1} should be set to 64 μs (shortest possible duration).

T_{Timer2} is set so that $T_{\text{Timer1}} + T_{\text{Timer2}}$ defines the time between two starts of reception.

In order to insure packet detection and optimize the receiver power consumption, the received packet Preamble should be defined so that $T_{\text{Preamble}} = T_{\text{Timer2}} - T_{\text{SyncAddress}}$ with $T_{\text{SyncAddress}} = (\text{SyncSize} + 1) * 8 / \text{BitRate}$.

An example of DIO configuration for this mode is described in the following table:

Table 38 *Listen Mode with PreambleDetect Condition Recommended DIO Mapping*

| DIO | Value | Description |
|-----|-------|--|
| 0 | 01 | CrcOk |
| 1 | 00 | FifoLevel |
| 2 | 11 | SyncAddress |
| 3 | 00 | FifoEmpty |
| 4 | 11 | PreambleDetect – Note: <i>MapPreambleDetect</i> bit should be set. |

7.4. Top Sequencer: Beacon Mode

In this mode, a repetitive message is transmitted periodically. If the Payload being sent is always identical, and *PayloadLength* is smaller than the FIFO size, the use of the *BeaconOn* bit in *RegPacketConfig2* together with the Sequencer permit to achieve periodic beacon without any user intervention.

7.4.1. Timing diagram

In this mode, the Radio is switched to Transmit mode every $T_{\text{Timer1}} + T_{\text{Timer2}}$ and back to Idle mode after *PacketSent*, as shown in the diagram below. The Sequencer insures minimal time is spent in Transmit mode, and therefore power consumption is optimized.

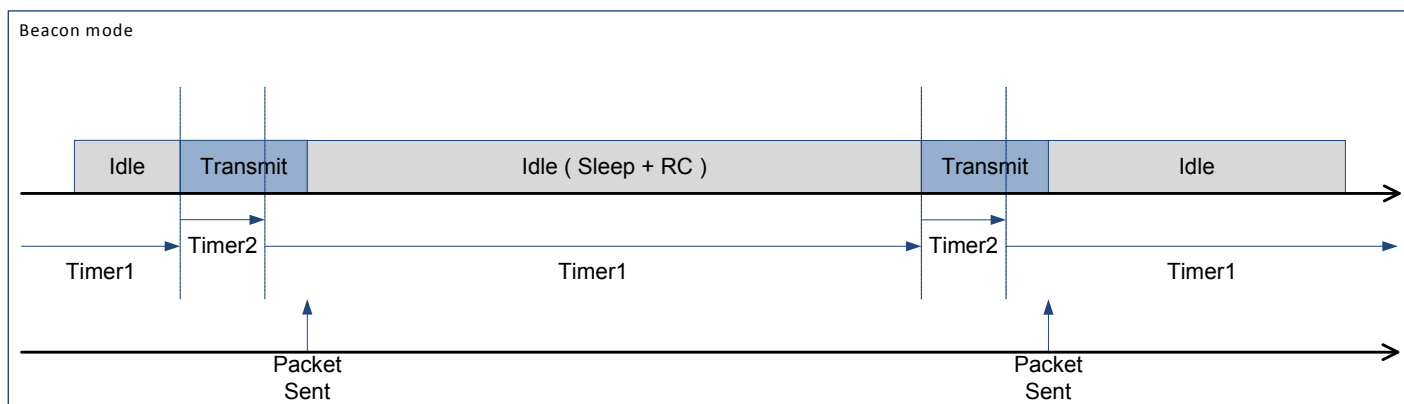


Figure 43. Beacon Mode Timing Diagram

7.4.2. Sequencer Configuration

The Beacon mode state machine is presented in the following graph. It is noticeable that the sequencer enters an infinite loop and can only be stopped by setting *SequencerStop* bit in *RegSeqConfig1*.

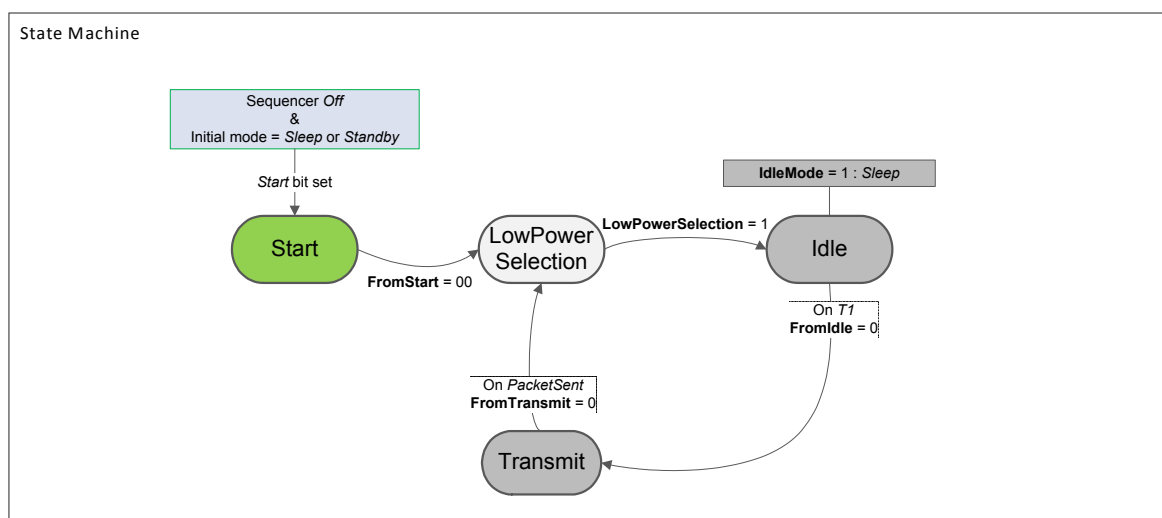


Figure 44. Beacon Mode State Machine

This example is achieved by programming the Sequencer as follows:

Table 39 Beacon Mode Settings

| Variable | Effect |
|-------------------|---|
| IdleMode | 1: Sleep mode |
| FromStart | 00: To LowPowerSelection |
| LowPowerSelection | 1: To Idle state |
| FromIdle | 0: To Transmit state on <i>T1</i> interrupt |
| FromTransmit | 0: To LowPowerSelection on <i>PacketSent</i> interrupt |

$T_{\text{Timer1}} + T_{\text{Timer2}}$ define the time between the start of two transmissions.

7.5. Example CRC Calculation

The following routine(s) may be implemented to mimic the CRC calculation of the SX1236:

```

1 // CRC types
2 #define CRC_TYPE_CCITT 0
3 #define CRC_TYPE_IBM 1
4
5 // Polynomial = X^16 + X^12 + X^5 + 1
6 #define POLYNOMIAL_CCITT 0x1021
7 // Polynomial = X^16 + X^15 + X^2 + 1
8 #define POLYNOMIAL_IBM 0x8005
9
10 // Seeds
11 #define CRC_IBM_SEED 0xFFFF
12 #define CRC_CCITT_SEED 0x1D0F
13
14 /*
15  * CRC algorithm implementation
16  *
17  * \param[IN] crc Previous CRC value
18  * \param[IN] data New data to be added to the CRC
19  * \param[IN] polynomial CRC polynomial selection [CRC_TYPE_CCITT, CRC_TYPE_IBM]
20  *
21  * \retval crc New computed CRC
22  */
23 U16 ComputeCrc( U16 crc, U8 data, U16 polynomial )
24 {
25     U8 i;
26     for( i = 0; i < 8; i++ )
27     {
28         if( ( ( crc & 0x8000 ) >> 8 ) ^ ( data & 0x80 ) ) != 0 )
29         {
30             crc <<= 1; // shift left once
31             crc ^= polynomial; // XOR with polynomial
32         }
33         else
34         {
35             crc <<= 1; // shift left once
36         }
37         data <<= 1; // Next data bit
38     }
39     return crc;
40 }
41
42 /*
43  * CRC algorithm implementation
44  *
45  * \param[IN] buffer Array containing the data
46  * \param[IN] bufferLength Buffer length
47  * \param[IN] crcType Selects the CRC polynomial[CRC_TYPE_CCITT, CRC_TYPE_IBM]
48  *
49  * \retval crc Buffer computed CRC
50  */
51 U16 RadioPacketComputeCrc( U8 *buffer, U8 bufferLength, U8 crcType )
52 {
53     U8 i;
54     U16 crc;
55     U16 polynomial;
56
57     polynomial = ( crcType == CRC_TYPE_IBM ) ? POLYNOMIAL_IBM : POLYNOMIAL_CCITT;
58     crc = ( crcType == CRC_TYPE_IBM ) ? CRC_IBM_SEED : CRC_CCITT_SEED;
59
60     for( i = 0; i < bufferLength; i++ )
61     {
62         crc = ComputeCrc( crc, buffer[i], polynomial );
63     }
64
65     if( crcType == CRC_TYPE_IBM )
66     {
67         return crc;
68     }
69     else
70     {
71         return ( U16 ) ( ~crc );
72     }
73 }

```

Figure 45. Example CRC Code

7.6. Example Temperature Reading

The following routine(s) may be implemented to read the temperature and calibrate the sensor:

```

1  Temperature.c
2  /*!
3   * Reads the raw temperature
4   * \retval temperature New raw temperature reading in 2's complement format
5   */
6  S8 RadioGetRawTemp( void )
7  {
8      int8_t temp = 0;
9      uint8_t previousOpMode;
10
11      // Save current Operation Mode
12      SX1276Read( REG_OPMODE, &SX1276->RegOpMode );
13      previousOpMode = SX1276->RegOpMode;
14
15      // Pass through LoRa sleep only necessary if reading temperature while in LoRa Mode
16      if( ( previousOpMode & RFLR_OPMODE_LONGRANGEMODE_ON ) == RFLR_OPMODE_LONGRANGEMODE_ON )
17      {
18          SX1276->RegOpMode = RFLR_OPMODE_SLEEP;
19          SX1276Write( REG_OPMODE, SX1276->RegOpMode ); // put device in LoRa Sleep Mode
20      }
21
22      // Put device in FSK Sleep Mode
23      SX1276->RegOpMode = RF_OPMODE_SLEEP;
24      SX1276Write( REG_OPMODE, SX1276->RegOpMode );
25      // Put device in FSK RxSynth
26      SX1276->RegOpMode = RF_OPMODE_SYNTHESIZER_RX;
27      SX1276Write( REG_OPMODE, SX1276->RegOpMode );
28      // Enable Temperature reading
29      SX1276Read( REG_IMAGECAL, &SX1276->RegImageCal );
30      SX1276->RegImageCal = ( SX1276->RegImageCal & RF_IMAGECAL_TEMPMONITOR_MASK ) | RF_IMAGECAL_TEMPMONITOR_ON;
31      SX1276Write( REG_IMAGECAL, SX1276->RegImageCal );
32
33      // Wait 150us
34      Delay( 150 );
35
36      // Disable Temperature reading
37      SX1276Read( REG_IMAGECAL, &SX1276->RegImageCal );
38      SX1276->RegImageCal = ( SX1276->RegImageCal & RF_IMAGECAL_TEMPMONITOR_MASK ) | RF_IMAGECAL_TEMPMONITOR_OFF;
39      SX1276Write( REG_IMAGECAL, SX1276->RegImageCal );
40
41      // Put device in FSK Sleep Mode
42      SX1276->RegOpMode = RF_OPMODE_SLEEP;
43      SX1276Write( REG_OPMODE, SX1276->RegOpMode );
44
45      // Read temperature
46      SX1276Read( REG_TEMP, &SX1276->RegTemp );
47
48      if( ( SX1276->RegTemp & 0x80 ) == 0x80 )
49      {
50          temp = 255 - SX1276->RegTemp;
51      }
52      else
53      {
54          temp = SX1276->RegTemp;
55          temp *= -1;
56      }
57
58      // We were in LoRa Mode prior to the temperature reading
59      if( ( previousOpMode & RFLR_OPMODE_LONGRANGEMODE_ON ) == RFLR_OPMODE_LONGRANGEMODE_ON )
60      {
61          SX1276->RegOpMode = RFLR_OPMODE_SLEEP;
62          SX1276Write( REG_OPMODE, SX1276->RegOpMode ); // put device in LoRa Sleep Mode
63      }
64
65      // Reload previous Op Mode
66      SX1276Write( REG_OPMODE, previousOpMode );
67      return temp;
68  }

```

Figure 46. Example Temperature Reading

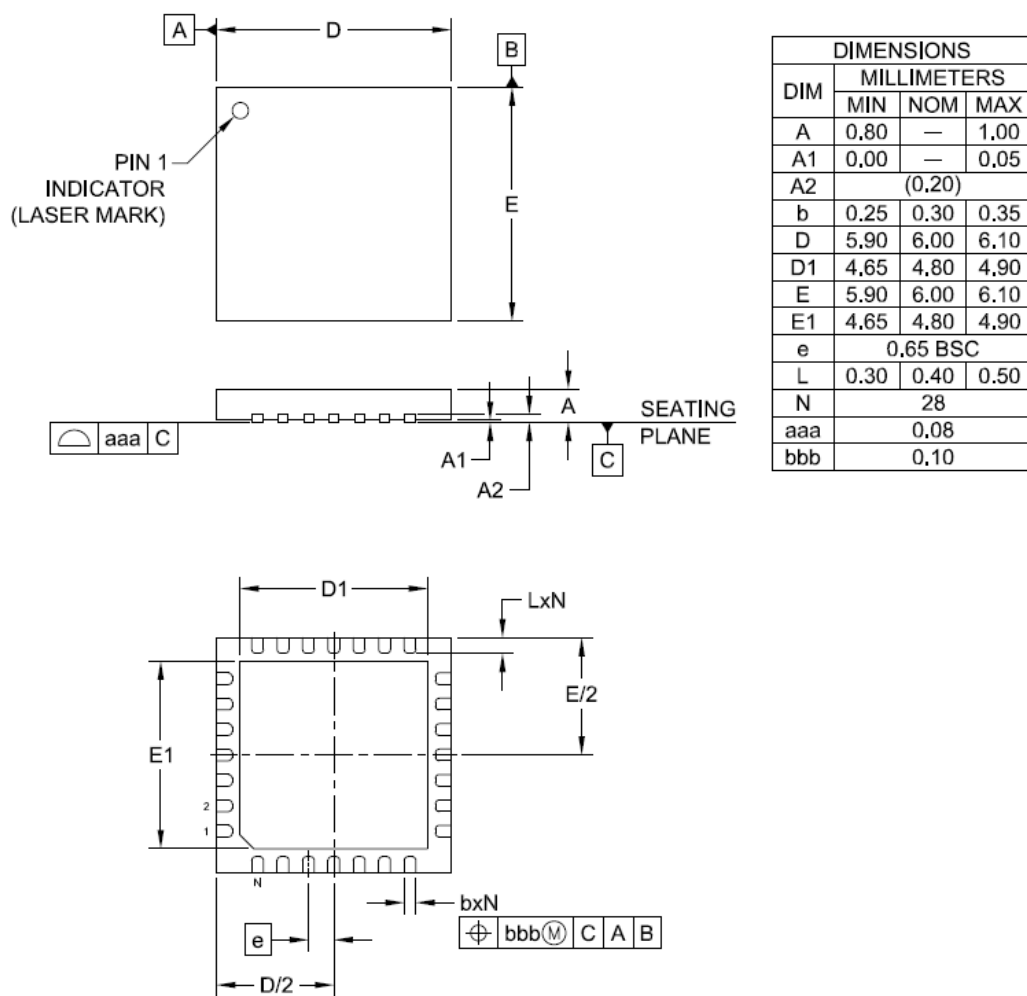
```
68
69  /*!
70   * Computes the temperature compensation factor
71   * \param [IN] actualTemp Actual temperature measured by an external device
72   * \retval compensationFactor Computed compensation factor
73   */
74  S8 RadioCalibreateTemp( S8 actualTemp )
75  {
76      return actualTemp - RadioGetRawTemp( );
77  }
78
79  /*!
80   * Gets the actual compensated temperature
81   * \param [IN] compensationFactor Return value of the calibration function
82   * \retval New compensated temperature value
83   */
84  S8 RadioGetTemp( S8 compensationFactor )
85  {
86      return RadioGetRawTemp( ) + compensationFactor;
87  }
88
89  /*!
90   * Usage example
91   */
92  void main( void )
93  {
94      S8 temp;
95      S8 actualTemp = 0;
96      S8 compensationFactor = 0;
97
98      // Ask user for the temperature during calibration
99      actualTemp = AskUserTemperature( );
100      compensationFactor = RadioCalibreateTemp( actualTemp );
101
102      while( True )
103      {
104          temp = RadioGetTemp( compensationFactor );
105      }
106  }
```

Figure 47. Example Temperature Reading (continued)

8. Packaging Information

8.1. Package Outline Drawing

The SX1236 is available in a 28-lead QFN package as shown in Figure 48.

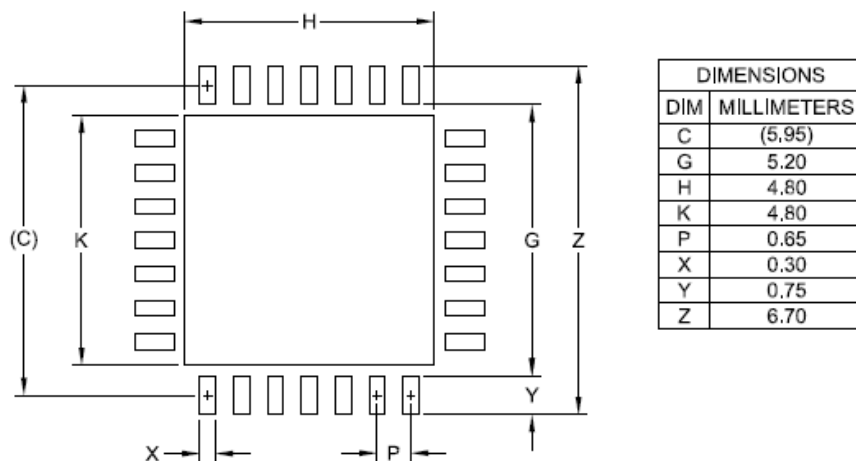


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 48. Package Outline Drawing

8.2. Recommended Land Pattern



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH "X" AND "Y" DIRECTIONS.

Figure 49. Recommended Land Pattern

8.3. Tape & Reel Information

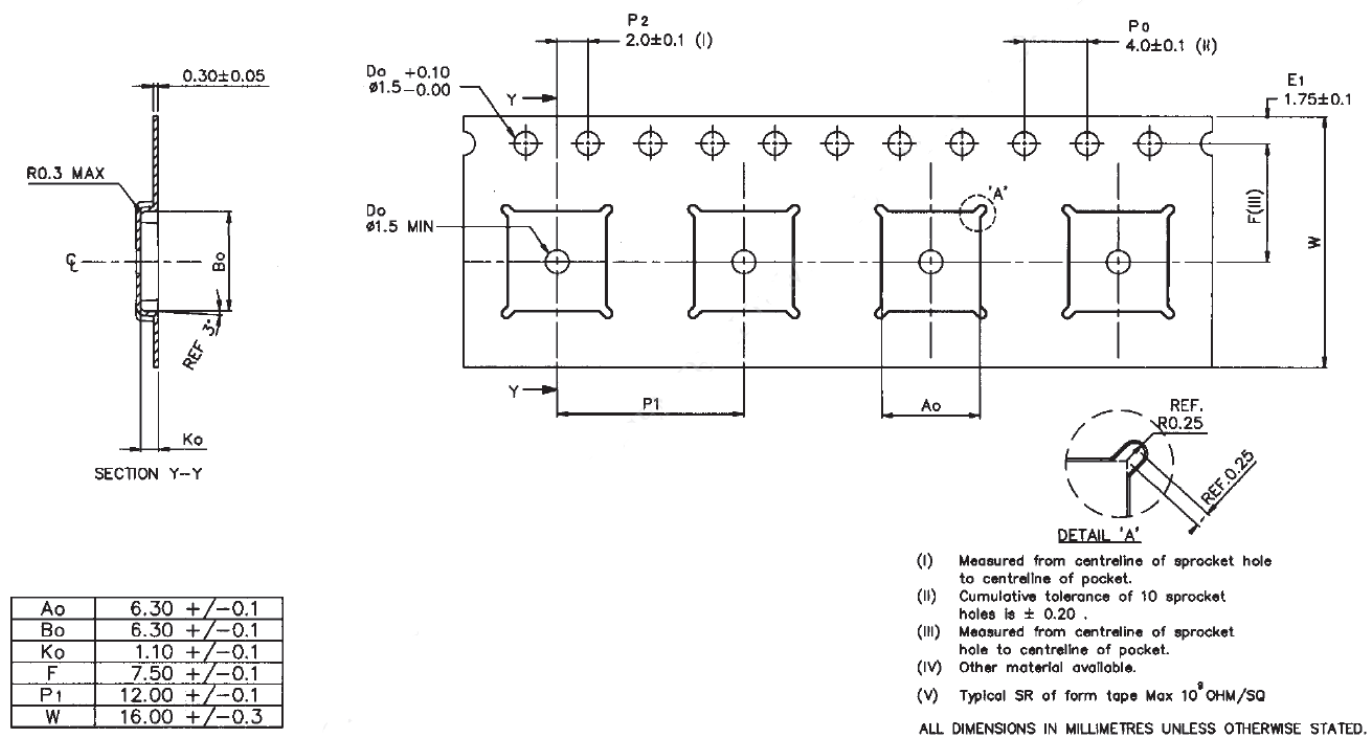


Figure 50. Tape and Reel Information

9. Revision History

Table 40 Revision History

| Revision | Date | Comment |
|----------|----------|---------------------|
| 1 | Dec 2013 | First FINAL Release |

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