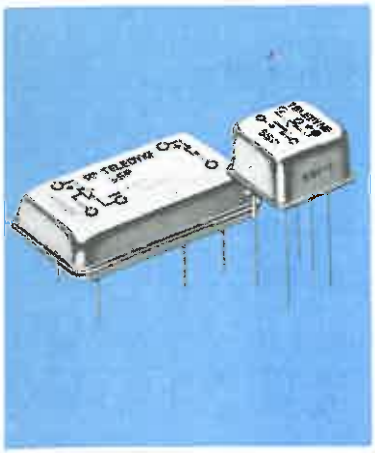


TELEDYNE SOLID STATE

MILITARY POWER FET AC/DC SOLID STATE RELAY

OPTICALLY ISOLATED UP TO 1.3 AMP AT 25°C

SERIES
685
686
690
691
RADIATION TESTED
SPST/NO

FEATURES

- DC or AC/DC units available
- Surge blocking voltage of 80 volts peak (per MIL-704)
- Power FET output
- Fast switching speed
- Low on-resistance (0.3 ohms typ.)
- Virtually no offset voltage
- Opto isolation up to 1200 volts
- Input CMOS or TTL compatible
- 3.8 to 32.0 volt input range (Table 1)
- Constant current input in TTL mode
- Schmitt trigger input in buffered mode at 50 microamps
- Built and tested to MIL-R-28750 utilizing the test methods of MIL-STD-883C
- Radiation hardening levels: contact factory

APPLICATIONS

- Low level switching applications
- Isolated line drivers
- Current loop switches
- Servo and synchro resolver control
- Load control from microcomputer I/O ports
- Data coupler
- General purpose analog and transducer signal switching in military/aerospace applications
- Telecommunications

DESCRIPTION

These all solid state relays utilize the latest power FET output technology to minimize on-state resistance and bipolar offset voltages normally associated with solid state relay outputs. The input and output are optically isolated to protect delicate input logic circuits from output voltage transients. The input is buffered to enable the relay to be driven directly by CMOS logic gates or standard interface circuitry. A Schmitt trigger at the input significantly increases noise margin when using the relay in the CMOS input mode. This prevents false triggering in noisy environments. State-of-the-art construction techniques maximizes MTBF and minimizes package size.

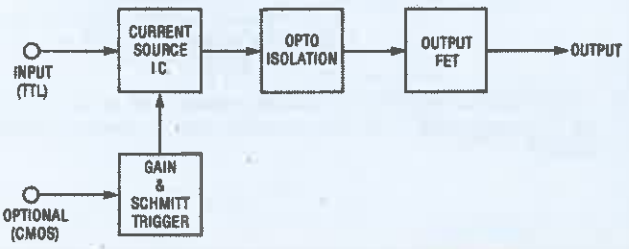
The 685 and 686 are housed in metal DIP packages which maximize heat dissipation.

The 690 and 691 are housed in low profile Centrigrid® packages which conserve space in high density packaging applications.

PART NUMBERING AND GENERAL SPECIFICATIONS

Teledyne Part No.	Maximum Continuous Operating Output Voltage	Maximum Load Current (25°C)
690-1	60 Volts DC	0.56 DC Amps
690-2	60 Volts DC	1.00 DC Amps
691-1	±60 Volts Peak	0.40 Amp (RMS)
691-2	±60 Volts Peak	0.70 Amp (RMS)
685-1	60 Volts DC	0.75 DC Amps
685-2	60 Volts DC	1.35 DC Amps
686-1	±60 Volts Peak	0.54 Amp (RMS)
686-2	±60 Volts Peak	0.95 Amp (RMS)

BLOCK DIAGRAM



INPUT (CONTROL) CHARACTERISTICS
When used in 5 terminal configuration (CMOS) See Fig. 3

	MIN.	TYP.	MAX.	UNITS
Input Current @ 5 VDC			250	μA
Control Voltage Range	2.5		18	VDC
Bias Supply Range V_C	3.8		32	VDC Table 1
Bias Current		13	16	mA
Turn-Off Minimum (For guaranteed off)		2.5	2.8	VDC
Turn-On Maximum (For guaranteed on)	0.5			VDC
Total Schmitt Hysteresis		1.8		VDC

INPUT (CONTROL) CHARACTERISTICS
When used in 4 terminal configuration (TTL) See Fig. 2

	MIN.	TYP.	MAX.	UNITS
Input Current		13	16	mA
Control Voltage Range	3.8		32	VDC Table 1
Turn-Off Maximum (For guaranteed off)			1.5	VDC
Turn-On Minimum (For guaranteed on)	3.8			VDC

ELECTRICAL CHARACTERISTICS AT 25°C

		690-1	685-1	690-2	685-2	691-1	686-1	691-2	686-2	Units
Maximum Continuous Operating Output Voltage		60 Volts DC				±60 Volts Peak				Volts (DC or Peak)
Maximum Load Current At 25°C		0.56	0.75	1.0	1.35	0.40	0.54	0.70	0.95	Amps (DC or RMS)
ON Resistance	Typ.	0.60		0.30		1.2		0.60		Ohms
	Max.	0.90		0.35		1.6		0.70		
Maximum Output Capacitance		160		400		80		200		pf at 25V 1 MHz
Maximum Input-Output Capacitance		5								pf at 25V 1 KHz
Typical Thermal Resistance	θJA	150	90	120	70	150	90	120	70	°C/Watt
	θJC	40	30	30	25	40	30	30	25	
t_r* (Typical Rise Time)		0.8		1.5		1.2		2.0		msec
t_{dON}* (Typical On Delay)		0.7		0.8		0.8		2.2		msec
t_f* (Typical Fall Time)		0.4		0.6		0.6		0.6		msec
t_{dOFF}* (Typical Off Delay)		1.8		2.0		2.4		2.5		msec
Maximum Surge Voltage Note 5 (Transient Blocking) 2 sec max.		80								Volt (DC or Peak)
Leakage Current at 60 Volts, 25°C		10								µA
Dielectric Strength (Input-Output)		1000	1200	1000	1200	1000	1200	1000	1200	VAC RMS 60Hz Sine Wave
Isolation (Input to Case at 500 Volts)		10^9								Ohms
Current Surge		200% of maximum load current at 25°C for 1 sec duration 10% duty cycle								

NOTES:

1. Used in the 5 terminal CMOS compatible configuration, the relays provide inversion such that when the control voltage is 0.5 VDC or less, the relay's output will be guaranteed "on." When the control voltage is 2.8 VDC or more the relay's output will be guaranteed "off."

2. In the 4 terminal TTL configuration the relays are non-inverting. When the TTL driving gate is sinking the drive current the relay output will be on.

3. All power FET relays may drive loads connected to either positive or negative referenced power supply lines. (Source or sink modes)

4. For on state resistance at temperatures other than 25°C, use the following equation —

$$R = R_{25} \times e^{0.006 \times \Delta T}$$

where R_{25} = resistance at 25°C from table
R = resistance at new temperature
ΔT = new temperature - 25°C
e = 2.7182818

5. If 600V transient capability is required, a zener diode across the output is recommended. If an internal zener diode is required, consult factory.

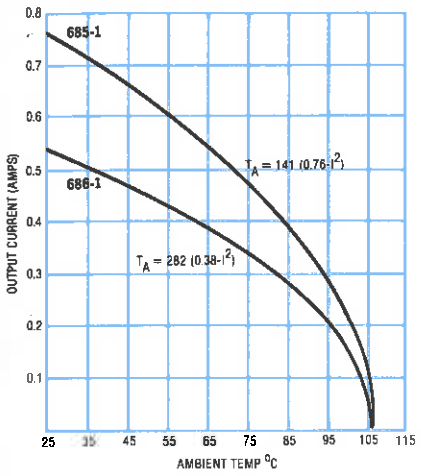
ENVIRONMENTAL SPECIFICATIONS*	
Temperature (Ambient Operating)	—55°C to Maximum Per Thermal Derating Curve
Temperature (Ambient Storage)	—55°C to 125°C
Vibration	100g, 10 to 3000 Hz
Shock	1500g, 0.5 mSec
Acceleration	5000g

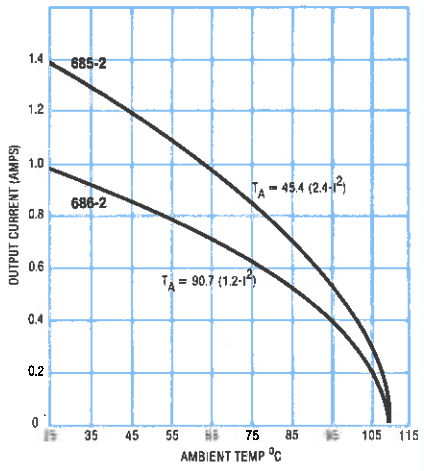
*For higher environmental requirements, contact factory.

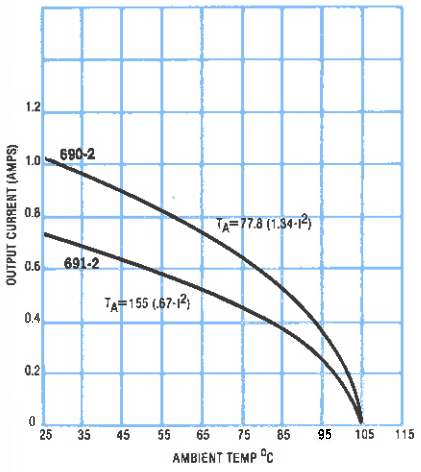
CONTROL INPUT RESISTANCE REQUIREMENTS							
Vc Range	3.8-6V	6.0-10V	10-14V	14-18V	18-22V	22-26V	26-32V
Rs Ohms	Not Required	300	620	910	1200	1500	2000
Power Rating Watts		¼	¼	½	½	½	1

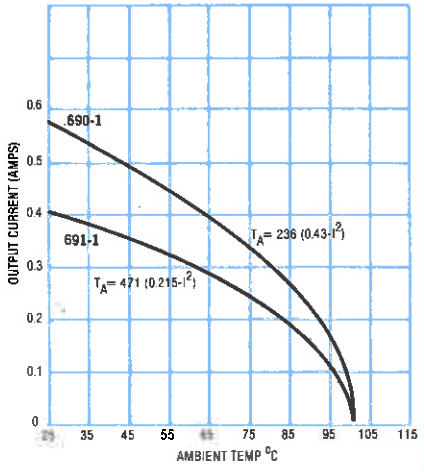
TABLE 1

THERMAL DERATING CURVES (FREE AIR)



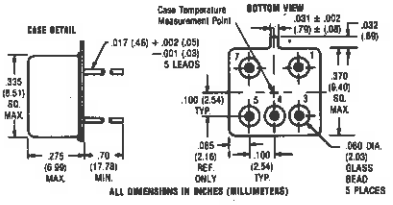






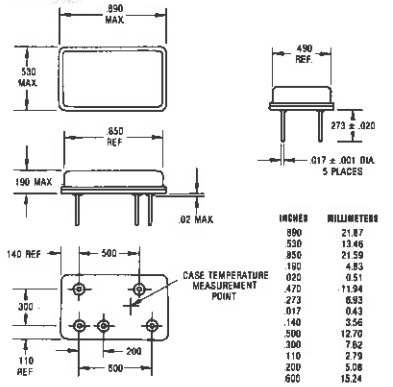
MECHANICAL SPECIFICATIONS

690 & 691



Weight: 1.5 Grams (Typical)

685 & 686



INCHES	MILLIMETERS
.890	21.87
.530	13.46
.850	21.59
.190	4.83
.020	0.51
.470	11.94
.273	6.93
.017	0.43
.140	3.56
.500	12.70
.300	7.62
.110	2.79
.200	5.08
.600	15.24

Weight: 5.0 Grams (Typical)

TURN-ON AND TURN-OFF TIMING

$^*t_{ON} = T_{dON} + T_r$

$t_{OFF} = T_{dOFF} + T_f$

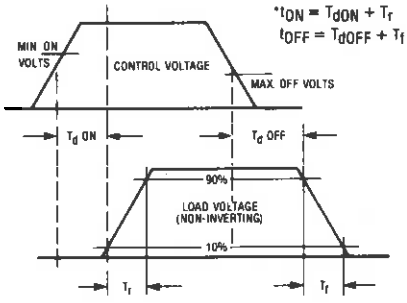
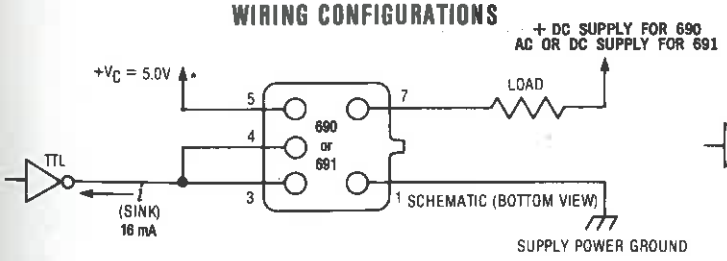
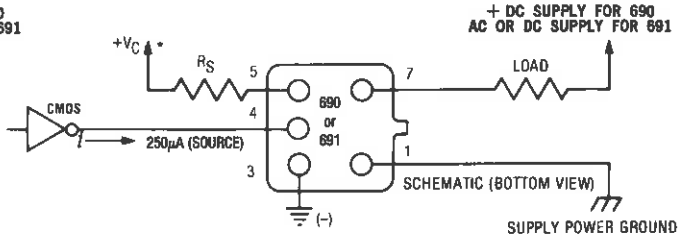


FIGURE 1

WIRING CONFIGURATIONS





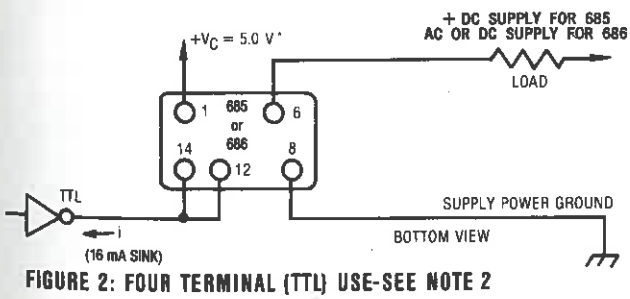


FIGURE 2: FOUR TERMINAL (TTL) USE-SEE NOTE 2

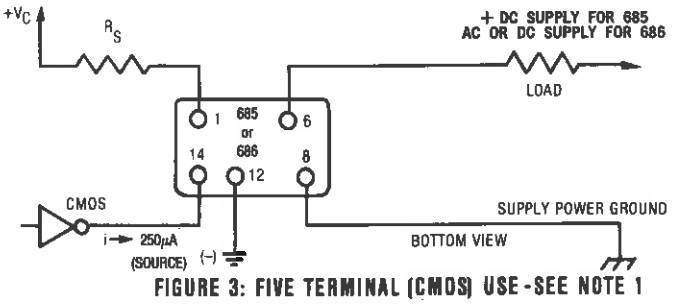


FIGURE 3: FIVE TERMINAL (CMOS) USE-SEE NOTE 1

* LIMITING RESISTOR REQUIRED OVER 6.0 VOLTS (TABLE 1) WHEN NOT USED WITH A HEAT SINK. WITH A HEAT SINK, THE VALUES ARE TO BE DETERMINED.

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