

Si537x-EVB EVALUATION BOARD USER'S GUIDE

Description

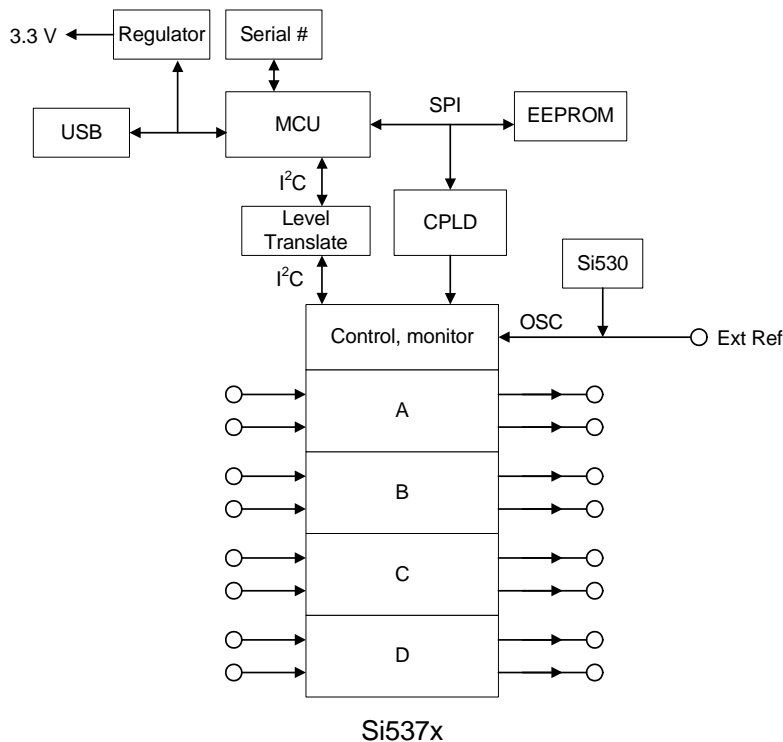
The Si5374/75/76 Any Frequency Precision Clocks are based on Silicon Labs 3rd-generation DSPLL technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The devices have excellent phase noise and jitter performance. All of the devices support 350 fs RMS jitter generation across the 12 kHz to 20 MHz jitter filter bandwidth. For all devices, the DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. These devices are ideal for providing clock multiplication/clock division and jitter attenuation in mid-range and high-performance timing applications where printed circuit board real estate is at a premium.

Features

The Si537x-EVB includes the following:

- CD with documentation and EVB software including the Si537x_DSPLLsim configuration software utility.
- EVB circuit board
- Si537x-EVB User's Guide (this document)

Functional Block Diagram



Si537x-EVB

1. Introduction

The Si537x-EVB provides a platform for evaluating Silicon Labs' Si5374, Si5375, and Si5376 Any Frequency Precision Clocks. These devices are jitter attenuating quad DSPLLs that are microprocessor controlled using an I²C interface. The Si5374 and the Si5376 have eight clock inputs and 8 clock outputs, whereas the Si5375 has 4 clock inputs and 4 clock outputs. The Si5374 has the added feature of lower loop BW than the Si5375 and Si5376.

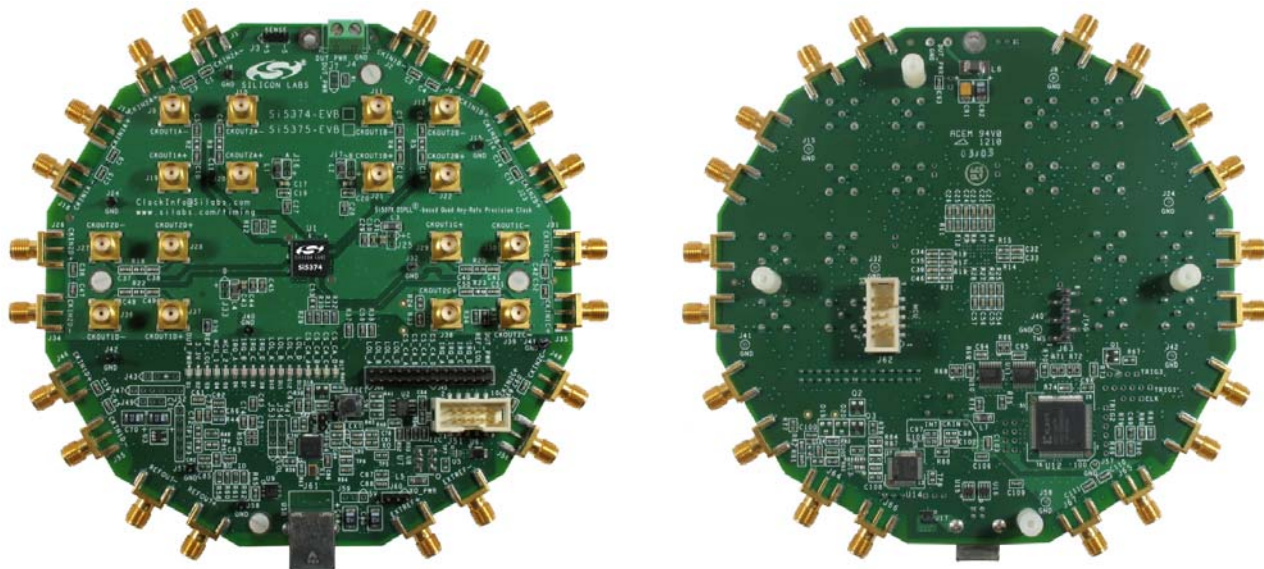


Figure 1. Si537x-EVB

Table 1. Si537x Selection Summary

| Device | # Input/ Output Clocks | Frequency Range | | DSPLL Loop Bandwidth Range | Hitless Switching | VCO Freeze | Free Run | Digital Hold | Package |
|--------|------------------------------|-----------------|---------------|----------------------------------|-------------------|------------|----------|--------------|---------------------|
| | | Input | Output | | | | | | |
| Si5374 | 8/8 | 2 kHz–710 MHz | 2 kHz–808 MHz | 4–525 Hz | ✓ | | ✓ | ✓ | 10x10 mm 80-PBGA |
| Si5375 | 4/4 | 2 kHz–710 MHz | 2 kHz–808 MHz | 60 Hz–8.4 kHz | | ✓ | ✓ | | 10x10 mm 80-PBGA |
| Si5376 | 8/8 | 2 kHz–710 MHz | 2 kHz–808 MHz | 60 Hz–8.4 kHz | ✓ | | ✓ | ✓ | 10x10 mm 80-PBGA |

2. Applications

The Si5374/75/76 Any Frequency Precision Clocks offer a comprehensive feature set, including any frequency synthesis, jitter attenuation, fully integrated loop filter, multiple clock inputs, multiple clock outputs, alarm and status outputs, hitless switching between multiple input clocks, programmable output clock format (LVPECL, LVDS, CML, CMOS), and output phase adjustment between all output clocks. For more details, consult the Silicon Labs timing products website at www.silabs.com/timing.

The Si537x-EVB has a Silicon Labs MCU (C8051F430) that supports USB communications with a PC host. The Si5374/75/76 devices are controlled and monitored through the I²C serial port. A CPLD is connected to the MCU and stores pin configuration data and reads the device status pins. The MCU communicates to the Si537x device using I²C through a voltage level translator. However, the user has the option of bypassing the MCU and controlling the devices from an external serial device. On-board termination is included so that the user can evaluate either single-ended or differential as well as ac or dc coupled clock inputs and outputs. A separate DUT (device under test) power supply connector is included. LEDs are provided for convenient monitor of key status signals. The user can select between a number of reference oscillator options, including external sources and various on-board options.

For more detailed information about the applications of these devices, please see their respective data sheets.

3. Si5374/75/76-EVB Quick Start

For more detailed information about these devices, see their respective data sheets.

4. Functional Description

The Si537x-EVB and software allows for a complete and simple evaluation of the functions, features, and performance of the Si5374/75/76 Any Frequency Precision Clocks. For the following material, refer to the schematics in section “7. Schematics.”

4.1. Block Diagram

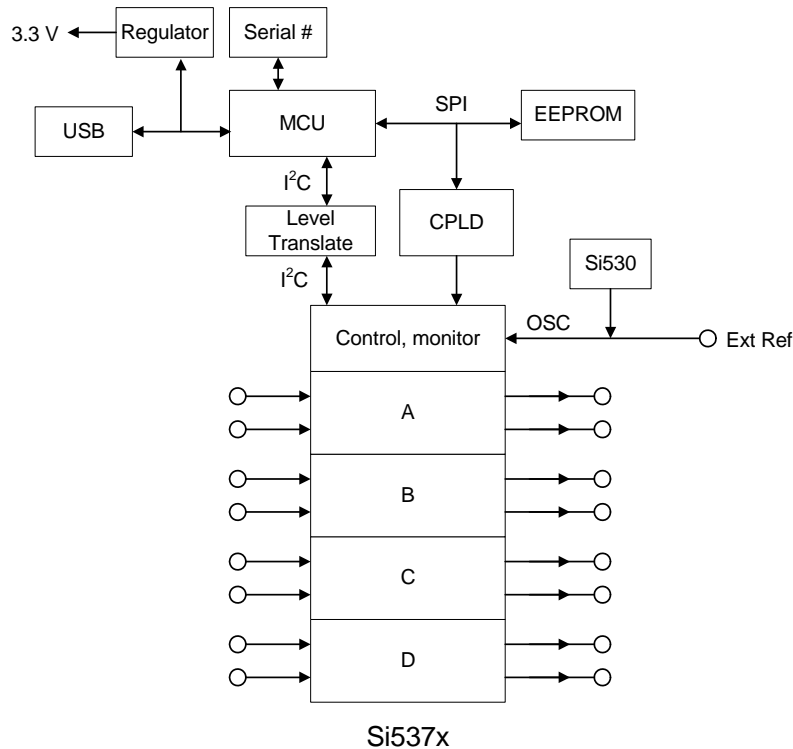


Figure 2. Si537x-EVB Block Diagram

Figure 2 is a block diagram of the evaluation board and it is helpful to refer to this diagram. The MCU communicates to the host PC over a USB connection. The MCU controls and monitors the Si537x pins through the CPLD, which provides level translation between the MCU and the Si537x. I²C level translation is provided separately. A number of different options are provided for the required Si537x external reference oscillator.

4.2. Si537x Device

To minimize noise and crosstalk, the Si537x device has separate and filtered V_{DD} supplies. Two-pin jumper plugs (J16, J17, J25, and J33) are provided so that the distinct power supplies can be monitored.

4.3. Input Clocks

The input clocks are all located at the edge of the board. For each clock input pair, each input is ac terminated with 50 Ω to ground. With this configuration, single ended inputs can be implemented by simply leaving the unused clock input disconnected. If low frequency clock inputs are in use, the reactance of the 100 nf capacitors (C12, C13, C14, etc.) can become significant and they should be replaced with 0 Ω resistors. In some circumstances, the ac termination should be removed and replaced. CMOS inputs are typically best terminated by using series source termination at the output of the CMOS driver and completely removing all of the on-board input termination.

Regardless of the termination scheme in use, a scope should be used to verify that none of the clock input specifications found in the data sheet are being violated.

4.4. Output clocks

The output clocks all use vertical mount SMA connectors and are ac coupled. There may be circumstances (e.g., CMOS outputs) for which the 100 nF capacitors should be replaced with 0 Ω resistors. Pads for resistors between the two halves of the outputs are provided for CMOS outputs so that the outputs can be put in parallel for greater drive strength.

4.5. OSC Reference Source

The Si537x requires a low-jitter reference on its OSC_P and OSC_N input pins. To provide a clock source, the user has a number of different options:

1. The factory default configuration is a 121.109 MHz Si530 crystal oscillator (XO). For this configuration install C78 and C81 (in the silkscreen XO box on the top of the board), remove C97 and C101 (in the INT silkscreen box on the bottom of the board), and remove C77 and C80 (in the silkscreen box EXT on the top of the board). J50 should be removed and J60 should select the desired XO supply voltage of 3.3 V by jumpering J60.2 to J60.3.
2. There are provisions for three different XO oscillator packages in industry standard pinouts: 5x7 mm, 3.2x5 mm, and 3.2x2.5 mm. If any of these are used, be sure to install C78 and C81 (in the silkscreen XO box on the top of the board), remove C97 and C101 (in the INT silkscreen box on the bottom of the board), and remove C77 and C80 (in the silkscreen box EXT on the top of the board). J50 should be removed and J60 should select the desired XO supply voltage of either the Si537x V_{DD} or 3.3 V.
3. An off-board, external reference oscillator may be used instead of the Si530 XO. If this is desired, C98 and C102 (in the CKIN silkscreen box on the bottom of the board), C101 and C97 (in the INT silkscreen box on the bottom of the board), and C78 and C81 (in the silkscreen XO box on the top of the board) should all be removed and C77 and C80 (in the EXT silkscreen box on the top of the board) should be installed. If this mode is selected, the clock input should be applied to J64 and J66. Both J50 and J60 should be removed so that the other references sources are not powered and do not add noise.
4. A PCB footprint for a reference Si5326 is included on the EVB. If it is installed, the Si5326 is initialized by the MCU and EEPROM so that it powers up with an output that is 114.285 MHz based on its crystal, X1. The output of the Si5326 can be monitored at J65 and J67 and can be changed to most any frequency using *DSPLLsim*. Free run at 114.285 MHz is the factory default Si5326 frequency plan. If a reference OSC frequency in the 37–41 MHz band is to be used, be sure to set the RATE register (reg 2) for all of the DSPLLs to 0101.

For options 2 and 4 above, an external OSC reference XO in the 37–41 MHz frequency band can also be used. With this approach, the output jitter will be higher by an amount that is illustrated in “AN591: Crystal Selection for the Si5315 and Si5317,” Figures 3 and 4. It will also be necessary to create an Si537xDSPLLsim frequency plan with the appropriate RATE_REG (at addr 2) setting of 0001.

It is also possible to have the reference Si5326 lock onto an external clock source instead of locking to its 114.285 MHz crystal in free run mode. If this mode is desired, install C98 and C102 (in the CKIN silkscreen box on the bottom of the board) and then load the appropriate frequency plan into the reference Si5326 using *DSPLLsim*. The external clock source is connected to J64 and J66. If the Si5326 is being used, J50 should be installed and J60 should be removed.

Though they will result in slightly lower performance, single ended reference clock inputs can be connected to J66, with the unused J64 connected to ground. In all cases, when a single ended reference oscillator is in use, C53 (located close to the Si537x) should be installed.

Si537x-EVB

4.6. CPLD

The CPLD provides various functions including level translation and the buffering of monitor/control of signals for the Si537x DUT and the Si5326 reference source. Examples are the LOL, IRQ, and CS_CA signals from the Si537x as well as the SPI port connection to the reference Si5326.

4.7. MCU

The MCU is the intermediary between the PC host and the Si537x DUT. The host's USB port provides power for the MCU and the LEDs through a 3.3 V regulator (U17). U6 provides I²C level translation to the DUT V_{DD} voltage level. U2 is an EEPROM that is used to initialize the reference Si5326. J51 is an I²C serial port connector by which an external I²C master can control the on-board Si537x or by which the on-board MCU can control an Si537x that resides on a external target board.

4.8. Power and LEDs

J4 is the main Si537x power connector. Remote sensing for the power supply is provided by J3. DUT current can be monitored by removing R1 and connecting to J7. U10 and U11 are buffers that are used to drive the LEDs. The status outputs are available at J44/45.

5. Connectors and LEDs

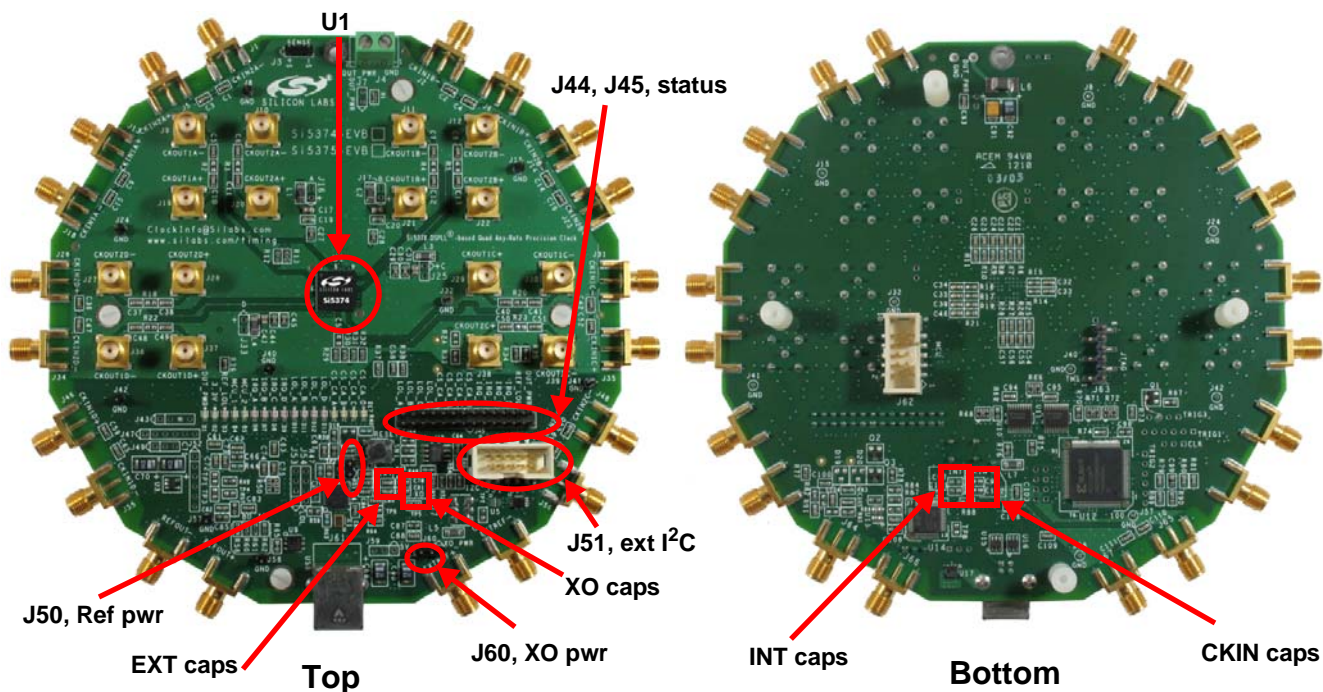


Figure 3. Connectors, Top, and Bottom Views

J51 can be used as an attachment point for controlling the Si537x DUT from an external I²C master or to use the MCU to control an Si537x DUT that resides on an external target board.

To control the on-board Si537x from an external I²C master, disconnect the cable from the USB connector (J61), thereby depriving the EVB of its 5 V power source. A lack of 3.3 V power will disable the U6 level translator (by virtue of U6.8) so that the MCU will be isolated from the external I²C bus that should be applied to J51.

To control an external Si537x from the on-board MCU, the on-board Si537x must be held in reset so that it does not assert either of the two I²C bus signals. This can be done by opening the Si537x Register Programmer and going to the Options pull down menu on the top toolbar and selecting "Switch to External Control Mode."

Table 2. External I²C

| J51 | Name | Comment |
|-------|-----------|--------------|
| J51.1 | SDA | serial data |
| J51.3 | SCL | serial clock |
| J51.9 | DUT_RST_L | DUT reset |

J45 is used to make external connections to status signals:

Table 3. Status

| J45 | Name | Comment |
|--------|---------|---------------|
| J45.27 | DUT_PWR | +2.5 or 1.8 V |
| J45.25 | REF_LOL | |
| J45.23 | IRQ_D | |
| J45.21 | IRQ_C | |
| J45.19 | IRQ_B | |
| J45.17 | IRQ_A | |
| J45.15 | CS_CA_D | |
| J45.13 | CS_CA_C | |
| J45.11 | CS_CA_B | |
| J45.9 | CS_CA_A | |
| J45.7 | LOL_D | |
| J45.5 | LOL_C | |
| J45.3 | LOL_B | |
| J45.1 | LOL_A | |

The LEDs are used to quickly determine the board status:

Table 4. LED Descriptions

| LED | Color | Label |
|-----|--------|---------|
| D17 | yellow | CS_CA_D |
| D16 | yellow | CS_CA_C |
| D15 | yellow | CS_CA_B |
| D14 | yellow | CS_CA_A |
| D13 | red | LOL_D |
| D12 | red | LOL_C |
| D11 | red | LOL_B |
| D10 | red | LOL_A |
| D9 | red | IRQ_D |
| D8 | red | IRQ_C |
| D7 | red | IRQ_B |
| D6 | red | IRQ_A |
| D5 | green | MCU_2 |
| D4 | green | MCU_1 |
| D3 | red | REF_LOL |
| D2 | green | 3.3 V |
| D1 | green | DUT_PWR |

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6. EVB Software Installation

The release notes and the procedure for installing the EVB software can be found on the release CD included with the EVB. These items can also be downloaded from the Silabs web site: www.silabs.com/timing. Follow the links for 4-PLL Jitter attenuators, and look under the Tools tab.

| Program | Description |
|-----------------|---|
| Si537x_DSPLLsim | Provides the high level control of the Si537x device. It has the frequency planning wizard as well as control of the pins in an organized, intuitive manner. Register maps and other configuration files can be saved and opened. |
| Setting Utility | This application allows for quick read/write access to each control word of the Si537x device. It can save and open text files. |
| Register Prgmr | Provides a low-level, hex register read/write capability on a byte basis (as opposed to control word). Register map files can be opened and saved in its batch mode. |
| Register Viewer | Displays the current register map data in a table format sorted by register address. Can save and print the register map. |

7. Schematics

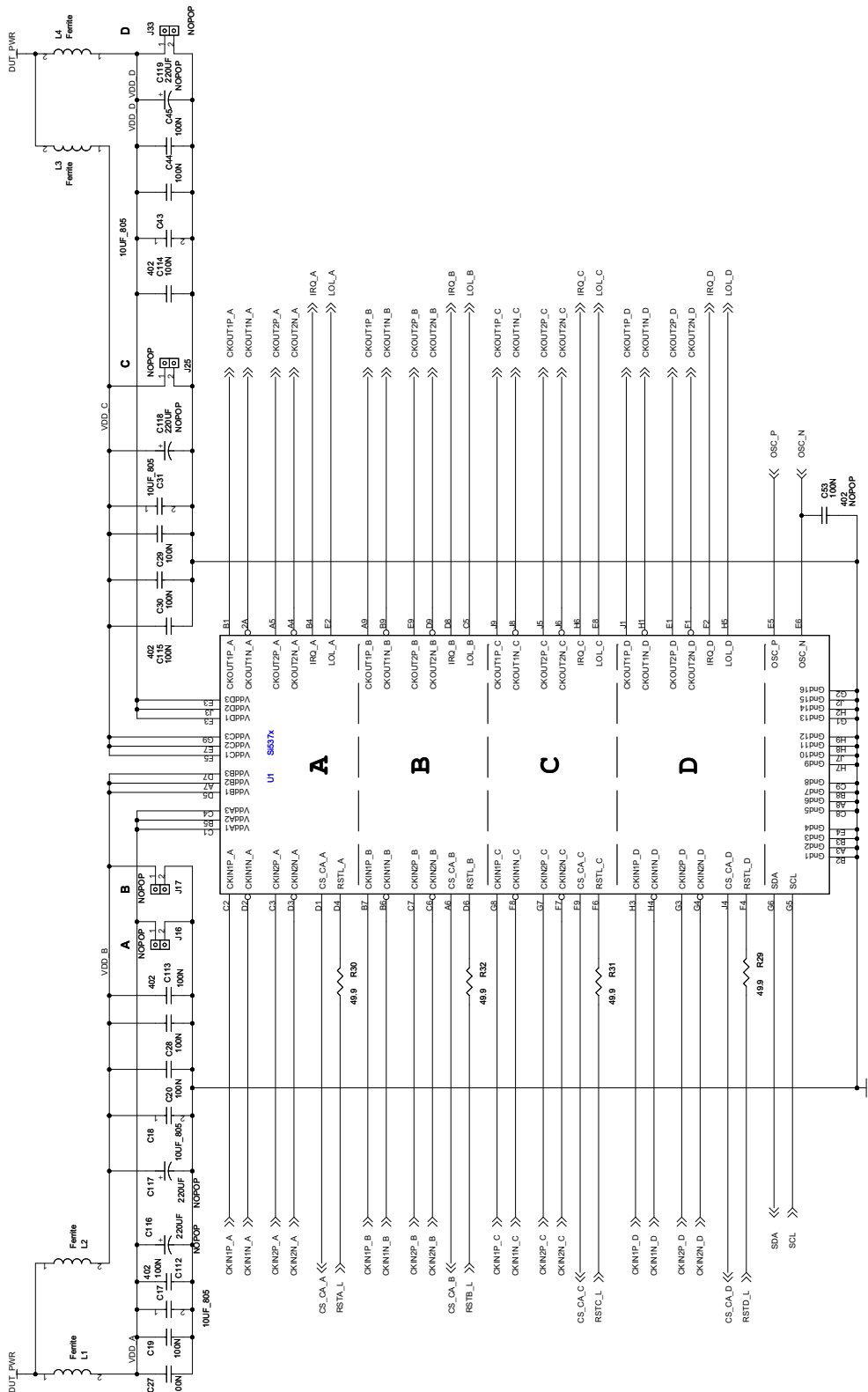


Figure 4. Si537x

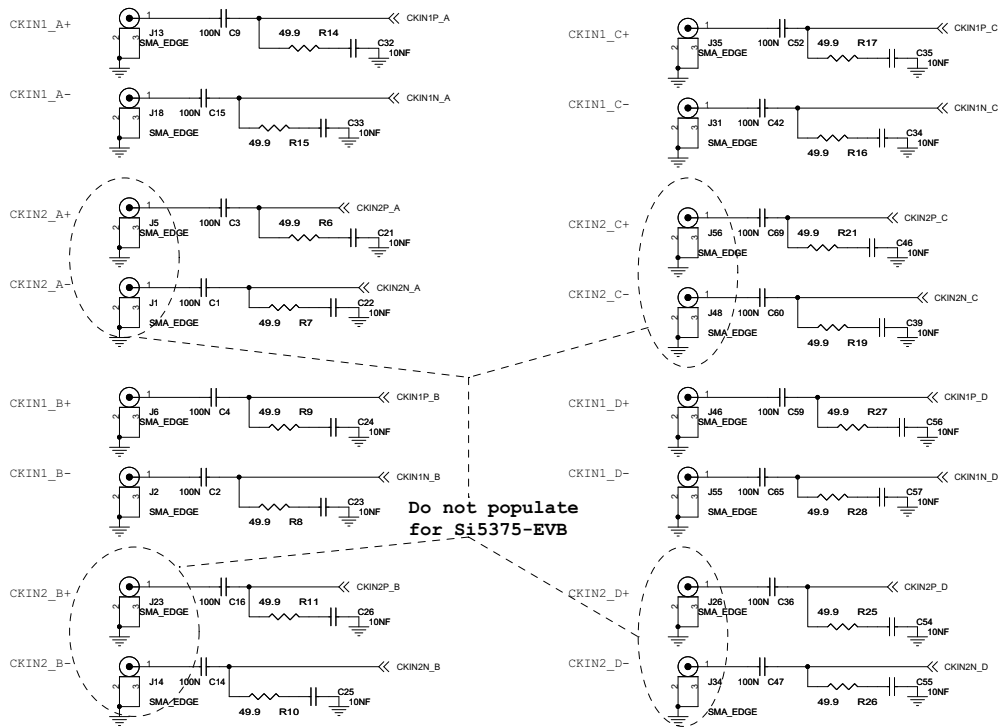


Figure 5. Clock Inputs

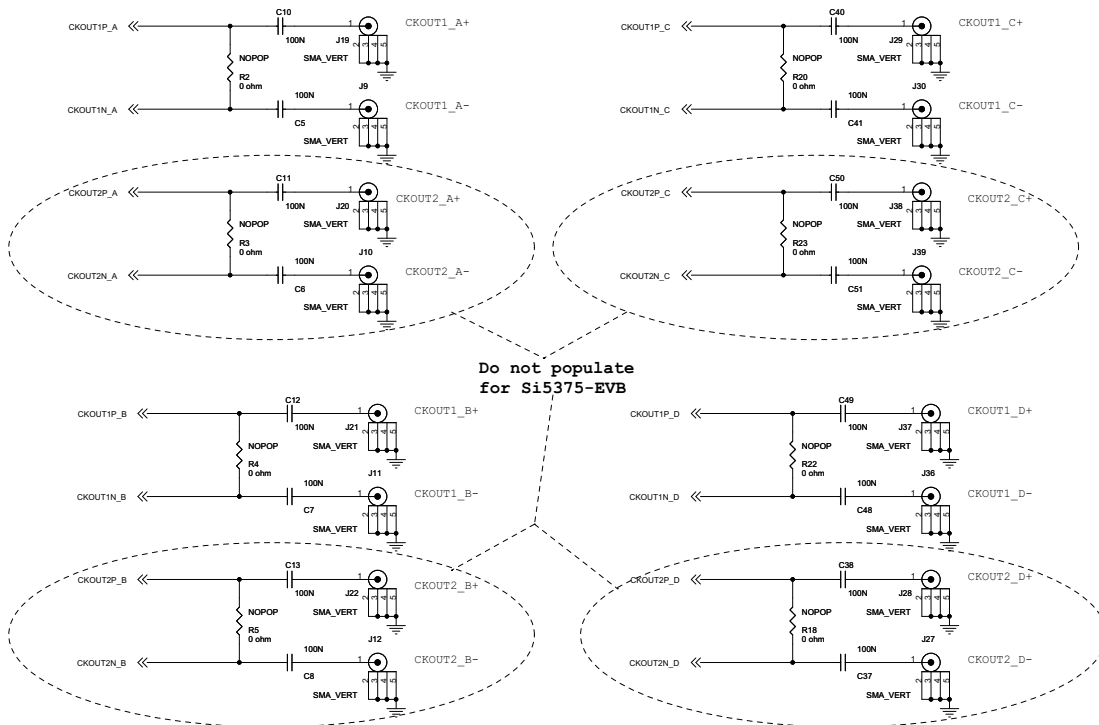


Figure 6. Clock Outputs

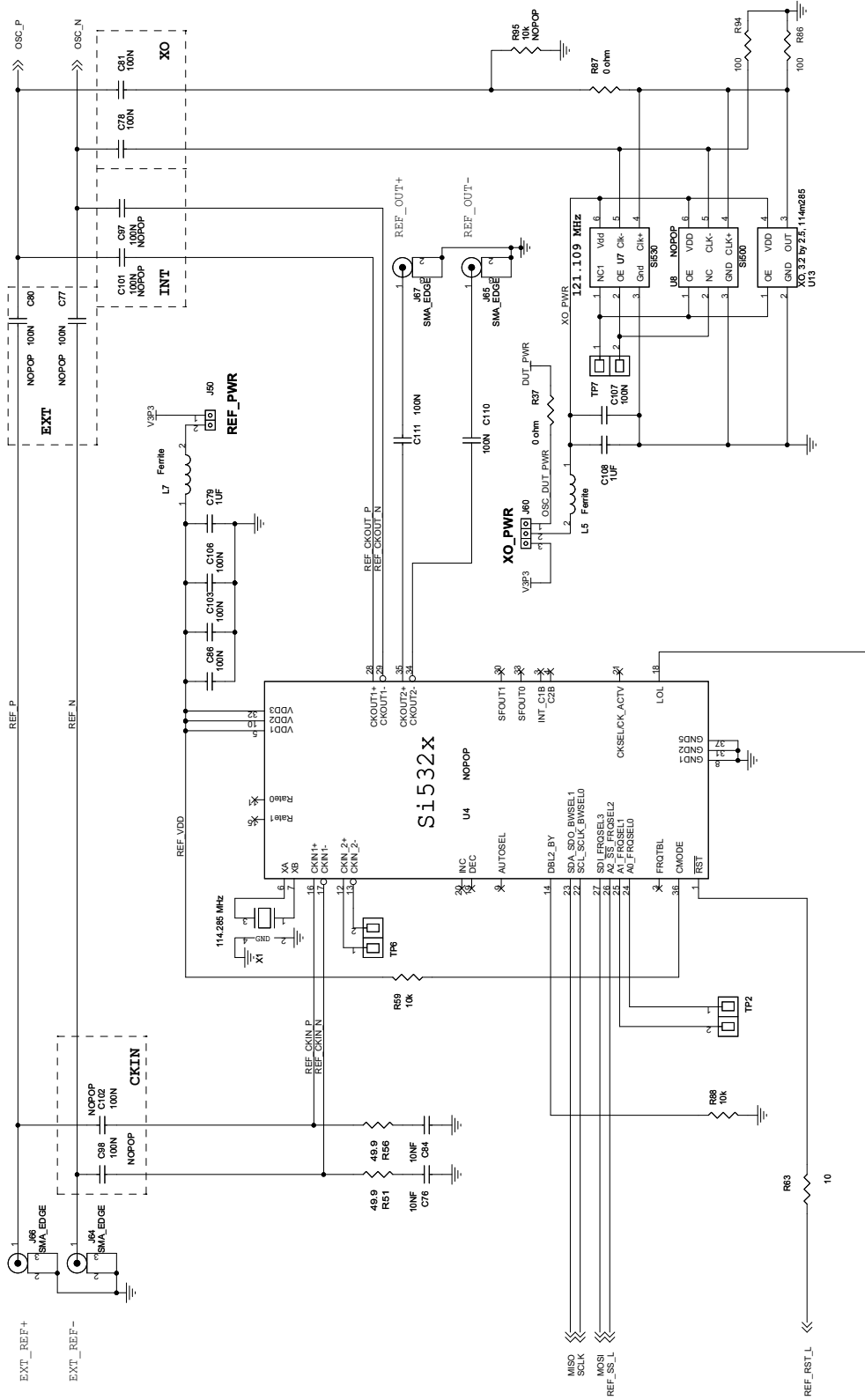
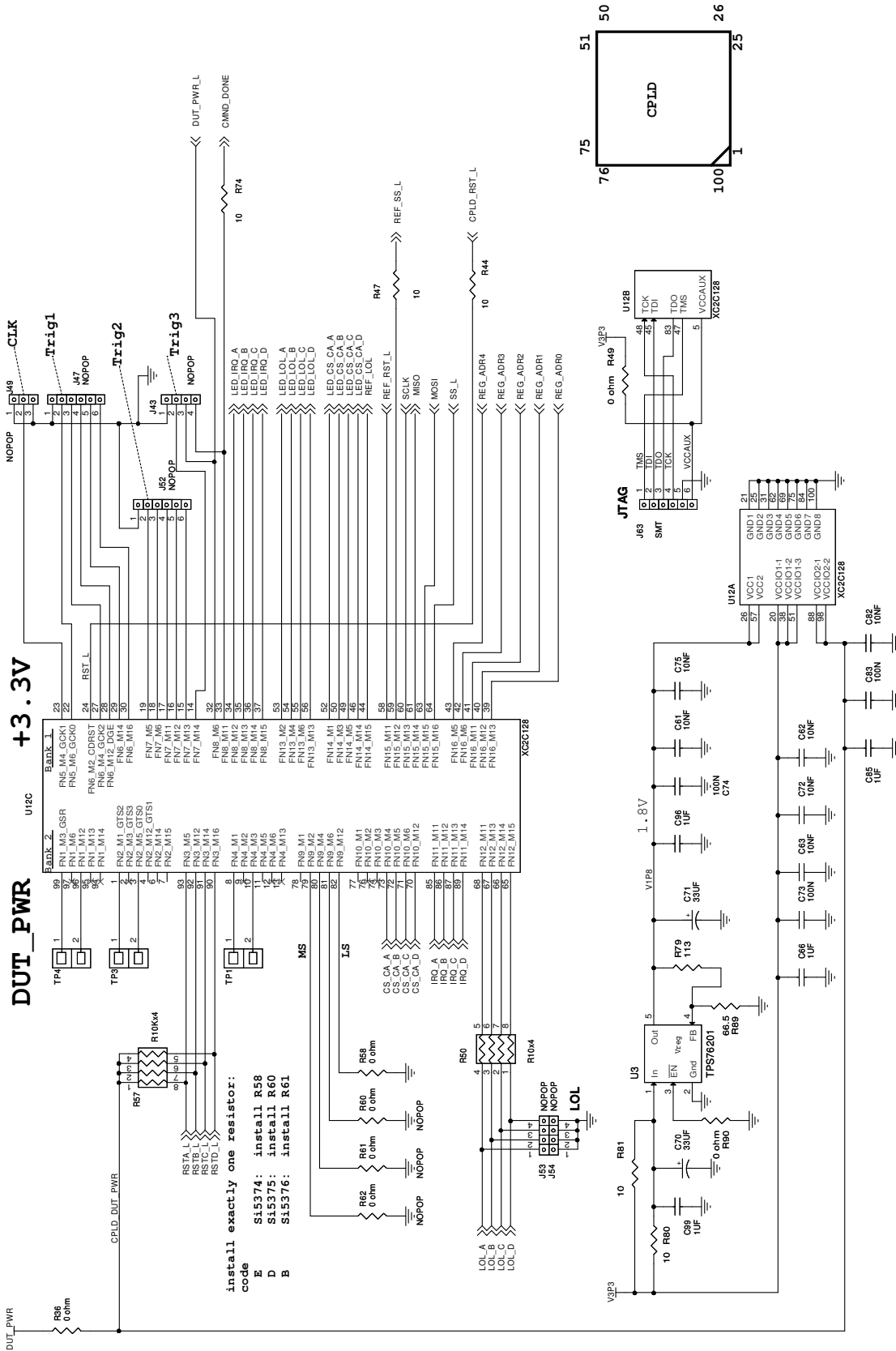


Figure 7. Reference Oscillators



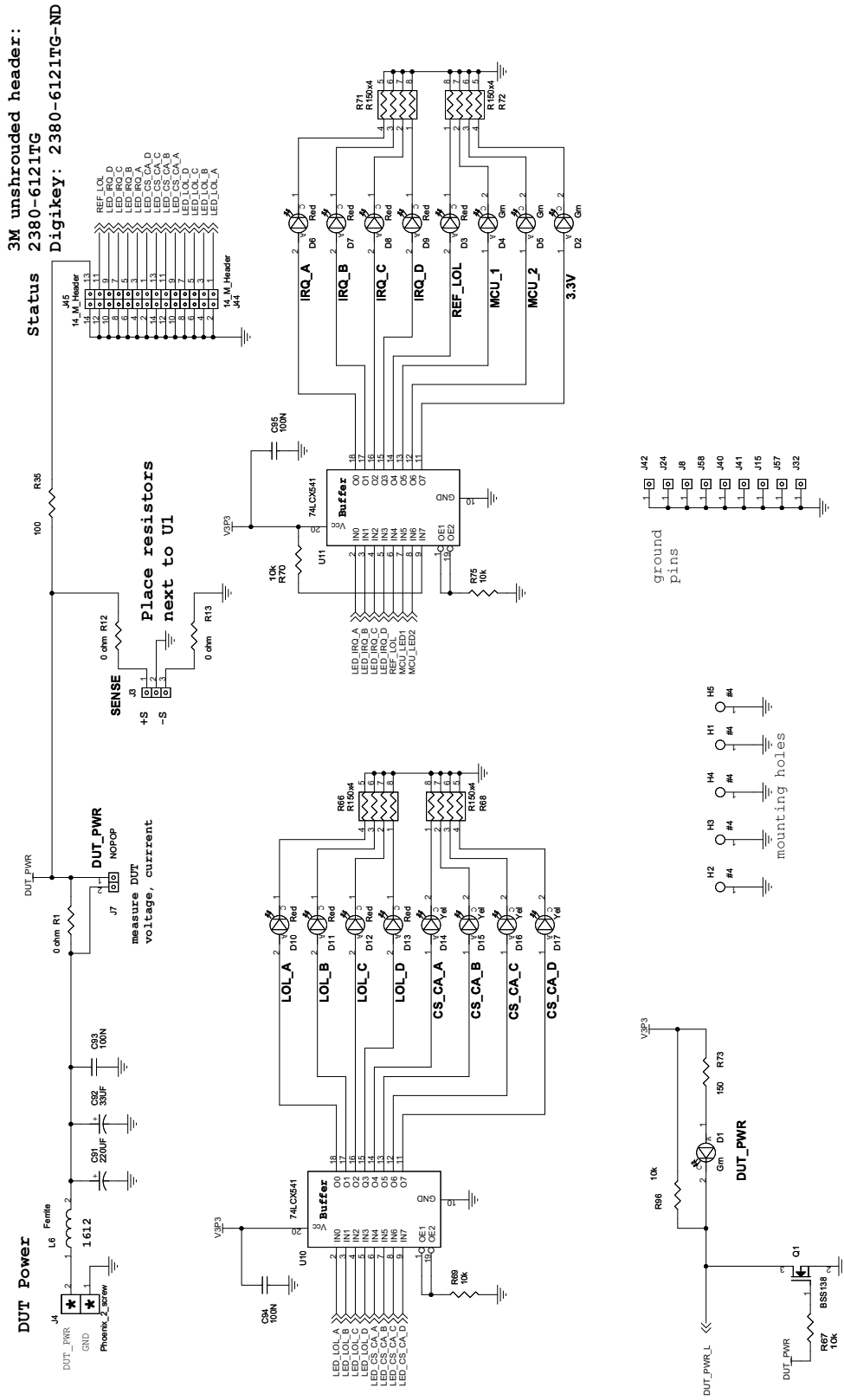


Figure 10. Power and LEDs

8. Bill of Materials

Table 5. Si537x-EVB Bill of Materials

| Item | Qty | Reference | Part | Mfgr | Mfr Part Num | BOM | Digikey | Footprint |
|------|-----|--|----------|-----------|--------------------|-----|----------------|--------------|
| 1 | 62 | C1,C2,C3,C4, C5,C6,C7,C8, C9,C10,C11, C12,C13,C14, C15,C16,C19, C20,C27,C28, C29,C30,C36, C37,C38,C40, C41,C42,C44, C45,C47,C48, C49,C50,C51, C52,C58,C59, C60,C64,C65, C67,C69,C73, C74,C83,C86, C88,C93,C94, C95,C97,C100, C101,C103, C104,C105, C106,C107, C109,C110,C111 | 100N | Venkel | C0603X7R160-104KNE | | | 603 |
| 2 | 4 | C17,C18,C31,C43 | 10UF_805 | Venkel | C0805Y5V6R3106ZN | | | 805 |
| 3 | 24 | C21,C22,C23,C24, C25,C26,C32,C33, C34,C35,C39,C46, C54,C55,C56,C57, C61,C62,C63,C72, C75,C76,C82,C84 | 10NF | Venkel | C0603X7R160-103KNE | | | 603 |
| 5 | 8 | C66,C68,C79,C85, C87,C96,C99,C108 | 1UF | Venkel | C0603X7R6R3-105KNE | | | 603 |
| 6 | 3 | C70,C89,C90 | 33UF | Venkel | TA006TCM336MBR | | | 3528 |
| 7 | 2 | C71,C92 | 33UF | Venkel | TA0006TCM336MBR | | | 3528 |
| 9 | 1 | C91 | 220UF | Kemet | T494B227M004AT | | 399-4631-1-ND | SM_C_3528_21 |
| 10 | 4 | D1,D2,D4,D5 | Grn | Panasonic | LN1371G | | P491CT-ND | LED_gull |
| 11 | 9 | D3,D6,D7,D8,D9, D10,D11, D12,D13 | Red | Lumex | LN1271RAL | | P493CT-ND | LED_gull |
| 12 | 4 | D14,D15,D16,D17 | Yel | Panasonic | LN1471YTR | | P11125CT-ND | LED_gull |
| 13 | 1 | D18 | BAT54S | Fairchild | BAT54S | | BAT54SFSCCT-ND | SOT23 |

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Table 5. Si537x-EVB Bill of Materials (Continued)

| Item | Qty | Reference | Part | Mfgr | Mfr Part Num | BOM | Digikey | Footprint |
|------|-----|---|-------------------|---------|---------------------|-----|------------------|-------------------------------|
| 16 | 20 | J1,J2,J5,J6,J13,J14,J18,J23,J26,J31,J34,J35,J46,J48,J55,J56,J64,J65,J66,J67 | SMA_EDGE | Johnson | 142-0701-801 | | J502-ND | SMA_EDGE_p062 |
| 17 | 2 | J3,J60 | Jmpr_3pin | | | | | 3pin_p1pitch |
| 18 | 1 | J4 | Phoenix_2_screw | Phoenix | MKDSN 1.5/2-5.08 | | 277-1247-ND | Phoenix2pinM_p2pitch |
| 20 | 9 | J8,J15,J24,J32,J40,J41,J42,J57,J58 | Jmpr_1pin | | | | | 1pin_p1pitch |
| 21 | 16 | J9,J10,J11,J12,J19,J20,J21,J22,J27,J28,J29,J30,J36,J37,J38,J39 | SMA_VERT | Johnson | 142-0701-211 | | J494-ND | SMA_VERT |
| 23 | 2 | J44,J45 | unshrouded_Header | 3M | 2380-6121TG | | 2380-6121TG-ND | 28pin thru hole header |
| 26 | 1 | J50 | Jmpr_2pin | | | | | |
| 27 | 2 | J51,J62 | 10_M_Head er_SMT | Samtec | HTST-105-01-lm-dv-a | | | 10pinM dualHeader_p1pitch_smt |
| 28 | 1 | J61 | USB | FCI | 61729-0010BLF | | 609-1039-ND | USB_typeB |
| 29 | 1 | J63 | SMT | Sullins | GZC36SABN-M30 | | S1033-36-ND | 6pin_m_smt |
| 30 | 6 | L1,L2,L3,L4,L5,L7 | Ferrite | Venkel | FBC1206-471H | | | 1206 |
| 31 | 1 | L6 | Ferrite | Steward | HI1612X560R-10 | | | 1612 |
| 32 | 3 | Q1,Q2,Q3 | BSS138 | On Semi | BSS138LT1G | | BSS138LT10SCT-ND | SOT23 |
| 33 | 14 | R1,R12,R13,R29,R30,R31,R32,R34,R36,R37,R38,R49,R61,R77,R87,R90,R23,R62,R85,R92 | 0 Ω | Venkel | CR0603-16W-000T | | | 603 |
| 35 | 25 | R6,R7,R8,R9,R10,R11,R14,R15,R16,R17,R19,R21,R25,R26,R27,R28,R43,R48,R51,R52,R53,R54,R55,R56,R64 | 49.9 | Venkel | CR0603-16W-49R9FT | | | 603 |
| 37 | 4 | R33,R42,R65,R76 | 1K | Venkel | CR0603-16W-1001FT | | | 603 |
| 38 | 1 | R35,R86,R94 | 100 | Venkel | CR0603-16W-1000FT | | | 603 |

Table 5. Si537x-EVB Bill of Materials (Continued)

| Item | Qty | Reference | Part | Mfgr | Mfr Part Num | BOM | Digikey | Footprint |
|------|-----|---|--------------------|---------------------|--------------------|-------|------------------------|---------------|
| 39 | 13 | R39,R41,R45,R46, R57,R59,R67,R69, R70,R75,R78,R84, R88 | 10k | Venkel | CR603-16W-1002FT | | | 603 |
| 40 | 7 | R40,R44,R47,R63, R74,R80,R81 | 10 | Venkel | CR0603-16W-10R0FT | | | 603 |
| 41 | 1 | R50 | R10x4 | Panasonic | EXB-38V100JV | | Y9100CT-ND | 1206x4 |
| 42 | 4 | R66,R68,R71,R72 | R150x4 | Panasonic | EXB-38V151JV | | Y9151CT-ND | 1206x4 |
| 43 | 1 | R73 | 150 | Venkel | CR0603-16W-1500FT | | | 603 |
| 44 | 1 | R79 | 113 | Venkel | CR0603-16W-1130FT | | | 603 |
| 45 | 2 | R82,R91 | 4.99K | Venkel | CR0603-16W-4991FT | | | 603 |
| 46 | 2 | R83,R93 | 1.5K | Venkel | CR0603-16W-1501FT | | | 603 |
| 48 | 1 | R89 | 66.5 | Venkel | CR0603-16W-66R5FT | | | 603 |
| 49 | 1 | SW1 | NO | Mountain Switch | 101-0161-EV | | 101- 0161(mouser) | 4pin Switch |
| 51 | 1 | U1 | Si537x | Silicon Labs | Si537x | | | 10x10 mm BGA |
| 52 | 1 | U2 | M95040 | ST Micro | M95040-WMN6P | | | SOIC-8 |
| 53 | 1 | U3 | TPS76201 | TI | TPS76201DBVT | | 296-11013-1-ND | SOT23-5 |
| 56 | 1 | U6 | PCA9306 | TI | PCA9306DCTR-ND | | 296-18509-1-ND | SM8 |
| 57 | 1 | U7 | Si530_2.5V PECL | Silicon Labs | 530EB121M109DG | | | 5x7 mm |
| 59 | 1 | U9 | DS2411 | Maxim/ Dallas | DS2411P | | | TSOC-6 |
| 60 | 2 | U10,U11 | 74LCX541 | Fairchild | 74LCX541MTC_NL | | TC74LCX541FTF CT-ND | TSSOP-20 |
| 61 | 1 | U12 | XC2C128 | Xilinx | XC2C128-7VQG100I | | | VQG100 |
| 63 | 1 | U14 | Si8051F340 | Silicon Labs | C8051F340-GQ | | | TQFP-48 |
| 64 | 2 | U15,U16 | SN65220 | TI | SN65220DBVT | | 296-9694-1-ND | SOT23-6 |
| 65 | 1 | U17 | FAN1540B | Fairchild | FAN1540BPMX | | FAN1540BMPXC T-ND | MLP6 |
| 66 | 1 | X1 | 114.285 MH z | TXC | 7MA1400014 | | | xtal_3p2by2p5 |
| | 4 | | spacer | SPC Tech- nology | 2397 | | | |
| | 4 | | screw | Richco | NSS-4-4-01 | | | |
| | | | | | | | | |
| 4 | 1 | C53 | 10NF | Venkel | C0603X7R160-103KNE | NOPOP | | 603 |
| 8 | 6 | C77,C78,C80,C81, C98,C102 | 100N | Venkel | C0603X7R160-104KNE | NOPOP | | 603 |

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Table 5. Si537x-EVB Bill of Materials (Continued)

| Item | Qty | Reference | Part | Mfgr | Mfr Part Num | BOM | Digikey | Footprint |
|------|-----|---|-------------------|---------------------|---|-------|-----------------------------|--------------|
| 14 | 2 | D19,D20 | BAT54S | Fairchild | BAT54S | NOPOP | BAT54SFSC-ND | SOT23 |
| 19 | 5 | J7,J16,J17,J25,J33 | Jmpr_2pin | | | NOPOP | | |
| 22 | 3 | J43,J53,J54 | Jmpr_4pin | | | NOPOP | | 4pin_p1pitch |
| 24 | 2 | J47,J52 | Jmpr_6pin | | | NOPOP | | 6pin_p1pitch |
| 25 | 2 | J49,J59 | Jmpr_3pin | | | NOPOP | | 3pin_p1pitch |
| 34 | 14 | R2,R3,R4,R5,R18, R20,R22, | 0 ohm | Venkel | CR0603-16W-000T Note: install R58 for Si5374-EVB, install R60 for Si5375-EVB | NOPOP | | 603 |
| 36 | 1 | R24 | 1K | Venkel | CR0603-16W-1001FT | NOPOP | | 603 |
| 50 | 8 | TP1,TP2,TP3,TP4, TP5,TP6, TP7,TP8 | test_points | none | none | NOPOP | | |
| 54 | 1 | U4 | Si5326 | Silicon Labs | Si5326C-C-GM | NOPOP | | QFN-36 |
| 55 | 1 | U5 | LTC4311 | LinearTech | LTC4311ISC6#TRMPBF | NOPOP | LTC4311CSC6#T RMPBFCT-ND | SC70 |
| 58 | 1 | U8 | Si500 | Silicon Labs | | NOPOP | | 3x5 mm_6pin |
| 62 | 1 | U13 | XO, 3.2 by 2.5 | Pericom | FKB420001 | NOPOP | | 3x2 mm |
| 67 | 1 | — | heatsink | Aavid Thermalloy | 375324B00035G | NOPOP | | 10x10 mm |

9. Layout

Contact Silicon Labs to obtain the Allegro Board file.

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Various changes to accommodate 1.8 V operation.

Revision 0.3 to Revision 0.4

- Removed software installation instructions and directed reader to refer to release CD or download from Silicon Labs web site.

Revision 0.4 to Revision 0.5

- Changed U7 to LVPECL, part number Si530EB121M109G.
- Installed 100 Ω resistors at R94 and R86.

Revision 0.5 to Revision 0.6

- Added Si5376.
- Updated "Description" on page 1.

NOTES:

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Patent Notice

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