

# P-Channel 100-V (D-S) 175 °C MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 100	0.043 at $V_{GS} = - 10$ V	- 37	54 nC
	0.048 at $V_{GS} = - 4.5$ V	- 35	

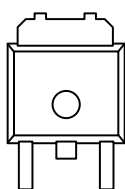
## FEATURES

- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT

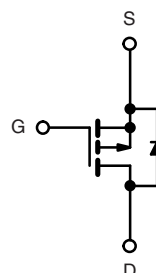
TO-252



G D S

Top View

Drain Connected to Tab



P-Channel MOSFET

Ordering Information: SUD50P10-43L-E3 (Lead (Pb)-free)

## ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C) <sup>b</sup>	$T_C = 25$ °C	- 37.1 <sup>a</sup>	A
	$T_C = 125$ °C	- 31 <sup>a</sup>	
	$T_A = 25$ °C	- 9.2 <sup>b, c</sup>	
	$T_A = 125$ °C	- 7.7 <sup>b, c</sup>	
Pulsed Drain Current	$I_{DM}$	- 40	A
Continuous Source Current (Diode Conduction)	$T_C = 25$ °C	- 50 <sup>a</sup>	
	$T_A = 25$ °C	- 6.9 <sup>b, c</sup>	
Avalanche Current	$I_{AS}$	- 35	mJ
Single Pulse Avalanche Energy	$E_{AS}$	61	
Maximum Power Dissipation	$T_C = 25$ °C	136	W
	$T_C = 70$ °C	95	
	$T_A = 25$ °C	8.3 <sup>b, c</sup>	
	$T_A = 70$ °C	5.8 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	15	18	°C/W
		40	50	
Junction-to-Case (Drain)	$R_{thJC}$	0.85	1.1	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c.  $t = 10$  s.

d. Maximum under Steady State conditions is 40 °C/W.

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

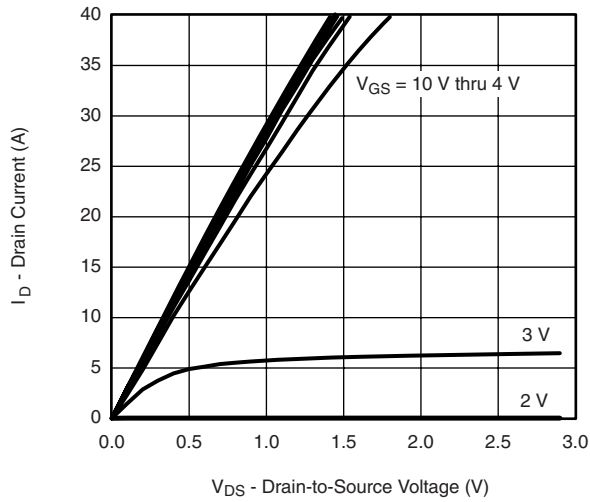
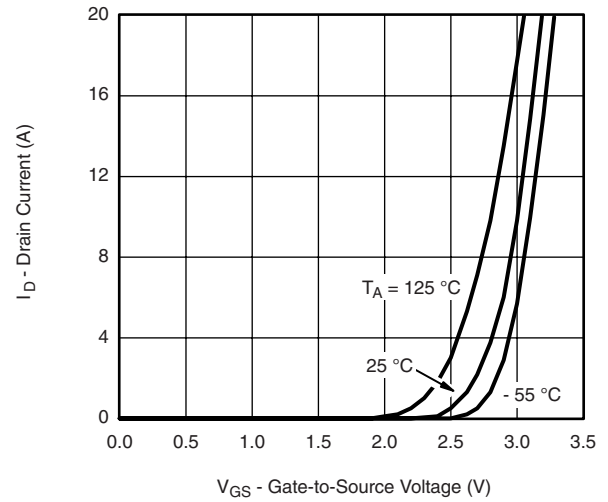
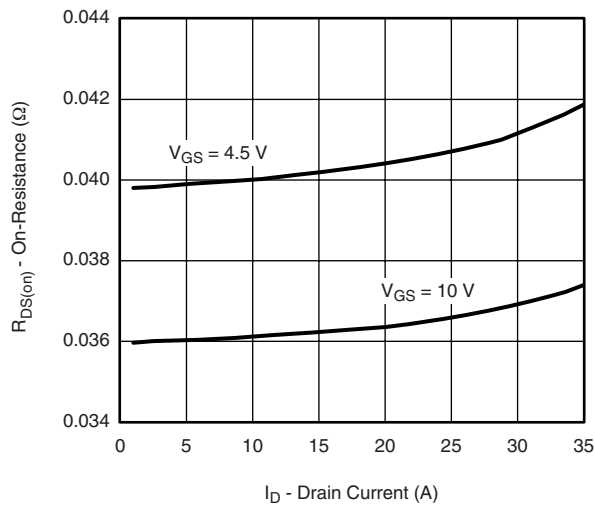
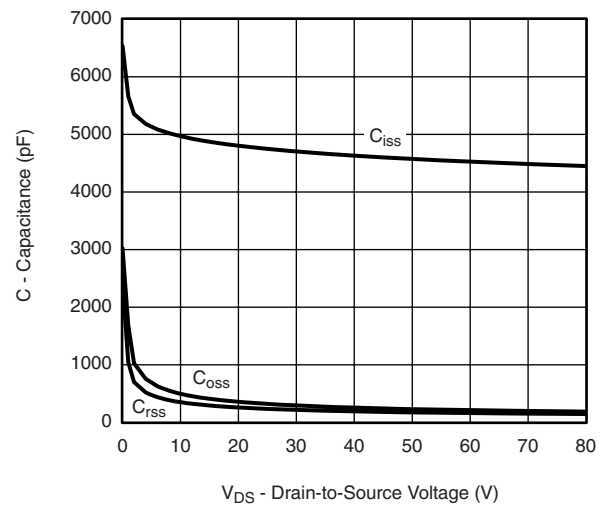
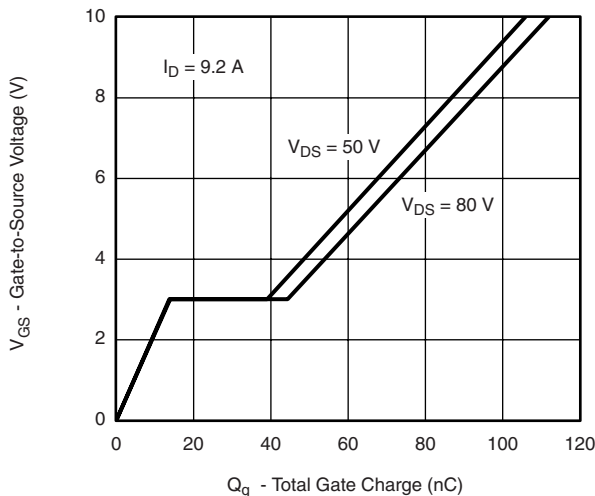
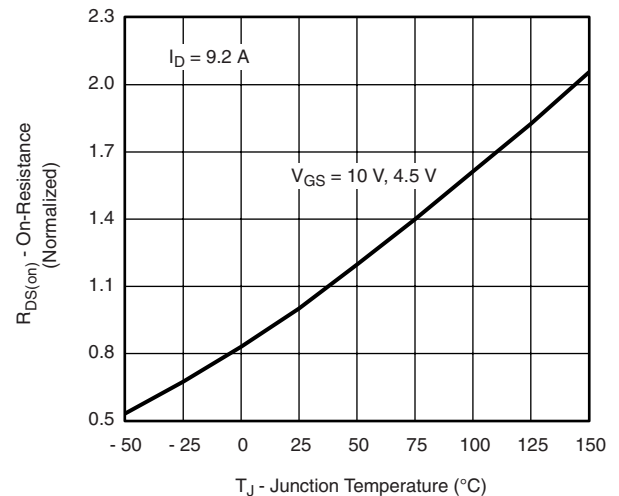
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 100			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 109		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			5.9		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1		- 3	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 100 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = - 10 V	- 40			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 9.2 A		0.036	0.043	Ω
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 7.7 A		0.040	0.048	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 9.2 A		38		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4600		pF
Output Capacitance	C <sub>oss</sub>			230		
Reverse Transfer Capacitance	C <sub>rss</sub>			175		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 50 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 9.2 A		106	160	nC
		V <sub>DS</sub> = - 50 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 9.2 A		54	81	
Gate-Source Charge	Q <sub>gs</sub>			14		
Gate-Drain Charge	Q <sub>gd</sub>			26		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		4		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 50 V, R <sub>L</sub> = 6.5 Ω I <sub>D</sub> ≅ - 7.7 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		15	25	ns
Rise Time	t <sub>r</sub>			20	30	
Turn-Off Delay Time	t <sub>d(off)</sub>			110	165	
Fall Time	t <sub>f</sub>			100	150	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 50 V, R <sub>L</sub> = 6.5 Ω I <sub>D</sub> ≅ - 7.7 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		42	65	ns
Rise Time	t <sub>r</sub>			160	240	
Turn-Off Delay Time	t <sub>d(off)</sub>			100	150	
Fall Time	t <sub>f</sub>			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 50	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				- 40	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 7.7 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 7.7 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			150	225	nC
Reverse Recovery Fall Time	t <sub>a</sub>			46		ns
Reverse Recovery Rise Time	t <sub>b</sub>			14		

Notes:

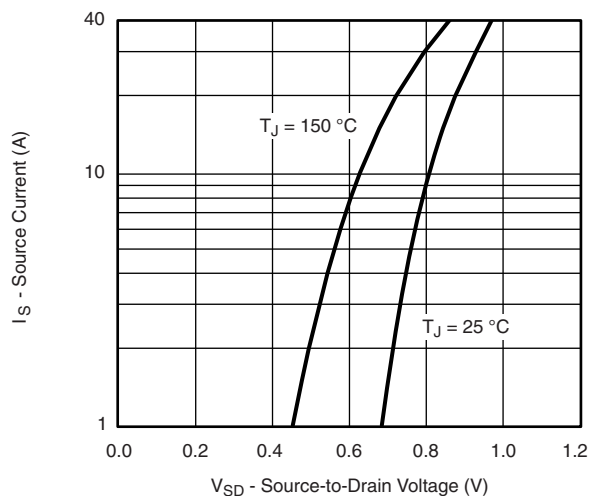
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

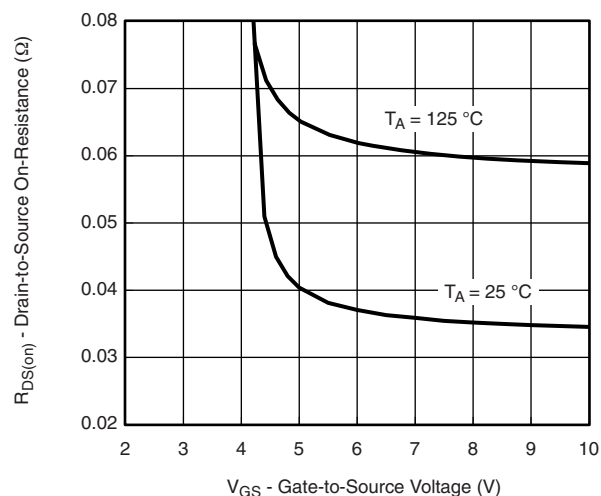
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

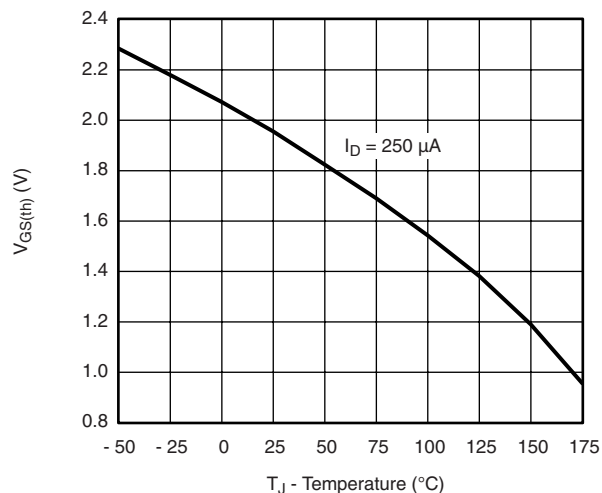
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



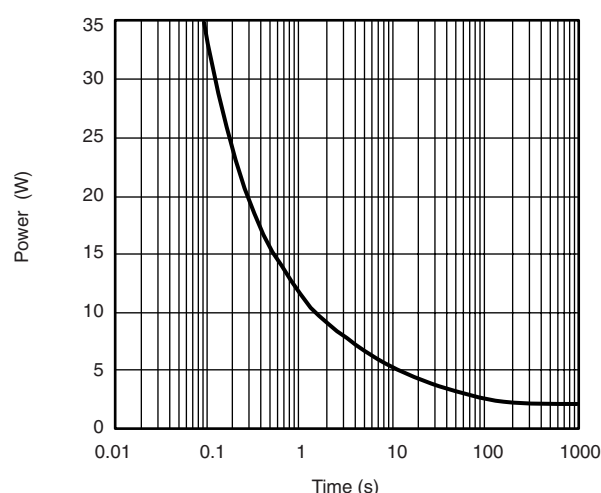
Source-Drain Diode Forward Voltage



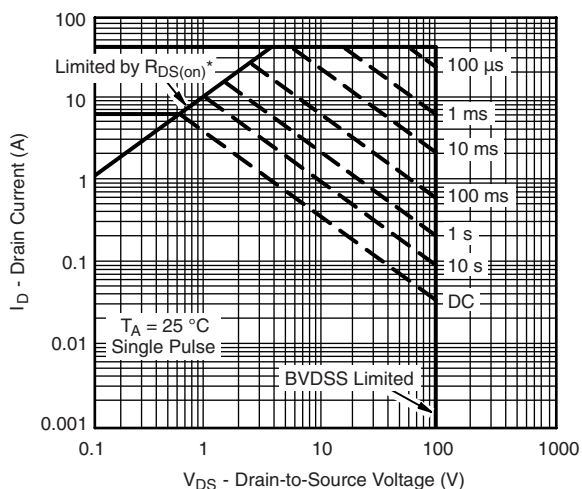
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



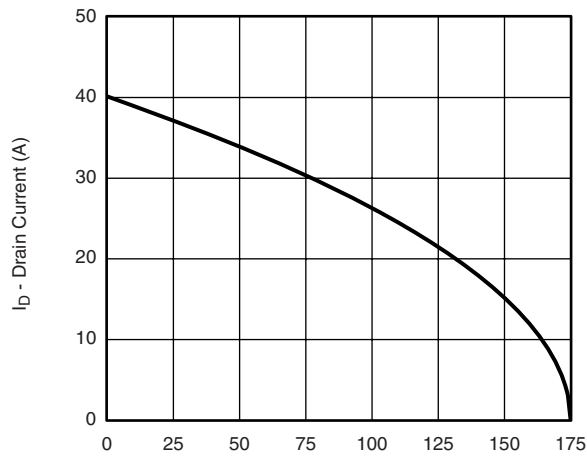
Single Pulse Power, Junction-to-Ambient



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

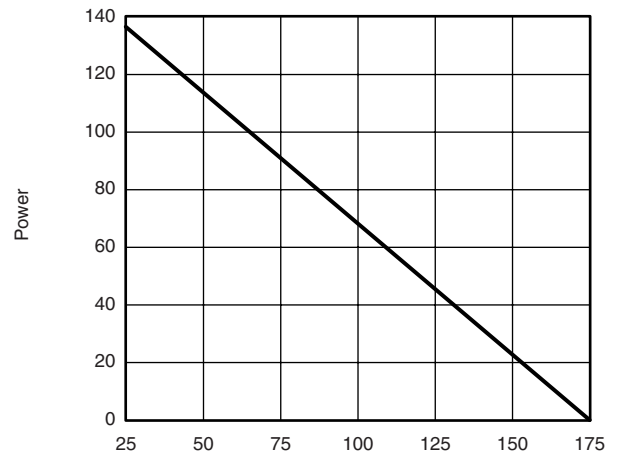
Safe Operating Area, Junction-to-Ambient

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



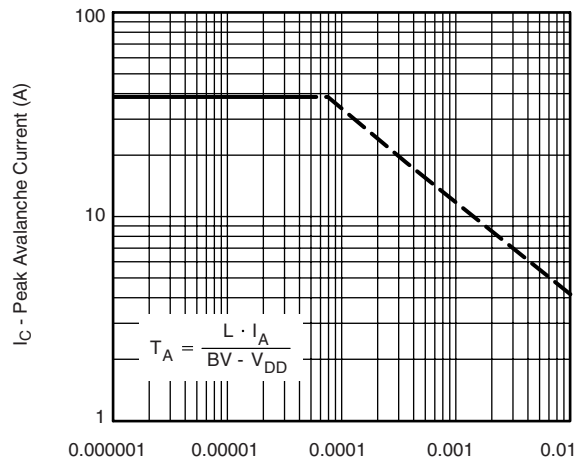
$T_C$  - Case Temperature (°C)

**Current Derating\***



$T_C$  - Case Temperature (°C)

**Single Pulse Power, Junction-to-Ambient**

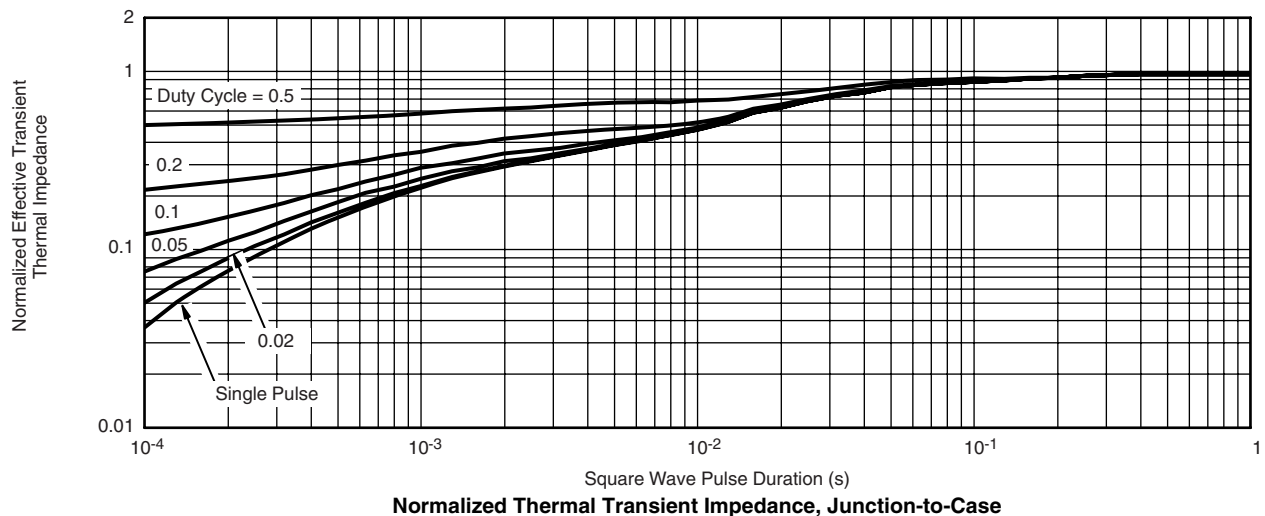
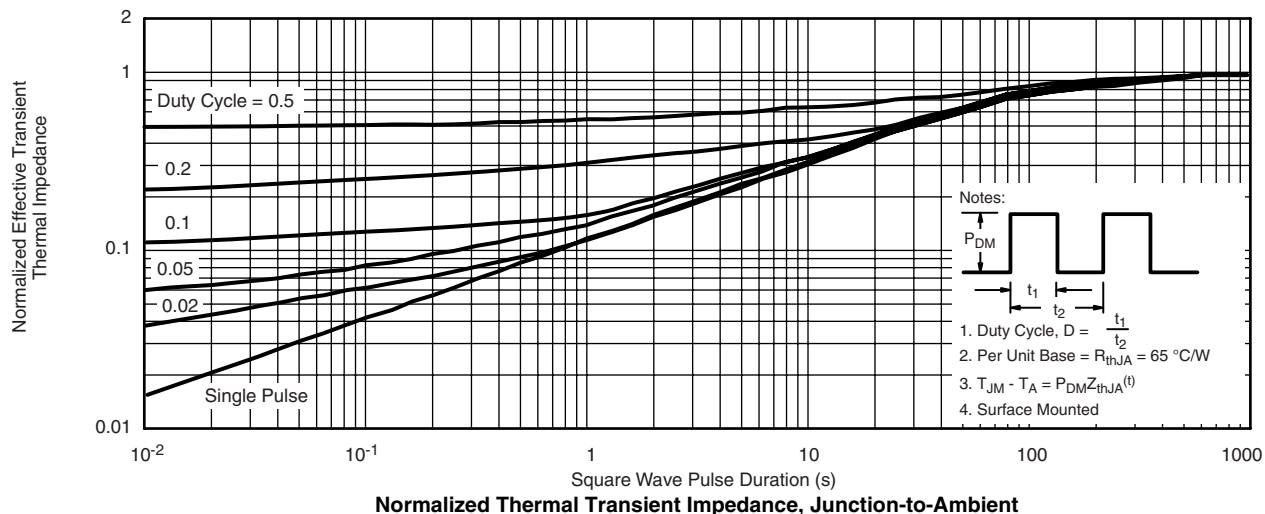


$T_A$  - Time In Avalanche (s)

**Single Pulse Avalanche Capability**

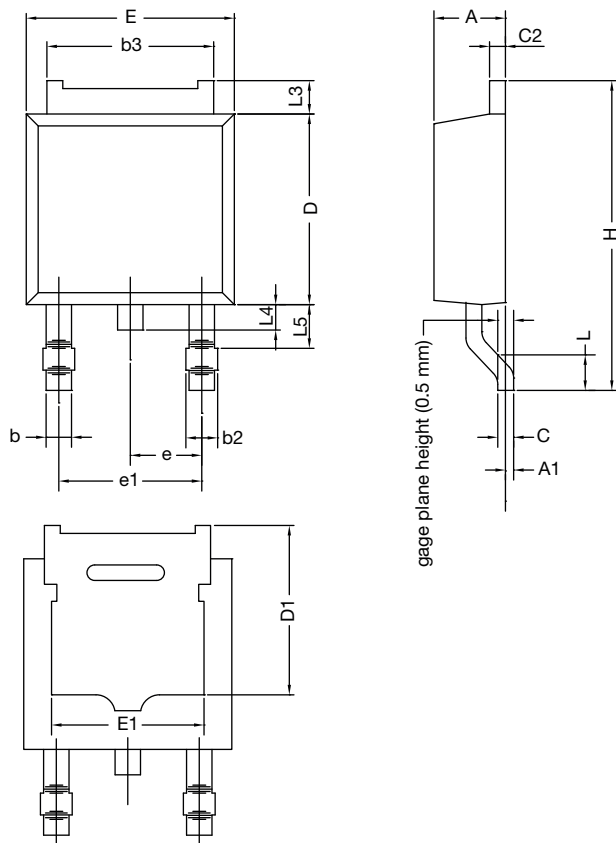
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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## TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

### Note

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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