

LV8968BB

LV8968BB Evaluation Board User's Manual

Overview

The LV8968BB evaluation board (EVB) provides a comprehensive platform to evaluate the LV8968BB functionalities for industrial and automotive applications. Maximum recommended power level is 250 W. Various optional periphery is included to support motor control implementations from simple sensor-less BEMF commutation, to complex field oriented algorithms. A microcontroller is NOT provided with this kit to allow customers to utilize their favorite solutions. The kit can be used as a shield to an Arduino DUE board.

Features

- General purpose Automotive 3Phase Gate Driver for 8 V to 25 V Applications
- Power MOSFET: 40 V, 85 A, 5.7 mΩ
- Interface to Microcontroller
- Plug-in Interface for Arduino Due Interface for Other Microcontrollers

Required:

- 20 V or Greater Power Supply with >10 A Output Current
- Arduino Due or
- Alternative Microcontroller Board with
 - ◆ 3 or more PWM Generators
 - ◆ 15 or more Digital IO Pins
 - ◆ 6 Analog IO Pins
 - ◆ 50pin Ribbon Cable and Connector
- 3 Phase PMSM Motor with 12 V Nominal Voltage and up to 200 W Power

Optional Periphery

- 7.5 V Regulator for Arduino Due or Other Microcontrollers
- Dual Current Sense Amplifier for Triple Shunt Current Sensing
- Star Point Comparator for BEMF Sensing Algorithms
- Low Voltage Charge Pump for Operation below 8 V
- PWM Oscillator plus Potentiometer for Speed Control Utilizing the PWM Interface of the LV8968
- Two Undedicated Pushbutton Switches for Microcontroller Use



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EVAL BOARD USER'S MANUAL



Figure 1. LV8968BB Evaluation Board

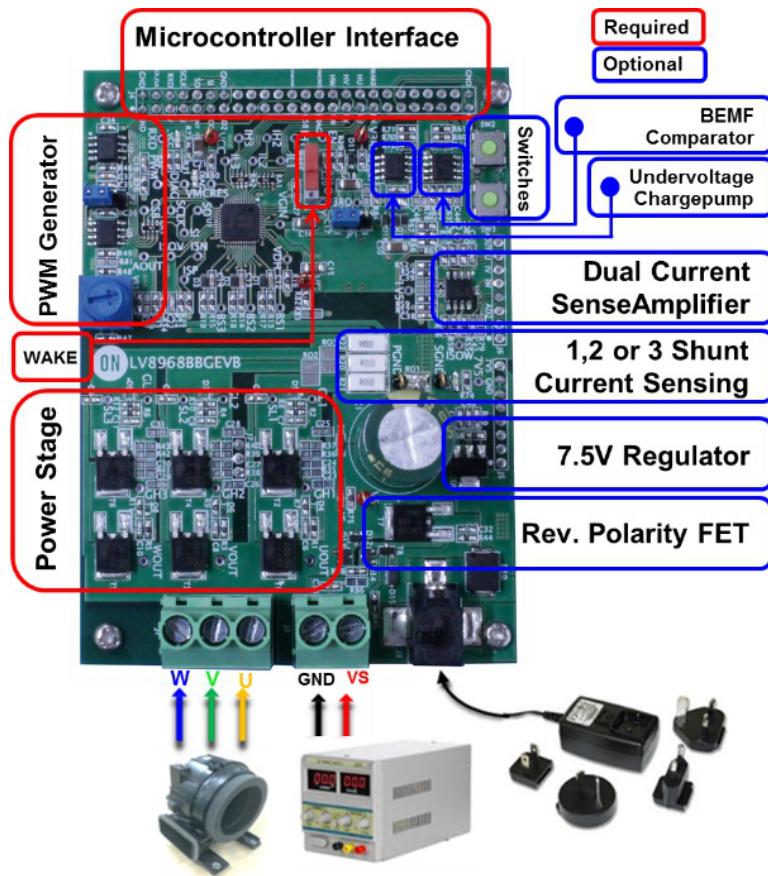


Figure 2. EVB Description

DETAILED DESCRIPTION

Power Up Initial Testing

The LV8968 EVB is designed to operate at 12 V (typ) with an operating voltage range from 8 V to 25 V. The power supply should be able to supply enough current to run the intended motor. If connected to an appropriate power supply either via the power Jack connector (J3), or the wire clamps (J2), the green VS LED and 7.5 V supply LED will light up.

Now it is possible to activate the LV8968 thought its WAKE pin using the red switch (SW1) in the center. The IC will power up with its default settings (for details consult the LV8968 Datasheet) and put out 3.3 V on its VCC supply (green VCC LED). The default settings are configured such that a microcontroller can instantly drive a motor. The IC will react to a high on the control lines and drive the corresponding power stage. Without a microcontroller to tell it what to do however, the LV8968 cannot accomplish much. Before proceeding further it is therefore necessary to power the EVB down and connect an appropriate microcontroller.

Table 1. POWER SUPPLY CURRENT

Power up procedure	Effect	Supply Current
Apply 12 V (typ) at J2 or J3	VS LEDs turns green, 7.5 V supply comes active and 7.5 V LED turns green	11 mA
Flip Wake switch SW1	V3RO and V3RI supply 3.3 V. VCC supply comes active and VCC LED turns green.	30 mA

Reverse Polarity Protection and Power Surges

The LV8968 EVB includes two reverse polarity protection circuits:

- Power jack connector J3 features a reverse polarity zener diode which is rated 3.9 A max. Power surges during motor braking or re-generation will not be fed

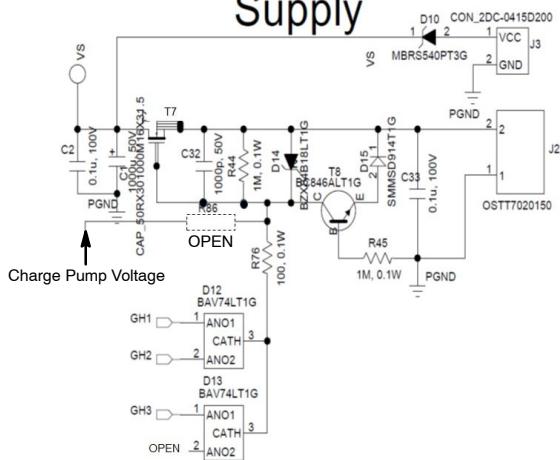
back into the supply and must be dealt with on the EVB by controlled braking, etc.

- Connector J2 bypasses the zener diode. This input is reverse polarity protected through the body diode of MOSFET T7 which is of the same type as an inverter. The gate of T7 is connected to a charge pump fed by inverter phases.

Once the LV8968 starts driving the power stage inverter, the switching of the phase voltages will charge the gate voltage of T7, turn on the MOSFET, and as a result bypass the reverse polarity body diode. Consequently a braking motor will feed its energy back into the supply. Once the motor is stopped, T7 will lose its gate charge and the reverse polarity protection will become active again.

Caution: When driving a high power load, ensure to make adequate arrangements to filter supply ripples.

Power Supply



NOTE: Reverse Polarity Protection MOSFET T7 gate voltage is selected by R76 or R86.
 R76 is Bootstrap voltage GH1–3.
 R86 is Charge Pump voltage.

Figure 3. Reverse Polarity Protection Schematic

Microcontroller Interface

Two microcontroller interfaces are available: an Arduino shield connection and a dual row pin header. The LV8968 is compatible with 3.3 V and 5 V level digital input signals. In order to bring the open drain outputs of the IC to the same level it may be necessary to raise the VCC voltage via SPI access from 3.3 V(default) to 5 V.

- Arduino Shield

The LV8968 EVB can act as an Arduino DUE shield and will plug directly onto an Arduino DUE board model R3-E. The Arduino board is then supplied from the EVB 7.5 V power supply and the pinout has been chosen to be supported by the Arduino peripheral circuitry.

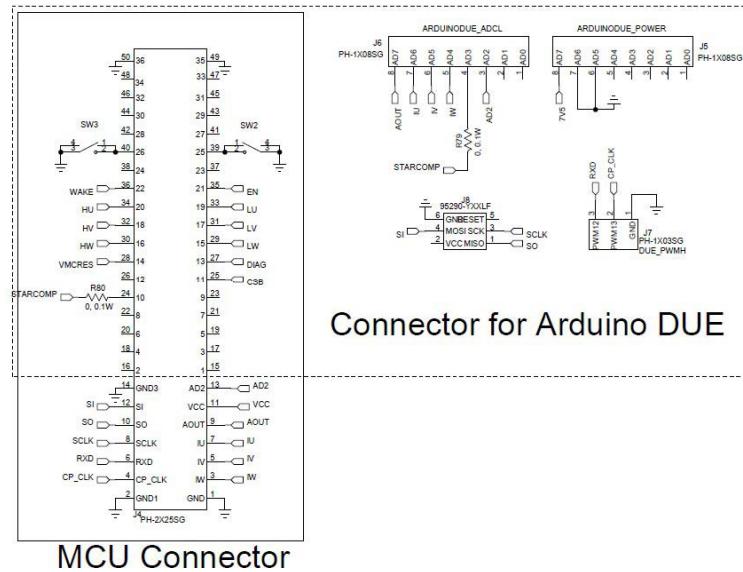
- Dual row 50 pin header (J4)

For users who prefer to use other microcontrollers, a 25x2 pin connector has been provided.

Pins are placed at 2.54 mm pitch, the exact connectivity depends on the microcontroller used and has to be configured by the user.

Table 2 below provides the pin mapping and descriptions for both solutions.

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MCU Connector

Figure 4. Arduino DUE and Pin Header Schematic

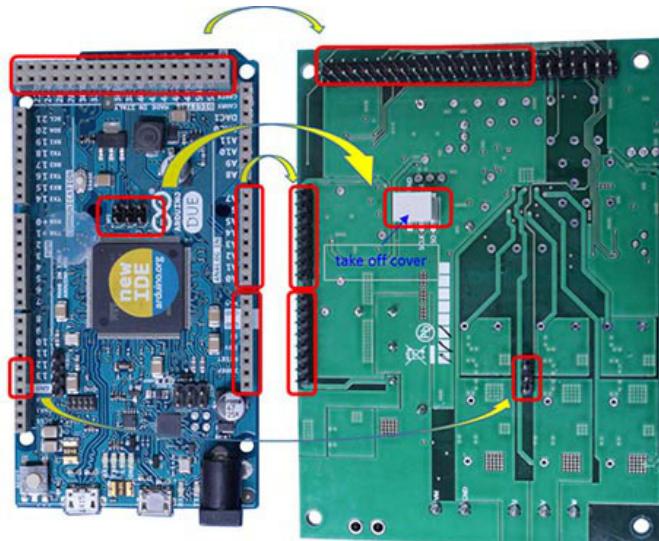


Figure 5. LV8968 Evaluation Board and Arduino DUE

LV8968BB

Table 2. ARDUINO DUE AND PIN HEADER MAPPING

Arduino Due SAM3X Evaluation Board					LV8968 EV-Kit					
Due Board Pin #	SAM3X Pin Name	Mapped Pin Name	Max Output Current (mA)	Max Current Sink (mA)	EVB Pin Name	J4 Connector Pin #	LV8968 Pin Name	LV8968 Pin #	Direction (relative to EVB)	Description
13	PB27	Digital Pin 13/ Amber LED "L"	3	6	CP_CLK	4			I	Clk (50 kHz) pin for optional Chargepump
14	PD4	TX3	15	9	RXD	6	RXD	10	O	Digital level pwm signal
30	PD9	Digital Pin 30	15	9	CSB	25	CSB	13	I	Active low SPI interface chip select
32	PD10	Digital Pin 32	15	9	DIAG	27	DIAG	9	O	Error and diagnostic output
33	PC1	Digital Pin 33	15	9	VMCRES	28	MCRE_S	8	O	Active low reset for watchdog
34	PC2	Digital Pin 34	15	9	LW	29	IL3	7	I	Active low GL3 control, Phase 3
35	PC3	Digital Pin 35	15	9	HW	30	IH3	6	I	Active high GH3 control, Phase 3
36	PC4	Digital Pin 36	15	9	LV	31	IL2	5	I	Active low GL2 control, Phase 2
37	PC5	Digital Pin 37	15	9	HV	32	IH2	4	I	Active high GH2 control, Phase 2
38	PC6	Digital Pin 38	15	9	LU	33	IL1	3	I	Active low GL1 control, Phase 1
39	PC7	Digital Pin 39	15	9	HU	34	IH1	2	I	Active high GH1 control, Phase 1
40	PC8	Digital Pin 40	15	9	EN	35	EN	46	I	Enable pin for inverter
41	PC9	Digital Pin 41	15	9	WAKE	36	WAKE	44	IO	Wake for LV8968 can be read or driven
44	PC19	Digital Pin 44	15	9	SW2	39			O	Pushbutton to GND (needs pullup)
45	PC18	Digital Pin 45	15	9	SW3	40			O	Pushbutton to GND (needs pullup)
56	PC23	Analog In 2	3	6	AD2	13			O	Analog output of Potentiometer
57	PC22	Analog In 3	3	6	STARCOMP	24			O	Output of star point comparator
58	PA6	Analog In 4	3	6	IU	7			O	Current of Phase U (ext. Amp)
59	PA4	Analog In 5	3	6	IV	5	ISO	20	O	Current of Phase V
60	PA3	Analog In 6	3	6	IW	3			O	Current of Phase W (ext. Amp)
61	PA2	Analog In 7	3	6	AOUT	9	AOUT	19	O	Analog BEMF, VDH sense pin
74	PA25	(MISO)	15	9	SO	10	SO	16	I	SPI master data in
75	PA26	(MOSI)	15	9	SI	12	SI	15	O	SPI master data out
76	PA27	(SCLK)	15	9	SCLK	8	SCLK	14	I	SPI clock

System Control

The LV8968 is configured by default to make it easy to control a motor without any SPI setup. To activate the motor power stage it is necessary to apply a high signal on EN along with the phase control signals. Be aware that the low side FETs are activated by low levels, while the high side signals are activated by high levels. A low on EN will disable the output stage.

In default state all errors are disabled and dead time is set at maximum (3.2 us) which can interfere with efficient motor drive. To gain control over the system parameters it is necessary to communicate via SPI interface. The SPI interface expects full duplex communication. Data is latched at the rising clock edge and should change at the falling clock edge. The CSB signal must go high after every data transmission. For further information consult the LV8968 datasheet.

To enable useful motor applications with this EVB, two pushbutton switches SW2 and SW3 are provided, as well as a PWM generator with a potentiometer for PWM control. See below for more information on their use.

System Monitoring

The red KEY switch (SW1) is provided to tie WAKE to VS. A high on WAKE activates the LV8968 from sleep mode. VCC goes high which would normally power up the external microcontroller. For the EVB this approach was not practical, so WAKE as well as 7V5 are brought out to the interface to be monitored by the microcontroller. (It is possible to drive WAKE from the microcontroller if it is not pulled high via SW1). In a typical motor application WAKE might be tied to the ignition key signal. In order to prevent a low on WAKE from disabling the system and the motor, the LV8968 will ignore WAKE as long as EN is held high by the microcontroller.

Two other important system signals should be monitored closely by the microcontroller: DIAG and VMCRES. DIAG will go low for system errors and warnings, while a low on VMCRES indicates a watchdog violation. The watchdog is initially disabled and must be activated by SPI access. In the final application VMCRES should be connected to the microcontroller master reset, on the EVB this is not practical as watchdog errors will interfere with programming and debug operations.

7.5 V Regulator (U6)

Power to the microcontroller board is provided by the on-board linear regulator NCV317M which supplies 7.5 V and up to 500 mA to:

- The 7.5 V LED
- The optional charge pump
- The PWM generator
- The Arduino DUE board

7.5V Regulator

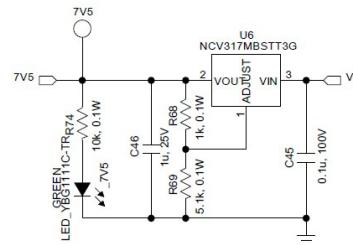


Figure 6. 7.5 V Regulator Schematic

PWM Generator (U2, U3)

Motor control applications are typically controlled via a PWM signal. This EVB allows two ways to generate a motor control PWM:

1. An external PWM signal can be fed directly to the PWM pin which is right next to the PWM generator circuit. This pin has a pullup to VS so it can be driven from a function generator as well as an open drain/collector transistor. To activate external PWM control place jumper JP2 (next to the PWM circuit) from pin1 to pin3.

2. Per default, an on board PWM generator will supply a VS level 100 Hz PWM signal to the LV8968. The blue Potentiometer VR1 controls the duty cycle from 0% to 100%.

In either case, the LV8968 level shifts the high voltage PWM signal to a digital VCC level signal which appears on RXD to be decoded by the microcontroller. See Figure 7 for details. The analog output of the potentiometer AD2 also appears at the microcontroller interface to be measured directly.

PWM OSC

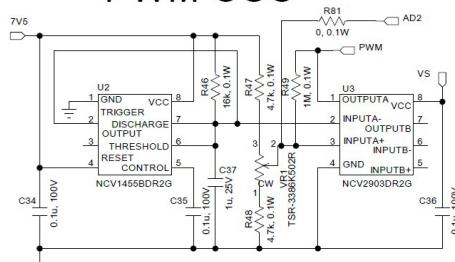


Figure 7. PWM Generator Schematic

Switches (SW2, SW3)

Two pushbutton switches to GND are included on the EVB to provide some additional motor control user interface. They can be used for motor ON/OFF and direction changes, or to cycle through demo programs, etc. These switches require microcontroller ports with pullup to function properly.



Figure 12. Jumper Switch JP1

3. External Charge Pump for 100% Output Duty

The evaluation board includes an undervoltage chargepump which can optionally be re-configuration to serve as a 100% duty cycle chargepump. For this conversion the comparator NCV33202V at U7 needs to be replaced with a rail to rail comparator NCS20072 with higher output drive. Also diodes D16 and D17 need to be replaced with Schottky types. To see the detailed description of the modifications consult Figures 15 and 16.

The 52 kHz clock signal for the chargepump CP_CLK needs to be provided by the microcontroller via J4 connector pin 4 or Arduino Due pin 13. This can be activated on demand depending on the use case:

1. Under-voltage Chargepump: Activate only during under-voltage. Keeping the chargepump running during normal operation may cause overvoltage damage to the circuit.
2. 100% duty-cycle chargepump: Operate during EN=high but disable during VH overvoltage to prevent overvoltage damage to the circuit.

Figure 13 shows the characteristic chart of the charge pump for 100% drive.

VGIN: VGIN=VS voltage

VG: Power supply pin for (JP1 1 and 2 pin short) low side gate drive the amplifier U7 is changed from NCV33202V to NCS20072.

BS: Charge pump circuit output for high side gate drive.

VGSH: High side gate voltage is 9.5 V at VS=12 V.

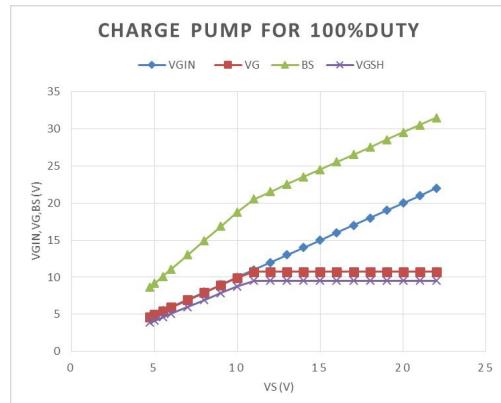


Figure 13. Charge Pump Characteristic Chart

Jumper switch JP1 set to connect 1 pin and 2 pin.



Figure 14. Jumper Switch JP1

Charge Pump

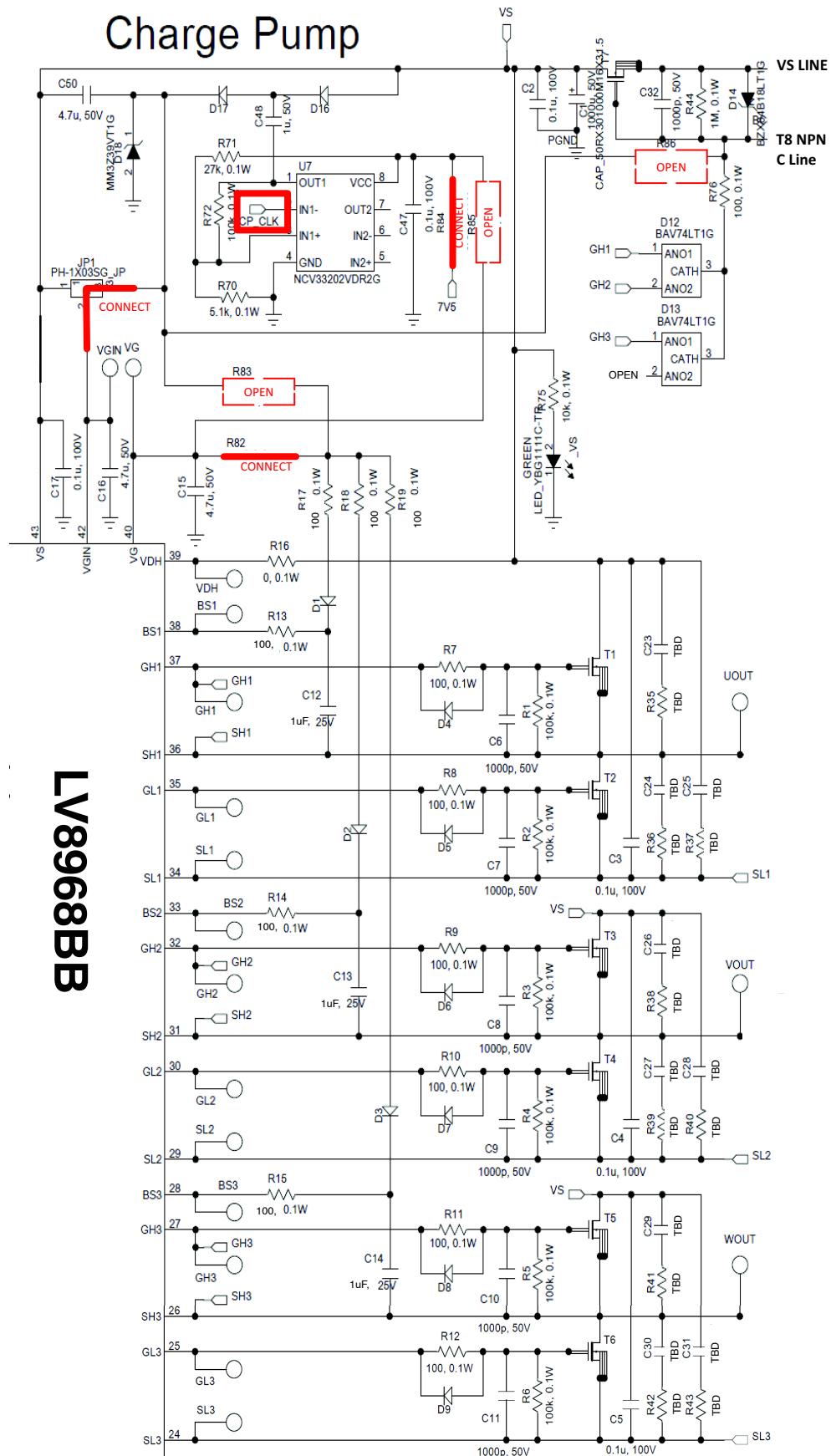


Figure 15. Bootstrap Type Layout of Evaluation Board Schematic

Charge Pump

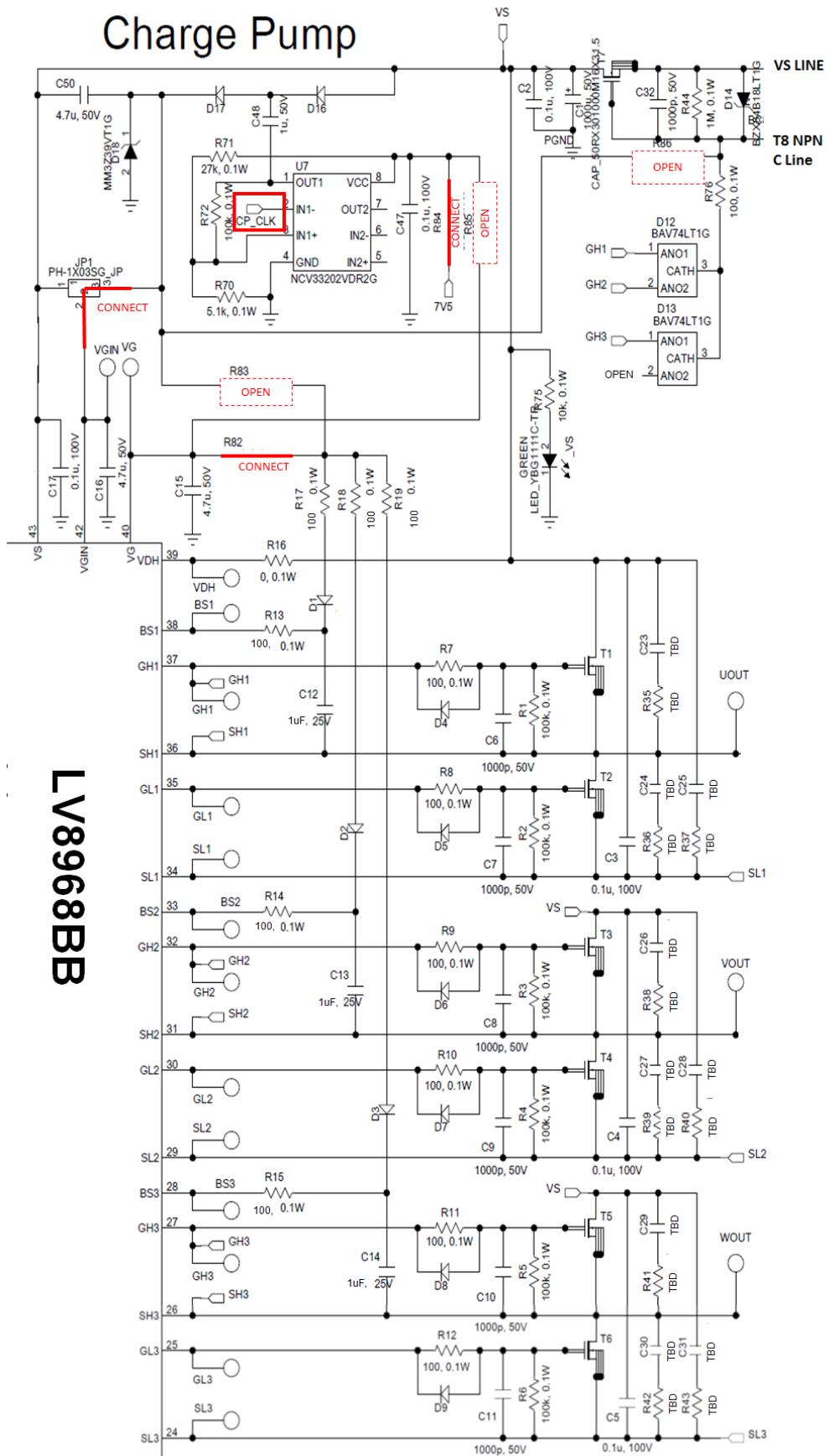


Figure 16. Under Voltage Charge Pump Configuration Schematic

Charge Pump

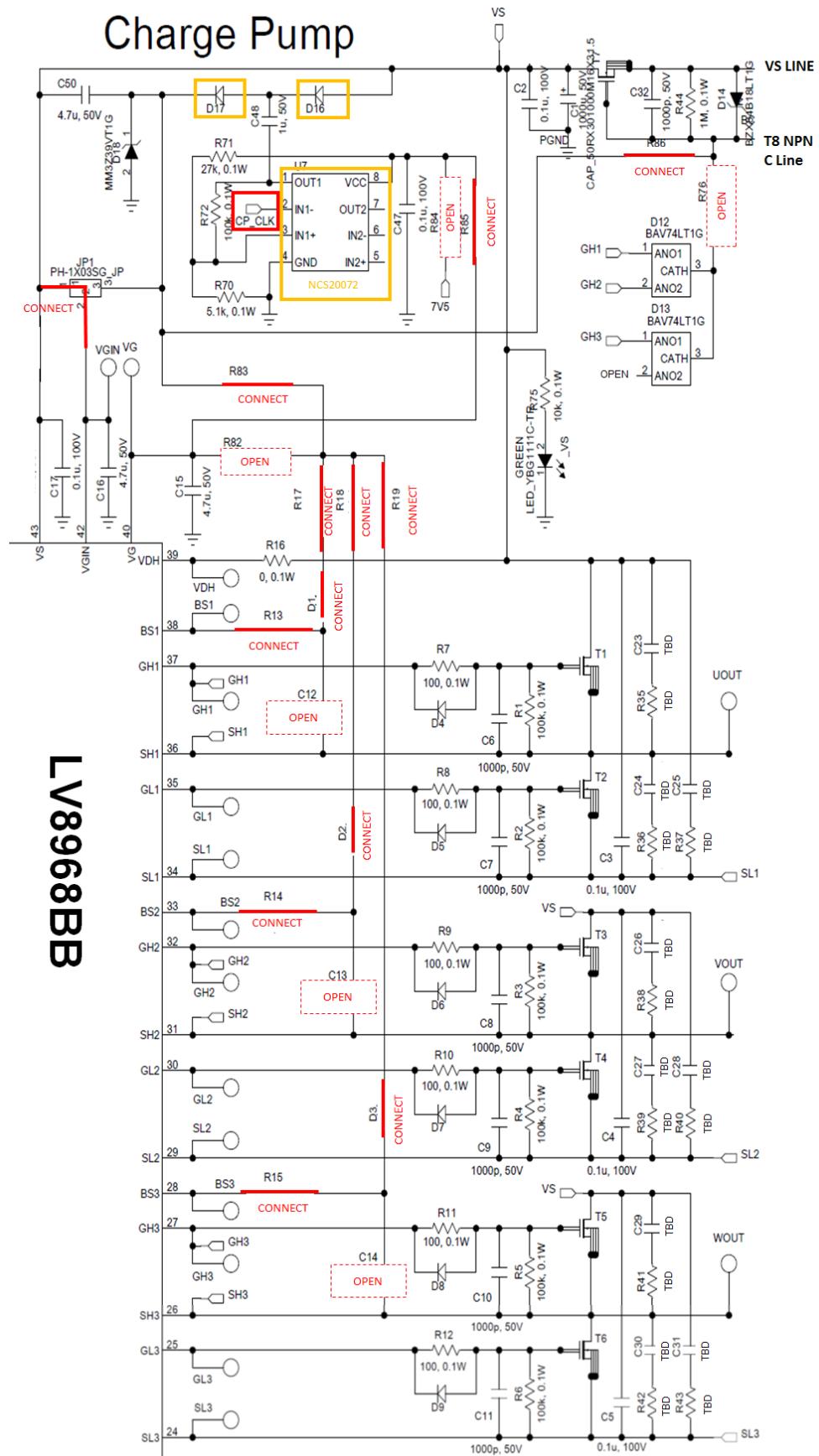


Figure 17. External Charge Pump for 100% Output Duty Cycle Schematic

POWER STAGE (T1 – T6)

The sole purpose of the LV8968 is to help a microcontroller drive and monitor the six N-MOSFET power stage in a three-phase inverter configuration. The FETs are 40 V, 85 A NVD5803NT4G with 5.7 mΩ typical on resistance. The FET footprint allows placement of D2PAK or SO8FL packages. The maximum power dissipation is 83 W ($R_{\Theta jc}, T_C = 25^\circ\text{C}$, see [NVD5803NT4G](#) data sheet).

NOTE: MOSFET may be changed by application unit or end of FET production. The user may change the MOSFET type depending on their need.

Figure 18 below shows the schematic of phase U as an example. The gate is driven through gate resistors (R7, R8). Between gate and source of each MOSFET, capacitors (C6, C7) are provided to adjust turn ON time with the gate resistor, and OFF time with gate diodes (D4, D5 not installed). Pull-down resistors (R1, R2) help protect the inverter against unintentional turn-on when the LV8968 is in sleep mode. A number of (unpopulated) snubber placements are also provided across the MOSFETs, to suppress parasitic ringing if necessary. The high-side gate voltage is generated by a capacitive bootstrapping circuit connection between each phase and the supply of the high-side drivers. The bootstrap capacitors are charged from the gate supply during the falling edge of the phase.

NOTE: It is important to start a motor with all phases low, to charge the bootstrap circuit.

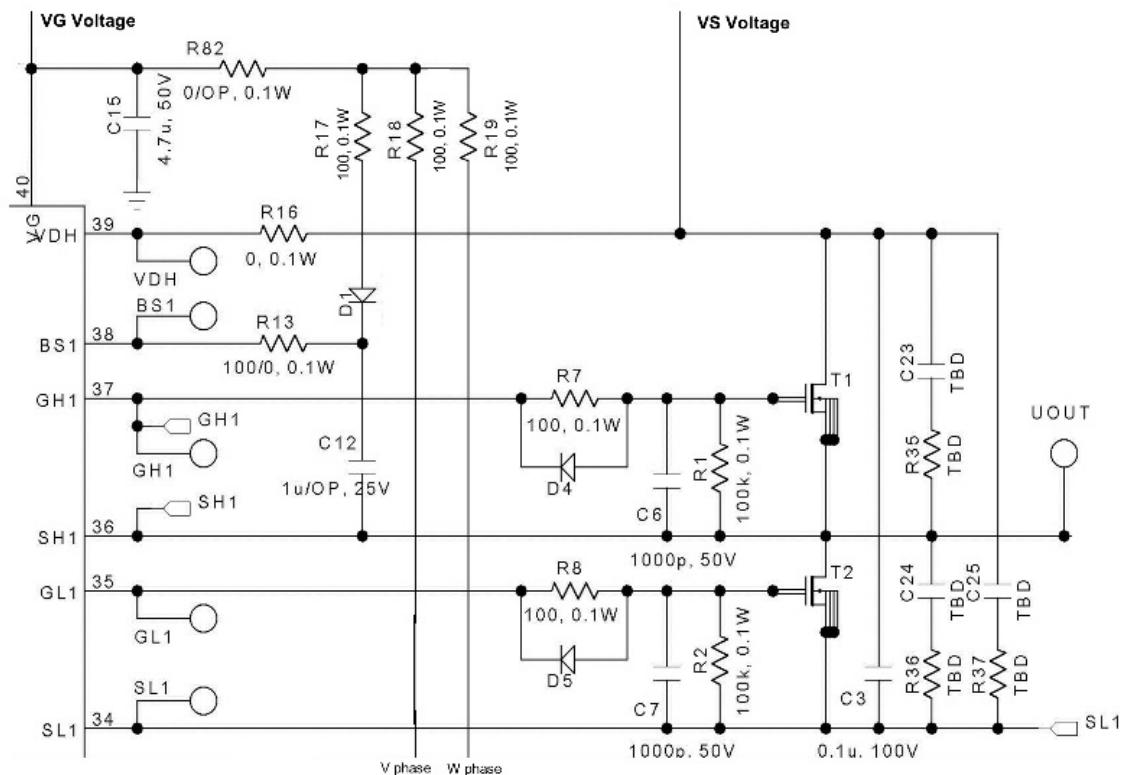


Figure 18. High and Low Side Gate Output Schematic

Shunt Resistance Operation

The EVB facilitates low side shunt current measurement of the three phase currents across shunt resistors R20,21,22. The LV8968BB includes a single programmable gain current sense amplifier which measures the motor current across the center resistor R20. Two additional current sense amplifiers are included on the EVB to measure the currents on the outside resistors. These amplifiers are configured for fixed a gain of 17 with external resistors matching the default gain of the internal amplifier of 7.5. If other gains are desired the resistors need to be reconfigured. See Table 2 for pin locations where the currents can be sampled.

The internal current amplifier of the LV8968BB is capable of single shunt FOC measurements. To enable single shunt current sensing short the solder jumpers RO2 and RO3 as shown in Figure 20. Now the resistance can be adjusted with the parallel configuration R20,21 and 22.

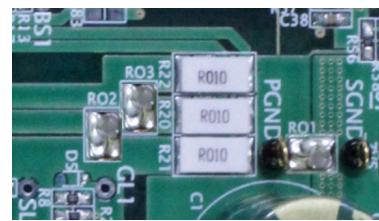


Figure 19. One Shunt Resistance Detection

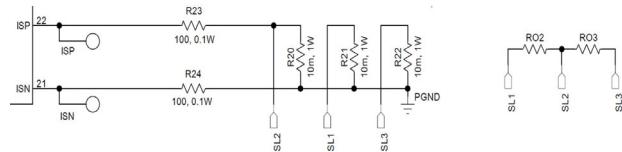


Figure 20. Shunt Resistor Detection Schematic

LV8968BB GEVB v1.0

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7.5V Regulator

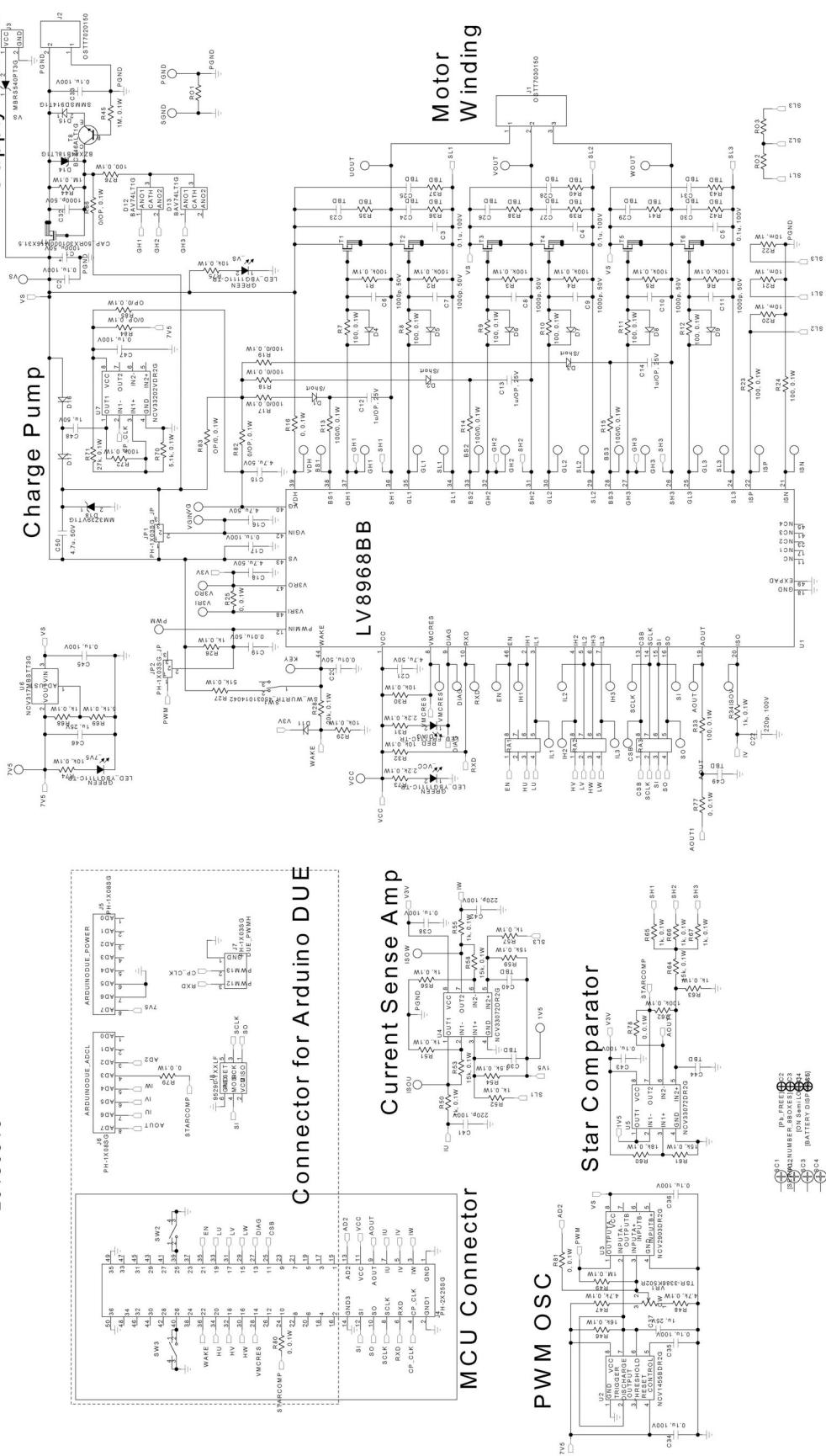


Figure 21. LV8968BB Evaluation Board Schematic

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Table 3. BILL OF MATERIALS FOR THE LV8968BB DEMO BOARD V1.0

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Part Number	Boot strap	Charge pump
U1	1	Multi-purpose BLDC Pre-driver			SQFP48K	ON Semiconductor	LV8968BB	on	on
U2	1	Timer			SOIC-8	ON Semiconductor	NCV1455BDR2G		
U3	1	Comparator			SOIC-8	ON Semiconductor	NCV2903DR2G		
U4-5	2	Dual operational amplifier			SOIC-8	ON Semiconductor	NCV33072DR2G		
U6	1	Voltage Regulator			SOT-223	ON Semiconductor	NCV317MBSTT3G		
U7	1	Dual operational amplifier			SOIC-8	ON Semiconductor	NCV33202VDR2G		
J1	1	Motor winding connector			Pitch 6.35 mm	ON-SHORE	OSTT7030150		
J2	1	Power supply connector			Pitch 6.35 mm	ON-SHORE	OSTT7020150		
J3	1	AC-DC adapter connector				Singatron	2DC-0415D200		
J4	1	EXT MCU connector			Pitch 2.54 mm	Useconn	PH-2x25SG		
J5	1	DUE POWER connector			Pitch 2.54 mm	Useconn	PH-1x40SG		
J6	1	DUE ADCL connector			Pitch 2.54 mm	Useconn	PH-1x40SG		
J7	1	DUE PWMH connector			Pitch 2.54 mm	Useconn	PH-1x40SG		
J8	1	SPI header			Pitch 2.54 mm	Amphenol FCI	95290-303ALF		
JP1-2	2	Jumper SW			Pitch 2.54 mm	Useconn	PH-1x40SG		
T1-7	7	N-ch power MOSFETs			DPAK	ON Semiconductor	NVD5803NT4G	on	on
T8	1	NPN TRANSISTOR			SOT-23	ON Semiconductor	BC846ALT1G		
D1-3 D11 D16-17	6	Diode			SOD-323	ON Semiconductor	MMDL6050T1G		
D4-9	6	Diode			SOD-323	ON Semiconductor	MMDL6050T1G	off	off
D10	1	Schottky diode			SMC	ON Semiconductor	MBRS540PT3G		
D12-13	2	Dual diode			SOT-23	ON Semiconductor	BAV74LT1G		
D14	1	ZENER-DIODE	18 V		SOT-23	ON Semiconductor	BZX84B18LT1G		
D15	1	Diode			SOD-123	ON Semiconductor	SMMSD914T1G		
D18	1	ZENER-DIODE	39 V		SOD-323	ON Semiconductor	MM3Z39VT1G		
SW1	1	Switch for WAKE			Pitch 2.54 mm	WURTH	45031014042		
SW2-3	2	Push button switch			6.5x6.2 mm	Omron	B3SL-1002P		
VR1	1	Potentiometer			10x10mm	SUNTAN	TSR-3386K502R		
_DIAG	1	LED	RED		1608 BIG	STANLEY	FR1111C-TR		
_VCC_VS _7V5	3	LED	GREEN		1608 BIG	STANLEY	YBG1111C-TR		
C1	1	Electrolytic CAP.	1000u, 50V	±20%	Pitch 7.5 mm	RUBYCON	50RX301000M16X31.5		
C2-5 C17 C33-36 C38 C43 C45 C47	13	Capacitor	0.1u, 100V	±10%	1608 BIG	MURATA	GRM188R72A104K		
C6-11 C32	7	Capacitor	1000p, 50V	±5%	1608 BIG	MURATA	GRM1882C1H102J		
C12-14 C37 C46	5	Capacitor	1u, 25V	±10%	1608 BIG	MURATA	GRM188B31E105K		
C15-16 C18 C21 C50	5	Capacitor	4.7u, 50V	±10%	3216 BIG	MURATA	GRM31CB31H475K		
C19-20	2	Capacitor	0.01u, 50V	±10%	1608 BIG	MURATA	GRM188B11H103K		

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Table 3. BILL OF MATERIALS FOR THE LV8968BB DEMO BOARD V1.0 (continued)

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Part Number	Boot strap	Charge pump
C22 C41-42	3	Capacitor	220p, 100V	$\pm 10\%$	1608 BIG	MURATA	GRM188R72A104K		
C23-31	9	Capacitor	TBD, 50V	$\pm 5\%$	1608 BIG	MURATA		off	off
C39-40 C44 C49	4	Capacitor	TBD, 50V	$\pm 10\%$	1608 BIG	MURATA		off	off
C48	1	Capacitor	1u, 50V	$\pm 10\%$	2012 BIG	MURATA	GRM21BR71H105K		
R1-6 R62 R72	8	Resistor	100k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R7-15 R17-19 R23-24 R33 R76	16	Resistor	100, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R16 R25 R77	3	Resistor	0, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R20-22	3	Current sense resistors	10m, 1W	$\pm 1\%$		SUSUMU	KRL3264-C-R010-F-T1		
R26 R34 R50-52 R55-57 R63 R65-68	13	Resistor	1k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R27	1	Resistor	51k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R28	1	Resistor	20k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R29-30 R32 R74-75	5	Resistor	10k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R31 R73	2	Resistor	2.2k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R35-43	9	Resistor	TBD, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ	off	
R44-45 R49	3	Resistor	1M, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R46	1	Resistor	16k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R47-48	2	Resistor	4.3k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R53-54 R58-59 R61 R64	6	Resistor	15k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R60	1	Resistor	18k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R69-70	2	Resistor	5.1k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R71	1	Resistor	27k, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R78-81	4	Resistor	0, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ	off	on
R82 R84	2	Resistor	0, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ		
R83 R85-86	3	Resistor	OP/0, 0.1W	$\pm 5\%$	1608 BIG	KOA	RK73B1JTxxxJ	off	on
RA1-3	3	Resistor Array	33 Ω	$\pm 5\%$		Bourns	CAY16-330J4LF		
RO1	1	Solder JP			4030				
RO2-3	2	Solder JP	0 Ω		4030				

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Board Layout

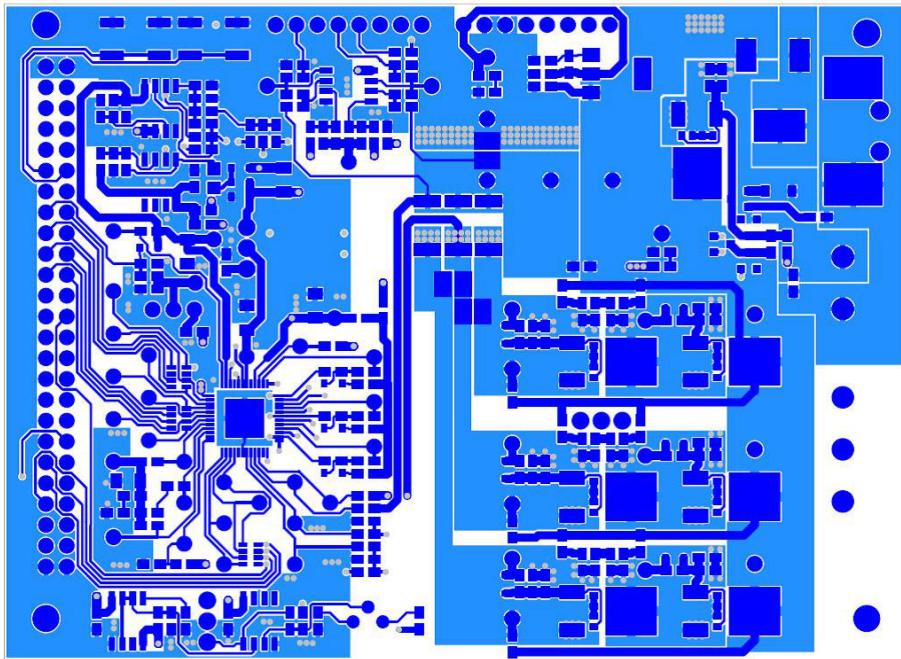


Figure 22. LV8968BB Evaluation Board Layout TOP

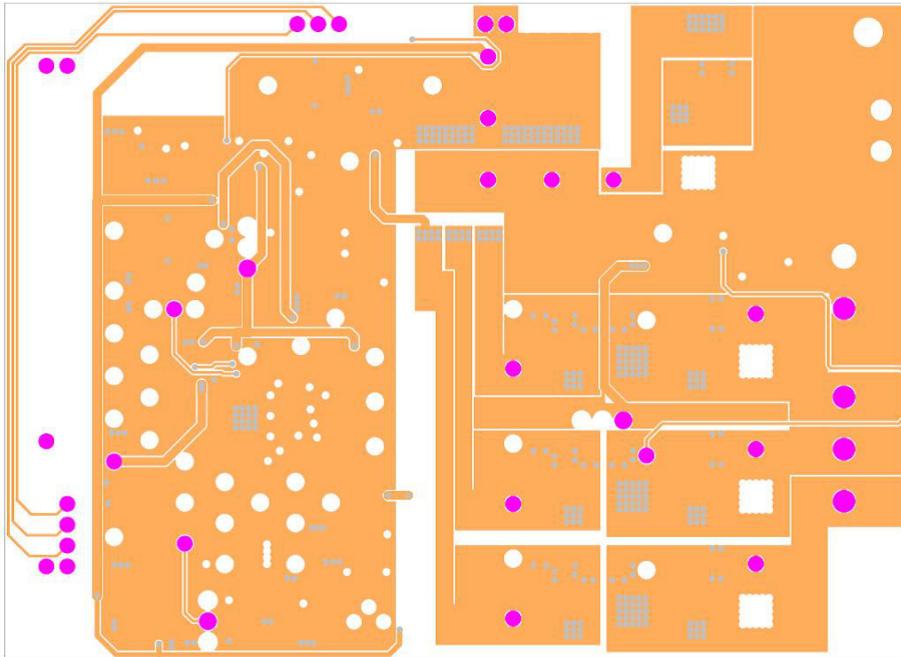


Figure 23. LV8968BB Evaluation Board Layout 2nd Layer

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Board Layout (continued)

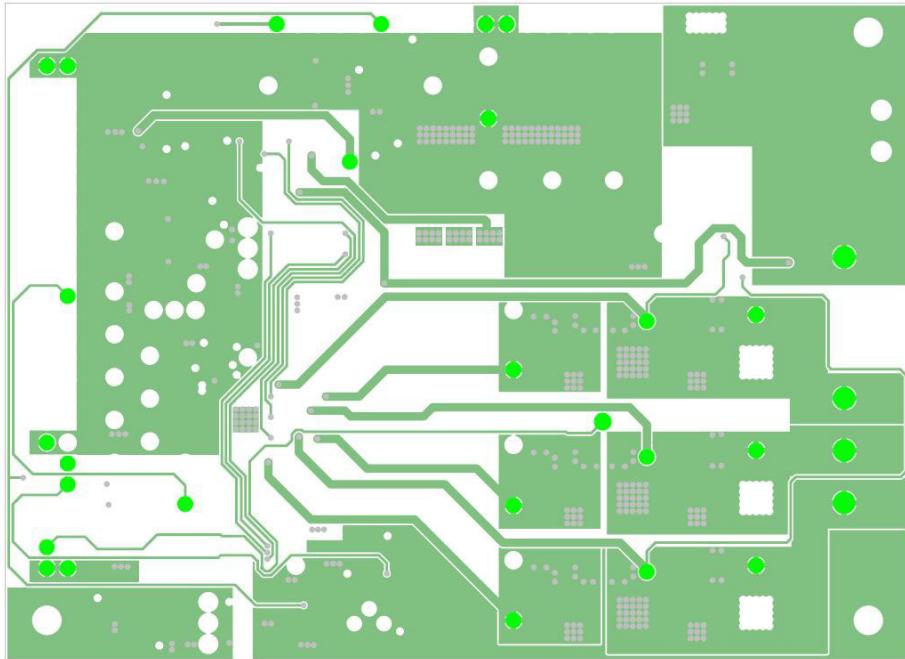


Figure 24. LV8968BB Evaluation Board Layout 3rd Layer

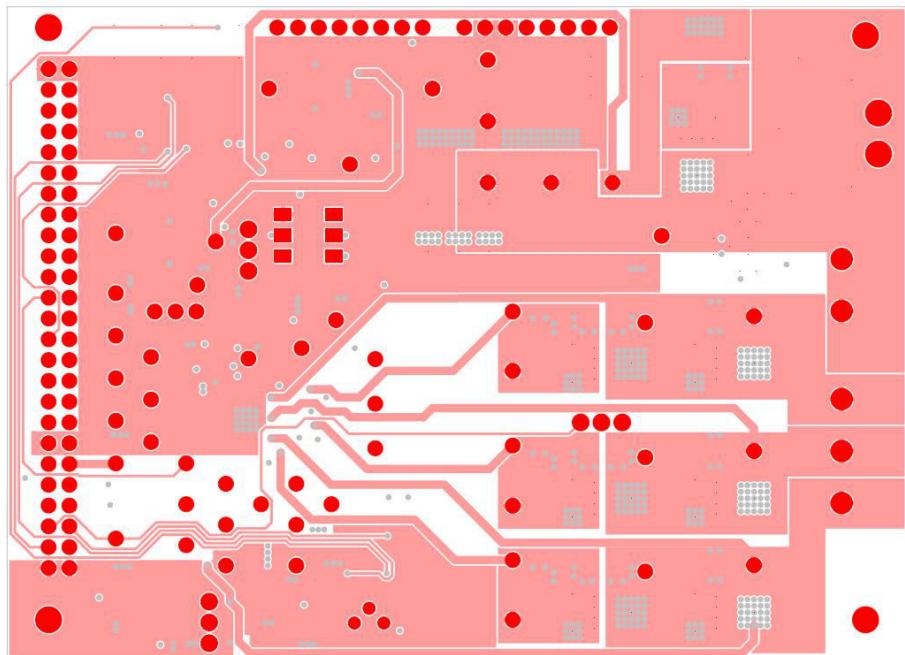


Figure 25. LV8968BB Evaluation Board Layout Bottom Layer

Board Layout (continued)

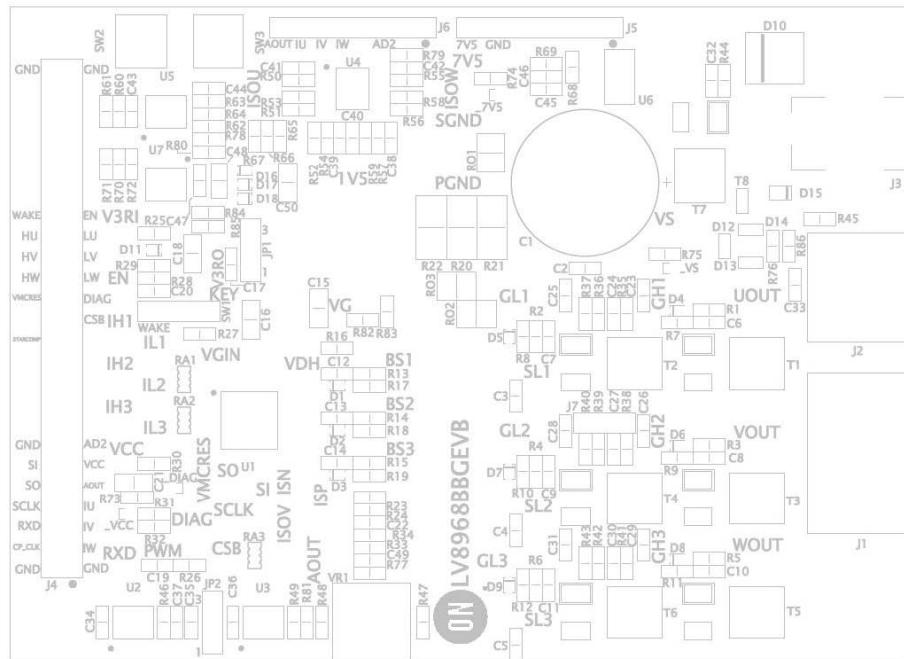


Figure 26. LV8968BB Evaluation Board Layout Silk Name

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