

# FOD2200

## Low Input Current Logic Gate Optocouplers

### Features

- 1kV/ $\mu$ s minimum common mode rejection
- Compatible with LSTTL, TTL, and CMOS logic
- Wide  $V_{CC}$  range (4.5V to 20V)
- 2.5Mbd guaranteed over temperature
- Low input current (1.6mA)
- Three state output (no pullup resistor required)
- Guaranteed performance from 0°C to 85°C
- Hysteresis
- Safety and regulatory approved
  - UL1577, 5000  $V_{RMS}$  for 1 min.
  - IEC60747-5-2
- >8.0mm clearance and creepage distance (option 'T' or 'TS')
- 1,414V Peak Working Insulation Voltage ( $V_{IORM}$ )

### Applications

- Isolation of high speed logic systems
- Computer peripheral interfaces
- Microprocessor system interfaces
- Ground loop elimination
- Pulse transformer replacement
- Isolated bus driver
- High speed line receiver

### Description

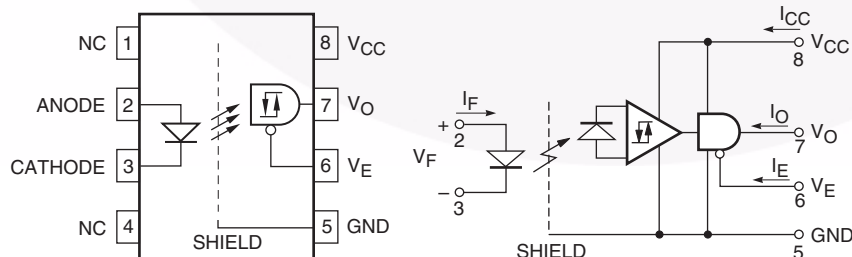
The FOD2200 is an optically coupled logic gate that combine an AlGaAs LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

The Electrical and Switching Characteristics of the FOD2200 are guaranteed over the temperature range of 0°C to 85°C and a  $V_{CC}$  range of 4.5V to 20V. Low  $I_F$  and wide  $V_{CC}$  range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed opto-couplers. Logic signals are transmitted with a maximum propagation delay of 300ns. The FOD2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

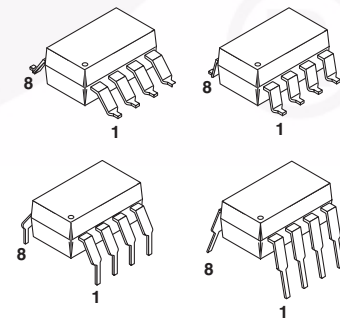
### Truth Table (Positive Logic)

| LED | Enable | Output |
|-----|--------|--------|
| On  | H      | Z      |
| Off | H      | Z      |
| On  | L      | H      |
| Off | L      | L      |

### Functional Block Diagram and Schematic



### Package Outlines



## Safety and Insulation Ratings

As per IEC 60747-5-2. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

| Symbol         | Parameter  | Min.   | Typ.     | Max. | Unit       |
|----------------|--|--------|----------|------|------------|
|                | Installation Classifications per DIN VDE 0110/1.89 Table 1   |        |          |      |            |
|                | For Rated Mains Voltage < 150Vrms  |        | I-IV     |      |            |
|                | For Rated Mains Voltage < 300Vrms  |        | I-IV     |      |            |
|                | For Rated Mains Voltage < 450Vrms  |        | I-III    |      |            |
|                | For Rated Mains Voltage < 600Vrms  |        | I-III    |      |            |
|                | For Rated Mains Voltage < 1000Vrms (Option T, TS)  |        | I-III    |      |            |
|                | Climatic Classification  |        | 40/85/21 |      |            |
|                | Pollution Degree (DIN VDE 0110/1.89)   |        | 2        |      |            |
| CTI            | Comparative Tracking Index   | 175    |          |      |            |
| $V_{PR}$       | Input to Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec., Partial Discharge < 5pC | 2651   |          |      |            |
|                | Input to Output Test Voltage, Method a, $V_{IORM} \times 1.5 = V_{PR}$ , Type and Sample Test with $t_m = 60$ sec., Partial Discharge < 5 pC | 2121   |          |      |            |
| $V_{IORM}$     | Max Working Insulation Voltage   | 1,414  |          |      | $V_{peak}$ |
| $V_{IOTM}$     | Highest Allowable Over Voltage   | 6000   |          |      | $V_{peak}$ |
|                | External Creepage  | 8      |          |      | mm         |
|                | External Clearance   | 7.4    |          |      | mm         |
|                | External Clearance (for Option T or TS - 0.4" Lead Spacing)  | 10.16  |          |      | mm         |
|                | Insulation Thickness   | 0.5    |          |      | mm         |
|                | Safety Limit Values – Maximum Values Allowed in the Event of a Failure   |        |          |      |            |
| $T_{Case}$     | Case Temperature   | 150    |          |      | °C         |
| $I_{S,INPUT}$  | Input Current  | 10     |          |      | mA         |
| $P_{S,OUTPUT}$ | Output Power (Duty Factor $\leq 2.7\%$ )   | 150    |          |      | mW         |
| $R_{IO}$       | Insulation Resistance at $T_S$ , $V_{IO} = 500V$   | $10^9$ |          |      | $\Omega$   |

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol          | Parameter   | Value          | Units            |
|-----------------|---|----------------|------------------|
| $T_{STG}$       | Storage Temperature   | -40 to +125    | $^\circ\text{C}$ |
| $T_{OPR}$       | Operating Temperature   | -40 to +85     | $^\circ\text{C}$ |
| $T_{SOL}$       | Lead Solder Temperature (1.6mm below seating plane)                       | 260 for 10 sec | $^\circ\text{C}$ |
| <b>EMITTER</b>  |   |                |                  |
| $I_F(PK)$       | Peak Transient Input Current ( $\leq 1\mu\text{s}$ PW, 300pps)            | 1.0            | A                |
| $I_F$           | Average Forward Input Current   | 10             | mA               |
| $V_R$           | Reverse Input Voltage   | 5.0            | V                |
| $P_D$           | Output Power Dissipation (No derating required up to $85^\circ\text{C}$ ) | 45             | mW               |
| <b>DETECTOR</b> |   |                |                  |
| $V_{CC}$        | Supply Voltage  | 0 to 20        | V                |
| $I_O$           | Average Output Current  | 25             | mA               |
| $V_E$           | Three State Enable Voltage  | -0.5 to 20     | V                |
| $V_O$           | Output Voltage  | -0.5 to 20     | V                |
| $P_D$           | Output Power Dissipation (No derating required up to $85^\circ\text{C}$ ) | 150            | mW               |

**Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol       | Parameter                  | Min. | Max. | Units            |
|--------------|----------------------------|------|------|------------------|
| $I_{F(ON)}$  | Forward Input Current      | 1.6* | 5    | mA               |
| $I_{F(OFF)}$ | Forward Input Current      |      | 0.1  | mA               |
| $V_{CC}$     | Supply Voltage, Output     | 4.5  | 20   | V                |
| $V_{EL}$     | Enable Voltage, LOW Level  | 0    | 0.8  | V                |
| $V_{EH}$     | Enable Voltage, HIGH Level | 2.0  | 20   | V                |
| $T_A$        | Operating Temperature      | 0    | +85  | $^\circ\text{C}$ |
| N            | Fan Out (TTL Load)         |      | 4    |                  |

\*The initial switching threshold is 1.6mA or less. It is recommended that 2.2mA be used to permit at least a 20% CTR degradation guardband.

**Electrical Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $20\text{V}$ ,  $I_{F(ON)} = 1.6\text{mA}$  to  $5\text{mA}$ ,  $V_{EH} = 2\text{V}$  to  $20\text{V}$ ,  $V_{EL} = 0\text{V}$  to  $0.8\text{V}$ ,  $I_{F(OFF)} = 0\text{mA}$  to  $0.1\text{mA}$  unless otherwise specified.)<sup>(1)</sup>

**Individual Component Characteristics**

| Symbol                  | Parameter                           | Test Conditions   | Min.                     | Typ.* | Max.  | Unit                 |
|-------------------------|-------------------------------------|---|--------------------------|-------|-------|----------------------|
| <b>EMITTER</b>          |                                     |   |                          |       |       |                      |
| $V_F$                   | Input Forward Voltage               | $I_F = 5\text{mA}$  |                          |       | 1.75  | V                    |
|                         |                                     |   | $T_A = 25^\circ\text{C}$ |       | 1.40  | 1.7                  |
| $B_{VR}$                | Input Reverse Breakdown Voltage     | $I_R = 10\mu\text{A}$   | 5.0                      |       |       | V                    |
| $C_{IN}$                | Input Capacitance                   | Pins 2 & 3, $V_F = 0$ , $f = 1\text{MHz}$                               |                          | 60    |       | pF                   |
| $\Delta V_F/\Delta T_A$ | Input Diode Temperature Coefficient | $I_F = 5\text{mA}$  |                          | -1.4  |       | mV/ $^\circ\text{C}$ |
| <b>DETECTOR</b>         |                                     |   |                          |       |       |                      |
| $I_{CCH}$               | High Level Supply Current           | $I_F = 5\text{mA}$ , $I_O = \text{Open}$ ,<br>$V_E = \text{Don't Care}$ | $V_{CC} = 5.5\text{V}$   | 3.5   | 4.5   | mA                   |
|                         |                                     |   | $V_{CC} = 20\text{V}$    | 4.0   | 6.0   |                      |
| $I_{CCL}$               | Low Level Supply Current            | $I_F = 0$ , $I_O = \text{Open}$ ,<br>$V_E = \text{Don't care}$          | $V_{CC} = 5.5\text{V}$   | 4.4   | 6.0   | mA                   |
|                         |                                     |   | $V_{CC} = 20\text{V}$    | 5.2   | 7.5   |                      |
| $I_{EL}$                | Low Level Enable Current            | $V_E = 0.4\text{V}$   |                          | -0.1  | -0.32 | mA                   |
| $I_{EH}$                | High Level Enable Current           | $V_E = 2.7\text{V}$   |                          |       | 20    | $\mu\text{A}$        |
|                         |                                     | $V_E = 5.5\text{V}$   |                          |       | 100   |                      |
|                         |                                     | $V_E = 20\text{V}$  | 0.005                    | 250   |       |                      |
| $V_{EH}$                | High Level Enable Voltage           |   | 2.0                      |       |       | V                    |
| $V_{EL}$                | Low Level Enable Voltage            |   |                          |       | 0.8   | V                    |

**Switching Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $I_{F(ON)} = 1.6\text{mA}$  to  $5\text{mA}$ ,  $I_{F(OFF)} = 0$  to  $0.1\text{mA}$ ,  $V_{CC} = 4.5\text{V}$  to  $20\text{V}$  unless otherwise specified.)

| Symbol    | AC Characteristics                                    | Test Conditions  | Min.   | Typ.*  | Max. | Unit             |
|-----------|---|--|--|--------|------|------------------|
| $T_{PLH}$ | Propagation Delay Time to Output High Level           | With Peaking Capacitor <sup>(2)(4)</sup> (Fig. 1)  |  | 120    | 300  | ns               |
| $T_{PHL}$ | Propagation Delay Time to Output Low Level            | With Peaking Capacitor <sup>(3)(4)</sup> (Fig. 1)  |  | 180    | 300  | ns               |
| $t_r$     | Output Rise Time (10% to 90%)                         | <sup>(5)</sup> (Fig. 1)  |  | 80     |      | ns               |
| $t_f$     | Output Fall Time (90% to 10%)                         | <sup>(6)</sup> (Fig. 1)  |  | 25     |      | ns               |
| $t_{pZH}$ | Enable Propagation Delay Time to Output High Level    | (Fig. 2)   |  | 40     |      | ns               |
| $t_{pZL}$ | Enable Propagation Delay Time to Output Low Level     | (Fig. 2)   |  | 50     |      | ns               |
| $T_{PHZ}$ | Disable Propagation Delay Time from Output High Level | (Fig. 2)   |  | 95     |      | ns               |
| $T_{PLZ}$ | Disable Propagation Delay Time from Output Low Level  | (Fig. 2)   |  | 80     |      | ns               |
| $ICM_H $  | Common Mode Transient Immunity (at Output High Level) | $T_A = 25^\circ\text{C}$ ,<br>$V_{OH} (\text{Min.}) = 2.0\text{V}$ ,<br>$V_{CC} = 5\text{V}^{(7)}$ (Fig. 3)                    | $I_F = 1.6\text{mA}$ ,<br>$ V_{CM}  = 50\text{V}$  | 1,000  |      | V/ $\mu\text{s}$ |
|           |   |  | $I_F = 5\text{mA}$ ,<br>$ V_{CM}  = 1,000\text{V}$ | 10,000 |      |                  |
| $ICM_L $  | Common Mode Transient Immunity (at Output Low Level)  | $T_A = 25^\circ\text{C}$ , $I_F = 0\text{mA}$<br>$V_{OL} (\text{Max.}) = 0.8\text{V}$ ,<br>$V_{CC} = 5\text{V}^{(8)}$ (Fig. 3) | $ V_{CM}  = 50\text{V}$                            | 1,000  |      | V/ $\mu\text{s}$ |
|           |   |  | $ V_{CM}  = 1,000\text{V}$                         | 10,000 |      |                  |

\*Typical values at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_{F(ON)} = 3\text{mA}$  unless otherwise specified.

**Electrical Characteristics** (Continued)

**Transfer Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $20\text{V}$ ,  $I_{F(\text{ON})} = 1.6\text{mA}$  to  $5\text{mA}$ ,  $V_{EH} = 2\text{V}$  to  $20\text{V}$ ,  $V_{EL} = 0\text{V}$  to  $0.8\text{V}$ ,  $I_{F(\text{OFF})} = 0\text{mA}$  to  $0.1\text{mA}$  unless otherwise specified.)<sup>(1)</sup>

| Symbol           | DC Characteristics  | Test Conditions  | Min. | Typ.*                 | Max. | Unit          |
|------------------|---|--|------|-----------------------|------|---------------|
| $I_{\text{OHH}}$ | Output Leakage Current ( $V_{\text{OUT}} > V_{\text{CC}}$ ) | $V_{\text{CC}} = 4.5\text{V}$ , $I_{\text{F}} = 5\text{mA}$  |      | 2.0                   | 100  | $\mu\text{A}$ |
|                  |   | $V_{\text{O}} = 5.5\text{V}$   |      | 2.5                   | 500  |               |
| $V_{\text{OL}}$  | Low Level Output Voltage                                    | $V_{\text{CC}} = 4.5\text{V}$ , $I_{\text{F}} = 0\text{mA}$ , $V_{\text{E}} = 0.4\text{V}$ , $I_{\text{OL}} = 6.4\text{mA}$ <sup>(2)</sup> |      | 0.33                  | 0.5  | V             |
| $I_{\text{FT}}$  | Input Threshold Current                                     | $V_{\text{CC}} = 4.5\text{V}$ , $V_{\text{O}} = 0.5\text{V}$ , $V_{\text{E}} = 0.4\text{V}$ , $I_{\text{OL}} = 6.4\text{mA}$               |      |                       | 1.6  | mA            |
| $V_{\text{OH}}$  | Logic High Output Voltage                                   | $I_{\text{OH}} = -2.6\text{mA}$  | 2.4  | $V_{\text{CC}} - 1.8$ |      | V             |
| $I_{\text{OZL}}$ | High Impedance State Output Current                         | $V_{\text{O}} = 0.4\text{V}$ , $V_{\text{EN}} = 2\text{V}$ , $I_{\text{F}} = 5\text{mA}$   |      |                       | -20  | $\mu\text{A}$ |
| $I_{\text{OZH}}$ | High Impedance State Output Current                         | $V_{\text{O}} = 2.4\text{V}$ , $V_{\text{EN}} = 2\text{V}$ , $I_{\text{F}} = 5\text{mA}$   |      |                       | 20   | $\mu\text{A}$ |
|                  |   | $V_{\text{O}} = 5.5\text{V}$ , $V_{\text{EN}} = 2\text{V}$ , $I_{\text{F}} = 5\text{mA}$   |      |                       | 100  |               |
|                  |   | $V_{\text{O}} = 20\text{V}$ , $V_{\text{EN}} = 2\text{V}$ , $I_{\text{F}} = 5\text{mA}$  |      |                       | 500  |               |
| $I_{\text{OSL}}$ | Logic Low Short Circuit Output Current <sup>(10)</sup>      | $V_{\text{O}} = V_{\text{CC}} = 5.5\text{V}$ , $I_{\text{F}} = 0\text{mA}$   | 25   |                       |      | mA            |
|                  |   | $V_{\text{O}} = V_{\text{CC}} = 20\text{V}$ , $I_{\text{F}} = 0\text{mA}$  | 40   |                       |      |               |
| $I_{\text{OSH}}$ | Logic High Short Circuit Output Current <sup>(10)</sup>     | $V_{\text{CC}} = 5.5\text{V}$ , $I_{\text{F}} = 5\text{mA}$ , $V_{\text{O}} = \text{GND}$  | -10  |                       |      | mA            |
|                  |   | $V_{\text{CC}} = 20\text{V}$ , $I_{\text{F}} = 5\text{mA}$ , $V_{\text{O}} = \text{GND}$   | -25  |                       |      |               |
| $I_{\text{HYS}}$ | Input Current Hysteresis                                    | $V_{\text{CC}} = 4.5\text{V}$  |      | 0.03                  |      | mA            |

**Isolation Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified)

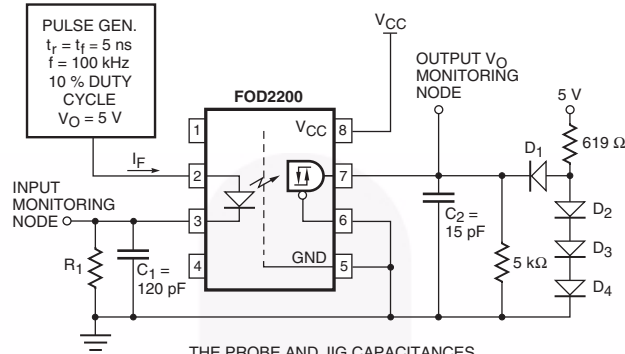
| Symbol           | Characteristics                   | Test Conditions   | Min. | Typ.*     | Max. | Unit             |
|------------------|-----------------------------------|---|------|-----------|------|------------------|
| $V_{\text{ISO}}$ | Withstand Insulation Test Voltage | $R_{\text{H}} < 50\%$ , $T_A = 25^\circ\text{C}$ , $t = 1\text{ min.}$ <sup>(9)</sup> | 5000 |           |      | $V_{\text{RMS}}$ |
| $R_{\text{I-O}}$ | Resistance (Input to Output)      | $V_{\text{I-O}} = 500\text{VDC}$ <sup>(9)</sup>                                       |      | $10^{12}$ |      | $\Omega$         |
| $C_{\text{I-O}}$ | Capacitance (Input to Output)     | $V_{\text{I-O}} = 0\text{V}$ , $f = 1\text{MHz}$ <sup>(9)</sup>                       |      | 0.6       |      | pF               |

\*Typical values at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{CC}} = 5\text{V}$ ,  $I_{\text{F}(\text{ON})} = 3\text{mA}$  unless otherwise stated.

**Notes:**

- The  $V_{\text{CC}}$  supply to each optoisolator must be bypassed by a  $0.1\mu\text{F}$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{\text{CC}}$  and GND pins of each device.
- $t_{\text{PLH}}$  – Propagation delay is measured from the 50% level on the LOW to HIGH transition of the input current pulse to the 1.3V level on the LOW to HIGH transition of the output voltage pulse.
- $t_{\text{PHL}}$  – Propagation delay is measured from the 50% level on the HIGH to LOW transition of the input current pulse to the 1.3V level on the HIGH to LOW transition of the output voltage pulse.
- When the peaking capacitor is omitted, propagation delay times may increase by 100ns.
- $t_r$  – Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
- $t_f$  – Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
- $\text{CM}_{\text{H}}$  – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the high state (i.e.,  $V_{\text{OUT}} > 2.0\text{V}$ ).
- $\text{CM}_{\text{L}}$  – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the low state (i.e.,  $V_{\text{OUT}} < 0.8\text{V}$ ).
- Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.
- Duration of output short circuit time should not exceed 10ms.

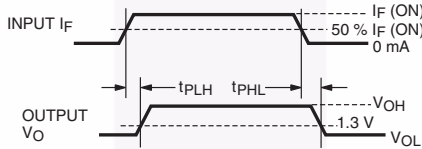
## Test Circuits



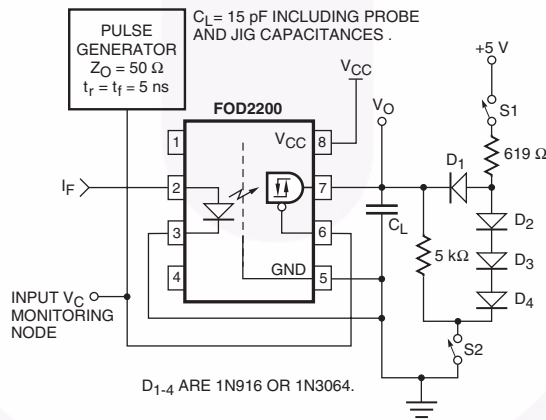
THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN C<sub>1</sub> AND C<sub>2</sub>.

|                     |         |         |       |
|---------------------|---------|---------|-------|
| R <sub>1</sub>      | 2.15 kΩ | 1.10 kΩ | 681 Ω |
| I <sub>F</sub> (ON) | 1.6 mA  | 3 mA    | 5 mA  |

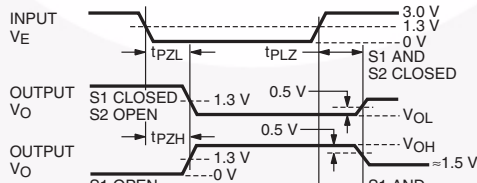
ALL DIODES ARE 1N916 OR 1N3064.



**Fig. 1. Test Circuit and Waveforms for t<sub>PLH</sub>, t<sub>PHL</sub>, t<sub>r</sub> and t<sub>f</sub>**

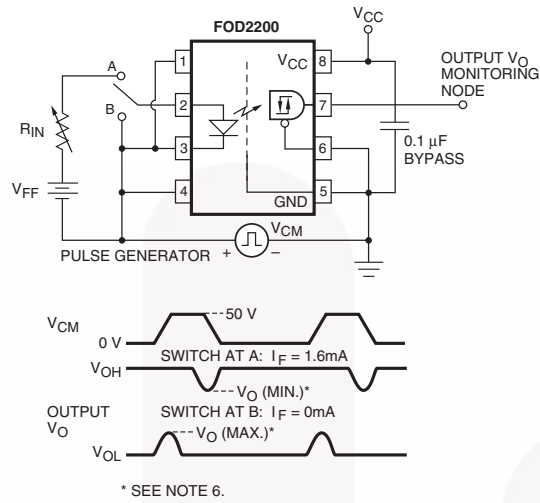


D<sub>1-4</sub> ARE 1N916 OR 1N3064.

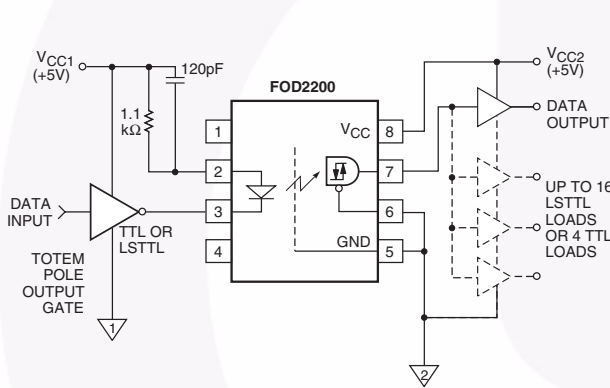


**Fig. 2. Test Circuit and Waveforms for t<sub>PZH</sub>, t<sub>PZH</sub>, t<sub>PLZ</sub>, and t<sub>PZL</sub>**

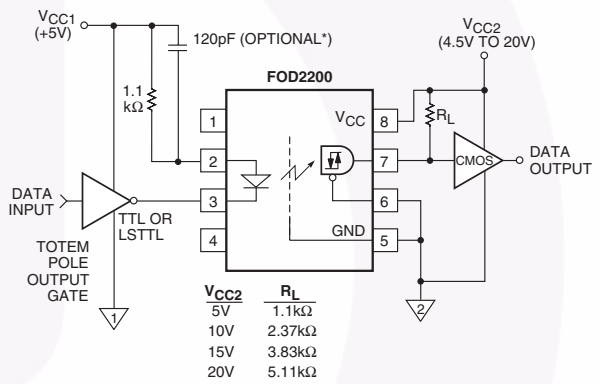
**Test Circuits** (Continued)



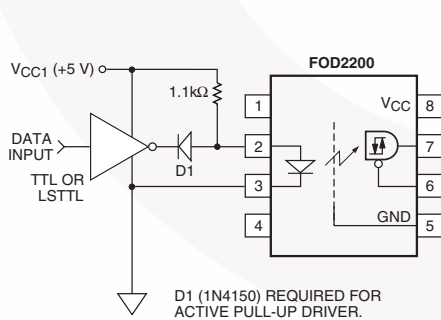
**Fig. 3. Test Circuit and Typical Waveforms for Common Mode Transient Immunity**



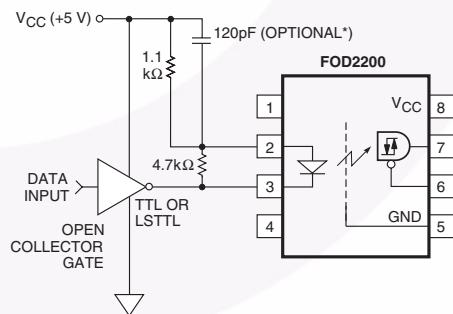
**Figure 4. Recommended LSTTL to LSTTL Circuit**



**Figure 5. LSTTL to CMOS Interface Circuit**



**Figure 6. Recommended LED Drive Circuit**

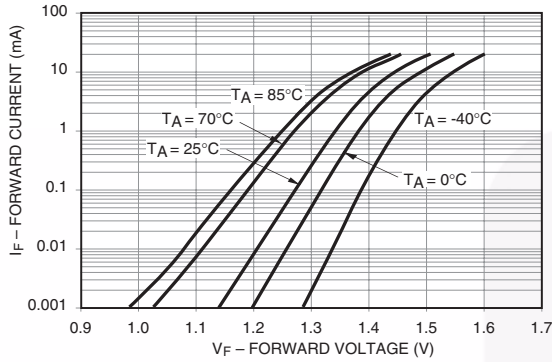


**Figure 7. Series LED Drive with Open Collector Gate (4.7kΩ Resistor Shunts IOH from the LED)**

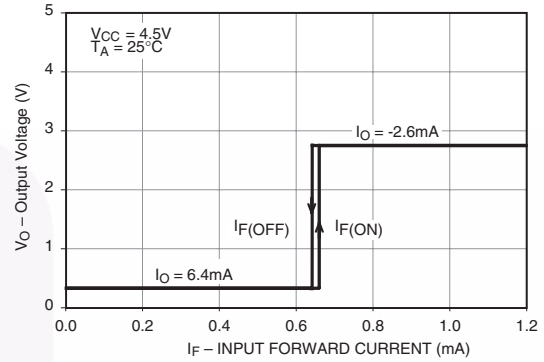
\*The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

## Typical Performance Curves

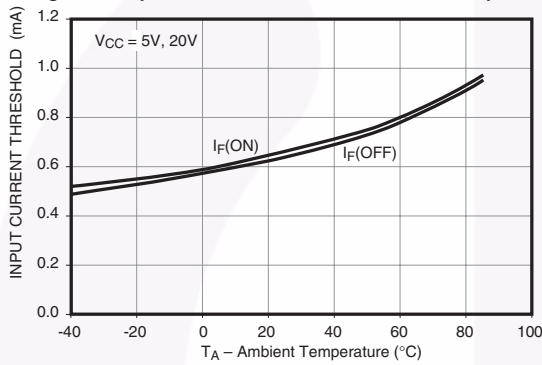
**Figure 8. Input Forward Current vs Forward Voltage**



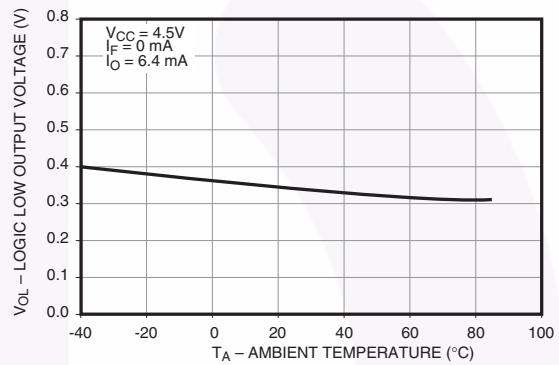
**Figure 9. Output Voltage vs. Input Forward Current**



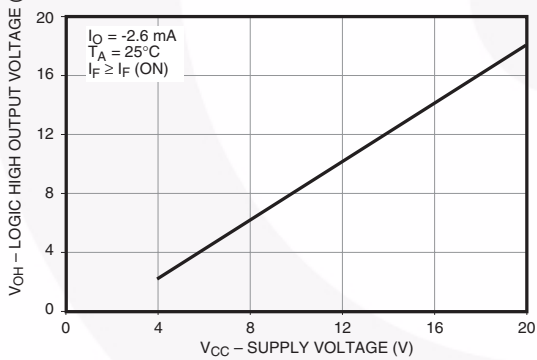
**Figure 10. Input Threshold Current vs. Ambient Temperature**



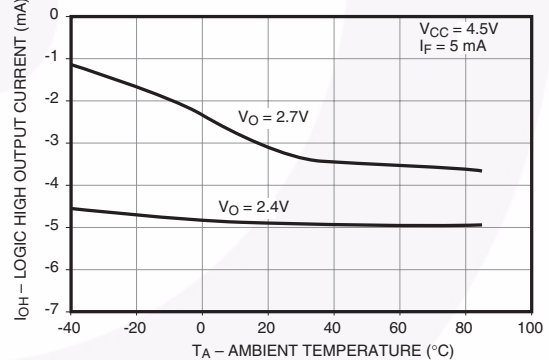
**Figure 11. Logic Low Output Voltage vs. Ambient Temperature**



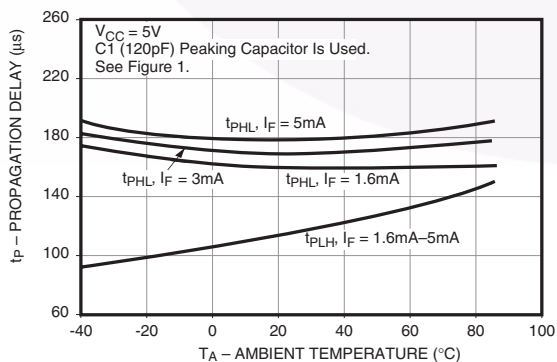
**Figure 12. Logic High Output Voltage vs. Supply Voltage**



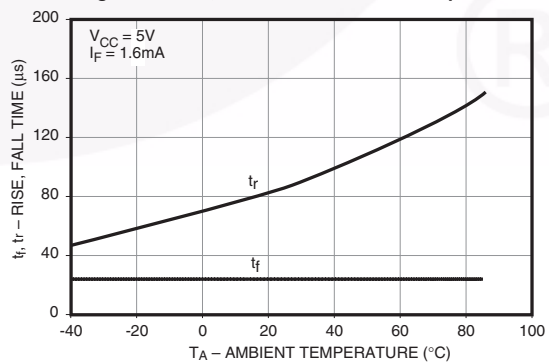
**Figure 13. Logic High Output Current vs. Ambient Temperature**



**Figure 14. Propagation Delay vs Ambient Temperature**



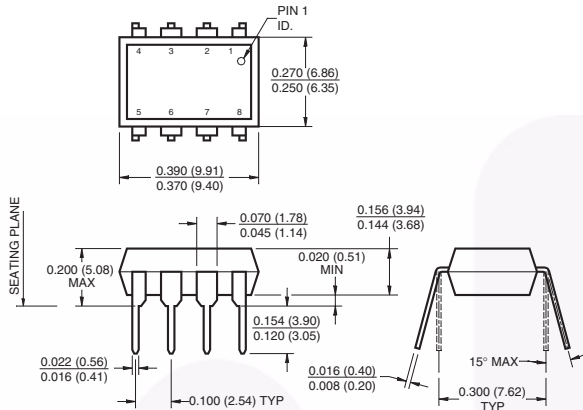
**Figure 15. Rise, Fall Time vs Ambient Temperature**



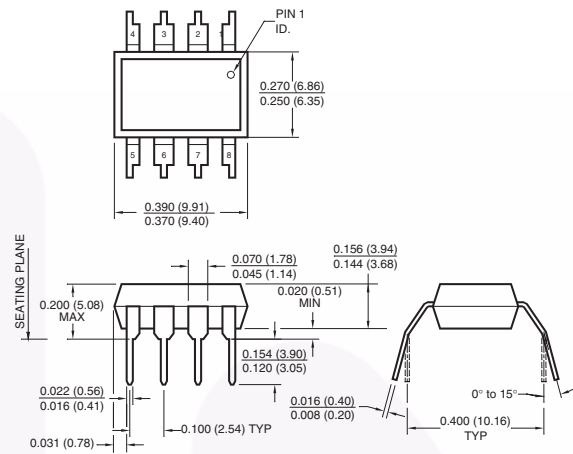


## Package Dimensions

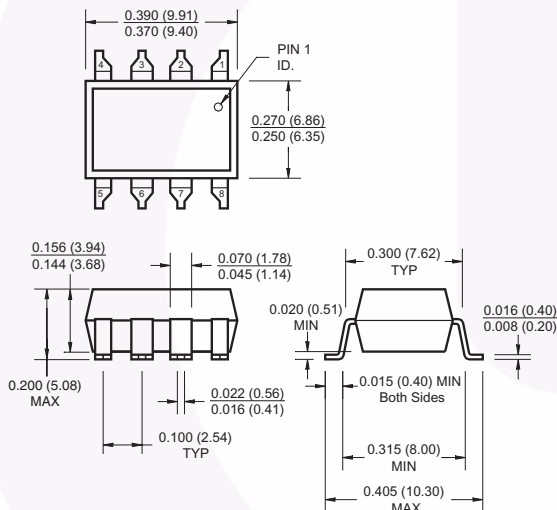
### Through Hole



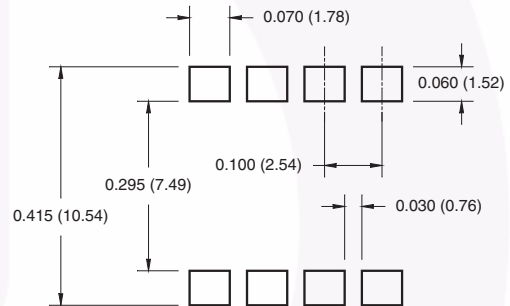
### 0.4" Lead Spacing (Option T)



### Surface Mount – 0.3" Lead Spacing (Option S)



### 8-Pin Surface Mount DIP – Land Pattern (Option S)



**Note:**

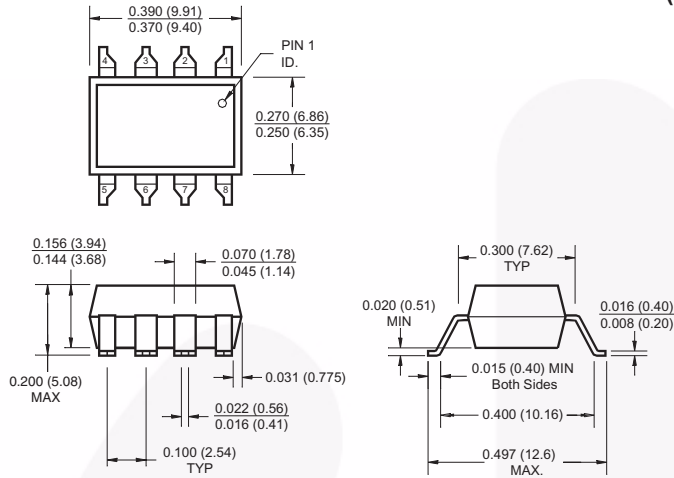
All dimensions are in inches (millimeters)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

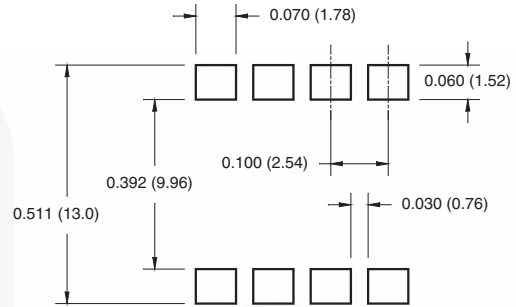
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## Package Dimensions (Continued)

### Surface Mount – 0.4" Lead Spacing (Option TS)



### 8-Pin Surface Mount DIP – Land Pattern (Option TS)



**Note:**

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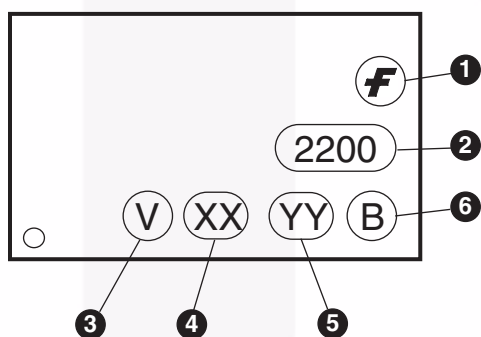
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## Ordering Information

| Part Number  | Package   | Packing Method                       |
|--------------|---|--------------------------------------|
| FOD2200      | DIP 8-Pin   | Tube (50 units per tube)             |
| FOD2200S     | SMT 8-Pin (Lead Bend)                             | Tube (50 units per tube)             |
| FOD2200SD    | SMT 8-Pin (Lead Bend)                             | Tape and Reel (1,000 units per reel) |
| FOD2200V     | DIP 8-Pin, IEC60747-5-2 option                    | Tube (50 units per tube)             |
| FOD2200SV    | SMT 8-Pin (Lead Bend), IEC60747-5-2 option        | Tube (50 units per tube)             |
| FOD2200SDV   | SMT 8-Pin (Lead Bend), IEC60747-5-2 option        | Tape and Reel (1,000 units per reel) |
| FOD2200TV    | DIP 8-Pin, 0.4" Lead Spacing, IEC60747-5-2 option | Tube (50 units per tube)             |
| FOD2200TSV   | SMT 8-Pin, 0.4" Lead Spacing, IEC60747-5-2 option | Tube (50 units per tube)             |
| FOD2200TSR2V | SMT 8-Pin, 0.4" Lead Spacing, IEC60747-5-2 option | Tape and Reel (700 units per reel)   |

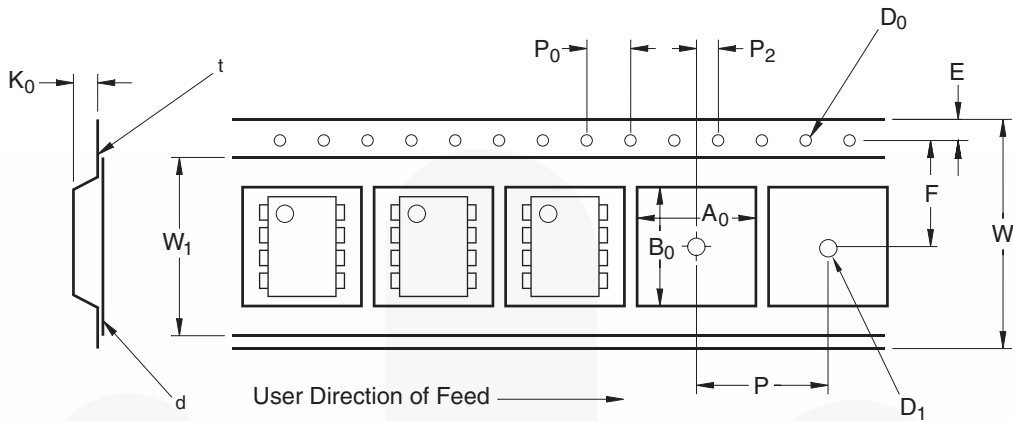
## Marking Information



### Definitions

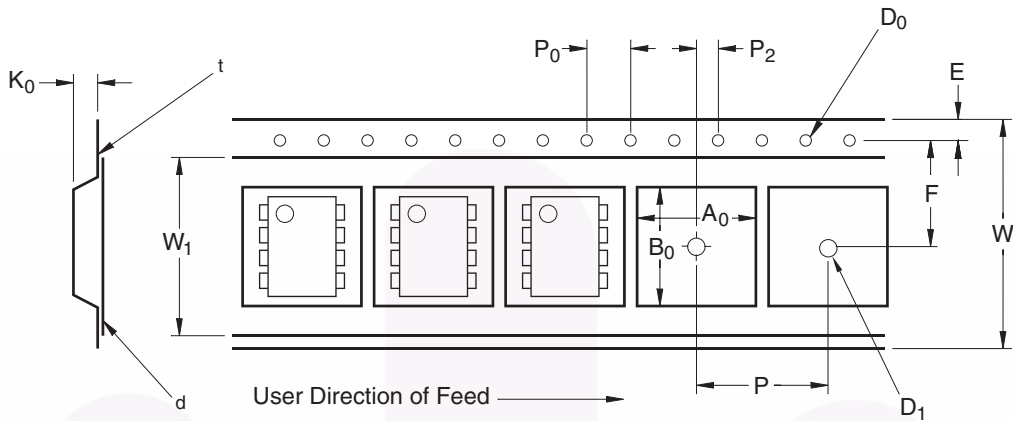
|   |   |
|---|---|
| 1 | Fairchild logo  |
| 2 | Device number   |
| 3 | IEC60747-5-2 Option (only appears on component ordered with this option) (Pending approval) |
| 4 | Two digit year code, e.g., '08'   |
| 5 | Two digit work week ranging from '01' to '53'   |
| 6 | Assembly package code   |

### Carrier Tape Specifications (Option SD)



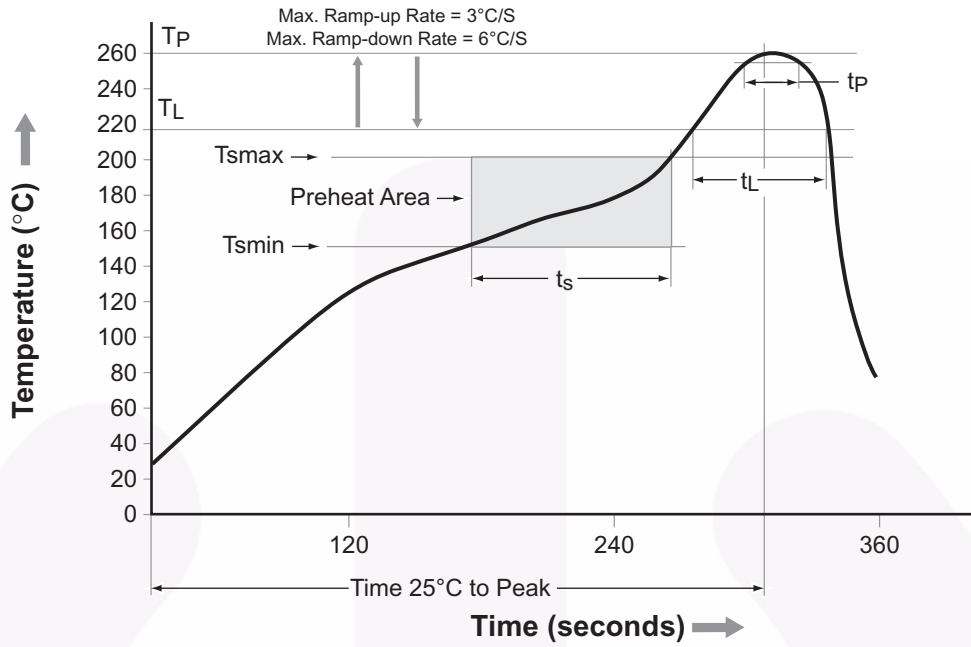
| Symbol         | Description                     | Dimension in mm |
|----------------|---------------------------------|-----------------|
| W              | Tape Width                      | 16.0 ± 0.3      |
| t              | Tape Thickness                  | 0.30 ± 0.05     |
| P <sub>0</sub> | Sprocket Hole Pitch             | 4.0 ± 0.1       |
| D <sub>0</sub> | Sprocket Hole Diameter          | 1.55 ± 0.05     |
| E              | Sprocket Hole Location          | 1.75 ± 0.10     |
| F              | Pocket Location                 | 7.5 ± 0.1       |
| P <sub>2</sub> |                                 | 2.0 ± 0.1       |
| P              | Pocket Pitch                    | 12.0 ± 0.1      |
| A <sub>0</sub> | Pocket Dimensions               | 10.30 ± 0.20    |
| B <sub>0</sub> |                                 | 10.30 ± 0.20    |
| K <sub>0</sub> |                                 | 4.90 ± 0.20     |
| W <sub>1</sub> | Cover Tape Width                | 13.2 ± 0.2      |
| d              | Cover Tape Thickness            | 0.1 max         |
|                | Max. Component Rotation or Tilt | 10°             |
| R              | Min. Bending Radius             | 30              |

### Carrier Tape Specifications (Option TSR2V)



| Symbol         | Description                     | Dimension in mm |
|----------------|---------------------------------|-----------------|
| W              | Tape Width                      | 24.0 ± 0.3      |
| t              | Tape Thickness                  | 0.40 ± 0.1      |
| P <sub>0</sub> | Sprocket Hole Pitch             | 4.0 ± 0.1       |
| D <sub>0</sub> | Sprocket Hole Diameter          | 1.55 ± 0.05     |
| E              | Sprocket Hole Location          | 1.75 ± 0.10     |
| F              | Pocket Location                 | 11.5 ± 0.1      |
| P <sub>2</sub> |                                 | 2.0 ± 0.1       |
| P              | Pocket Pitch                    | 16.0 ± 0.1      |
| A <sub>0</sub> | Pocket Dimensions               | 12.80 ± 0.1     |
| B <sub>0</sub> |                                 | 10.35 ± 0.1     |
| K <sub>0</sub> |                                 | 5.7 ± 0.1       |
| W <sub>1</sub> | Cover Tape Width                | 21.0 ± 0.1      |
| d              | Cover Tape Thickness            | 0.1 max         |
|                | Max. Component Rotation or Tilt | 10°             |
| R              | Min. Bending Radius             | 30              |

## Reflow Profile



| Profile Feature                                  | Pb-Free Assembly Profile |
|--|--------------------------|
| Temperature Min. ( $T_{smin}$ )                  | 150°C                    |
| Temperature Max. ( $T_{smax}$ )                  | 200°C                    |
| Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ ) | 60–120 seconds           |
| Ramp-up Rate ( $t_L$ to $t_p$ )                  | 3°C/second max.          |
| Liquidous Temperature ( $T_L$ )                  | 217°C                    |
| Time ( $t_L$ ) Maintained Above ( $T_L$ )        | 60–150 seconds           |
| Peak Body Package Temperature                    | 260°C +0°C / -5°C        |
| Time ( $t_p$ ) within 5°C of 260°C               | 30 seconds               |
| Ramp-down Rate ( $T_P$ to $T_L$ )                | 6°C/second max.          |
| Time 25°C to Peak Temperature                    | 8 minutes max.           |



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| Build it Now™            | Global Power Resource <sup>SM</sup> | PowerXS™                              |   |
| CorePLUS™                | Green FPS™                          | Programmable Active Droop™            |   |
| CorePOWER™               | Green FPS™ e-Series™                | QFET®                                 |   |
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| EfficientMax™            | MicroFET™                           | SmartMax™                             |   |
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| FAST®                    | OPTOLOGIC®                          | SuperSOT™-8                           |   |
| FastvCore™               | OPTOPLANAR®                         | SupreMOS®                             |   |
| FETBench™                | ™                                   | SyncFET™                              |   |
| FlashWriter®*            | PDP SPM™                            | Sync-Lock™                            |   |
| FPS™                     |                                     |                                       |   |

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