P-Channel Power MOSFET

-20V, -6.4A, 40mΩ

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

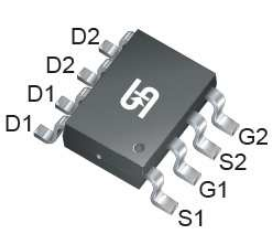
KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-20	V
$R_{DS(on)}$ (max)	V_{GS} = -10V	40	mΩ
	V_{GS} = -4.5V	60	
Q_g		19	nC

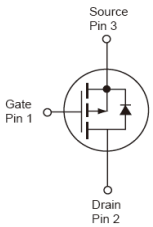
Application

- Load Switch
- PA Switch

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8





Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	-6.4	A
	T_C = 100°C		-3.8	
Pulsed Drain Current (Note 2)		I_{DM}	-19.2	A
Total Power Dissipation @ T_A = 25°C		P_{DTOT}	2.5	W
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	13.94	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	16.7	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	30	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	50	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-0.4	--	-1.0	V
Gate Body Leakage	V_{GS} = ±8V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V	I_{DSS}	--	--	-1	μA
On-State Drain Current	V_{DS} ≤ -5V , V_{GS} = -4.5V	$I_{D(ON)}$	-10	--	--	A
Drain-Source On-State Resistance	V_{GS} = -4.5V, I_D = -6.4A	$R_{DS(ON)}$	--	31	40	mΩ
	V_{GS} = -2.5V, I_D = -5.1A		--	45	60	
Forward Transconductance	V_{DS} = -9V, I_D = -6.4A	g_{fs}	--	14	--	S
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = -10V, I_D = -6.4A, V_{GS} = -4.5V	Q_g	--	12	19	nC
Gate-Source Charge		Q_{gs}	--	1.7	--	
Gate-Drain Charge		Q_{gd}	--	3.3	--	
Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1020	--	pF
Output Capacitance		C_{oss}	--	191	--	
Reverse Transfer Capacitance		C_{rss}	--	140	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	3	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = -10V, R_{GEN} = 6Ω, I_D = -1A, V_{GS} = -4.5V,	$t_{d(on)}$	--	25	40	ns
Turn-On Rise Time		t_r	--	43	65	
Turn-Off Delay Time		$t_{d(off)}$	--	71	110	
Turn-Off Fall Time		t_f	--	48	75	
Source-Drain Diode (Note 4)						
Forward On Voltage	I_S = -2.5A, V_{GS} = 0V	V_{SD}	--	-0.9	-1.2	V
Reverse Recovery Time	I_S = -4A, dI_F/dt = 100A/μs	t_{rr}	--	12.6	--	ns
Reverse Recovery Charge		Q_{rr}	--	2.84	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. L = 0.1mH, I_{AS} = 16.7A, V_{DD} = 25V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM9434CS RLG	SOP-8	2,500pcs / 13” Reel

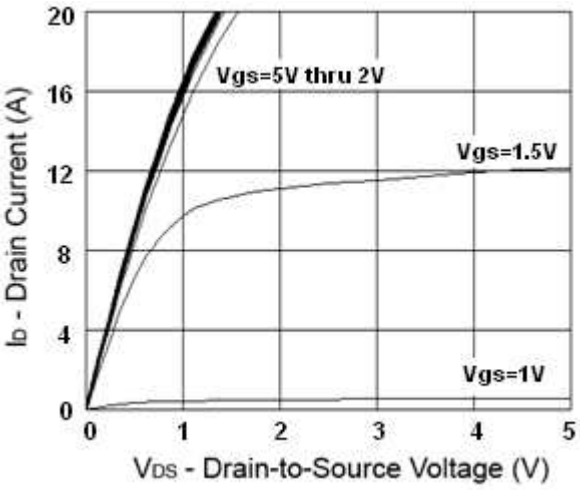
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

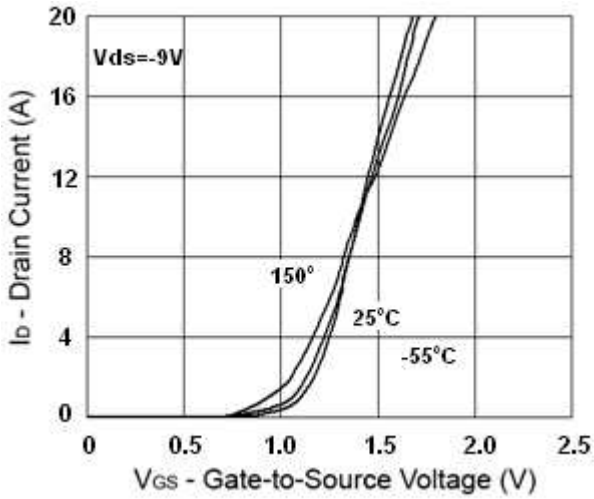
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

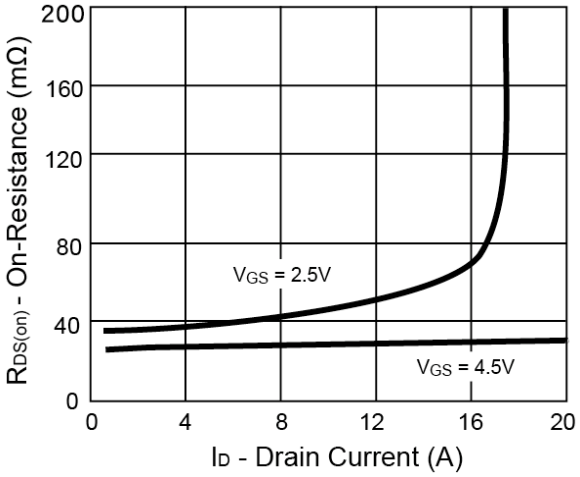
Output Characteristics



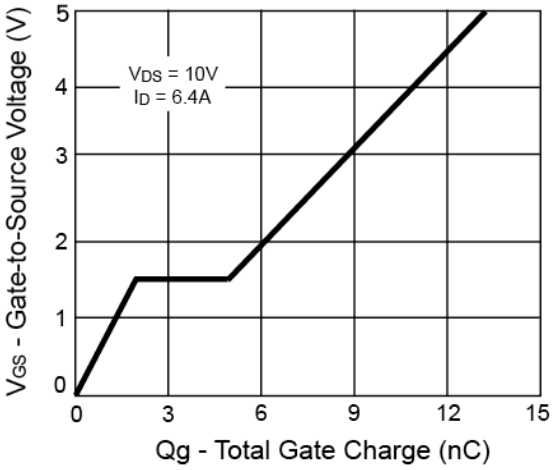
Transfer Characteristics



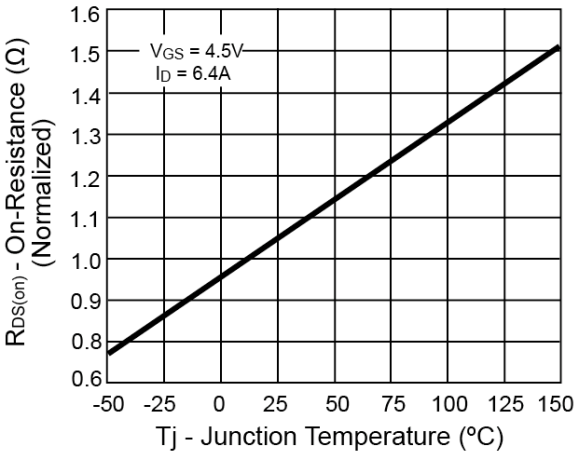
On-Resistance vs. Drain Current



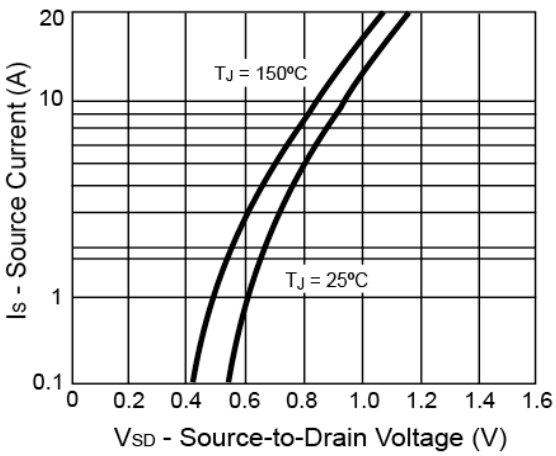
Gate Charge



On-Resistance vs. Junction Temperature



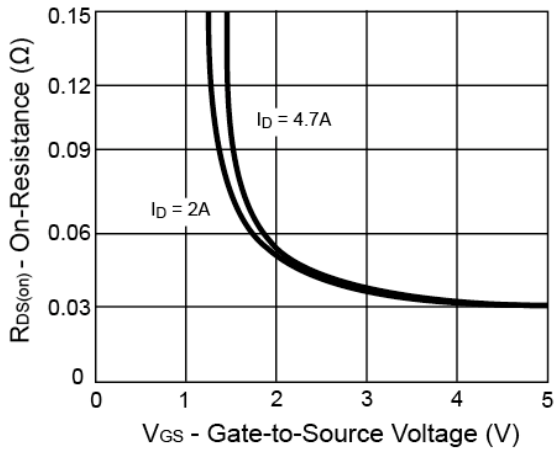
Source-Drain Diode Forward Voltage



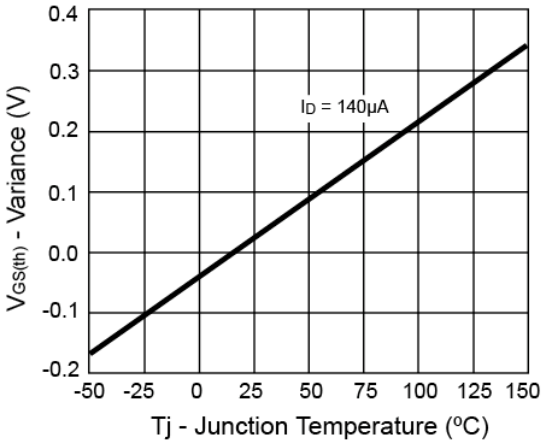
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

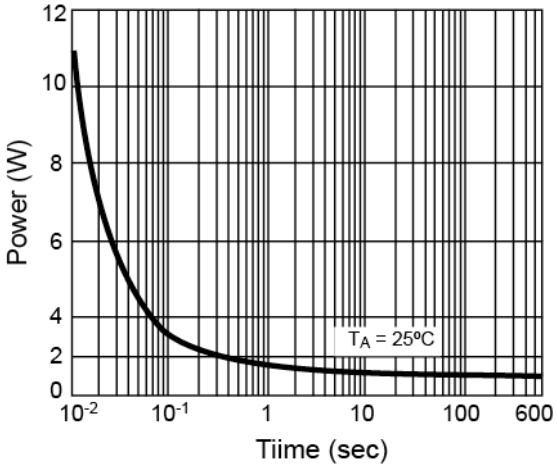
On-Resistance vs. Gate-Source Voltage



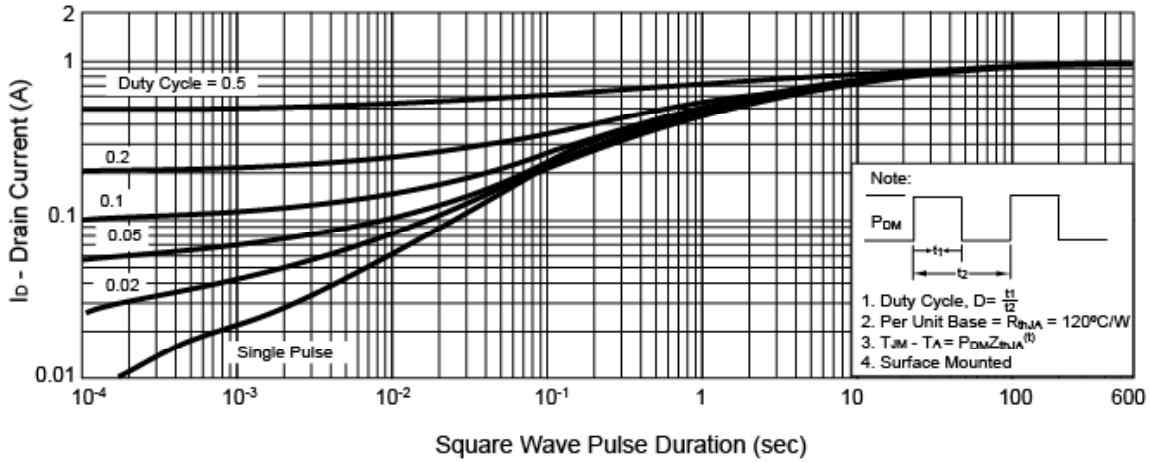
Threshold Voltage



Single Pulse Power

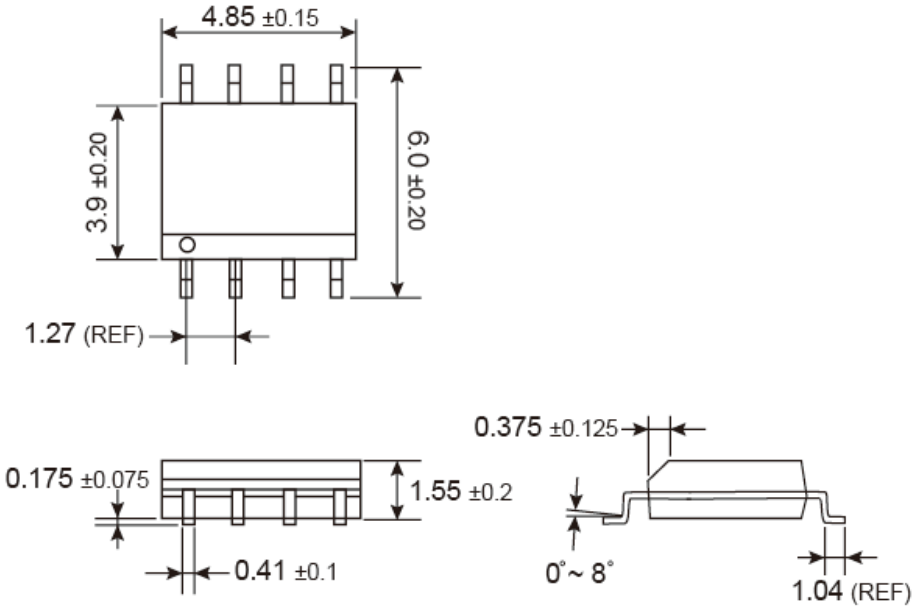


Normalized Thermal Transient Impedance, Junction-to-Ambient

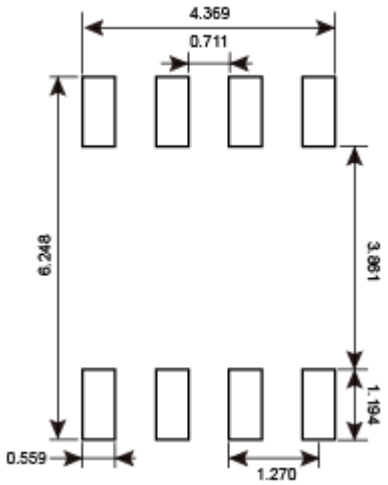


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

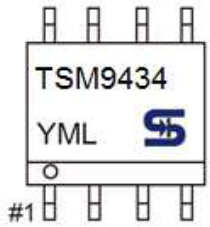
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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