# Advanced Battery Management PMIC with Inductive Boost LED and Three LDO Regulators

Data Sheet

# ADP5350

## FEATURES

- Switching mode USB battery charger
  - High accuracy and programmable charge terminal voltage and charge current
  - 3 MHz buck for high efficiency and small footprint
  - Tolerant input voltage from −0.5 V to +20 V (USB $V_{VBUSx}$)
  - Power path control allows system to operate with dead or missing battery
  - Compliant with JEITA charge temperature specification
- Voltage-based state of charge (SOC) calculation algorithm
  - Extra low quiescent current in sleep mode
  - Battery impedance chemistry (Li-Ion) compensation
  - Battery temperature compensation
  - No need for external sense resistor
- Boost regulator with 5-channel LED driver
  - Support up to 4 LED in series or in parallel
  - 5 independent programmable LED current sinks
  - 64 programmable LED current levels (up to 20 mA)
  - Programmable on and off timer for LED blinking
  - Adaptive headroom control to maximize the efficiency
- Three 150 mA linear LDO regulators
  - Ultralow $I_Q$ with zero load at 1 µA typical for LDO1
  - Optional load-switch full turn-on mode
- Full I²C programmability with dedicated interrupt pin

## APPLICATIONS

- Rechargeable Li-Ion and Li-Ion polymer battery-powered devices
- Portable consumer devices
- Portable medical devices
- Portable instrumentation devices
- Wearable devices

## GENERAL DESCRIPTION

The ADP5350, a power management IC (PMIC), combines one high performance buck regulator for single Li-Ion/Li-Ion polymer battery charging, a fuel gauge, a highly programmable boost regulator for LED backlight illumination, and three 150 mA LDO regulators.

The ADP5350 operates in trickle charge mode and in constant current (CC) and constant voltage (CV) fast charge mode. It features an internal field effect transistor (FET) that permits battery isolation on the system power side.

The ADP5350 fuel gauge is a space-saving and low current consuming solution. It is optimal for rechargeable Li-Ion battery-powered devices, and features a voltage-based, battery SOC measurement function.

## TYPICAL APPLICATION CIRCUIT

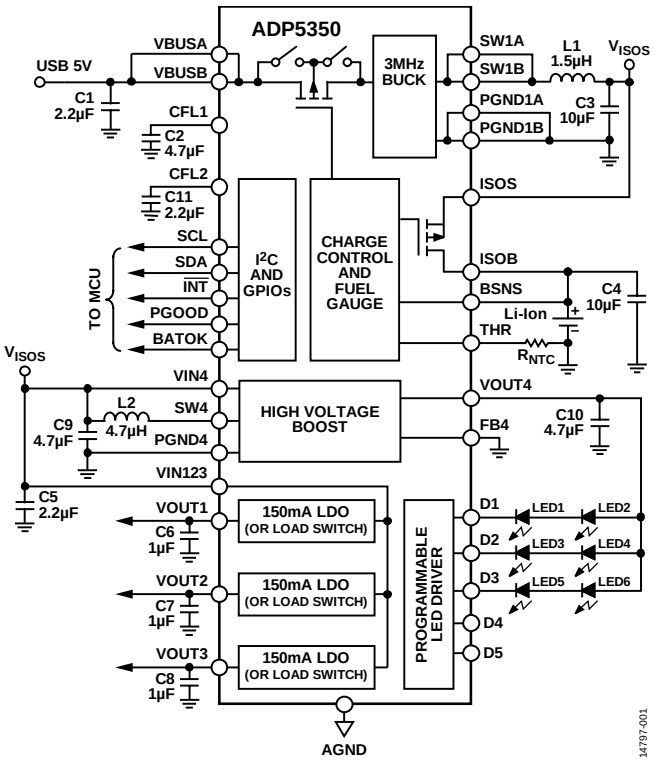


*Figure 1.*

The ADP5350 boost regulator operates at a 1.5 MHz switching frequency. It can be operated as a constant voltage regulator or as a supplemental constant current regulator for multiple LED backlight drivers.

The ADP5350 LED drivers can support a wide range of LED backlight configurations, either multiple LEDs in parallel or in series.

The ADP5350 low dropout (LDO) regulators are optimized to operate at low shutdown current and quiescent current to extend battery life. The device also operates as a load switch that can be fully turned off or on.

The I²C-compatible interface enables the programmability of all parameters, including status bit readback for operation monitoring and safety control.

The ADP5350 operates over the −40°C to +125°C junction temperature range and is available in a 32-lead, 5 mm × 5 mm LFCSP package and a 32-ball, 3 mm × 3 mm WLCSP package.


**Rev. B** Document Feedback





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# DETAILED FUNCTIONAL BLOCK DIAGRAM

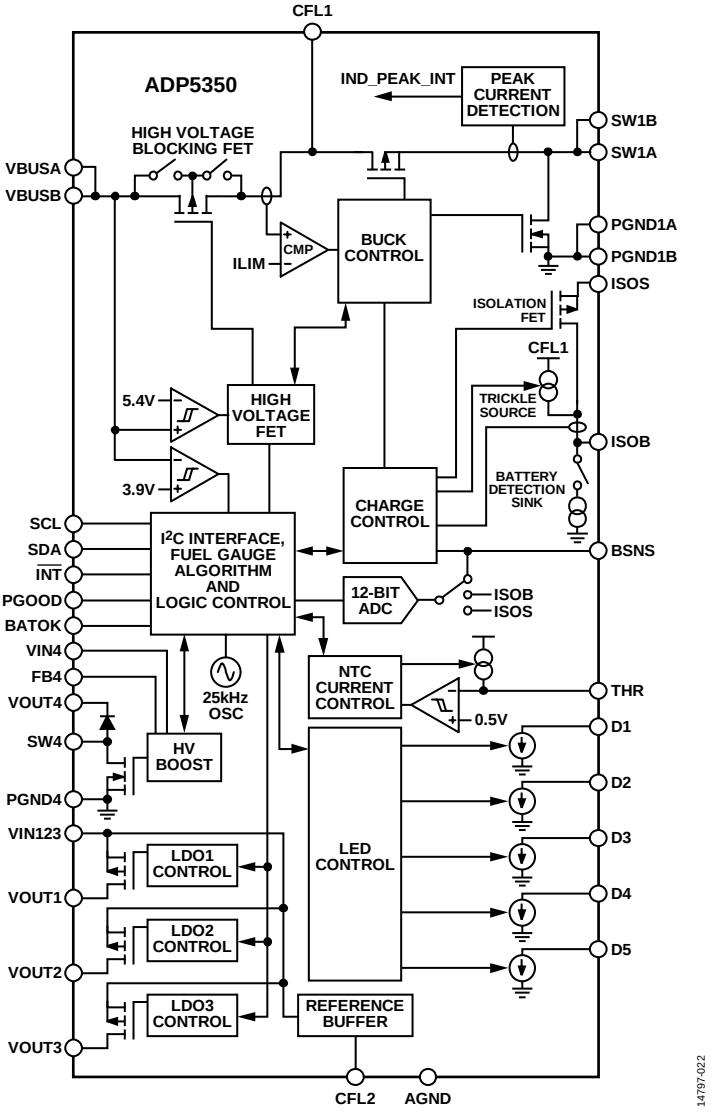



*Figure 2. Detailed Functional Block Diagram*

# SPECIFICATIONS

## BATTERY CHARGER SPECIFICATIONS

$-40°C < T_J < 125°C$, $V_{VBUSx} = 5.0$ V, $R_{NTC} = 47$ kΩ, $V_{VIN4} = V_{VIN123} = V_{ISOS} = 3.6$ V, C1 = 2.2 µF, C2 = 4.7 µF, C3 = 10 µF, C4 = 10 µF, C11 = 2.2 µF, L1 = 1.5 µH, all registers are at default values, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| GENERAL PARAMETERS | | $T_J = 0°C$ to 85°C | | | | |
| Undervoltage Lockout | $V_{UVLO}$ | On BSNS, rising threshold, no $V_{VBUSx}$ | | 2.45 | 2.6 | V |
| | | On BSNS, falling threshold, no $V_{VBUSx}$ | 2.2 | 2.3 | | V |
| Input Current Limit | $I_{LIM}$ | Set ILIM[3:0] = 100 mA | | 92 | 100 | mA |
| | | Set ILIM[3:0] = 500 mA | | 475 | 500 | mA |
| Operation Current | $I_Q$ | All enabled, no load, from VBUSx pin | | 4 | 6 | mA |
| | | Only fuel gauge enabled (active), from ISOB, no $V_{VBUSx}$ | | 160 | 230 | µA |
| | | Only fuel gauge enabled (sleep), from ISOB, no $V_{VBUSx}$[1] | | 4 | | µA |
| | | Only boost regulator enabled, all LEDs enabled, no LED current, from ISOB, no $V_{VBUS}$ | | 2 | 2.6 | mA |
| | | Only LDO1 enabled, from ISOB, no $V_{VBUSx}$ | | 0.8 | 4 | µA |
| | | Only LDO2 enabled, from ISOB, no $V_{VBUSx}$ | | 160 | 230 | µA |
| | | Only LDO3 enabled, from ISOB, no $V_{VBUSx}$ | | 160 | 230 | µA |
| Shutdown Current | $I_{STDN}$ | All disabled, from ISOB and BSNS, no $V_{VBUSx}$ | | 0.2 | 2.8 | µA |
| CHARGING PARAMETERS | | | | | | |
| Fast Charge Current, Constant Current Mode | $I_{CHG}$ | Programmable via I²C, battery voltage > $V_{TRK\_DEAD}$ | 25 | | 650 | mA |
| Fast Charge Current Accuracy | | $I_{CHG} = 200$ mA | 180 | 200 | 220 | mA |
| | | $T_J = 25°C$, $I_{CHG} = 200$ mA | −2.5 | | +2.5 | % |
| Trickle Charge Current[2] | $I_{TRK\_DEAD}$ | | 16 | 20 | 25 | mA |
| Weak Charge Current | $I_{CHG\_WEAK}$ | When $V_{TRK\_DEAD} < V_{BSNS} < V_{WEAK}$ | | $I_{CHG} + I_{TRK\_DEAD}$ | | mA |
| Dead Battery, Trickle to Weak Charge Threshold[2] | $V_{TRK\_DEAD}$ | On BSNS | 2.4 | 2.5 | 2.62 | V |
| Weak Battery | | | | | | |
| Weak to Fast Charge Threshold[2] | $V_{WEAK}$ | On BSNS | 2.9 | 3.0 | 3.15 | V |
| Weak Battery Threshold Hysteresis[1] | $\Delta V_{WEAK}$ | | | 90 | | mV |
| Battery Termination Voltage[2] | $V_{TRM}$ | On BSNS, $T_J = 0°C$ to 85°C | 4.158 | 4.200 | 4.242 | V |
| | | On BSNS, $T_J = 25°C$ | −0.3 | | +0.3 | % |
| Battery Overvoltage Threshold | $V_{BAT\_OV}$ | Relative to CFL1 voltage, BSNS rising, $V_{CLF1} = 4.0$ V | $V_{CFL1} - 0.15$ | | | V |
| Charge Complete Current[2] | $I_{END}$ | $V_{BSNS} = V_{TRM}$, $T_J = 0°C$ to 85°C | 20 | 35 | 50 | mA |
| Recharge Voltage Differential[2] | $V_{RCH}$ | Relative to $V_{TRM}$, BSNS falling | | 260 | | mV |
| Battery Node Short Threshold Voltage[2] | $V_{BAT\_SHR}$ | | 2.3 | 2.4 | 2.52 | V |
| CHARGER DC-TO-DC REGULATOR | | | | | | |
| Switching Frequency | $f_{SW\_CHG}$ | | 2.7 | 3 | 3.3 | MHz |
| Maximum Duty Cycle[3] | $D_{MAX}$ | | | 96 | | % |
| Peak Inductor Current | $I_{L1\_PK}$ | | 1500 | 1750 | 2200 | mA |
| Regulated System Voltage | $V_{ISOS\_TRK}$ | $V_{BSNS} < V_{TRK\_DEAD}$, trickle charge mode | | $V_{TRM} + 0.1$ | | V |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC to DC Power | | | | | | |
| PMOS On Resistance | $R_{DSON\_P}$ | | | 220 | 280 | mΩ |
| NMOS On Resistance | $R_{DSON\_N}$ | | | 160 | 210 | mΩ |
| SW1x Pin Leakage Current | $I_{SW1x}$ | $V_{SW1x}$ = 5.0 V | | | 2 | µA |
| BATTERY ISOLATION FIELD EFFECT TRANSISTOR (FET) | | | | | | |
| LFCSP Package | | | | 202 | 300 | mΩ |
| WLCSP Package | | | | 125 | 170 | mΩ |
| | $V_{ISOS\_FC}$ | $V_{TRK\_DEAD} < V_{BSNS}$, fast charging constant current mode | 3.15 | 3.3 | 3.45 | V |
| Battery Supplementary Threshold | $V_{TH\_ISO}$ | $V_{ISOS} < V_{ISOB}$ | 0 | 5 | 14 | mV |
| HIGH VOLTAGE BLOCKING FET | | | | | | |
| VBUSx Input | | | | | | |
| High Voltage Blocking FET On Resistance | $R_{DSON\_HV}$ | $I_{VBUS}$ = 100 mA, $T_J$ = 0°C to 85°C | | 330 | | mΩ |
| Current, Suspend Mode | $I_{SUSPEND}$ | EN_DCDC = low | | 1.45 | 1.8 | mA |
| Input Voltage | | | | | | |
| Power-Good Threshold | $V_{VBUSOK}$ | | | | | |
| Rising | $V_{VBUSOK\_RISE}$ | | 3.77 | 3.9 | 4.03 | V |
| Falling | $V_{VBUSOK\_FALL}$ | | 3.47 | 3.6 | 3.73 | V |
| Overvoltage Threshold | $V_{VBUS\_OV}$ | | 5.38 | 5.45 | 5.53 | V |
| Overvoltage Threshold Hysteresis | | | | 75 | | mV |
| THERMAL CONTROL | | | | | | |
| Thermal Early Warning Temperature[1] | $T_{SD\_W}$ | | | 130 | | °C |
| Thermal Shutdown Temperature[1] | $T_{SD}$ | $T_J$ rising | | 140 | | °C |
| | | $T_J$ falling | | 110 | | °C |
| THERMISTOR CONTROL | | | | | | |
| Resistance Thresholds by Battery Temperature[4] | | $R_{NTC}$ = 47 kΩ, BETA_NTC = 3800, $T_J$ = 0°C to +85°C | | | | |
| LFCSP Package | | | | | | |
| Cool to Cold | $R_{COOL\_COLD}$ | | 131 | 151.2 | 175 | kΩ |
| Cold to Cool | $R_{COLD\_COOL}$ | | 126 | 145.6 | 168 | kΩ |
| Typical to Cool[4] | $R_{TYP\_COOL}$ | | 75 | 86.5 | 99 | kΩ |
| Cool to Typical[4] | $R_{COOL\_TPY}$ | | 72.5 | 83.1 | 95 | kΩ |
| Warm to Typical[4] | $R_{WARM\_TYP}$ | | 20 | 23.7 | 27 | kΩ |
| Typical to Warm[4] | $R_{TYP\_WARM}$ | | 19.3 | 22 | 24.6 | kΩ |
| Hot to Warm | $R_{HOT\_WARM}$ | | 12 | 13.9 | 16 | kΩ |
| Warm to Hot | $R_{WARM\_HOT}$ | | 11 | 12.7 | 14.4 | kΩ |
| WLCSP Package | | | | | | |
| Cool to Cold | $R_{COOL\_COLD}$ | | 140 | 162 | 185 | kΩ |
| Cold to Cool | $R_{COLD\_COOL}$ | | 133 | 156 | 180 | kΩ |
| Typical to Cool[4] | $R_{TYP\_COOL}$ | | 77 | 90 | 102 | kΩ |
| Cool to Typical[4] | $R_{COOL\_TPY}$ | | 75 | 86 | 100 | kΩ |
| Warm to Typical[4] | $R_{WARM\_TYP}$ | | 20 | 23 | 26 | kΩ |
| Typical to Warm[4] | $R_{TYP\_WARM}$ | | 18.5 | 21 | 24 | kΩ |
| Hot to Warm | $R_{HOT\_WARM}$ | | 11.5 | 13 | 15 | kΩ |
| Warm to Hot | $R_{WARM\_HOT}$ | | 10.5 | 12 | 13.5 | kΩ |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BATTERY DETECTION | | | | | | |
| Sink Current | $I_{SINK}$ | | 15 | 25 | 35 | mA |
| Source Current | $I_{SOURCE}$ | | 7 | 10 | 13 | mA |
| Battery Threshold | | | | | | |
| Low | $V_{BATL}$ | | 1.8 | 1.9 | 2.0 | V |
| High | $V_{BATH}$ | | 3.3 | 3.4 | 3.55 | V |
| Battery Detection Timer | $t_{BATOK}$ | | | 333 | | ms |
| TIMERS | | | | | | |
| Start Charging Delay Timer | $t_{START}$ | | | 1 | | sec |
| Trickle Charge Timer[2] | $t_{TRK}$ | | | 60 | | min |
| Fast Charge Timer[2] | $t_{CHG}$ | | | 600 | | min |
| Charge Complete Timer | $t_{END}$ | $V_{BSNS} = V_{TRM}$, $I_{CHG} < I_{END}$ | | 7.5 | | min |
| Deglitch Timer | $t_{DG}$ | Applies to $V_{TRM}$, $V_{RCH}$, $I_{END}$, $V_{WEAK}$, $V_{TRK\_DEAD}$, $V_{VBUSOK\_FALL}$, and $V_{VBUSOK\_RISE}$ | | 31 | | ms |
| Watchdog Timer[2] | $t_{WD}$ | | | 32 | | sec |
| Safety Timer | $t_{SAFE}$ | | | 40 | | min |
| Battery Node Short Timer[2] | $t_{BAT\_SHR}$ | | | 30 | | sec |
| I²C (SCL AND SDA) | | | | | | |
| Input Voltage | | | | | | |
| Low Level | $V_{IL}$ | Applies to SCL, SDA | | | 0.5 | V |
| High Level | $V_{IH}$ | Applies to SCL, SDA | 1.2 | | | V |
| Low Level Output Voltage | $V_{OL}$ | Applies to SDA, $I_{SDA\_SINK}$ = 2 mA | | | 0.4 | V |
| PGOOD AND BATOK | | | | | | |
| PGOOD Pin | | | | | | |
| Leakage Current | $I_{PGOOD\_LEAK}$ | $V_{PGOOD}$ = 5 V | | | 0.5 | µA |
| Output Low Voltage | $V_{PGOOD\_LOW}$ | $I_{PGOOD}$ = 1 mA | | 50 | 100 | mV |
| BATOK Pin | | | | | | |
| Leakage Current | $I_{BATOK\_LEAK}$ | $V_{BATOK}$ = 5 V | | | 0.5 | µA |
| Output Low Voltage | $V_{BATOK\_LOW}$ | $I_{BATOK}$ = 1 mA | | 50 | 100 | mV |

[1] Specification is not production tested, but is supported by characterization data at initial product release.
[2] These values are programmable via the I²C interface. Values are given with default register values.
[3] Guaranteed by design.
[4] Typical temperature is the normal operation temperature.

## BATTERY FUEL GAUGE SPECIFICATIONS

$V_{VIN4} = V_{VIN123} = V_{ISOS}$ = 4.2 V, $T_J$ = −40°C to +125°C for minimum/maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| BATTERY VOLTAGE MONITORING | | | | | |
| Battery Monitor Voltage | | | | | |
| Range | | 2.7 | | 4.5 | V |
| Resolution | Based on 12-bit ADC | | 1.09 | | mV |
| Voltage Reading Accuracy | $T_J$ = 25°C | −12.5 | | +12.5 | mV |
| | $T_J$ = 0°C to +85°C | −30 | | +30 | mV |

## BOOST AND LED DRIVER SPECIFICATIONS

$V_{VIN4}$ = $V_{VIN123}$ = $V_{ISOS}$= 3.6 V, C9 = 4.7 µF, C10 = 4.7 µF, L2 = 4.7 µH, $T_J$ = −40°C to +125°C for minimum/maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted.

**Table 3.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Range | $V_{VIN4}$ | | 2.85 | | 5.5 | V |
| UNDERVOLTAGE LOCKOUT | $V_{UVLO\_VIN4\_RISE}$ | VIN4 rising | | 2.7 | 2.85 | V |
| | $V_{UVLO\_VIN4\_FALL}$ | VIN4 falling | 2.5 | 2.6 | | V |
| OUTPUT CHARACTERISTICS | | Standalone operation mode | | | | |
| Output Voltage Range | $V_{VOUT4}$ | | $V_{ISOS}$ | | 16 | V |
| FB4 Voltage Reference | $V_{FB4}$ | | 0.62 | 0.65 | 0.68 | V |
| | | $T_J$ = 25°C | −1.5 | | +1.5 | % |
| Line Regulation[1] | $\Delta V_{VOUT4}/V_{VIN4}$ | | | 0.1 | | %/V |
| POWER GOOD (PGOOD) | | Standalone operation mode | | | | |
| PGOOD Rising Threshold | $V_{PGOOD4\_RISE}$ | | | 90 | | % |
| PGOOD Hysteresis | $V_{PGOOD4\_HYS}$ | | | 5.5 | | % |
| PGOOD Falling Delay | $t_{PGOOD4\_FALL}$ | | | 2 | | ms |
| PGOOD Rising Delay | $t_{PGOO4\_RISE}$ | | | 2 | | ms |
| SW4 CHARACTERISTICS | | | | | | |
| SW4 On Resistance | $R_{DSON\_NFET}$ | NFET at $V_{VIN4}$ = 3.6 V | | 460 | 800 | mΩ |
| Overvoltage Threshold | $V_{OVP4}$ | Boost OVP threshold = 18.5 V | 17.5 | 18.5 | 19.5 | V |
| | | Boost OVP threshold = 15 V | 14.2 | 15 | 15.8 | V |
| | | Boost OVP threshold = 10 V | 9.5 | 10 | 10.5 | V |
| | | Boost OVP threshold = 5.6 V | 5.32 | 5.6 | 5.9 | V |
| | $V_{OVP4\_HYS}$ | OVP recovery hysteresis[1] | | 5 | | % |
| Start-Up Time | $t_{SS4}$ | | | 1.0 | 2.7 | ms |
| CURRENT LIMIT | $I_{LIM4}$ | BST_IPK = 0 | 510 | 600 | 690 | mA |
| | | BST_IPK = 1 | | 300 | | mA |
| OSCILLATOR CIRCUIT | | | | | | |
| Switching Frequency | $f_{SW4}$ | | 1.35 | 1.5 | 1.65 | MHz |
| Minimum On Time | $t_{MIN\_ON4}$ | | | 50 | | ns |
| LED CURRENT CONTROL | | | | | | |
| LED Current | | | | | | |
| Range, 6-Bit | $I_{Dx}$ | | 0 | | 20 | mA |
| Accuracy | | $I_{Dx}$ = 20 mA | −10 | | +10 | % |
| Matching | | $I_{Dx}$ = 20 mA | | 2.0 | | % |
| LED Pin Leakage Current | $I_{Dx\_LEAK}$ | | | | 0.5 | µA |
| LED Current Ramp-Up Time | $t_{Dx\_RISE}$ | $I_{Dx}$ = 20 mA | | 20 | | µs |
| LED Current Ramp-Down Time | $t_{Dx\_FALL}$ | $I_{Dx}$ = 20 mA | | 20 | | µs |
| LED Source Headroom | $V_{Dx\_HDRM}$ | ILEDx[5:0] =11111 | | 0.65 | 0.75 | V |
| LED ON/OFF TIMER | | | | | | |
| LED Timer Accuracy | | Including on timer and off timer | −10 | | +10 | % |

[1] Specification is not production tested, but is supported by characterization data at initial product release.

## LDO SPECIFICATIONS

$V_{VBUSx}$ = 5.0 V, $V_{VIN4}$ = $V_{VIN123}$ = $V_{ISOS}$= 3.6 V, C5 = C6 = C7 = C8 = 1 µF; $T_J$ = −40°C to +125°C for minimum/maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted.

**Table 4.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LDO1 INPUT VOLTAGE RANGE | $V_{VIN123}$ | | 2.56 | | 5.5 | V |
| KEEPALIVE LDO1 | | | | | | |
| UNDERVOLTAGE LOCKOUT | $V_{UVLO\_LDO1\_RISE}$ | VIN123 rising | | | 2.56 | V |
| | $V_{UVLO\_LDO1\_FALL}$ | VIN123 falling | 1.78 | | | V |
| | $V_{UVLO\_LDO1\_HYS}$ | | | 200 | | mV |
| Output Voltage Range | $V_{VOUT1}$ | Fuse trim or I²C, four bits | 1.0 | | 4.2 | V |
| Output Accuracy | | $I_{OUT1}$ = 10 mA, $T_J$ = 25°C | −1 | | +1 | % |
| | | $I_{OUT1}$ = 10 mA | −2.0 | | +2.0 | % |
| Line Regulation | $\Delta V_{VOUT1}/V_{IN123}$ | $V_{VIN123}$ = ($V_{VOUT1}$ + 0.5 V) to 5.5 V | −0.1 | | +0.1 | %/V |
| Load Regulation | $\Delta V_{VOUT1}/I_{OUT1}$ | $I_{OUT1}$ = 100 µA to 150 mA | | | 0.015 | %/mA |
| Dropout Voltage | $V_{DROP\_OUT1}$ | $V_{VOUT1}$ = 3.3 V, $I_{OUT1}$ = 10 mA | | 54 | 130 | mV |
| | | $V_{VOUT1}$ = 3.3 V, $I_{OUT1}$ = 150 mA | | 150 | 240 | mV |
| Current-Limit Threshold | $I_{LIM\_LDO1}$ | | 200 | 300 | 440 | mA |
| Output Noise[1] | $V_{NOISE\_LDO1}$ | 10 Hz to 100 kHz, $V_{VIN123}$= 3.6 V, $V_{VOUT1}$ = 3.3 V | | 100 | | µV rms |
| Power Supply Rejection Ratio[1] | PSRR | 100 Hz, $V_{VIN123}$= 3.6 V, $V_{VOUT1}$ = 3.3 V, $I_{OUT1}$ = 10 mA | | 40 | | dB |
| | | 1 kHz, $V_{VIN123}$= 3.6 V, $V_{VOUT1}$ = 3.3 V, $I_{OUT1}$ = 10 mA | | 35 | | dB |
| LDO Start-Up Time | $t_{SS\_LDO1}$ | $V_{VOUT1}$ = 3.3 V, LDO mode | | 600 | | µs |
| PGOOD Rising Threshold | $V_{PGOOD1\_RISE}$ | Only effective in LDO mode | | 90 | | % |
| PGOOD Hysteresis | $V_{PGOOD1\_HYS}$ | | | 4.5 | | % |
| PGOOD Falling Delay | $t_{PGOOD1\_Fall}$ | | | 120 | | µs |
| PGOOD Rising Delay | $t_{PGOOD1\_RISE}$ | | | 2 | | ms |
| Load Switch Turn-On Rise Time | $t_{RISE\_SWITCH1}$ | $V_{OUT1}$ = 3.3 V, load switch mode | | 120 | | µs |
| Load Switch On Resistance | $R_{DSON\_SWITCH1}$ | | | 700 | | mΩ |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS\_LDO1}$ | $V_{VIN123}$ = 3.6 V | | 500 | | Ω |
| LDO2 INPUT VOLTAGE RANGE | $V_{VIN4}$ | $V_{VIN4}$ = $V_{VIN123}$ | 2.85 | | 5.5 | V |
| GENERAL-PURPOSE LDO2 | | | | | | |
| Undervoltage Lockout | $V_{UVLO\_LDO2\_RISE}$ | VIN4 rising | | 2.7 | 2.85 | V |
| | $V_{UVLO\_LDO2\_FALL}$ | VIN4 falling | 2.5 | 2.6 | | V |
| | $V_{UVLO\_LDO2\_HYS}$ | | | 100 | | mV |
| Output Voltage Range | $V_{VOUT2}$ | Fuse trim or I²C, 4 bits | 1.0 | | 4.2 | V |
| Output Accuracy | | $I_{OUT2}$ = 10 mA, $T_J$ = 25°C | −0.75 | | +0.75 | % |
| | | $I_{OUT2}$ = 10 mA | −1.5 | | +1.5 | % |
| Line Regulation | $(\Delta V_{VOUT2})/V_{VIN123}$ | $V_{VIN123}$ = ($V_{VOUT2}$ + 0.5 V) to 5.5 V | −0.1 | | +0.1 | %/V |
| Load Regulation | $(\Delta V_{VOUT2})/I_{OUT2}$ | $I_{OUT2}$ = 100 µA to 150 mA | | | 0.01 | %/mA |
| Dropout Voltage | | | | | | |
| LFCSP Package | $V_{DROP\_OUT2}$ | $V_{VOUT2}$ = 3.3 V, $I_{OUT2}$ = 10 mA | | 76 | 140 | mV |
| WFCSP Package | $V_{DROP\_OUT2}$ | $V_{VOUT2}$ = 3.3 V, $I_{OUT2}$ = 10 mA | | 65 | 120 | mV |
| LFCSP Package | $V_{DROP\_OUT2}$ | $V_{VOUT2}$ = 3.3 V, $I_{OUT2}$ = 150 mA | | 100 | 180 | mV |
| WFCSP Package | $V_{DROP\_OUT2}$ | $V_{VOUT2}$ = 3.3 V, $I_{OUT2}$ = 150 mA | | 80 | 150 | mV |
| Current-Limit Threshold | $I_{LIM\_LDO2}$ | | 220 | 320 | 430 | mA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Noise[1] | $V_{NOISE\_LDO2}$ | 10 Hz to 100 kHz, $V_{VIN123}$ = 3.6 V, $V_{VOUT2}$ = 3.3 V | | 120 | | µV rms |
| Power Supply Rejection Ratio[1] | PSRR | 100 Hz, $V_{IN123}$ = 3.6 V, $V_{VOUT2}$ = 3.3V, $I_{OUT2}$ = 10 mA | | 60 | | dB |
| | | 1 kHz, $V_{IN123}$ = 3.6 V, $V_{VOUT2}$ = 3.3 V, $I_{OUT2}$ = 10 mA | | 50 | | dB |
| LDO Start-Up Time | $t_{SS\_LDO2}$ | $V_{VOUT2}$ = 3.3 V, LDO mode | | 80 | | µs |
| Load Switch Turn-On Rise Time | $t_{RISE\_SWITCH2}$ | $V_{VOUT2}$ = 3.3 V, load switch mode | | 80 | | µs |
| Load Switch On Resistance | | | | | | |
| LFCSP Package | $R_{DSON\_SWITCH2}$ | | | 400 | 600 | mΩ |
| WFCSP Package | $R_{DSON\_SWITCH2}$ | | | 300 | 500 | mΩ |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS\_LDO2}$ | $V_{VIN123}$ = 3.6 V | | 500 | | Ω |
| LDO3 INPUT VOLTAGE RANGE | $V_{VIN4}$ | $V_{VIN4}$ = $V_{VIN123}$ | 2.85 | | 5.5 | V |
| GENERAL-PURPOSE LDO3 | | | | | | |
| UNDERVOLTAGE LOCKOUT | $V_{UVLO\_LDO3\_RISE}$ | VIN4 rising | | 2.7 | 2.85 | V |
| | $V_{UVLO\_LDO3\_FALL}$ | VIN4 falling | 2.5 | 2.6 | | V |
| | $V_{UVLO\_LDO3\_HYS}$ | | | 100 | | mV |
| Output Voltage Range | $V_{VOUT3}$ | Fuse trim or $I^2C$, four bits | 1.0 | | 4.2 | V |
| Output Accuracy | $V_{VOUT3}$ | $I_{OUT3}$ = 10 mA, $T_J$ = +25°C | −0.75 | | +0.75 | % |
| | | $I_{OUT3}$ = 10 mA | −1.5 | | +1.5 | % |
| Line Regulation | $\Delta V_{OUT3}/V_{VIN123}$ | $V_{VIN123}$ = ($V_{VOUT3}$ + 0.5 V) to 5.5 V | −0.1 | | +0.1 | %/V |
| Load Regulation | $\Delta V_{OUT3}/I_{OUT3}$ | $I_{OUT3}$ = 100 µA to 150 mA | | | 0.01 | %/mA |
| Dropout Voltage | | | | | | |
| LFCSP Package | $V_{DROP\_OUT3}$ | $V_{VOUT3}$ = 3.3 V, $I_{OUT3}$ = 10 mA | | 76 | 140 | mV |
| WFCSP Package | $V_{DROP\_OUT3}$ | $V_{VOUT3}$ = 3.3 V, $I_{OUT3}$ = 10 mA | | 65 | 120 | mV |
| LFCSP Package | $V_{DROP\_OUT3}$ | $V_{VOUT3}$ = 3.3 V, $I_{OUT3}$ = 150 mA | | 100 | 180 | mV |
| WFCSP Package | $V_{DROP\_OUT3}$ | $V_{VOUT3}$ = 3.3 V, $I_{OUT3}$ = 150 mA | | 80 | 150 | mV |
| Current Limit Threshold | $I_{LIM\_LDO3}$ | | 220 | 320 | 430 | mA |
| Output Noise[1] | $V_{NOISE\_LDO3}$ | 10 Hz to 100 kHz, $V_{VIN123}$ = 3.6 V, $V_{VOUT3}$ = 3.3 V | | 120 | | µV rms |
| Power Supply Rejection Ratio[1] | PSRR | 100 Hz, $V_{VIN123}$ = 3.6 V, $V_{VOUT3}$ = 3.3 V, $I_{OUT3}$ = 10 mA | | 60 | | dB |
| | | 1 kHz, $V_{VIN123}$ = 3.6 V, $V_{VOUT3}$ = 3.3 V, $I_{OUT3}$ = 10 mA | | 50 | | dB |
| LDO Start-Up Time | $t_{SS\_LDO3}$ | $V_{VOUT3}$ = 3.3 V, LDO mode | | 80 | | µs |
| Load Switch Turn-On Rise Time | $t_{RISE\_SWITCH3}$ | $V_{VOUT3}$ = 3.3 V, load switch mode | | 80 | | µs |
| Load Switch On Resistance | | | | | | |
| LFCSP Package | $R_{DSON\_SWITCH3}$ | | | 400 | 600 | mΩ |
| WFCSP Package | $R_{DSON\_SWITCH3}$ | | | 300 | 500 | mΩ |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS\_LDO3}$ | $V_{IN123}$ = 3.6 V | | 500 | | Ω |

[1] Guaranteed by design.

## RECOMMENDED INPUT AND OUTPUT CAPACITANCE AND INDUCTANCE SPECIFICATIONS

**Table 5.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| EFFECTIVE CAPACITANCE | | | | |
| Charger Capacitance | | | | |
| VBUSx Pin | 1.0 | 2.2 | | µF |
| CFL1 Pin | 2.0 | 4.7 | | µF |
| CFL2 Pin | 1.0 | 2.2 | | µF |
| ISOS Pin | 4.0 | 10 | | µF |
| ISOB Pin | 4.0 | 10 | | µF |
| LDO Capacitance | | | | |
| VIN123 Pin | 0.7 | 1 | | µF |
| LDO1 | 0.7 | 1 | | µF |
| LDO2 | 0.7 | 1 | | µF |
| LDO3 | 0.7 | 1 | | µF |
| Boost Capacitance | | | | |
| VIN4 Pin | 1 | 4.7 | | µF |
| VOUT4 Pin | 0.47 | 4.7 | | µF |
| INDUCTANCE | | | | |
| Buck | 0.5 | 1.5 | 2.2 | µH |
| Boost | 2 | 4.7 | 10 | µH |

## I²C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

**Table 6.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| I²C-COMPATIBLE INTERFACE | | | | | |
| Capacitive Load, Each Bus Line | $C_S$ | | | 400 | pF |
| SCL | | | | | |
| Clock Frequency | $f_{SCL}$ | | | 400 | kHz |
| High Time | $t_{HIGH}$ | 0.6 | | | µs |
| Low Time | $t_{LOW}$ | 1.3 | | | µs |
| Data | | | | | |
| Setup Time | $t_{SU,DAT}$ | 100 | | | ns |
| Hold Time[1] | $t_{HD,DAT}$ | 0 | | 0.9 | µs |
| Setup Time for Repeated Start | $t_{SU,STA}$ | 0.6 | | | µs |
| Hold Time for Start/Repeated Start | $t_{HD,STA}$ | 0.6 | | | µs |
| Bus Free Time Between a Stop and a Start Condition | $t_{BUF}$ | 1.3 | | | µs |
| Setup Time for Stop Condition | $t_{SU,STO}$ | 0.6 | | | µs |
| SCL/SDA | | | | | |
| Rise Time | $t_R$ | | | 300 | ns |
| Fall Time | $t_F$ | | | 300 | ns |
| Pulse Width of Suppressed Spike | $t_{SP}$ | 0 | | 50 | ns |

[1] A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL. See Figure 3, the I²C timing diagram.

### *Timing Diagram*

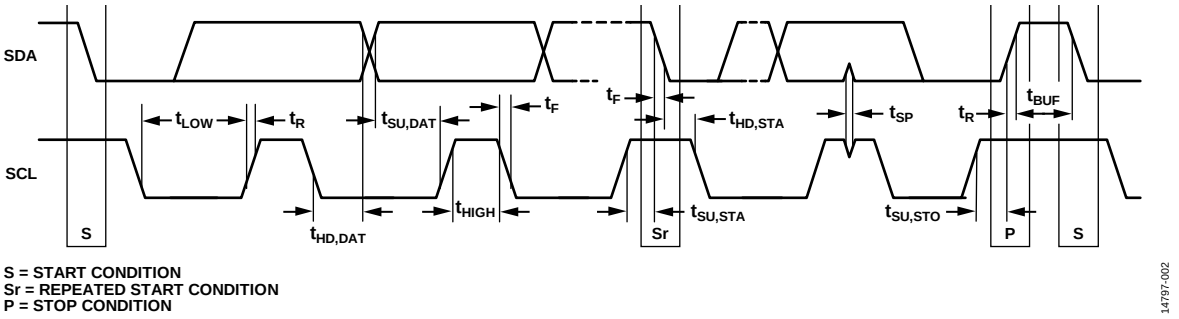



*Figure 3. I²C Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 7.**

| Parameter | Rating |
|---|---|
| VBUSA, VBUSB to PGND1 | −0.5 V to +20 V |
| SW4, VOUT4, D1, D2, D3, D4, D5 to PGND4 | −0.5 V to +20 V |
| FB4 | −0.3 V to +6 V |
| CFL2 to AGND | −0.3 V to +3.3 V |
| PGND1, PGND4 to AGND | −0.3 V to +0.3 V |
| All Other Pins to AGND | −0.3 V to +6 V |
| Continuous Drain Current, Battery Supplementary Mode, from ISOB to ISOS, $T_J$ = 125°C | 1.1 A |
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required. $\theta_{JA}$ is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. $\theta_{JC}$ is the junction to case thermal resistance.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| CP-32-12[1] | 42 | 2.1 | °C/W |
| CB-32-1 | 64 | 0.7 | °C/W |

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

### *Maximum Power Dissipation*

The maximum safe power dissipation in the ADP5350 package is limited by the associated rise in junction temperature ($T_J$) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADP5350. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices that potentially cause failure.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

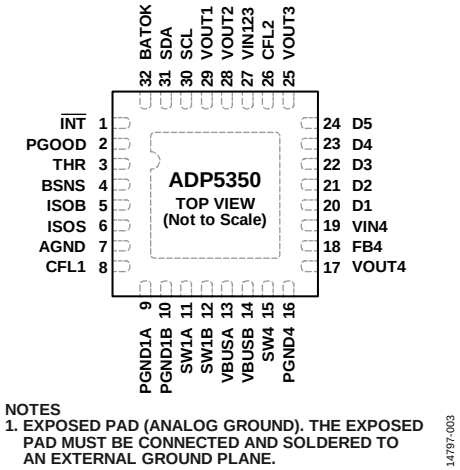



*Figure 4. LFCSP Pin Configuration (Top View)*

**Table 9. LFCSP Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $\overline{\text{INT}}$ | Processor Interrupt (Active Low). This pin requires an external pull-up resistor. If this pin is not used, it can be left floating. |
| 2 | PGOOD | Power-Good Signal Output. This open-drain output is the power-good signal for the selected channels. |
| 3 | THR | Battery Pack Thermistor Connection. |
| 4 | BSNS | Battery Voltage Sense Pin. |
| 5 | ISOB | Battery Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. |
| 6 | ISOS | Charger Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. |
| 7 | AGND | Analog Ground. |
| 8 | CFL1 | Power input to the charger regulator. Connect a ceramic filter capacitor between this pin and either PGND1A or PGND1B. |
| 9, 10 | PGND1A, PGND1B | Power Ground for the Battery Charger. |
| 11, 12 | SW1A, SW1B | Switching Node for the Battery Charger. |
| 13, 14 | VBUSA, VBUSB | Power Connection to USB Bus Voltage. |
| 15 | SW4 | Switching Node for the Boost Regulator. |
| 16 | PGND4 | Power Ground for the Boost Regulator. |
| 17 | VOUT4 | Power Output for the Boost Regulator. |
| 18 | FB4 | Feedback Sensing Input for the Boost Regulator. In standalone mode, connect this pin to a resistor divider from $V_{VOUT4}$. In LED operation mode, connect FB4 to ground. |
| 19 | VIN4 | Input Voltage for the Boost Regulator and LDO Control Block. |
| 20 | D1 | LED 1 Sink Channel. Connect this pin to the cathode of the LED. |
| 21 | D2 | LED 2 Sink Channel. Connect this pin to the cathode of the LED. |
| 22 | D3 | LED 3 Sink Channel. Connect this pin to the cathode of the LED. |
| 23 | D4 | LED 4 Sink Channel. Connect this pin to the cathode of the LED. |
| 24 | D5 | LED 5 Sink Channel. Connect this pin to the cathode of the LED. |
| 25 | VOUT3 | Power Output for LDO3. |
| 26 | CFL2 | Internal Regulator Output for the Fuel Gauge. Connect a ceramic capacitor between this pin and AGND. |
| 27 | VIN123 | Power Input for LDO1, LDO2, and LDO3. |
| 28 | VOUT2 | Power Output for LDO2. |
| 29 | VOUT1 | Power Output for LDO1. |
| 30 | SCL | $I^2C$ Serial Clock. This pin requires an external pull-up resistor. |
| 31 | SDA | $I^2C$ Serial Data. This pin requires an external pull-up resistor. |
| 32 | BATOK | Battery Status Open-Drain Output Flag (Active High). This pin enables the system when the battery reaches $V_{WEAK}$. |
| | EPAD | Exposed Pad (Analog Ground). The exposed pad must be connected and soldered to an external ground plane. |

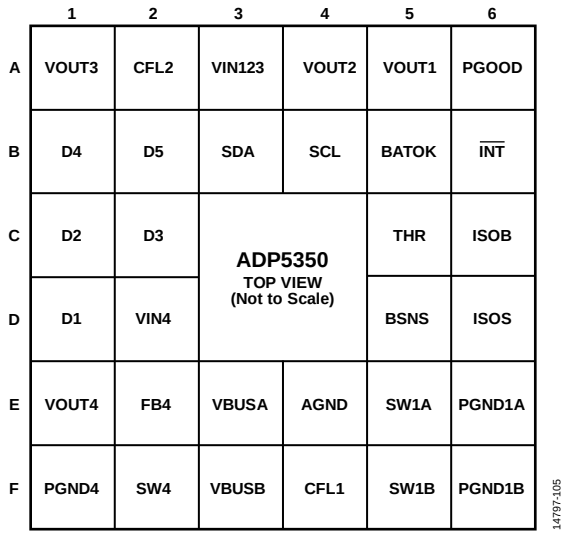



*Figure 5. WLCSP Pin Configuration (Top View)*

**Table 10. WLCSP Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| B6 | $\overline{\text{INT}}$ | Processor Interrupt (Active Low). This pin requires an external pull-up resistor. If this pin is not used, it can be left floating. |
| A6 | PGOOD | Power-Good Signal Output. This open-drain output is the power-good signal for the selected channels. |
| C5 | THR | Battery Pack Thermistor Connection. |
| D5 | BSNS | Battery Voltage Sense Pin. |
| C6 | ISOB | Battery Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. |
| D6 | ISOS | Charger Supply Side Input to Internal Isolation FET/Battery Current Regulation FET. |
| E4 | AGND | Analog Ground. |
| F4 | CFL1 | Power input to the charger regulator. Connect a ceramic filter capacitor between this pin and either PGND1A or PGND1B. |
| E6, F6 | PGND1A, PGND1B | Power Ground for the Battery Charger. |
| E5, F5 | SW1A, SW1B | Switching Node for the Battery Charger. |
| E3, F3 | VBUSA, VBUSB | Power Connection to USB Bus Voltage. |
| F2 | SW4 | Switching Node for the Boost Regulator. |
| F1 | PGND4 | Power Ground for the Boost Regulator. |
| E1 | VOUT4 | Power Output for the Boost Regulator. |
| E2 | FB4 | Feedback Sensing Input for the Boost Regulator. In standalone mode, connect this pin to a resistor divider from $V_{VOUT4}$. In LED operation mode, connect FB4 to ground. |
| D2 | VIN4 | Input Voltage for the Boost Regulator and LDO Control Block. |
| D1 | D1 | LED 1 Sink Channel. Connect this pin to the cathode of the LED. |
| C1 | D2 | LED 2 Sink Channel. Connect this pin to the cathode of the LED. |
| C2 | D3 | LED 3 Sink Channel. Connect this pin to the cathode of the LED. |
| B1 | D4 | LED 4 Sink Channel. Connect this pin to the cathode of the LED. |
| B2 | D5 | LED 5 Sink Channel. Connect this pin to the cathode of the LED. |
| A1 | VOUT3 | Power Output for LDO3. |
| A2 | CFL2 | Internal Regulator Output for the Fuel Gauge. Connect a ceramic capacitor between this pin and AGND. |
| A3 | VIN123 | Power Input for LDO1, LDO2, and LDO3. |
| A4 | VOUT2 | Power Output for LDO2. |
| A5 | VOUT1 | Power Output for LDO1. |
| B4 | SCL | $I^2C$ Serial Clock. This pin requires an external pull-up resistor. |
| B3 | SDA | $I^2C$ Serial Data. This pin requires an external pull-up resistor. |
| B5 | BATOK | Battery Status Open-Drain Output Flag (Active High). This pin enables the system when the battery reaches $V_{WEAK}$. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VBUSx}$ = 5.0 V, $V_{VIN4}$ = $V_{VIN123}$ = $V_{ISOS}$ = 3.6 V, $C_{BUS}$ = 2.2 µF, $C_3$ = 10 µF, $C_4$ = 10 µF, $C_{CFL1}$ = 4.7 µF, $L_{OUT1}$ = 1.5 µH, all registers are at default values, unless otherwise noted.

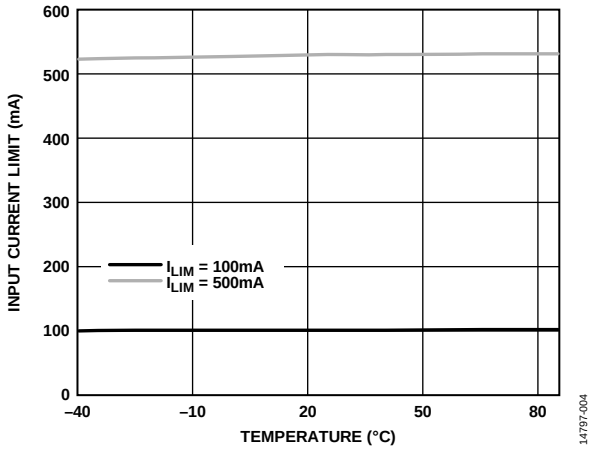



Figure 6. Input Current Limit vs. Temperature

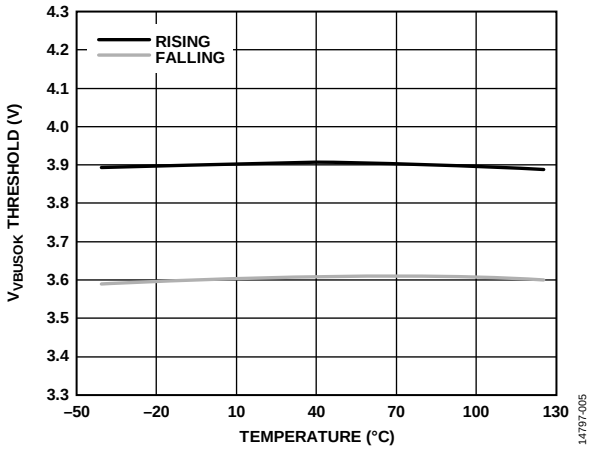



Figure 7. $V_{VBUSOK}$ Threshold vs. Temperature

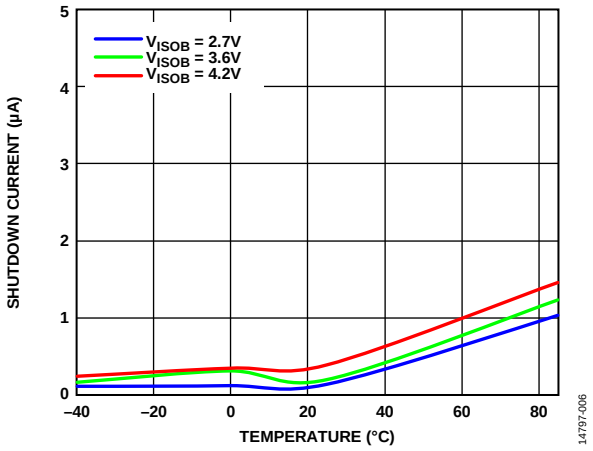



Figure 8. Shutdown Current vs. Temperature

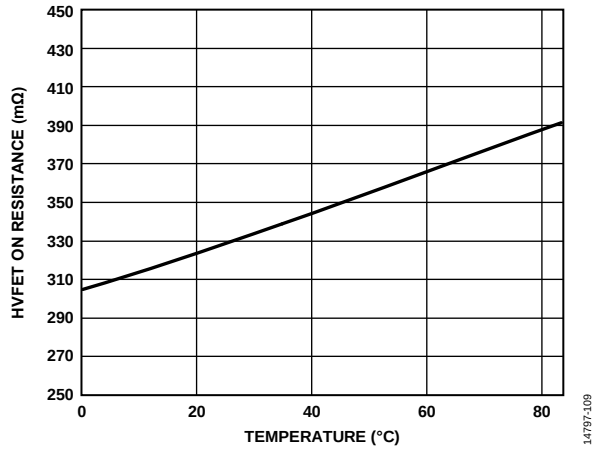



Figure 9. High Voltage FET (HVFET) On Resistance vs. Temperature

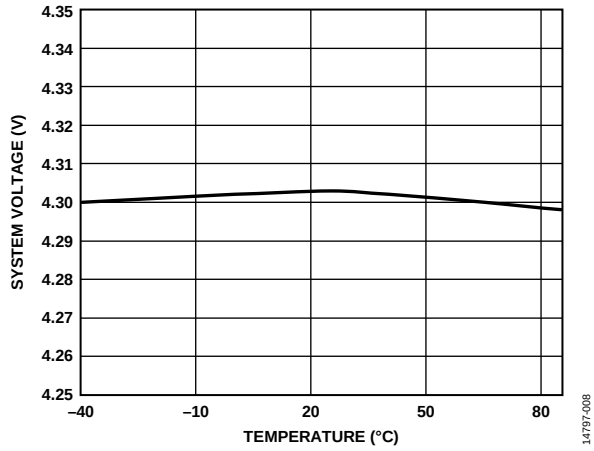



Figure 10. System Voltage vs. Temperature

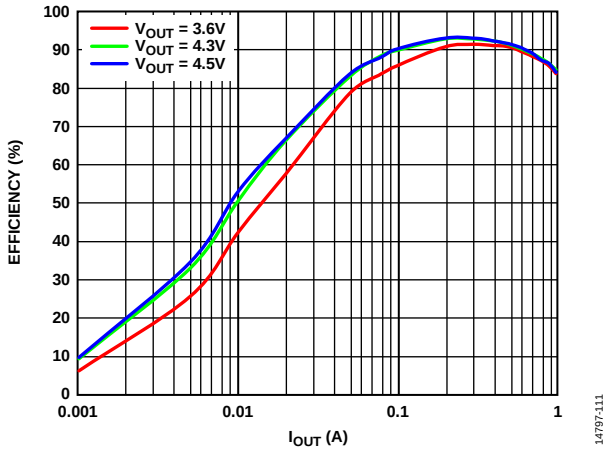



Figure 11. Efficiency vs. Ouptut Current ($I_{OUT}$), Buck Regulator Efficiency

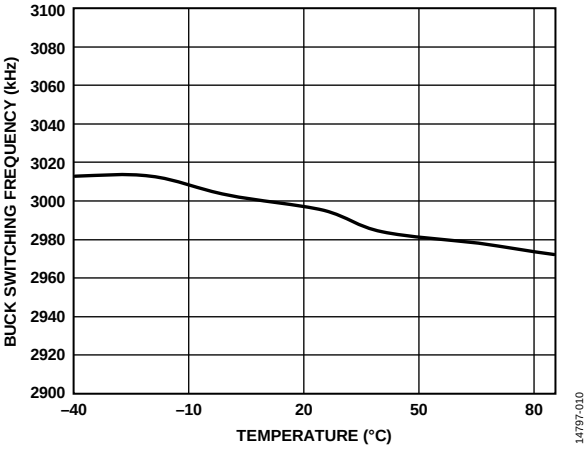



Figure 12. Buck Switching Frequency vs. Temperature

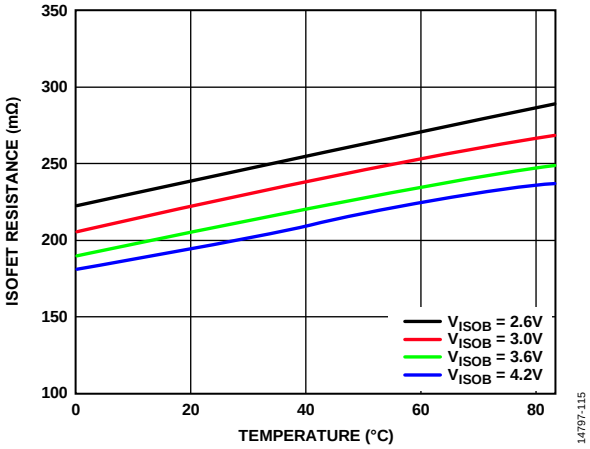



Figure 15. Isolation FET (ISOFET) Resistance vs. Temperature at Various Battery Voltage Levels, LFCSP Package

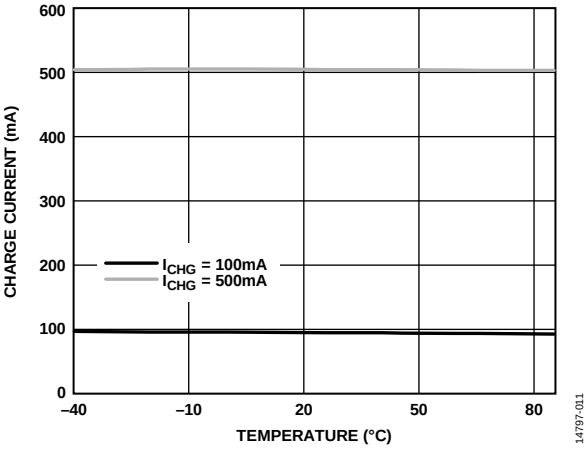



Figure 13. Charge Current vs. Temperature

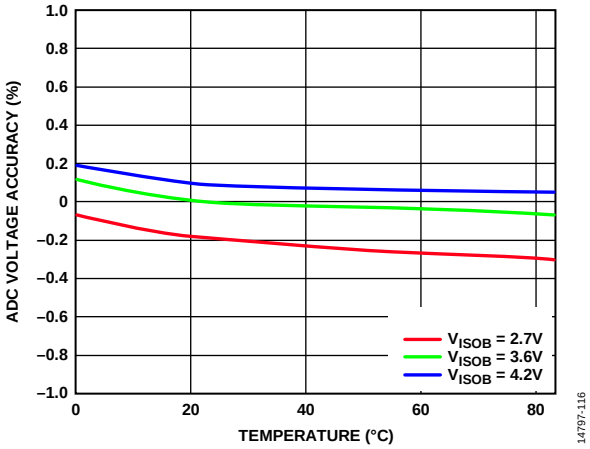



Figure 16. ADC Voltage Accuracy vs. Temperature

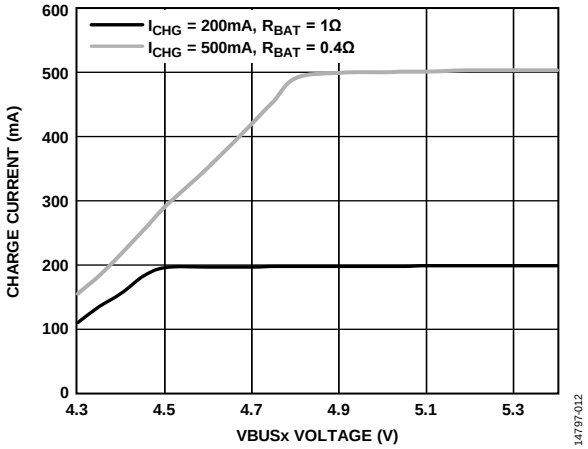



Figure 14. Charge Current vs. VBUSx Voltage

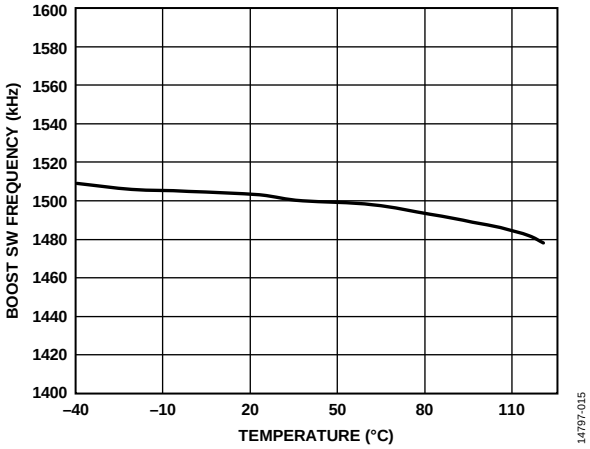



Figure 17. Boost Switching Frequency vs. Temperature

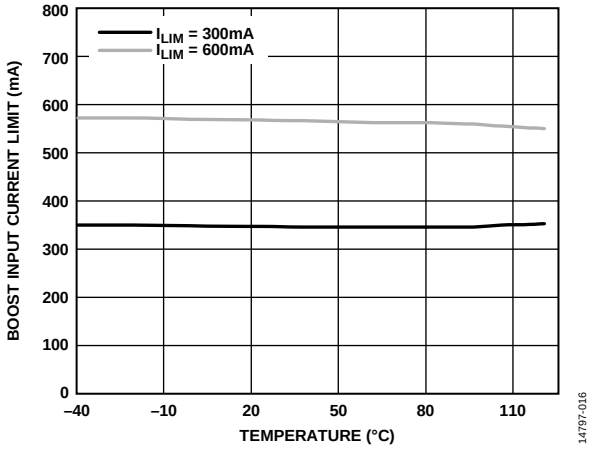



Figure 18. Boost Input Current Limit vs. Temperature

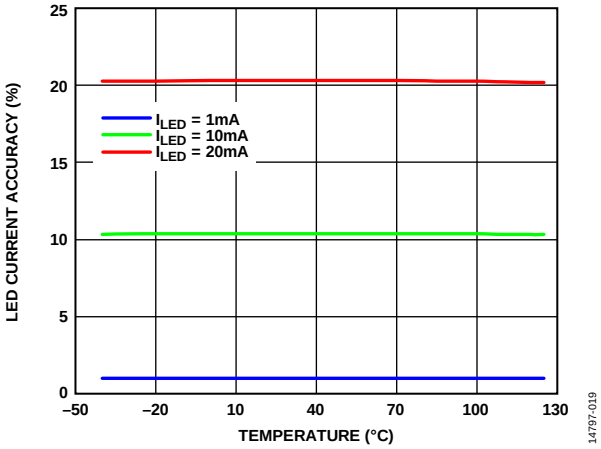



Figure 21. LED Current Accuracy vs. Temperature

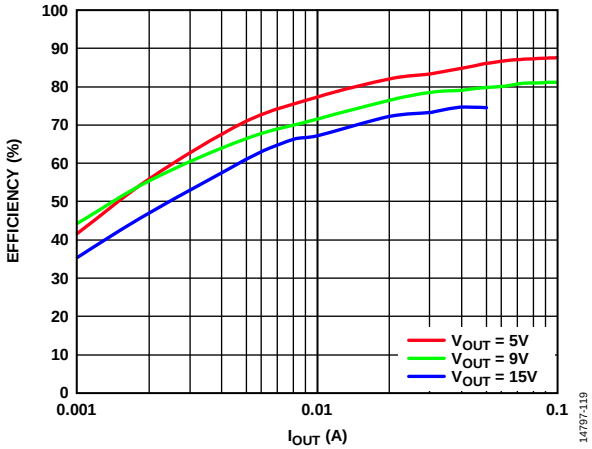



Figure 19. Boost Efficiency vs. Output Current ($I_{OUT}$)

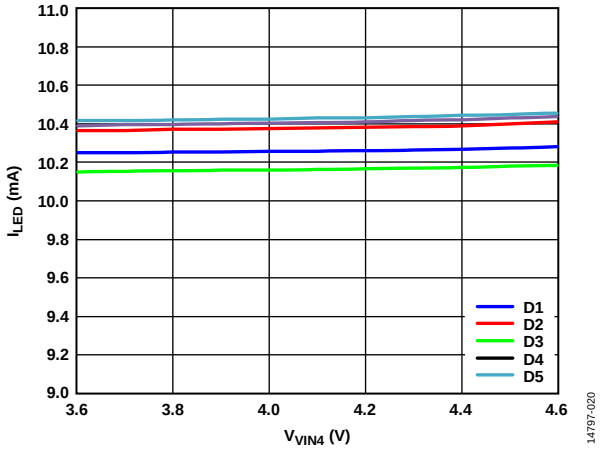



Figure 22. LED Channel Current ($I_{LED}$) vs. $V_{VIN4}$

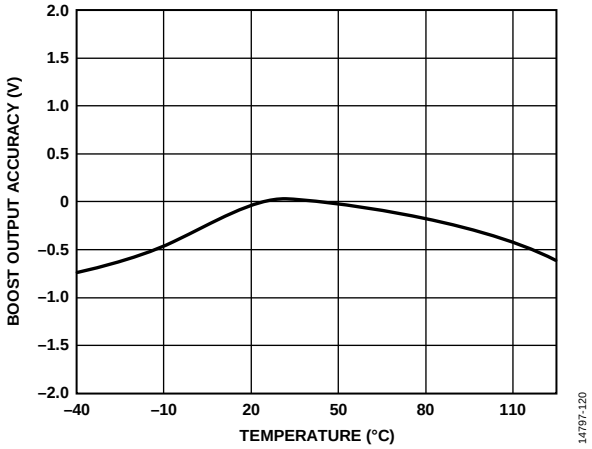



Figure 20. Boost Output Accuracy vs. Temperature, $V_{VOUT4}$ = 5 V

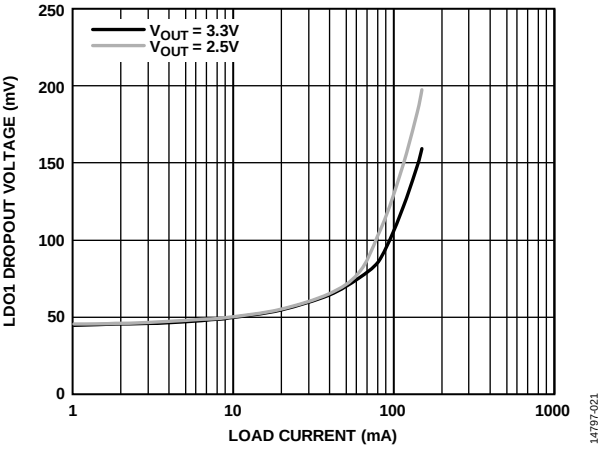



Figure 23. LDO1 Dropout Voltage vs. Load Current, LFCSP Package

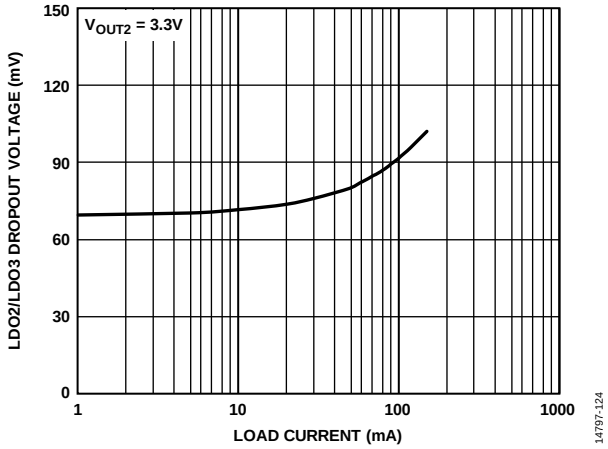



Figure 24. LDO2/LDO3 Dropout Voltage vs. Load Current, LFCSP Package

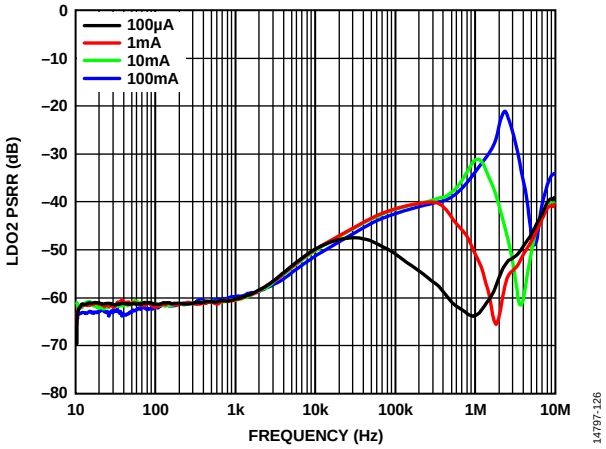



Figure 26. LDO2 Power Supply Rejection Ratio (PSRR) vs. Frequency, $V_{VOUT2}$ = 3.3 V, $V_{IN123}$ = 3.6 V

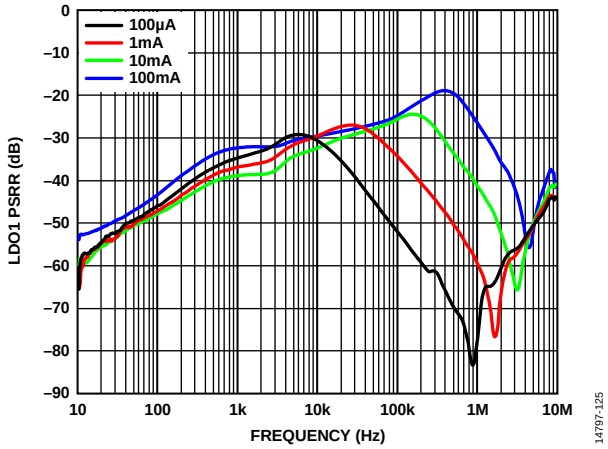



Figure 25. LDO1 PSRR vs. Frequency, $V_{VOUT1}$ = 3.3 V, $V_{VIN123}$ = 3.6 V

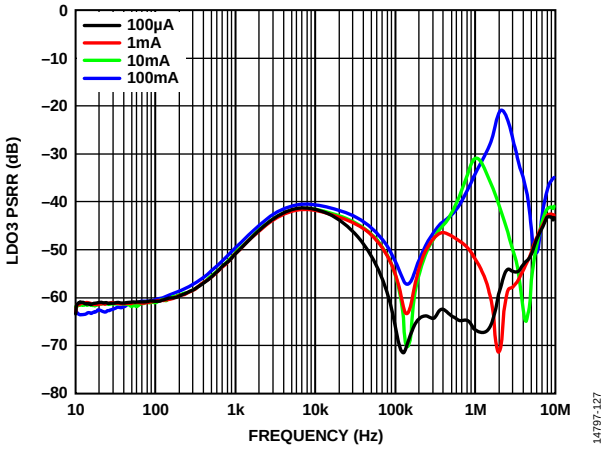



Figure 27. LDO3 PSRR vs. Frequency, $V_{VOUT3}$ = 3.3 V, $V_{IN123}$ = 3.6 V

## TYPICAL WAVEFORMS

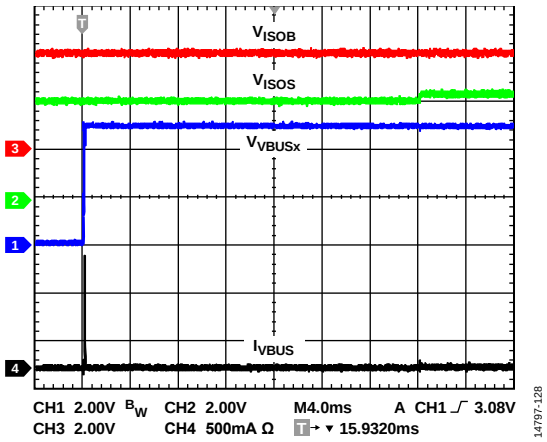



Figure 28. VBUSx Connected to USB Power

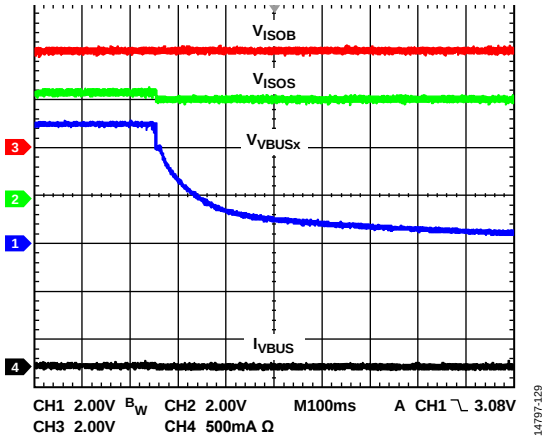



Figure 29. VBUSx Disconnected from USB Power

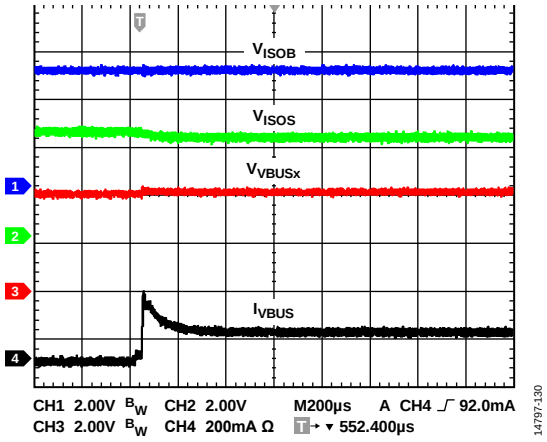



Figure 30. Charger Start with EN_CHG Set High, $I_{LIM}$ = 500 mA, $I_{CHG}$ = 150 mA, $V_{VBUSx}$ = 5 V

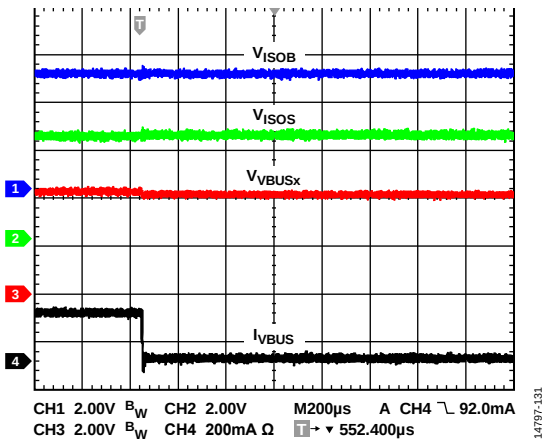



Figure 31. Charger Stop with EN_CHG Set Low, $I_{LIM}$ = 500 mA, $I_{CHG}$ = 200 mA, $V_{VBUSx}$ = 5 V

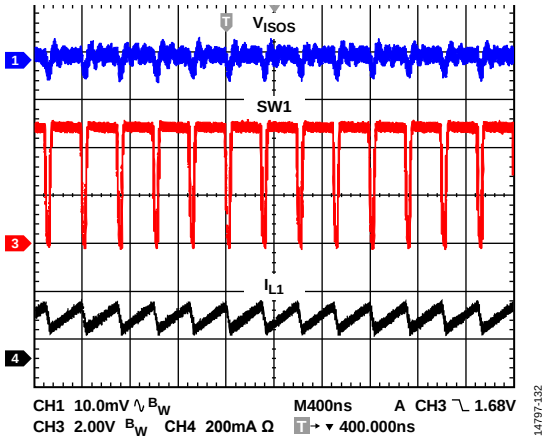



Figure 32. Fast Charger Status, $I_{CHG}$ = 200 mA, $V_{VBUSx}$ = 5 V

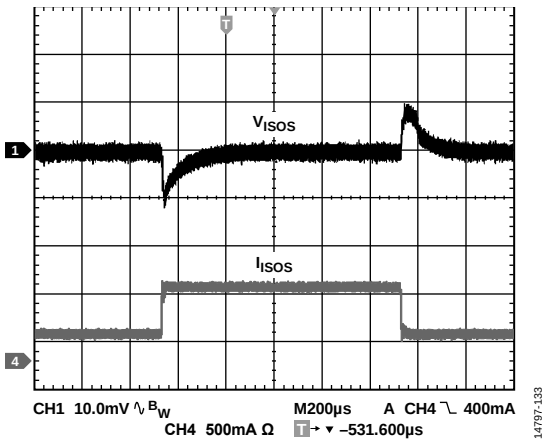



Figure 33. $V_{ISOS}$ Voltage Load Transient Response, $V_{ISOS}$ = 4.3 V, $V_{VBUSx}$ = 5 V,

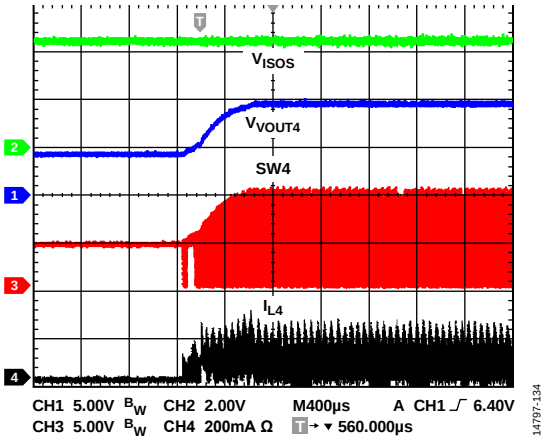



Figure 34. Boost Voltage Soft Start, LED Mode; $I_{LED1} = I_{LED2} = I_{LED3} = 10$ mA

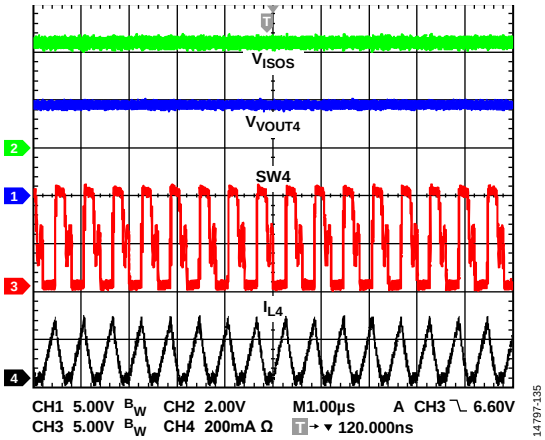



Figure 35. Boost Operation, LED Mode; $I_{LED1} = I_{LED2} = I_{LED3} = 10$ mA

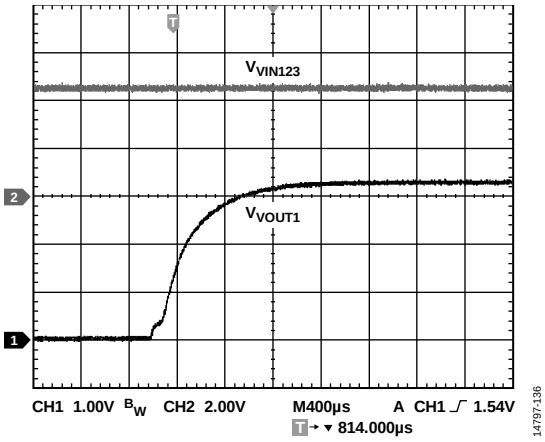



Figure 36. LDO1 Output Soft Start, $R_{LDO1} = 330\ \Omega$

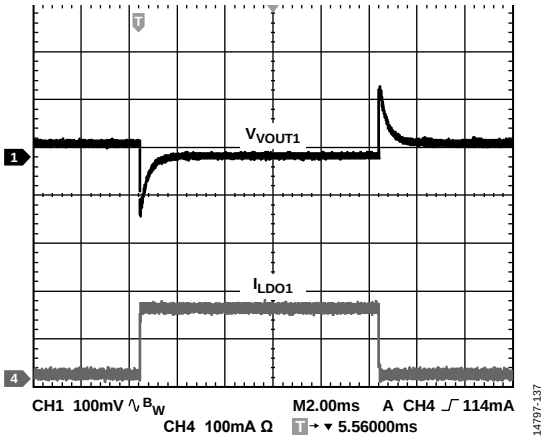



Figure 37. LDO1 Output Load Transient Response

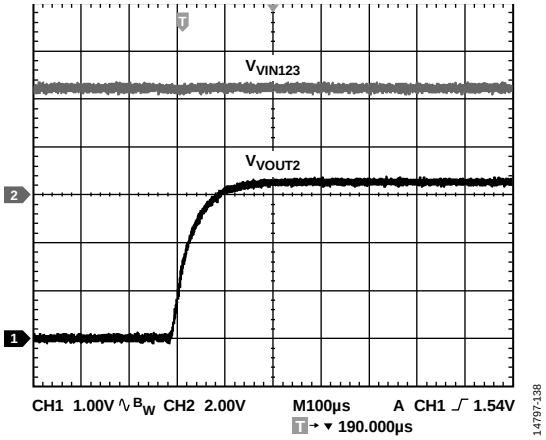



Figure 38. LDO2 Output Soft Start, $R_{LDO1} = 330\ \Omega$

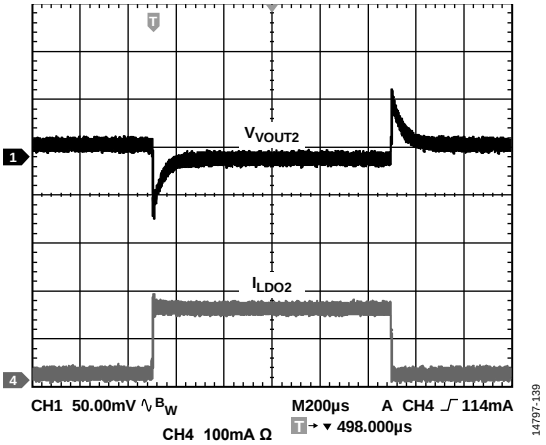



Figure 39. LDO2 Output Load Transient Response

# THEORY OF OPERATION

## BATTERY CHARGER OVERVIEW

The ADP5350 integrates a fully I²C-programmable charger for single-cell Li-Ion or Li-Ion polymer batteries suitable for a wide range of portable applications.

Figure 40 shows the complete charge cycle of the ADP5350 when VBUSx is connected. The ISOS pin voltage remains at $V_{ISOS\_TRK}$ when the device is not charging or when it is in trickle charge mode. When the device begins a fast charge, the $V_{ISOS}$ voltage follows the battery voltage until the charge is complete. The charge current keeps constant in CC mode and reduces to $I_{END}$ in CV mode. When the battery voltage, $V_{ISOB}$, drops to $V_{TRM} - V_{RCH}$, the charger resumes to charge until the charge completes.

The highly efficient switch dc-to-dc architecture enables higher charging currents as well as a lower temperature charging operation that results in faster charging times.

The charger of the ADP5350 operates from an input voltage from 4 V to 5.4 V but is tolerant of voltages of up to 20 V. This tolerance alleviates concerns about USB bus spiking during disconnection or connection.

The ADP5350 features an internal FET between the dc-to-dc charger output and the battery. This FET permits battery isolation and, therefore, system powering in a dead battery or no battery scenario, which allows immediate system function upon connection to a USB power supply.

The charger of the ADP5350 is fully compliant with the USB 3.0 specification and enables charging via the mini USB VBUSx pin from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the ADP5350 can be set to apply the correct current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB compliant sources, such as wall chargers, host chargers, hub chargers, and standard hosts and hubs.

A processor is able to control the USB charger using the I²C to program the charging current and numerous other parameters, including

- Trickle charge current level and voltage threshold
- Fast charge (CC) current level
- Fast charge (CV) voltage level
- Fast charge safety timer period
- Watchdog safety timer parameters
- Weak battery threshold detection
- End of charge current level for charge complete
- Recharge threshold
- VBUSx input current limit
- Charge enable and disable

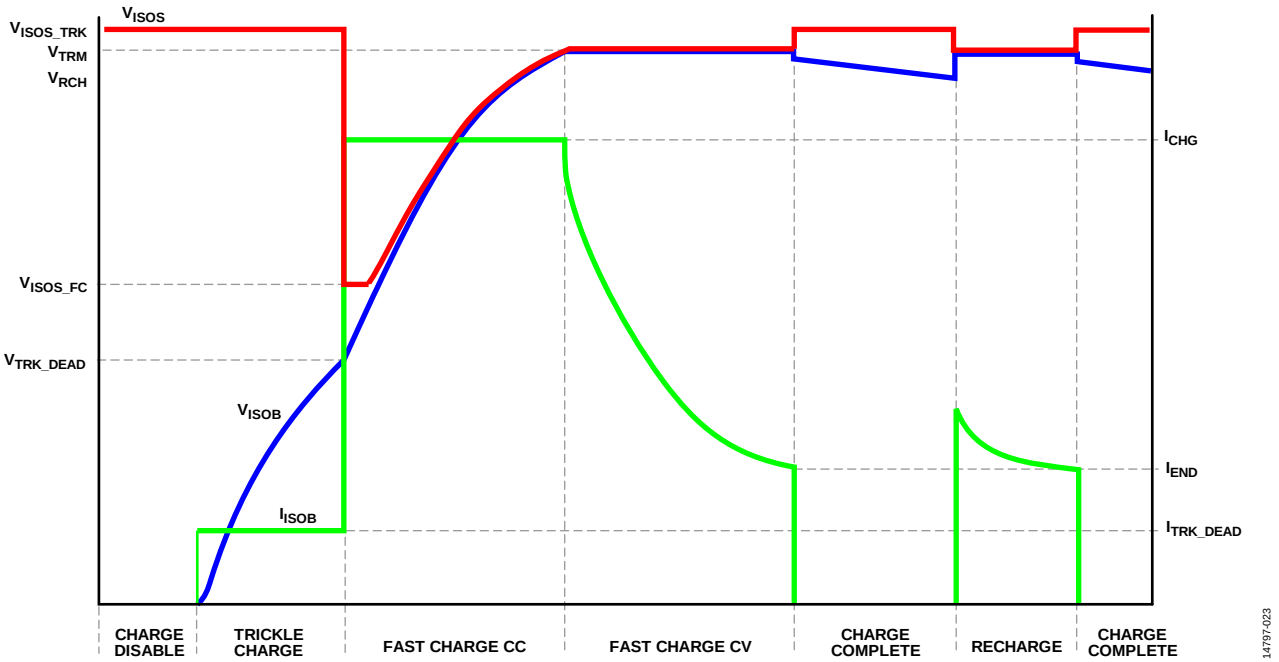



*Figure 40. ADP5350 Battery Charging Profile*

## CHARGER MODES

### Input Current Limit

The ADP5350 features a programmable input current limit, from 100 mA to 1500 mA, via the ILIM[3:0] I²C bits, which ensures compatibility with the USB limits requirements listed in Table 11. The current limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured. This input current limit resets to the 100 mA default value during every power cycle on VBUSx to protect the USB port.

When the input current limit feature is used, the available input current may be too low for the charger to meet the programmed charging current, $I_{CHG}$, and the rate of charge is reduced. In this case, the VBUS_ILIM flag is set.

When connecting an improper voltage level to VBUSx, the dc-to-dc regulator shuts down, the ISOFET turns on, and the high voltage blocking part is in a state wherein it draws only 1.3 mA (typical) of current until $V_{VBUSx}$ reaches the $V_{VBUS\_OV\_FALL}$ level.

The ADP5350 always monitors the $V_{VBUSx}$ voltage when there is a proper USB power connection. The VBUSOK bit, Bit 3 in Register 0x36, indicates whether the $V_{VBUSx}$ voltage is within $V_{VBUS\_OV}$ and $V_{VBUSOK}$, which can be programmed to be masked to the PGOOD pin via the VBUSOK_MASK bit in Register 0x37.

The default setting of the VBUSOK_MASK is programmed via a factory fuse trim.

### Trickle Charge Mode

A deeply discharged Li-Ion cell may exhibit a very low cell voltage, making it unsafe to charge the cell at high current rates. The ADP5350 charger uses a trickle charge mode to reset the battery pack protection circuit and lift the cell voltage to a safe level for fast charging. A cell with a voltage below $V_{TRK\_DEAD}$ is charged with the trickle mode current, $I_{TRK\_DEAD}$. During trickle charge mode, the CHARGER_STATUS[3:0] bits are set.

During trickle charging, the ISOS node is regulated to $V_{ISOS\_TRK}$ by the dc-to-dc regulator and the battery isolation FET is off, which means the battery is isolated from the system power supply.

The enable of the trickle charging function is controlled via the I²C EN_TRK bit.

### Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure the battery is revived from its deeply discharged state. If trickle charge mode runs for longer than 60 minutes without the cell voltage reaching $V_{TRK\_DEAD}$, a fault condition is assumed and the charging stops. The battery isolation FET turns on and the dc-to-dc regulator stops working. The fault condition is asserted in the CHARGER_STATUS register, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

### Weak Charge Mode (Constant Current)

When the battery voltage exceeds $V_{TRK\_DEAD}$ but is less than $V_{WEAK}$, the charger switches to weak charge mode and the ISOS node is regulated to $V_{ISOS\_FC}$ by turning on the battery isolation FET.

In weak charge mode, the battery charges with the programmed $I_{CHG}$ current from the ISOS node through the isolation FET and trickle charge current, $I_{TRK\_DEAD}$. Due to the VBUSx input current limit, the real $I_{CHG}$ charge current from the ISOS node may be less than the programmed value. The system load can also share the current from the ISOS node. However, the trickle charge current, $I_{TRK\_DEAD}$, remains on to charge the battery in weak charge mode.

### Fast Charge Mode (Constant Current)

When the battery voltage exceeds $V_{TRK\_DEAD}$ and $V_{WEAK}$, the charger switches to fast charge mode, charging the battery with the constant current, $I_{CHG}$. During fast charge mode (CC), the CHARGER_STATUS[3:0] bits are set.

During CC mode, other features may prevent the current, $I_{CHG}$, from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility may affect the value of $I_{CHG}$ under certain operating conditions. The voltage on ISOS is regulated to stay at $V_{ISOS\_FC}$ by the battery isolation FET when $V_{ISOB} < V_{ISOS\_FC}$.

### Fast Charge Mode (Constant Voltage)

As the battery charges, its voltage rises and approaches the termination voltage, $V_{TRM}$. The ADP5350 charger monitors the voltage on the BSNS pin to determine when charging ends. However, the internal ESR of the battery pack combined with PCB and other parasitic series resistances creates a voltage drop between the sense point at the BSNS pin and the cell terminal itself. To compensate for this and ensure a fully charged cell, the ADP5350 enters a constant voltage charge mode when the BSNS voltage reaches the termination voltage. The ADP5350 reduces charge current gradually as the cell continues to charge, maintaining a voltage of $V_{TRM}$ on the BSNS pin. During fast charge mode (constant voltage), the CHARGER_STATUS[3:0] bits are set.

### Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than $t_{CHG}$ without the voltage at the BSNS pin reaching $V_{TRM}$, a fault condition is assumed and charging stops. The battery isolation FET remains on, and the dc-to-dc regulator shuts down. The fault condition is asserted on the CHARGER_STATUS register, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

If the fast charge mode runs for longer than $t_{CHG}$, and $V_{TRM}$ is reached on the BSNS pin but the charge current is not yet below $I_{END}$, charging stops by turning the battery isolation FET off, but the system voltage is maintained at $V_{ISOS\_TRK}$ by the dc-to-dc regulator. No fault condition is asserted in this circumstance, and the ADP5350 transitions to charge complete status.

**Table 11. Input Current Compatibility with Standard USB Limits**

| Mode | Standard USB Limit | ADP5350 Function |
|---|---|---|
| USB 2.0 | 100 mA limit for standard USB host or hub<br>500 mA limit for standard USB host or hub | 100 mA input current limit or I²C programmed value<br>500 mA input current limit or I²C programmed value |
| USB 3.0 | 150 mA limit for super speed USB 3.0 host or hub<br>900 mA limit for super speed, high speed USB host or hub charger | 150 mA input current limit or I²C programmed value<br>900 mA input current limit or I²C programmed value |
| Dedicated Charger | 1500 mA limit for dedicated charger or low/full speed USB host or hub charger | 1500 mA input current limit or I²C programmed value |

### *Watchdog Timer*

The ADP5350 charger features a programmable watchdog timer function to ensure charging is under the control of the processor. The watchdog timer starts running when the ADP5350 charger determines that the processor is operational, that is, when the processor sets the RESET_WD bit for the first time or when the battery voltage is greater than the weak battery threshold, $V_{WEAK}$. When the watchdog timer triggers, it must be reset regularly within the watchdog timer period, $t_{WD}$.

If the watchdog timer expires without being reset while in charger mode, the ADP5350 charger assumes there is a software problem and triggers the safety timer, $t_{SAFE}$. For more information, see the Safety Timer section. Meanwhile, the $I_{LIM}$ current limit resets to the default value.

### *Safety Timer*

If the watchdog timer (see the Watchdog Timer section for more information) expires while in charger mode, the ADP5350 charger initiates the safety timer, $t_{SAFE}$. Charging continues for a period of $t_{SAFE}$, and then stops. The battery isolation FET remains on while the dc-to-dc regulator shuts down. The CHARGER_STATUS[3:0] bits are then set. Resetting the charger requires VBUSx to be powered down and powered up.

### *Charge Complete*

The ADP5350 charger monitors the charging current while in CV fast charge mode. If the current falls below $I_{END}$ and remains below $I_{END}$ for $t_{END}$, the charger is stopped by turning the battery isolation FET off, but the system voltage is maintained at $V_{ISOS\_TRK}$ by the dc-to-dc regulator and the CHDONE flag is set. If the charging current falls below $I_{END}$ for less than $t_{END}$ and then rises above $I_{END}$ again, the $t_{END}$ timer resets.

### *Recharge*

After the detection of a complete charge, and the isolated FET turns off, the ADP5350 charger continues to monitor the BSNS pin. If the BSNS pin voltage falls below $V_{TRM} - V_{RCH}$, the charger reactivates charging. Under most circumstances, triggering the recharge threshold results in the charger entering fast charge constant current mode.

### *Battery Charging Enable/Disable*

The ADP5350 charging function can be disabled by setting the I²C EN_CHG bit to low. If the I²C EN_CHG bit is low, the dc-to-dc regulator is still on and regulates the ISOS voltage to $V_{ISOS\_TRK}$, the battery isolation FET turns off, and the dc-to-dc regulator provides the power for the system.

## BATTERY ISOLATION FET

The ADP5350 charger features an integrated battery isolation FET for power path control. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in trickle charge mode and when charging is complete, thereby allowing the system to be powered from the VBUSx node.

When the $V_{VBUSx}$ voltage is below $V_{VBUSOK\_FALL}$, the battery isolation FET is in full conduction mode.

The battery isolation FET is off during trickle charge mode. When the battery voltage exceeds $V_{TRK\_DEAD}$, the battery isolation FET switches to the system voltage regulation mode and the battery isolation FET maintains the $V_{ISOS\_FC}$ voltage on the ISOS pin. When the battery voltage exceeds $V_{ISOS\_FC}$, the battery isolation FET is in full conduction mode.

The battery isolation FET supplements the battery to support high current functions on the system power supply.

When the voltage on ISOS drops below ISOB, the battery isolation FET enters full conduction mode.

When the voltage on ISOS rises above ISOB, the isolation FET enters regulating mode or full conduction mode, depending on the Li-Ion cell voltage and the dc-to-dc charger mode.

## BATTERY DETECTION

### *Battery Level Detection*

The ADP5350 charger features a battery detection mechanism to detect an absent battery. The charger actively sinks and sources current into the ISOB/BSNS node when the enable charger and $V_{VBUSx}$ have reached the $V_{VBUSOK\_RISE}$ level, and voltage vs. time is detected. The sink phase is used to detect a charged battery, whereas the source phase is used to detect a discharged battery.

The sink phase (see Figure 41) sinks $I_{SINK}$ current from the ISOB and BSNS pin for a time, $t_{BATOK}$. If the BSNS pin is below $V_{BATL}$ when the $t_{BATOK}$ timer expires, the charger assumes no battery is present or battery is shorted, and starts the source phase. If the BSNS exceeds the $V_{BATL}$ voltage when the $t_{BATOK}$ timer expires, the charger assumes the battery is present and begins a new charge cycle.

The source phase sources $I_{SOURCE}$ current to ISOB or the BSNS pin for a time, $t_{BATOK}$. If the BSNS pin exceeds $V_{BATH}$ before the

$t_{BATOK}$ timer expires, the charger assumes that no battery is present. If the BSNS does not exceed the $V_{BATH}$ voltage when the $t_{BATOK}$ timer expires, the charger assumes that a battery is present, and begins a new charge cycle.

When the ADP5350 battery monitor is enabled and detects that the battery voltage is higher than $V_{WEAK}$, Bit 2 in Register 0x36, BATOK, asserts high. The PGOOD pin can be programmed to mask BATOK, which indicates whether the battery voltage is higher than $V_{WEAK}$.

### *Battery (ISOB) Short Detection*

A battery short occurs under a damaged battery condition or when the battery protection circuitry is enabled.

After a source phase, if the voltage on ISOB or BSNS remains below $V_{BATH}$, either the battery voltage is low or the battery node is shorted. When the battery voltage is low, trickle charge mode is initiated (see Figure 42). If the voltage on BSNS remains below $V_{BAT\_SHR}$ after $t_{BAT\_SHR}$ has elapsed, the ADP5350 assumes that the battery node is shorted. A fault is declared on Register 0x0A, Bit 3.

The trickle charge branch is active during the battery short scenario, and trickle charge current to the battery is maintained until the 60 minutes of the trickle charge mode timer expires.

## BATTERY TEMPERATURE

### *Battery Pack Thermistor Input*

The ADP5350 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside the specified range. The THR pin provides an on and off switching current source, which must be connected directly to the battery pack thermistor, $R_{NTC}$. The activation interval of the THR current source is 167 ms.

The battery pack temperature sensing can be controlled by I²C using the conditions shown in Table 12. Note that the I²C register default setting for EN_THR (Register 0x07) is 0 = temperature sensing off.

**Table 12. THR Input Function**

| Conditions | | |
|---|---|---|
| **VBUSx** | **$V_{ISOB}$** | **THR Function** |
| Open or $V_{BUS}$ = 0 V to 4.0 V | <2.5 V | Off |
| Open or $V_{BUS}$ = 0 V to 4.0 V | >2.5 V | Controlled by I²C |
| $V_{BUS}$ = 4.0 V to 5.5 V | Don't care | Always on |

If the battery pack thermistor is not connected directly to the ADP5350 THR pin, connect a 47 kΩ (tolerance ±20%) dummy resistor between THR and AGND. Leaving the THR pin open results in a false detection of the battery temperature of <0°C and charging being disabled. Alternatively, select the temperature source from the I²C interface by setting Register 0x20, Bit 6.

The ADP5350 charger suspends charging if the battery temperature is outside the range of less than 0°C or greater than 60°C. For temperatures greater than 0°C, and likewise for temperatures lower than 60°C, the THR_STATUS[2:0] bits are set accordingly. The ISOFET remains on while the dc-to-dc regulator shuts down.

The ADP5350 charger is designed for use with a negative temperature coefficient (NTC) thermistor in the battery pack with a nominal resistance value of 47 kΩ, 10 kΩ, or 100 kΩ at 25°C, which is selected via the I²C interface in Register 0x0C, Bit 4, and Register 0x3D, Bit 0. The temperature coefficient curve (beta) of $R_{NTC}$ also can be fuse selected in the ADP5350.

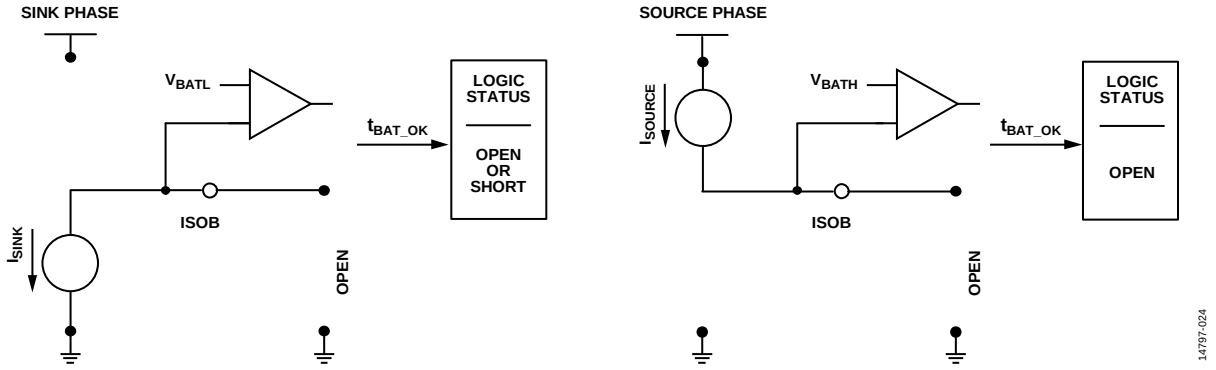



*Figure 41. Battery Detection Sequence*

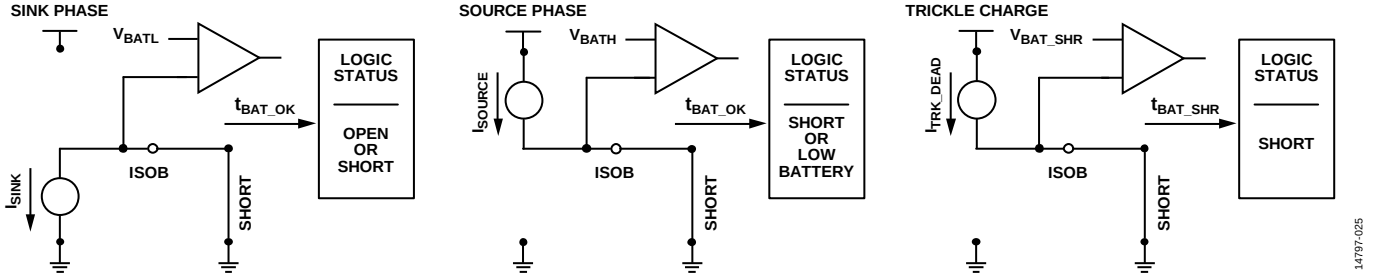



*Figure 42. Battery Short Detection Sequence*

### *Battery Temperature from I²C*

If a microcontroller has another accuracy temperature sense in system, it can select the temperature source via the I²C setting and write the temperature value to the BAT_TEMP[5:0] bits. The I²C source battery temperature range is between −2°C and +61°C.

### *JEITA Li-Ion Battery Temperature Charging Specification*

The charge of the ADP5350 is compliant with the JEITA Li-Ion battery charging temperature specifications, as shown in Table 14.

The JEITA function is enabled via the I²C interface. When the ADP5350 detects a JEITA cool condition, charging current is reduced according to Table 13.

When the ADP5350 identifies a hot or cold battery condition, the battery isolation FET turns on and the dc-to-dc regulator shuts down. In this condition, the battery provides the $V_{ISOS}$ supply.

**Table 13. JEITA Cool Temperature Limit—Reduced Charge Current Levels**

| | $I_{CHG}$ JEITA (mA) | |
|---|---|---|
| ICHG[3:0] | ILIM_JEITA_COOL = 0 | ILIM_JEITA_COOL = 1 |
| 0000 = 25 mA | 25 | 25 |
| 0001 = 50 mA | 25 | 25 |
| 0010 = 75 mA | 25 | 25 |
| 0011 = 100 mA | 50 | 25 |
| 0100 = 125 mA | 50 | 25 |
| 0101 = 150 mA | 75 | 25 |
| 0110 = 200 mA | 100 | 25 |
| 0111 = 250 mA | 125 | 25 |
| 1000 = 300 mA | 150 | 50 |
| 1001 = 350 mA | 175 | 50 |
| 1010 = 400 mA | 200 | 50 |
| 1011 = 450 mA | 225 | 50 |
| 1100 = 500 mA | 250 | 50 |
| 1101 = 550 mA | 275 | 50 |
| 1110 = 600 mA | 300 | 50 |
| 1111 = 650 mA | 325 | 50 |

**Table 14. JEITA Default Li-Ion Battery Charging Specifications**

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| JEITA Cold Temperature Limits | $T_{JEITA\_COLD}$ | No battery charging occurs. | | 0 | °C |
| JEITA Cool Temperature Limits | $T_{JEITA\_COOL}$ | Battery charging occurs at approximately 50% or 10% of programmed level. See Table 13 for specific charging current reduction levels. | 0 | 10 | °C |
| JEITA Typical Temperature Limits | $T_{JEITA\_TYP}$ | Normal battery charging occurs at default/programmed levels. | 10 | 45 | °C |
| JEITA Warm Temperature Limits | $T_{JEITA\_WARM}$ | Battery termination voltage ($V_{TRM}$) is reduced by 100 mV from the programmed value. | 45 | 60 | °C |
| JEITA Hot Temperature Limits | $T_{JEITA\_HOT}$ | No battery charging occurs. | 60 | | °C |

## BATTERY CHARGER OPERATIONAL FLOWCHART

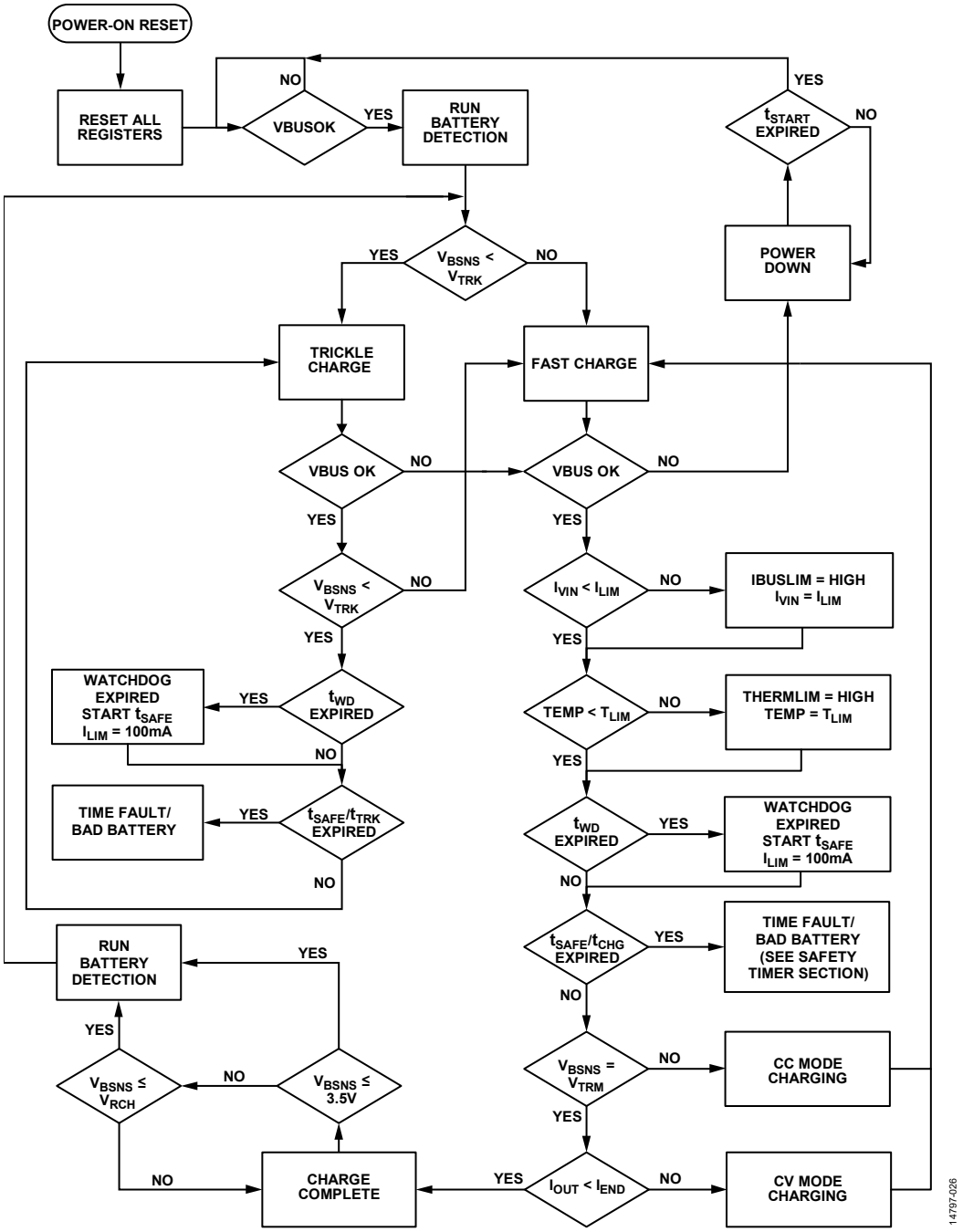



*Figure 43. ADP5350 Charger Operational Flowchart*

## BATTERY VOLTAGE-BASED FUEL GAUGE

### *Overview*

The ADP5350 Li-Ion battery fuel gauge is based on the voltage measurement with a 12-bit ADC. SOC is calculated with a battery model integrated in the ADP5350. Ten voltage values based on the battery characterization and the battery internal resistance at different temperatures must be written to the V_SOC_x register and RBAT_x register of the ADP5350 for SOC calculation.

### *Operation Mode*

The ADP5350 fuel gauge, in shut down mode by default, provides extremely low standby current consumption from the battery. After the fuel gauge function is enabled, two operation modes can be selected: active mode and sleep mode. The fuel gauge operation mode is controlled by the $I^2C$.

In active mode, the battery SOC is updated every 1 sec by the sensed battery voltage, which achieves better accuracy and indicates the remaining battery capacity but consumes 160 µA

(typical) of operation current. In sleep mode, the battery SOC is updated every 5 min and the battery instant current ($I_{INS}$) is updated every 37.5 sec, which reduces the current to typically 4 µA (see Table 15). The ADP5350 automatically switches from sleep mode to active mode when the current through the isolation FET is higher than typically 35 mA. The system current must be less than 35 mA when switching to sleep mode. Depending on the system load, the mode can be switched to active mode to achieve better SOC accuracy.

**Table 15. Fuel Gauge Operation Mode**

| Operation Mode | Current (Typical) | ADC Sample Rate | SOC Update Rate |
|---|---|---|---|
| Shutdown | 0.2 µA | None | None |
| Sleep | 4 µA | 37.5 sec | 5 min |
| Active | 160 µA | 0.125 sec | 1 sec |

### *Battery Voltage Compensation*

The battery internal resistance impacts the accuracy of a traditional voltage-based SOC. A higher load current translates to a higher voltage drop ($\Delta V_{DROP}$) over the internal resistance, $R_{BAT}$ (see Figure 44).

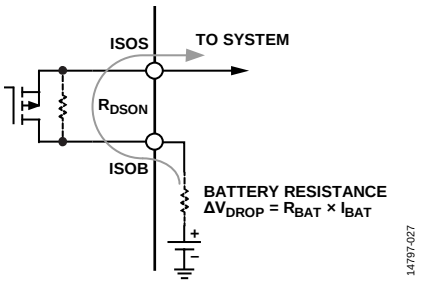



*Figure 44. Discharge Current Sensing Through Battery Isolation FET*

The ADP5350 uses the battery isolation FET for battery discharge current sensing. The device senses the ISOS and ISOB node voltages to obtain the delta voltage. Divide the delta voltage by $R_{DSON}$ to achieve the discharge current, which can be used for SOC calculation compensation.

The voltage reading from the BSNS pin is compensated using the following equation and can be read in the VBAT_READ_H and VBAT_READ_L registers.

$$V_{BAT} = V_{BSNS} + R_{BAT} \times I_{BAT}$$

where:
$V_{BSNS}$ is the voltage on the BSNS pin.
$R_{BAT}$ is the internal resistance of the battery.
$I_{BAT}$ is the current through the battery.

When the battery is charging, $I_{BAT}$ is the charging current.

During the battery discharges, $I_{BAT}$ is calculated by the voltage sense on the isolated FET.

The internal resistance of the battery has strong temperature dependency. Figure 45 shows the internal resistance temperature coefficient using a 280 mAh, 3.7 V Li-Ion cell battery.

The ADP5350 contains I²C registers to calculate the $R_{BAT}$ value, where the user can program the battery internal resistance characterized from the battery at certain temperatures. The ADP5350 uses this data to calculate the battery internal resistance at different temperatures.

It is strongly recommended to use the I²C bits, BAT_TEMP, to obtain an accurate battery temperature if the system has such temperature sense information. If using the ADP5350 internal sense circuitry as the temperature source, only four temperature levels for battery resistance compensation are available, which may cause errors in the SOC calculation relating to the battery resistance temperature coefficient.

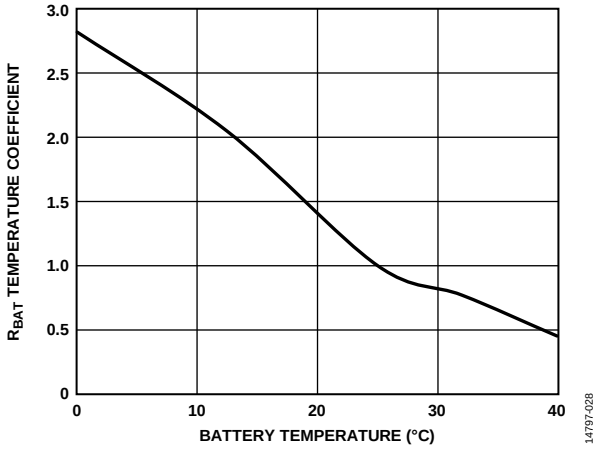



*Figure 45. $R_{BAT}$ Temperature Coefficient vs. Battery Temperature, Temperature Coefficient of the Li-Ion Battery, Relative to Battery $R_{BAT}$ at 25°C*

In addition, the internal resistance of the battery has a remaining capacity dependency, especially when the SOC is less than 20%. The ADP5350 allows the user to program different internal resistance coefficients when the SOC is in the 20% to 0% range during a discharge by programming the corresponding bits, K_RBAT_SOC (see Figure 46).

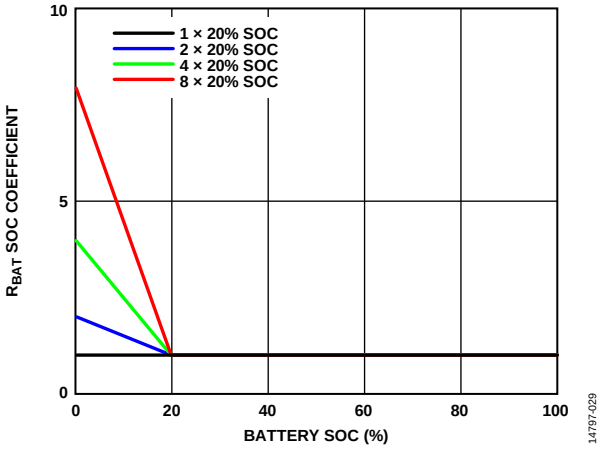



*Figure 46. $R_{BAT}$ SOC Coefficient vs. Battery SOC, SOC Coefficient of the Li-Ion Battery, Relative to Battery $R_{BAT}$ at 25°C*

For some batteries, the internal resistance is different when the battery is in charge vs. discharge mode. Use the K_RBAT_CHARGE bits to program the battery internal resistance coefficient when charging.

### State of Charge Limit Filter

To avoid impacting SOC accuracy caused by the effects of a battery discharge and the instantaneous interference on the battery current sense, the ADP5350 uses filter limitation for delta SOC calculation of each step. The filter limitation can be selected from a 0.125 C rate to a 3 C rate via I²C programming, which is equal to or greater than real system current consumption (the C rate is the battery charge or discharge current rate over the battery capacity). For example, when the full system load is 60 mA with 300 mAh, and the discharge current rate is 0.2 C, the filter limitation can be programmed to 0.25 C using the FILTER_DISCHARGE bits.

When the fuel gauge is enabled, the SOC value is reset based on the current battery voltage and internal resister compensation, without any initial filter effects. Repeatedly disabling and enabling the fuel gauge or setting Register 0x25, Bit 7 to reset the SOC value during a battery discharge increases errors in SOC calculation. It is recommended that the SOC be reset only when there is no discharge current and the battery voltage is in a completely relaxed state; that is, the battery voltage is stable.

During sleep mode, the filter limitation is reduced because the ADP5350 outputs a low discharge current.

## FLOWCHART OF SOC CALCULATION

See Figure 47 for a flowchart of the SOC calculation. Down_Lim is the delta SOC in each step when the SOC reduces. Up_Lim is the delta SOC in each step when the SOC increases.

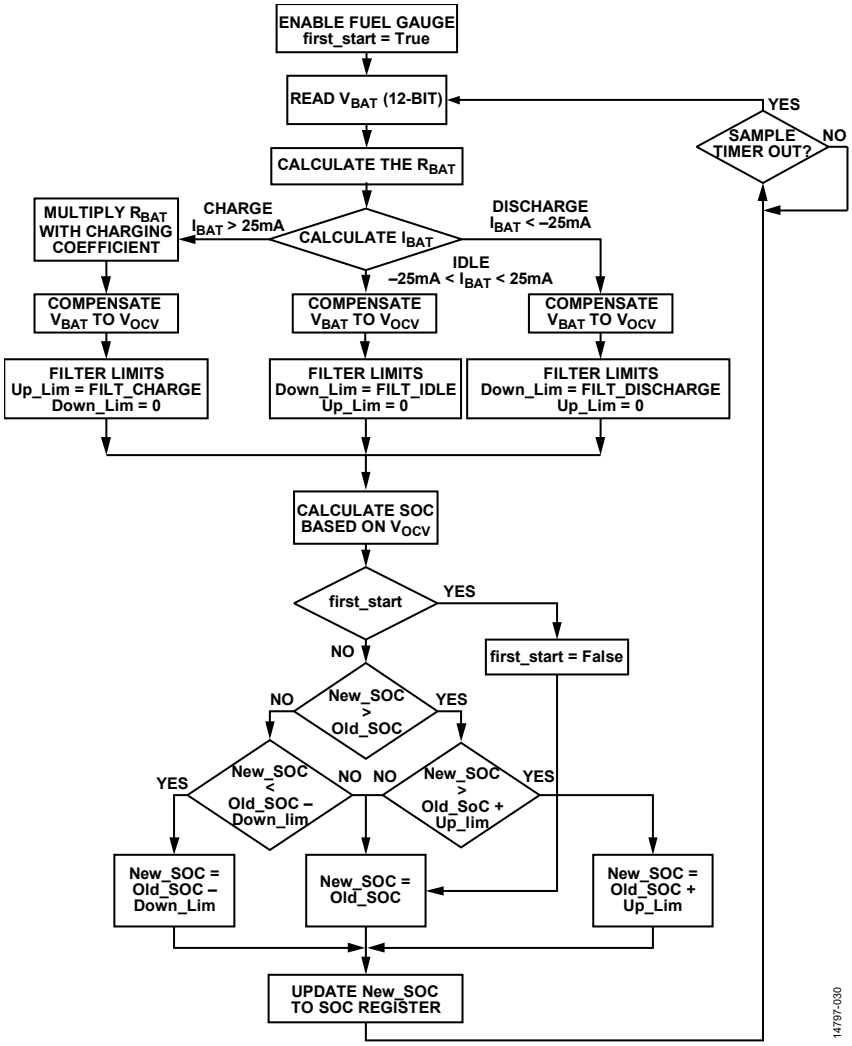



*Figure 47. ADP5350 SOC Calculation Flowchart*

## BOOST AND WHITE LED DRIVERS

The ADP5350 integrates a powerful 1.5 MHz frequency boost regulator with programmable LED control. Different LED configurations, like LEDs in parallel or LEDs in serial, are supported with careful design. Up to five LED strings are independently programmable up to 20 mA (typical) in 64 levels. All LED strings can be individually programmed or combined into a group to operate as the backlight LEDs or individual LED current sinks.

A full suite of safety features, including current-limit, overvoltage, LED open-circuit, and overtemperature protection, allows a robust and safe design. The integrated soft start limits inrush currents during start-up and restart attempts.

### *White LED Driver*

White LEDs are common in backlighting the displays of modern portable devices. White LEDs require a high forward voltage, $V_F$ (typically 3.3 V), before conducting current and emitting light. Display panels, depending on the size, can be backlit with multiple white LEDs in series or in parallel. The LEDs need a common current passing through all of them to achieve uniform brightness. The LED, however, must be biased with a voltage greater than the sum of each LED $V_F$ voltage before it can conduct.

The ADP5350 integrates a 1.5 MHz boost regulator to power the LED bias voltage. If the LED forward voltage plus the current sink headroom voltage is higher than the battery voltage, the boost regulator turns on. If the battery voltage is higher than the sum of the LED forward voltage plus the required current sink headroom voltage, the boost regulator operates in passthrough mode.

The ADP5350 uses an integrated negative channel field effect transistor (NFET) low-side current regulator for accurate brightness control, with up to five channels of current sink.

The ADP5350 supports setting different LED currents for each LED string. Any mismatch in the forward voltage of the LEDs translates directly to lower efficiency, as well as lower accuracy of the current for the lower voltage LED string.

The boost regulator in the ADP5350 has two operation modes, LED operation mode and boost standalone operation mode, which can be selected via the I²C-compatible interface.

### *LED Operation Mode*

When the boost regulator is required to provide a higher output voltage to the LED bias voltage, the boost regulator must be configured in LED operation mode by setting BST_MODE = 0 in the BST_CFG register.

In LED operation mode, the boost regulator provides the adaptive LED bias voltage with adaptive headroom regulation to optimize the system efficiency against LED forward voltage variation and aging. The boost regulator is attached to the LED current source control and, therefore, is automatically activated by any active LED current source. The EN_BST bit is not effective in this mode.

Because the LED bias voltage may be coming from the battery system voltage instead of the boost output voltage (for example, LED indicators with relatively low forward voltage), those LEDs can be used in individual current sink channels by using the battery system voltage as the LED bias voltage. Use the BST_BL bit in the BST_CFG register to determine whether the bias voltage for individual current sink channels is coming from the boost regulator output or from the battery system voltage.

Write 0 to BST_BL to set the boost regulator to provide the bias voltage for all active LED channels. In this configuration, the boost regulator provides the adaptive headroom regulation according to all active LED current sources, including both backlight and individual current sinks.

Write 1 to BST_BL to set the boost regulator to provide the bias voltage only for the active LED backlight channels, excluding individual current sink. The bias voltage for an individual LED sink can be from the battery system voltage or from some other fixed rail; therefore, the headroom status in individual LED sinks does not affect the boost output regulation. BST_BL must be set to 1 when the indicator LED is connected to the battery system voltage instead of the boost output voltage; otherwise, the boost voltage may risk an overvoltage. The adaptive headroom control in the boost regulator may include individual LED channels whose bias voltage is not coming from the boost regulator.

The boost feedback pin (FB4 pin) is tied to ground in LED operation mode.

### *Boost Standalone Operation Mode*

When the boost regulator is used to provide the fixed output voltage for other system uses, including organic light emitting diode (OLED) backlight, audio system, or other auxiliary circuitries, the boost regulator must be configured in standalone operation mode by setting BST_MODE = 1 in the BST_CFG register. It is recommended that total output power be limited below 800 mW when the boost peak current is set to 600 mA.

In standalone operation mode, the boost regulator provides the adjustable output voltage, $V_{OUT4}$, configured by the external resistor divider.

$$V_{OUT4} = V_{FB4} \times (R_{FB1} + R_{FB2})/R_{FB2}$$

The activation status of the boost regulator is determined by the EN_BST bit in the BST_CFG register. In boost standalone operation mode, all LED functions are turned off and not allowed.

In standalone operation mode, the boost feedback pin (FB4 pin) must be tied to the boost output through an external resistor divider.

Figure 48 shows the typical boost regulator diagram in standalone operation. Table 16 summarizes the difference between LED operation mode and standalone operation mode. Table 16 provides four programmable OVP thresholds according to the boost output voltage. The various OVP thresholds provide different internal compensation depending on the boost output voltage. It strongly recommended to select the proper OVP level related to the set output voltage.

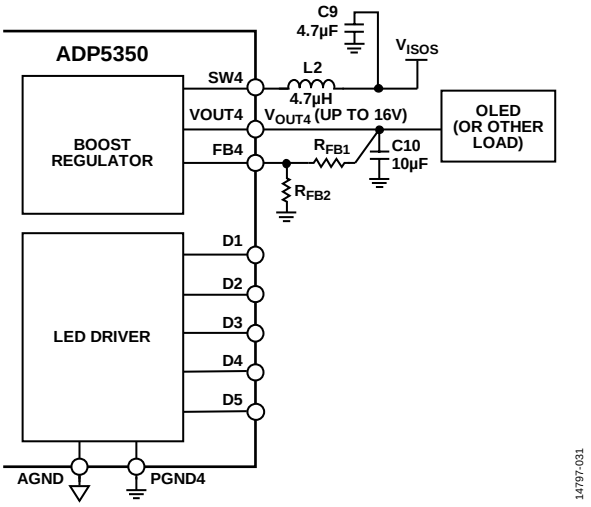



*Figure 48. Boost Regulator in Standalone Operation Mode*

**Table 16. Two Operation Modes for the Boost Regulator**

| Operation | LED Operation Mode | Standalone Operation Mode |
|---|---|---|
| Activation Control | Activated by active LED EN_LEDx | Activated by EN_BST |
| Output Regulation | Adaptive to LED $V_F$ voltage variation | Fixed and determined by external resistor divider |
| FB4 Pin | Tied to ground | Tied to boost output via resistor divider |
| OVP | 5.6 V, 10 V, 15 V, or 18.5 V threshold on the VOUT4 pin | 5.6 V, 10 V, 15 V, or 18.5 V threshold on the VOUT4 pin |

### PGOOD Indicator of Boost Output

In boost standalone mode, the PGOOD pin can be programmed to indicate whether the boost PGOOD signal is output to the external PGOOD pin by setting the PG4_BST_MASK bit high in Register 0x37. The ADP5350 monitors the FB4 pin voltage, and asserts the PGOOD signal high when the FB4 pin voltage reaches up to 90% of the typical voltage with a typical 2 ms deglitch time. The PGOOD signal asserts low when the FB4 pin voltage drops to 86.5% of the typical voltage.

The boost output PGOOD status can be read via the $I^2C$ interface, Register 0x36, Bit 1.

### Soft Start

The boost regulator in the ADP5350 includes soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current of the battery. The soft start time is typically fixed at 1 ms for the boost regulator.

### Backlight Current Settings

The backlight current setting is determined by a 6-bit code programmed by the user via the IBL_SET[5:0] bits. This 6-bit code allows the user to set the backlight to one of 64 levels between 0 mA and 20 mA.

The ADP5350 uses a square law algorithm for the 64 levels, where the backlight current increases linearly for a corresponding increase of input code. The backlight current, in milliamperes (mA), is determined by the following equations:

$$Backlight\ Current\ (mA) = \left( Code \times \frac{\sqrt{Full\text{–}Scale\ Current}}{63} \right)^2$$

where:
*Code* is the input code programmed by the user.
*Full-Scale Current* is the maximum sink current allowed (typically, 20 mA).

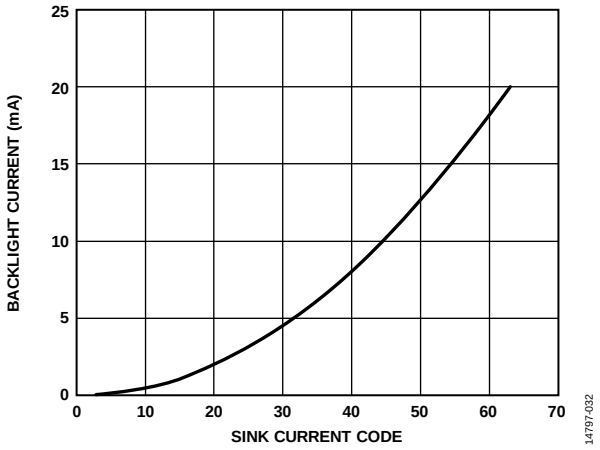



*Figure 49. Backlight Current vs. Sink Current Code*

### Backlight Linear Fade In and Fade Out

When the ADP5350 operates in normal operation, the backlight can be turned on using the EN_BL bit. The backlight turns on when EN_BL = 1, and turns off when EN_BL = 0.

To prevent abrupt turn on and turn off of the backlight, the ADP5350 contains timers to facilitate smooth fading between the turn on and turn off states. Fading is implemented using the square law backlight code algorithm.

The BL_FI timer and BL_FO timer in the BL_FR register can be used for smooth fade in transitions from a low to high backlight setting. The BL_FI timer and BL_FO timer can be programmed to one of 15 settings ranging from 0.3 sec to 4.5 sec. The timer must be programmed before asserting EN_BL.

The time programmed in the BL_FI timer and BL_FO timer represents the time it takes the backlight current to go from 0 mA to 20 mA. Therefore, the fading time between intermediate settings is shorter. Smaller changes in current reduces the fade time. For square law fades, the fade time is given by

$$Fade\ Time = Fade\ Rate \times (Code/63)$$

where the *Fade Rate* is as shown in Table 17.

**Table 17. Available Fade In and Fade Out Times**

| Code | Fade Rate (sec) |
|---|---|
| 0000 | Fade in or fade out disabled |
| 0001 | 0.3 |
| 0010 | 0.6 |
| 0101 | 0.9 |
| 0110 | 1.2 |
| 0111 | 2.1 |
| 1000 | 2.4 |
| 1001 | 2.7 |
| 1010 | 3.0 |
| 1011 | 3.3 |
| 1100 | 3.6 |
| 1101 | 3.9 |
| 1110 | 4.2 |
| 1111 | 4.5 |

### Backlight Fade Override

A fade override feature allows the BL_FI and BL_FO timers to be overridden when the EN_BL bit is reasserted during a fade in or fade out period and to set the backlight to its targeted current setting value immediately (see Figure 50). Setting the FOVR bit to 1 in the BST_CFG register enables the backlight fade override feature.

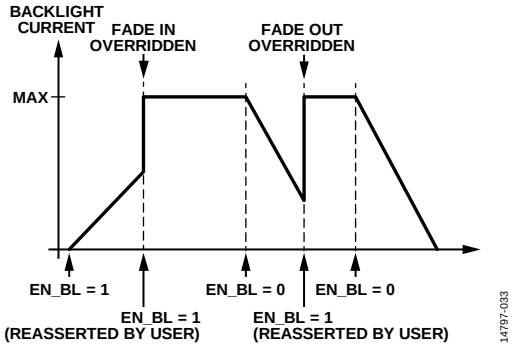



*Figure 50. LED Backlight Fade Override*

### Independent Sink Controls

The LED current sink in Channel 2 to Channel 5 can be configured to operate as either part of a grouped backlight, or to operate as an independent LED channel.

Setting BL_LEDx = 1 configures the selected LED channel (Channel 2 to Channel 5) as the part of a grouped backlight. In this setting, the backlight current setting and on/off control in Channel 1 apply to the configured channel.

Setting BL_LEDx = 0 configures the selected LED channel (Channel 2 to Channel 5) as an independent current sink channel. Each channel current and on/off control are determined by independent register settings.

### Individual LED Blinking Timer

The independent current sinks in Channel 3, Channel 4, and Channel 5 have additional timers to facilitate the blinking functions. The on timer and the off timer in the LEDx_BLINK register allow individual LED current sinks to be configured in various blinking modes. Blink mode can be activated by setting the off timers to any setting other than disabled. The blink mode setting has no effect if the channel is configured as part of a grouped backlight.

The fade in and fade out function is effective in blink mode but the fade override feature is not effective in blink mode. See Figure 51 for a timing diagram of LED blinking with fading.

Some applications (for example, red/green/blue (RGB) LEDs in blink mode) need the blinking timer to be in synchronization. If the blinking LEDs are enabled in the same $I^2C$ command, the rising time of the on timer for each blinking LED is synchronized.

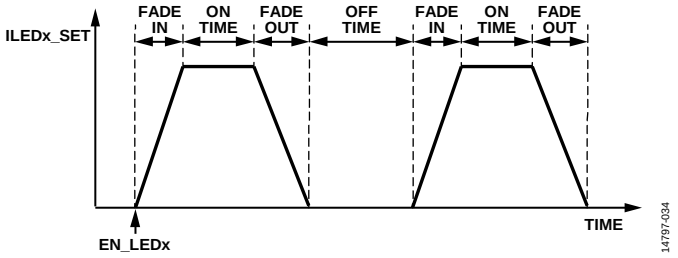



*Figure 51. LED Blinking with Fading*

### *LEDs in Parallel*

Different configurations, for example, LEDs in series or LEDs in parallel, can be supported by ADP5350.

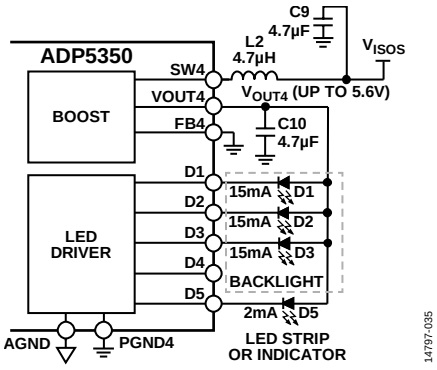



*Figure 52. Thee LEDs in Parallel for Grouped Backlight and One LED Strip or Indicator*

Figure 52 shows three LEDs in parallel (15 mA each), in grouped backlight configuration, connected to D1, D2, and D3, and one additional LED indicator (2 mA) connected to D5.

1. Configure the boost regulator as follows:
   a. Set BST_MODE = 0 to configure the boost regulator in LED operation mode.
   b. Set BST_BL = 0 to configure the boost regulator to provide the bias voltage to all current sink channels.
   c. Set BST_OVP = 1 to configure the boost OVP threshold = 5.6 V.
2. Configure the grouped backlight as follows:
   a. Set BL_LED2 = 1 and BL_LED3 = 1 to configure D1 to D3 as the grouped backlight.
   b. Set IBL[5:0] = 15 mA for the LED grouped backlight current.
   c. Set the BL_FI and BL_FO code for the fade in and fade out timer (if required).
   d. Set FOVR = 1 to enable the fading overwritten feature (if required).
3. Configure the individual current sink as follows:
   a. Set ILED5 = 2 mA for the D5 sink current.
   b. Set the LED5_ON and LED5_OFF code for the blinking timer (if required).
4. Set EN_BL = 1 to enable the LED backlight.
5. Set EN_LED5 = 1 to enable the LED indicator.

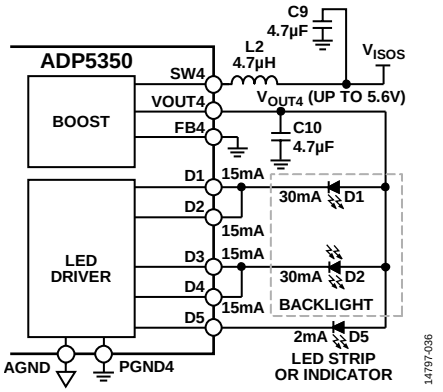



*Figure 53. Two LEDs in Parallel (30 mA each) for Grouped Backlight and One LED Strip or Indicator (2 mA)*

Figure 53 shows two LEDs in parallel (30 mA each), in grouped backlight configuration, connected from D1 to D4, and one additional LED indicator (2 mA) connected to D5.

1. Configure the boost regulator as follows:
   a. Set BST_MODE = 0 to configure the boost regulator in LED operation mode.
   b. Set BST_BL = 0 to configure the boost regulator to provide the bias voltage to all current sink channels.
   c. Set BST_OVP = 1 to configure the boost OVP threshold = 5.6 V. Set EN_BL bit = 1 to enable the LED backlight.
2. Configure the grouped backlight as follows:
   a. Set BL_LED2 = 1, BL_LED3 = 1, and BL_LED4 = 1 to configure D1 to D4 as the grouped backlight.
   b. Set IBL[5:0] = 15 mA for the LED grouped backlight current (two channels in parallel with 30 mA for each LED current).
   c. Set the BL_FI and BL_FO code for the fade in and fade out timer (if required).
   d. Set FOVR = 1 to enable the fading overwritten feature (if required).
3. Configure the individual current sink as follows:
   a. Set ILED5 = 2 mA for the D5 sink current.
   b. Set the LED5_ON and LED5_OFF code for the blinking timer (if required).
4. Set EN_BL = 1 to enable the LED backlight.
5. Set EN_LED5 = 1 to enable the LED indicator.

### LED in Series

The ADP5350 supports connecting LEDs in series (see Figure 54 for an example).

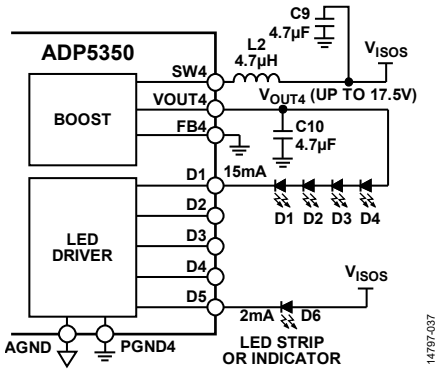



*Figure 54. Four LEDs in Series (15 mA Each) for Grouped Backlight Connected to D1, and One LED Strip or Indicator (2 mA) in D5 with Connection to $V_{ISOS}$ Rail*

Figure 54 shows four LEDs in series (15 mA each), in grouped backlight configuration, connected to D1, and one additional LED indicator (2 mA) connected to D5 and the $V_{ISOS}$ rail.

1. Configure the boost regulator as follows:
   a. Set BST_MODE = 0 to configure the boost in LED operation mode.
   b. Set BST_BL = 1 to configure the boost to provide the bias voltage to the LED backlight only.
   c. Set BST_OVP = 0 to configure the boost OVP threshold = 18.5 V.
2. Configure the grouped backlight as follows:
   a. Set IBL[5:0] = 15 mA for the LED backlight current.
   b. Set the BL_FI and BL_FO code for the fade in and fade out timer (if required).
   c. Set FOVR = 1 to enable the fading overwritten feature (if required).
3. Configure the individual current sink as follows:
   a. Set ILED5 = 2 mA for D5 sink current.
   b. Set the LED5_ON and LED5_OFF code for the blinking timer (if required).
4. Set EN_BL = 1 to enable the LED backlight.
5. Set EN_LED5 = 1 to enable the LED indicator.

### Boost Switching Frequency

The boost regulator of the ADP5350 operates in 1.5 MHz fixed switching frequency and it is synchronized with the switching frequency in battery charger.

### Boost Current Limit

The boost regulator in the ADP5350 includes the peak current-limit protection circuitry to limit the amount of positive current flowing through the battery to the output. Two current-limit thresholds (600 mA or 300 mA) can be selected using the BST_IPK bit. The programmable current-limit threshold feature allows the use of a small size inductor for low power applications.

As the battery discharges, the lower battery voltage results in higher peak current through the battery ESR, which may cause early shutdown of other devices on the battery. The programmable current threshold can be used to change the current limit according to different battery voltages.

### Overvoltage Fault

The boost regulator contains OVP circuits to prevent damage if the $V_{OUT4}$ voltage becomes excessive for any reason. To keep a safe output level, the integrated OVP circuit monitors the $V_{OUT4}$ voltage. When the $V_{OUT4}$ voltage exceeds the OVP rising threshold, the boost regulator stops switching, causing the output voltage to drop. When the $V_{OUT4}$ voltage goes lower than the OVP falling threshold, the boot regulator begins switching, causing the output to rise. The overvoltage threshold is programmable (default of 18.5 V) in the BST_OVP register.

The overvoltage threshold level must be programmed according to the output voltage because the various OVP thresholds provide different internal compensation depending on the boost output voltage.

### LED Open-Circuit Protection

The LED circuit contains a headroom control circuit to minimize power loss at each current source. Therefore, the minimum feedback voltage is achieved by regulating the output voltage of the boost regulator. If any LED string is opened during normal operation, the current source headroom voltage is pulled to AGND. In this condition, LED open-circuit protection activates when the voltage on the Dx pin is less than 200 mV and the $V_{OUT4}$ voltage rises to the OVP level. If LED open-circuit protection is triggered, the open LED channel turns off while the other LED channel continues to work, and the LEDx_OPEN bit is set to 1 in the LED_STATUS register. The open LED channel remains disabled to ensure protection against a potential LED open circuit, until the processor clears the fault register by rewriting a 1 to the fault bit or the ADP5350 is power cycled.

When one channel is selected for independent LED operation and the bias voltage is separate from the LED backlight group (BST_BL = 1), the LED open-circuit protection has no effect on this channel due to the boost OVP never being detected on this channel.

## LINEAR LOW DROPOUT (LDO) REGULATORS

The ADP5350 integrates three LDO regulators. LDO1 is a low quiescent current LDO that can be used as a supply that is always on for the system. LDO2 and LDO3 are general-purpose LDO regulators.

All LDO input power rails are supplied from the VIN123 pin and share the input power of the control circuits with the VIN4 pin. Thus, the VIN123 pin must be tied to the VIN4 pin in all applications.

The LDO regulator operates with an input voltage range of 2.7 V to 5.5 V. The wide supply range makes the regulator suitable for cascading configurations where the LDO supply

voltage is provided from the system voltage. The LDO output voltage is set by the factory fuse or I²C.

The LDO regulator provides a high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with small 1 µF ceramic input and output capacitors.

The LDO1, LDO2, and LDO3 fixed output voltages are set by the factory fuse and include the following options: 1.0 V, 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, 1.8 V, 2.1 V, 2.3 V, 2.5 V, 2.85 V, 3.0 V, 3.15 V, 3.3 V, 3.6 V, and 4.2 V.

### *Load Switch Mode*

All LDO regulators can be configured as a load switch via the I²C. The load switch allows power domain isolation and helps to extend the battery life.

### *LDO Output Discharge*

Each LDO has an output discharge feature that can be selected by the I²C. When the output discharge feature is enabled, the selected LDO output connects the internal 500 Ω load to ground and pulls down the output voltage quickly when the LDO channel is disabled.

### *PGOOD Indicator of LDO1 Output*

The ADP5350 PGOOD pin can mask various power-good channels, including LDO1, the boost regulator, and $V_{VBUSx}$ by setting Register 0x37, Bit 0.

When the PGOOD pin masks the LDO1 power-good output and enables LDO1, the PGOOD pin indicates the LDO1 output voltage power-good signal, and asserts high when the VOUT1 pin voltage reaches up to 90% of the typical voltage with a typical 2 ms deglitch time. The PGOOD signal asserts low when the VOUT1 pin voltage drops to 86.5% of the typical voltage.

The default setting of the PG1_LDO1_MASK is a factory fuse trim that is programmable. The LDO1 power-good status can be read via the I²C interface, using Register 0x36, Bit 0.

## THERMAL MANAGEMENT

### *Isothermal Charging and Thermal Early Warning*

To assist with the thermal management of the ADP5350 charger, the battery charger provides an isothermal charging function. As the on-chip power dissipation and die temperature increase, the ADP5350 charger monitors the die temperature and limits the output current when the temperature reaches $T_{SD\_W}$. The die temperature is maintained at $T_{SD\_W}$ through the control of the charging current into the battery. A reduction in power dissipation or ambient temperature may allow the charging current to return to its original value, and the die temperature subsequently drops below $T_{SD\_W}$. During isothermal charging, the THERM_LIM flag is set to high.

The early warning bit is set if $T_{SD\_W}$ is exceeded. This warning bit allows the system to accommodate power consumption before thermal shutdown occurs.

### *Thermal Shutdown*

The ADP5350 switching charger features a thermal shutdown threshold detector. If the die temperature exceeds $T_{SD}$, the ADP5350 charger is disabled, and the TSD_140 bit is set. The ADP5350 charger can be reenabled when the die temperature drops below the $T_{SD}$ falling limit and the TSD_140 bit is reset. To reset the TSD_140 bit, write to the I²C Fault Register 0x0A or cycle the power.

### *Fault Recovery*

Before performing the following operation, it is important to ensure that the cause of the fault is rectified.

To reset the fault bits in the CHARGER_FAULT register, cycle the power on VBUSx or write the corresponding I²C bit high.

# I²C INTERFACE

The ADP5350 includes an I²C-compatible serial interface to control the battery charging, fuel gauge, boost regulator, and LED driver, and to read back the system status.

## I²C ADDRESSES

The I²C address can be factory programmable. The I²C address options help to avoid conflicts with other I²C slave chipsets in the system. For alternative I²C chip address requirements, contact a local Analog Devices sales or distribution representative.

## SDA AND SCL PINS

The ADP5350 has two dedicated I²C interface pins, SDA and SCL. SDA is an open-drain line for receiving and transmitting data. SCL is an input line for receiving the clock signal. Pull up these pins to an external input/output supply using external resistors.

Serial data is transferred on the rising edge of SCL. The read data is generated at the SDA pin in read mode.

The subaddress content selects the ADP5350 registers to be written to first. The ADP5350 sends an acknowledgement to the master after the 8-bit data byte is written (see Figure 55 for an example of the I²C write sequence to a single register). The ADP5350 increments the subaddress automatically and starts receiving a data byte at the next register until the master sends an I²C stop as shown in Figure 56.

Figure 57 shows the I²C read sequence of a single register. The ADP5350 sends the data from the register denoted by the subaddress and increments the subaddress automatically, sending data from the next register until the master sends an I²C stop condition as shown in Figure 58.

## DEFAULT RESET

The ADP5350 contains one write only register, DEFAULT_SET, to reset all registers to the factory default values.

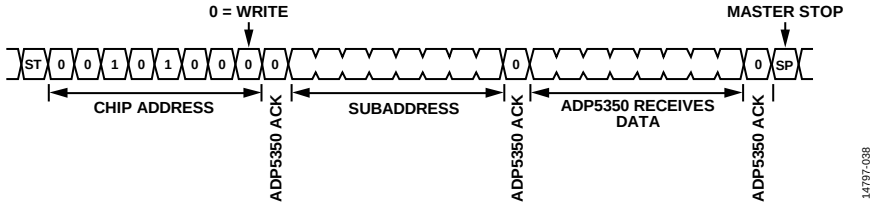



*Figure 55. I²C Single Register Write Sequence*

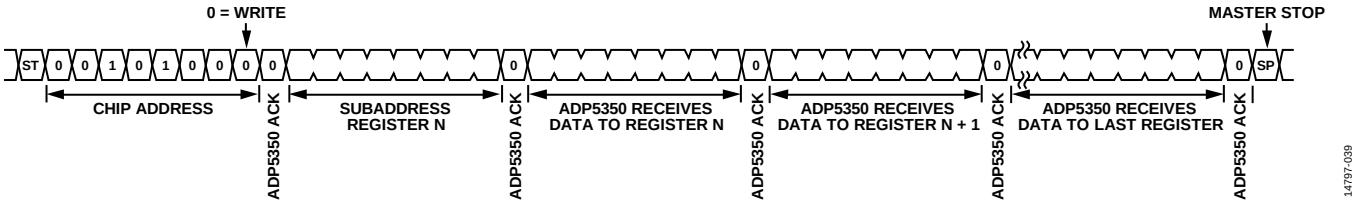



*Figure 56. I²C Multiple Register Write Sequence*

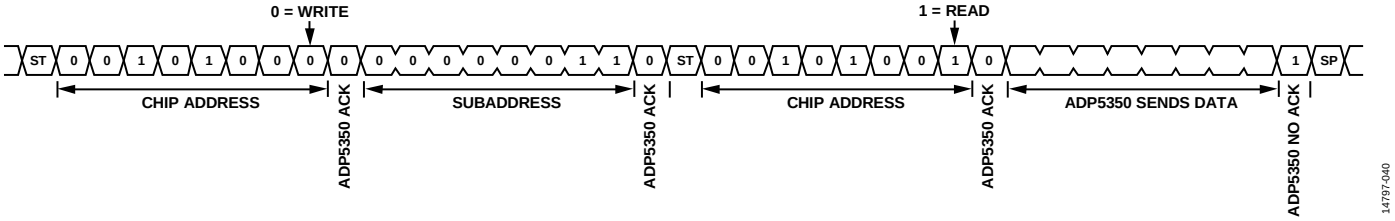



*Figure 57. I²C Single Register Read Sequence*

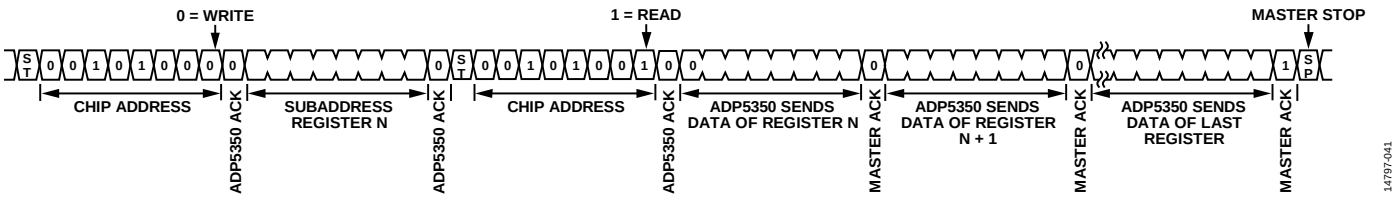



*Figure 58. I²C Multiple Register Read Sequence*

## INTERRUPTS

The ADP5350 provides an interrupt output (the $\overline{INT}$ pin) for fault conditions. During normal operation, when the $\overline{INT}$ pin is pulled high, use an external pull-up resistor. When a fault condition occurs, the ADP5350 pulls the $\overline{INT}$ pin low to alert the $I^2C$ host that a fault condition occurred.

Many different interrupt sources can trigger the $\overline{INT}$ pin. By default, no interrupt sources are configured. To select one or more interrupt sources to trigger the $\overline{INT}$ pin, set the appropriate bits to 1 in the CHARGER_INTERRUPT_ENABLE register and the BOOST_LDO_INTERRUPT_ENABLE register.

When the $\overline{INT}$ pin is triggered, one or more bits in the CHARGER_INTERRUPT_FLAG register and the BOOST_LDO_INTERRUPT_FLAG register are set to 1. The fault condition that triggered the $\overline{INT}$ pin can be read from the CHARGER_INTERRUPT_FLAG register and the BOOST_LDO_INTERRUPT_FLAG register.

To clear an interrupt, read the appropriate bit in the CHARGER_INTERRUPT_FLAG register and the BOOST_LDO_INTERRUPT_FLAG register, or power cycle the ADP5350.

# CONTROL REGISTER MAP

**Table 18. Register Map**

| Address (Hex) | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Manufacture and model ID | MANUF[3:0] | | | | Model[3:0] | | | |
| 0x01 | Silicon revision | Not used | | | | REV[3:0] | | | |
| 0x02 | CHARGER_ VBUS_ILIM | Not used | | | | ILIM[3:0] | | | |
| 0x03 | CHARGER_ TERMINATION_ SETTING | VTRM[5:0] | | | | | | IEND[1:0] | |
| 0x04 | CHARGER_ CURRENT_ SETTING | C_20_EOC | C_10_EOC | ICHG[3:0] | | | | ITRK_DEAD[1:0] | |
| 0x05 | CHARGER_ VOLTAGE_ THRESHOLD | Not used | VRCH[1:0] | | VTRK_DEAD[1:0] | | VWEAK[2:0] | | |
| 0x06 | CHARGER_ TIMER_SETTING | Not used | EN_TEND | EN_CHG_ TIMER | CHG_TMR_PERIOD | | EN_WD | WD_PERIOD | RESET_WD |
| 0x07 | CHARGER_ FUNCTION_ SETTING1 | EN_JEITA | DIS_IPK_SD | EN_BMON | EN_THR | EN_DCDC | EN_EOC | EN_TRK | EN_CHG |
| 0x08 | CHARGER_ STATUS1 | VBUS_OV | Not used | VBUS_ILIM | THERM_ LIM | CHDONE | CHARGER_STATUS[2:0] | | |
| 0x09 | CHARGER_ STATUS2 | THR_STATUS[2:0] | | | IPK_STAT | Not used | BATTERY_STATUS[2:0] | | |
| 0x0A | CHARGER_ FAULT | Not used | | | | BAT_SHR | IND_PEAK | TSD_130 | TSD_140 |
| 0x0B | BATTERY_ SHORT | TBAT_SHR[2:0] | | | Not used | | VBAT_SHR[2:0] | | |
| 0x0C | BATTERY_ THERMISTOR_ CONTROL | ILIM_JEITA_ COOL | TBAT_LOW | TBAT_ HIGH | R_NTC | BETA_NTC[3:0] | | | |
| 0x0D | V_SOC_0 | V_SOC_0[7:0] | | | | | | | |
| 0x0E | V_SOC_5 | V_SOC_5[7:0] | | | | | | | |
| 0x0F | V_SOC_11 | V_SOC_11[7:0] | | | | | | | |
| 0x10 | V_SOC_19 | V_SOC_19[7:0] | | | | | | | |
| 0x11 | V_SOC_28 | V_SOC_28[7:0] | | | | | | | |
| 0x12 | V_SOC_41 | V_SOC_41[7:0] | | | | | | | |
| 0x13 | V_SOC_55 | V_SOC_55[7:0] | | | | | | | |
| 0x14 | V_SOC_69 | V_SOC_69[7:0] | | | | | | | |
| 0x15 | V_SOC_84 | V_SOC_84[7:0] | | | | | | | |
| 0x16 | V_SOC_100 | V_SOC_100[7:0] | | | | | | | |
| 0x17 | FILTER_ SETTING1 | Not used | FILTER_CHARGE[2:0] | | | Not used | FILTER_DISCHARGE[2:0] | | |
| 0x18 | FILTER_ SETTING2 | Not used | | | | | | FILT_IDLE[1:0] | |
| 0x19 | RBAT_0 | RBAT_0[7:0] | | | | | | | |
| 0x1A | RBAT_10 | RBAT_10[7:0] | | | | | | | |
| 0x1B | RBAT_20 | RBAT_20[7:0] | | | | | | | |
| 0x1C | RBAT_30 | RBAT_30[7:0] | | | | | | | |
| 0x1D | RBAT_40 | RBAT_40[7:0] | | | | | | | |
| 0x1E | RBAT_60 | RBAT_60[7:0] | | | | | | | |
| 0x1F | K_RBAT_CHARGE | Not used | | K_RBAT_SOC[1:0] | | K_RBAT_CHARGE[3:0] | | | |
| 0x20 | BAT_TEMP | Not used | BAT_TEMP_ SOURCE | BAT_TEMP[5:0] | | | | | |
| 0x21 | BAT_SOC | Not used | BAT_SOC[6:0] | | | | | | |
| 0x22 | VBAT_READ_H | VBAT_READ[12:5] | | | | | | | |
| 0x23 | VBAT_READ_L | VBAT_READ[4:0] | | | | | Not used | | |

| Address (Hex) | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x24 | FUEL_GAUGE_ MODE | Not used | | | | | SLEEP_ UPDATE_ TIME | FUEL_GAUGE_ MODE | FUEL_ GAUGE_ ENABLE |
| 0x25 | SOC_RESET | SOC reset | Not used | | | | | | |
| 0x26 | BST_LED_CTRL | Not used | | EN_BST | EN_LED5 | EN_LED4 | EN_LED3 | EN_LED2 | EN_BL |
| 0x27 | BST_CFG | BST_MODE | BST_BL | FOVR | Not used | BST_OVP | | Not used | BST_IPK |
| 0x28 | IBL_SET | Not used | IBL[5:0] | | | | | | |
| 0x29 | ILED2_SET | BL_LED2 | Not used | ILED2[5:0] | | | | | |
| 0x2A | ILED3_SET | BL_LED3 | Not used | ILED3[5:0] | | | | | |
| 0x2B | ILED4_SET | BL_LED4 | Not used | ILED4[5:0] | | | | | |
| 0x02C | ILED5_SET | BL_LED5 | Not used | ILED5[5:0] | | | | | |
| 0x2D | BL_FR | BL_FO[3:0] | | | | BL_FI[3:0] | | | |
| 0x2E | LED3_BLINK | LED3_OFF[3:0] | | | | LED3_ON[3:0] | | | |
| 0x2F | LED4_BLINK | LED4_OFF[3:0] | | | | LED4_ON[3:0] | | | |
| 0x30 | LED5_BLINK | LED5_OFF[3:0] | | | | LED5_ON[3:0] | | | |
| 0x31 | LED_STATUS | Not used | | | LED5_ OPEN | LED4_ OPEN | LED3_OPEN | LED2_OPEN | LED1_OPEN |
| 0x32 | LDO_CTRL | Not used | | | | | EN_LDO3 | EN_LDO2 | EN_LDO1 |
| 0x33 | LDO_CFG | Not used | DSCG_LDO3 | DSCG_ LDO2 | DSCG_ LDO1 | Not used | MODE_LDO3 | MODE_LDO2 | MODE_LDO1 |
| 0x34 | VID_LDO12 | VID_LDO2[3:0] | | | | VID_LDO1[3:0] | | | |
| 0x35 | VID_LDO3 | Not used | | | | VID_LDO3[3:0] | | | |
| 0x36 | PGOOD_STATUS | Not used | | | | VBUSOK | BATOK | PG4_BST | PG1_LDO1 |
| 0x37 | PGOOD_MASK | Not used | | | | VBUSOK_ MASK | BATOK_ MASK | PG4_BST_MASK | PG1_LDO1_ MASK |
| 0x38 | CHARGER_ INTERRUPT_ ENABLE | EN_IND_ PEAK_INT | EN_THERM_ LIM_INT | EN_WD_ INT | EN_TSD_ INT | EN_THR_ INT | EN_BAT_INT | EN_CHG_INT | EN_VIN_INT |
| 0x39 | CHARGER_ INTERRUPT_ FLAG | IND_PEAK_ INT | THERM_ LIM_INT | WD_INT | TSD_INT | THR_INT | BAT_INT | CHG_INT | VIN_INT |
| 0x3A | BOOST_LDO_ INTERRUPT_ ENABLE | Not used | | | | | EN_LED_ OPEN_INT | EN_PG4_BST_ INT | EN_PG1_ LDO1_INT |
| 0x3B | BOOST_LDO_ INTERRUPT_ FLAG | Not used | | | | | LED_OPEN_ INT | PG4_BST_INT | PG1_ LDO1_INT |
| 0x3C | DEFAULT_SET | DEFAULT_SET | | | | | | | |
| 0x3D | NTC47K_SET | Not used | | | | | | | NTC_47K |

## REGISTER BIT DESCRIPTIONS

**Table 19. Manufacturer and Model ID, Register Address 0x00 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | MANUF[3:0] | R | 0001 | The 4-bit manufacturer identification bus. |
| [3:0] | Model[3:0] | R | 1011 | The 4-bit model identification bus. |

**Table 20. Silicon Revision, Register Address 0x01 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | Not used | R | | |
| [3:0] | REV[3:0] | R | 0011 | The 4-bit silicon revision identification bus. |

**Table 21. CHARGER_VBUS_ILIM, Register Address 0x02 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | Not used | R | | Not used. |
| [3:0] | ILIM[3:0] | R/W | 0000 | VBUSx pin input current-limit programming bus. The current into VBUSx can be limited to the following programmed values:<br>0000 = 100 mA.<br>0001 = 150 mA.<br>0010 = 200 mA.<br>0011 = 300 mA.<br>0100 = 400 mA.<br>0101 = 500 mA.<br>0110 = 600 mA.<br>0111 = 700 mA.<br>1000 = 800 mA.<br>1001 = 900 mA.<br>1010 = 1000 mA.<br>1011 = 1100 mA.<br>1100 = 1200 mA.<br>1101 = 1300 mA.<br>1110 = 1400 mA.<br>1111 = 1500 mA. |

**Table 22. CHARGER_TERMINATION_SETTINGS, Register Address 0x03 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:2] | VTRM[5:0] | R/W | 100011 | Termination voltage programming bus. The values of the float voltage can be programmed to the following values:<br>000000 = 3.50 V.<br>000001 = 3.52 V.<br>000010 = 3.54 V.<br>000011 = 3.56 V.<br>000100 = 3.58 V.<br>000101 = 3.60 V.<br>000110 = 3.62 V.<br>000111 = 3.64 V.<br>001000 = 3.66 V.<br>001001 = 3.68 V.<br>001010 = 3.70 V.<br>001011 = 3.72 V.<br>001100 = 3.74 V.<br>001101 = 3.76 V.<br>001110 = 3.78 V.<br>001111 = 3.80 V.<br>010000 = 3.82 V. |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| | | | | 010001 = 3.84 V.<br>010010 = 3.86 V.<br>010011 = 3.88 V.<br>010100 = 3.90 V.<br>010101 = 3.92 V.<br>010110 = 3.94 V.<br>010111 = 3.96 V.<br>011000 = 3.98 V.<br>011001 = 4.00 V.<br>011010 = 4.02 V.<br>011011 = 4.04 V.<br>011100 = 4.06 V.<br>011101 = 4.08 V.<br>011110 = 4.10 V.<br>011111 = 4.12 V.<br>100000 = 4.14 V.<br>100001 = 4.16 V.<br>100010 = 4.18 V.<br>100011 = 4.20 V.<br>100100 = 4.22 V.<br>100101 = 4.24 V.<br>100110 = 4.26 V.<br>100111 = 4.28 V.<br>101000 = 4.30 V.<br>101001 = 4.32 V.<br>101010 = 4.34 V.<br>101011 = 4.36 V.<br>101100 = 4.38 V.<br>101101 = 4.40 V.<br>101110 = 4.42 V.<br>101111 = 4.44 V.<br>110000 = 4.46 V.<br>110001 = 4.48 V.<br>110010 to 111111 = 4.5 V. |
| [1:0] | IEND[1:0] | R/W | 01 | Termination current programming bus. The values of the termination current can be programmed to the following values:<br>00 = 25 mA.<br>01 = 35 mA.<br>10 = 45 mA.<br>11 = 55 mA. |

**Table 23. CHARGER_CURRENT_SETTING, Register Address 0x04 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | C_20_EOC | R/W | 0 | This bit has priority over the other settings (C_10_EOC and IEND).<br>When this bit is set to high, 1/20 C programming is used. The minimum value is 25 mA. |
| 6 | C_10_EOC | R/W | 0 | This bit has priority over the other setting (IEND) but not C_20_EOC.<br>When this bit is set to high, 1/10 C programming is used unless C_20_EOC is set to high. The minimum value is 25 mA. |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [5:2] | ICHG[3:0] | R/W | 1100 | Fast charge current programming bus. The values of the constant current charge can be programmed to the following values:<br>0000 = 25mA.<br>0001 = 50 mA.<br>0010 = 75 mA.<br>0011 = 100 mA.<br>0100 = 125 mA.<br>0101 = 150 mA.<br>0110 = 200 mA.<br>0111 = 250 mA.<br>1000 = 300 mA.<br>1001 = 350 mA.<br>1010 = 400 mA.<br>1011 = 450 mA.<br>1100 = 500 mA.<br>1101 = 550 mA.<br>1110 = 600 mA.<br>1111 = 650 mA. |
| [1:0] | ITRK_DEAD[1:0] | R/W | 10 | Trickle and weak charge current programming bus. The values of the trickle and weak charge currents can be programmed as per the following values:<br>00 = 5 mA.<br>01 = 10 mA.<br>10 = 20 mA.<br>11 = 50 mA. |

**Table 24. CHARGER_VOLTAGE_THRESHOLD, Register Address 0x05 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | Not used | R | | Not used. |
| [6:5] | VRCH[1:0] | R/W | 11 | Recharge voltage programming bus. The values of the recharge threshold can be programmed as per the following values:<br>00 = 80 mV.<br>01 = 140 mV.<br>10 = 200 mV.<br>11 = 260 mV. |
| [4:3] | VTRK_DEAD[1:0] | R/W | 01 | Trickle to fast charge dead battery voltage programming bus. The values of the trickle to fast charge threshold can be programmed to the following values:<br>00 = 2.4 V.<br>01 = 2.5 V.<br>10 = 2.6 V.<br>11 = 3.3 V. |
| [2:0] | VWEAK[2:0] | R/W | 011 | Weak battery voltage rising threshold. The values of the weak battery voltage rising threshold can be programmed to the following values:<br>000 = 2.7 V.<br>001 = 2.8 V.<br>010 = 2.9 V.<br>011 = 3.0 V.<br>100 = 3.1 V.<br>101 = 3.2 V.<br>110 = 3.3 V.<br>111 = 3.4 V. |

**Table 25. CHARGER_TIMER_SETTING, Register Address 0x06 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | Not used | R | | Not used. |
| 6 | EN_TEND | R/W | 1 | When low, this bit disables the charge complete timer ($t_{END}$), and a 31 ms deglitch timer remains on this function. |
| 5 | EN_CHG_TIMER | R/W | 1 | When high, the trickle/fast charge timer is enabled. |
| [4:3] | CHG_TMR_PERIOD | R/W | 11 | Trickle/fast charge timer period.<br>00 = 15 minutes/150 minutes.<br>01 = 30 minutes/300 minutes.<br>10 = 45 minutes/450 minutes.<br>11 = 60 minutes/600 minutes. |
| 2 | EN_WD | R/W | 0 | 0 = the watchdog timer is disabled even when $V_{BSNS}$ exceeds $V_{TRK\_DEAD}$.<br>1 = the watchdog timer safety timer is enabled. |
| 1 | WD_PERIOD | R/W | 0 | Watchdog safety timer period.<br>0 = 32 sec to 40 min.<br>1 = 64 sec to 40 min. |
| 0 | RESET_WD | W | 0 | When this bit is high, the watchdog safety timer resets. This bit is reset automatically. |

**Table 26. CHARGER_FUNCTION_SETTING1, Register Address 0x07 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | EN_JEITA | R/W | 0 | When low, this bit disables the JEITA Li-Ion temperature battery charging specification. |
| 6 | DIS_IPK_SD | R/W | 1 | When high, this bit disables the automatic shutdown of the device if four peak inductor current limits are reached in succession. In addition, when this bit is high, it only flags the IPK_STAT status bit. |
| 5 | EN_BMON | R/W | 0 | When this bit is high, the battery monitor is enabled even when the voltage at the VBUSx pins is below $V_{VBUSOK\_FALL}$. |
| 4 | EN_THR | R/W | 0 | When this bit is high, the THR current source is enabled even when the voltage at the VBUSx pins is below $V_{VBUSOK\_FALL}$. |
| 3 | EN_DCDC | R/W | 1 | When this bit is low, the dc-to-dc converter is disabled. When this bit is high, the dc-to-dc converter is enabled. |
| 2 | EN_EOC | R/W | 1 | When this bit is high, end of charge is allowed. |
| 1 | EN_TRK | R/W | 1 | When this bit is low, trickle charger is disabled and the dc-to-dc converter is enabled. |
| 0 | EN_CHG | R/W | Factory setting | When this bit is low, charging is disabled. When this bit is high and EN_DCDC = high, charging is enabled. |

**Table 27. CHARGER_STATUS1, Register Address 0x08 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | VBUS_OV | R | Not applicable | When high, this bit indicates that the voltage at the VBUSx pins exceeds $V_{VBUS\_OV}$. |
| 6 | Not used | R | | Not used. |
| 5 | VBUS_ILIM | R | Not applicable | When high, this bit indicates that the current into a VBUSx pin is limited by the high voltage blocking FET and the charger is not running at the full programmed $I_{CHG}$. |
| 4 | THERM_LIM | R | Not applicable | When high, this bit indicates that the charger is not running at the full programmed $I_{CHG}$ but is limited by the die temperature. |
| 3 | CHDONE | R | Not applicable | When high, this bit indicates the end of charge cycle is reached. This bit latches on, in that it does not reset to low when the $V_{RCH}$ threshold is breached. |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [2:0] | CHAGER_STATUS[2:0] | R | Not applicable | Charger status bus.<br>000 = off.<br>001 = trickle charge.<br>010 = fast charge (CC mode).<br>011 = fast charge (CV mode).<br>100 = charge complete.<br>101 = suspend.<br>110 = trickle, fast, or safety charge timer expired.<br>111 = battery detection. |

**Table 28. CHARGER_STATUS2, Register Address 0x09 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:5] | THR_STATUS[2:0] | R | Not applicable | THR pin status.<br>000 = off.<br>001 = battery cold.<br>010 = battery cool.<br>011 = battery warm.<br>100 = battery hot.<br>111 = thermistor is in normal operating temperature, between the battery cool and battery warm settings. |
| 4 | IPK_STAT | R | Not applicable | Peak current limit status bit. Set high if four or more peak inductor current limits are reached in succession. |
| 3 | Not used | R | | Not used. |
| [2:0] | BATTERY_STATUS[2:0] | R | Not applicable | Battery status bus.<br>000 = battery monitor off.<br>001 = no battery.<br>010 = $V_{BSNS} < V_{TRK}$.<br>011 = $V_{TRK} \leq V_{BSNS} < V_{WEAK}$.<br>100 = $V_{BSNS} \geq V_{WEAK}$. |

**Table 29. CHARGER_FAULT, Register Address 0x0A Bit Descriptions[1]**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | Not used | R | | Not used. |
| 3 | BAT_SHR | R/W | 0 | When this bit is high, a battery short circuit is detected. |
| 2 | IND_PEAK | R/W | 0 | When this bit is high, an inductor peak current-limit fault has occurred. |
| 1 | TSD_130 | R/W | 0 | When this bit is high, the overtemperature early warning has occurred. |
| 0 | TSD_140 | R/W | 0 | When this bit is high, the overtemperature condition is detected. The device shuts down due to an overtemperature condition. |

[1] To reset the fault bits in the CHARGER_FAULT register, cycle the power on VBUSx, or read and then write the corresponding $I^2C$ bit high continuously.

**Table 30. BATTERY_SHORT, Register Address 0x0B Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:5] | TBAT_SHR[2:0] | R/W | 100 | Battery short timeout timer:<br>000 = 1 sec<br>001 = 2 sec<br>010 = 4 sec<br>011 = 10 sec<br>100 = 30 sec<br>101 = 60 sec<br>110 = 120 sec<br>111 = 180 sec |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [4:3] | Not used | R | | Not used. |
| [2:0] | VBAT_SHR[2:0] | R/W | 100 | Battery short voltage threshold level:<br>000 = 2.0 V<br>001 = 2.1 V<br>010 = 2.2 V<br>011 = 2.3 V<br>100 = 2.4 V<br>101 = 2.5 V<br>110 = 2.6 V<br>111 = 2.7 V |

**Table 31. BATTERY_THERMISTOR_CONTROL, Register Address 0x0C Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | ILIM_JEITA_COOL | R/W | 0 | Selects the battery charging current when in the cool temperature range of 0°C and 10°C (see Table 14).<br>0 = approximately 50% of programmed charge current.<br>1 = approximately 10% of programmed charge current. |
| 6 | TBAT_LOW | R/W | 0 | Selects the battery temperature low threshold. When the battery temperature is lower than TBAT_LOW, charging stops.<br>0 = 0°C.<br>1 = 10°C. |
| 5 | TBAT_HIGH | R/W | 1 | Selects the battery temperature high threshold. When the battery temperature is higher than TBAT_HIGH, charging stops.<br>0 = 45°C.<br>1 = 60°C. |
| 4 | R_NTC | R/W | Factory setting | Selects the battery thermistor NTC resistance.<br>0 = 10 kΩ at 25°C.<br>1 = 100 kΩ or 47 kΩ at 25°C. |
| [3:0] | BETA_NTC[1] | R/W | Factory setting | 4-bit programming bus for NTC beta setting.<br>0000 = 2350.<br>0001 = 2600.<br>0010 = 2750.<br>0011 = 3000.<br>0100 = 3150.<br>0101 = 3350.<br>0110 = 3500.<br>0111 = 3600.<br>1000 = 3800.<br>1001 = 4000.<br>1010 = 4200.<br>1011 = 4400.<br>1100 = 4600.<br>1101 = 4800.<br>1110 = 5000.<br>1111 = 5200. |

[1] The BETA_NTC bits are trimmed by factory setting; writing these bits in the application is not recommended.

**Table 32. V_SOC_0, Register Address 0x0D Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_0 | R/W | 0x7C | The battery voltage when SOC is 0%. The default voltage is 3.5 V. Battery voltage (V) = (2.5 + V_SOC_0 × 0.008). |

**Table 33. V_SOC_5, Register Address 0x0E Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_5 | R/W | 0x91 | The battery voltage when SOC is 5%. The default voltage is 3.66 V. Battery voltage (V) = (2.5 + V_SOC_5 × 0.008). |

**Table 34. V_SOC_11, Register Address 0x0F Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_11 | R/W | 0x94 | The battery voltage when SOC is 11%. The default voltage is 3.684 V. Battery voltage (V) = (2.5 + V_SOC_11 × 0.008). |

**Table 35. V_SOC_19, Register Address 0x10 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_19 | R/W | 0x99 | The battery voltage when SOC is 19%. The default voltage is 3.724 V. Battery voltage (V) = (2.5 + V_SOC_19 × 0.008). |

**Table 36. V_SOC_28, Register Address 0x11 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_28 | R/W | 0x9E | The battery voltage when SOC is 28%. The default voltage is 3.764 V. Battery voltage (V) = (2.5 + V_SOC_28 × 0.008). |

**Table 37. V_SOC_41, Register Address 0x12 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_41 | R/W | 0xA3 | The battery voltage when SOC is 41%. The default voltage is 3.804 V. Battery voltage (V) = (2.5 + V_SOC_41 × 0.008) |

**Table 38. V_SOC_55, Register Address 0x13 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_55 | R/W | 0xAB | The battery voltage when SOC is 55%. The default voltage is 3.868 V. Battery voltage (V) = (2.5 + V_SOC_55 × 0.008). |

**Table 39. V_SOC_69, Register Address 0x14 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_69 | R/W | 0xB5 | The battery voltage when SOC is 69%. The default voltage is 3.948 V. Battery voltage (V) = (2.5 + V_SOC_69 × 0.008). |

**Table 40. V_SOC_84, Register Address 0x15 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_84 | R/W | 0xC4 | The battery voltage when SOC is 84%. The default voltage is 4.068 V. Battery voltage (V) = (2.5 + V_SOC_84 × 0.008) |

**Table 41. V_SOC_100, Register Address 0x16 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | V_SOC_100 | R/W | 0xD5 | The battery voltage when SOC is 100%. The default voltage is 4.204 V. Battery voltage (V) = (2.5 + V_SOC_100 × 0.008). |

**Table 42. FILTER_SETTING1, Register Address 0x17 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | Not used | R | | Not used. |
| [6:4] | FILTER_CHARGE | R/W | 100 | The filter limit (in C rate) of SOC in battery charging mode. The C rate is the battery charge or discharge current rate over the battery capacity.<br>000 = 0.125 C.<br>001 = 0.25 C.<br>010 = 0.5 C.<br>011 = 0.75 C.<br>100 = 1 C.<br>101 = 1.5 C.<br>110 = 2 C.<br>111 = 3 C. |
| 3 | Not used | R | | Not used. |
| [2:0] | FILTER_DISCHARGE | R/W | 010 | The filter limit (in C rate) of SOC in battery discharging mode. The C rate is the battery charge or discharge current rate over the battery capacity.<br>000 = 0.125 C.<br>001 = 0.25 C.<br>010 = 0.5 C.<br>011 = 0.75 C.<br>100 = 1 C.<br>101 = 1.5 C.<br>110 = 2 C.<br>111 = 3 C |

**Table 43. FILTER_SETTING2, Register Address 0x18 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:2] | Not used | R/W | 000000 | Not used. |
| [1:0] | FILTER_IDLE | R/W | 00 | The filter limit of SOC during battery idle mode.<br>00 = FILTER_CHARGE/8.<br>01 = FILTER_CHARGE/16.<br>10 = FILTER_CHARGE/32.<br>11 = FILTER_CHARGE/64. |

**Table 44. RBAT_0, Register Address 0x19 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | RBAT_0 | R/W | 0x3F | The battery internal resistance at 0°C. The resistance range is 0 mΩ to 8160 mΩ and the default resistance is 2016 mΩ. Resistance value = RBAT_0 × 32 mΩ. |

**Table 45. RBAT_10, Register Address 0x1A Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | RBAT_10 | R/W | 0x3F | The battery internal resistance at 10°C. The resistance range is 0 mΩ to 8160 mΩ and the default resistance is 2016 mΩ. Resistance value = RBAT_10 × 32 mΩ. |

**Table 46. RBAT_20, Register Address 0x1B Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | RBAT_20 | R/W | 0x3F | The battery internal resistance at 20°C. The resistance range is 0 mΩ to 8160 mΩ and the default resistance is 2016 mΩ. Resistance value = RBAT_20 × 32 mΩ. |

**Table 47. RBAT_30, Register Address 0x1C Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | RBAT_30 | R/W | 0x3F | The battery internal resistance at 30°C. The resistance range is 0 mΩ to 8160 mΩ and the default resistance is 2016 mΩ. Resistance value = RBAT_30 × 32 mΩ. |

**Table 48. RBAT_40, Register Address 0x1D Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | RBAT_40 | R/W | 0x3F | The battery internal resistance at 40°C. The resistance range is 0 mΩ to 8160 mΩ and the default resistance is 2016 mΩ. Resistance value = RBAT_40 × 32 mΩ. |

**Table 49. RBAT_60, Register Address 0x1E Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | RBAT_60 | R/W | 0x3F | The battery internal resistance at 60°C. The resistance range is 0 mΩ to 8160 mΩ and the default resistance is 2016 mΩ. Resistance value = RBAT_60 × 32 mΩ. |

**Table 50. K_RBAT_CHARGE, Register Address 0x1F Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:6] | Not used | R | | Not used. |
| [5:4] | K_RBAT_SOC | R/W | 00 | Battery internal resistance coefficient less than 20% capacity.<br>00 = RBAT at 0% SOC = $R_{BAT}$ at 20% SOC.<br>01 = $R_{BAT}$ at 0% SOC = 2 × $R_{BAT}$ at 20% SOC.<br>10 = $R_{BAT}$ at 0% SOC = 4 ×$R_{BAT}$ at 20% SOC.<br>11 = $R_{BAT}$ at 0% SOC = 8 × $R_{BAT}$ at 20% SOC. |
| [3:0] | K_RBAT_CHARGE | R/W | 1000 | Battery internal resistance coefficient for charging. The coefficient = 0.75 + K_RBAT_CHARGE/32. |

**Table 51. BAT_TEMP, Register Address 0x20 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | Not used | R | | Not used. |
| 6 | BAT_TEMP_SOURCE | R/W | 0 | Battery temperature source selection bit.<br>0: from THR input.<br>1: from $I^2C$. |
| [5:0] | BAT_TEMP | R/W | 11011 | Battery temperature from $I^2C$. The program battery temperature range is between −2°C and +61°C. Temperature value (°C) = (BAT_TEMP − 2). |

**Table 52. BAT_SOC, Register Address 0x21 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | Not used | R | | Not used. |
| [6:0] | BAT_SOC | R | Not applicable | Battery state of charge. SOC = BAT_SOC %, only valued between 0% and 100%. |

**Table 53. VBAT_READ_H, Register Address 0x22 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | VBAT_READ[12:5] | R | Not applicable | The battery voltage reading, highest eight bits, unit is mV. $V_{BAT}$ (mV) = (VBAT_READ_H × 32 + VBAT_READ_L/8). |

**Table 54. VBAT_READ_L, Register Address 0x23 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:3] | VBAT_READ[4:0] | R | Not applicable | The battery voltage reading, lowest 5 bits, unit is mV. $V_{BAT}$ (mV) = (VBAT_READ_H × 32 + VBAT_READ_L/8). |
| [2:0] | Not used | R | | Not used. |

**Table 55. FUEL_GAUGE_MODE, Register Address 0x24 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:2] | Not used | R | | Not used. |
| 2 | SLEEP_UPDATE_TIME | R/W | 0 | Select SOC update time in sleep mode.<br>0: 5 min.<br>1: 20 min. |
| 1 | FUEL_GAUGE_MODE | R/W | 0 | Fuel gauge operation mode.<br>1: enable sleep mode.<br>0: disable sleep mode. |
| 0 | FUEL_GAUGE_ENABLE | R/W | 0 | 0: disable fuel gauge.<br>1: enable fuel gauge. |

**Table 56. SOC_RESET, Register Address 0x25 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | SOC reset | W | 0 | Write 1 to reset the BAT_SOC, VBAT_READ_H, and VBAT_READ_L registers. |
| [6:0] | Not used | R | | Not used. |

**Table 57. BST_LED_CTRL, Register Address 0x26 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:6] | Not used | R | | Not used. |
| 5 | EN_BST | R/W | 0 | Boost enable signal (only effective when the boost regulator is in standalone operation mode).<br>0 = disable boost output.<br>1 = enable boost output. |
| 4 | EN_LED5 | R/W | 0 | Enable signal for LED5 individual sink (not effective if LED5 is configured as the grouped backlight).<br>0 = disable individual LED5 current sink.<br>1 = enable individual LED5 current sink. |
| 3 | EN_LED4 | R/W | 0 | Enable signal for LED4 individual sink (not effective if LED4 is configured as the grouped backlight).<br>0 = disable individual LED4 current sink.<br>1 = enable individual LED4 current sink. |
| 2 | EN_LED3 | R/W | 0 | Enable signal for LED3 individual sink (not effective if LED3 is configured as the grouped backlight).<br>0 = disable individual LED3 current sink.<br>1 = enable individual LED3 current sink. |
| 1 | EN_LED2 | R/W | 0 | Enable signal for LED2 individual sink (not effective if LED2 is configured as the grouped backlight).<br>0 = disable individual LED2 current sink.<br>1 = enable individual LED2 current sink. |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 0 | EN_BL | R/W | 0 | The grouped backlight enable signal.<br>0 = disable the grouped backlight.<br>1 = enable the grouped backlight. |

**Table 58. BST_CFG, Register Address 0x27 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | BST_MODE | R/W | 0 | This bit sets the boost regulator operation mode.<br>0 = LED operation mode.<br>1 = boost standalone operation mode. |
| 6 | BST_BL | R/W | 0 | This bit configures the boost regulator to provide the bias voltage to all active LED channels or only to the active LED backlight channels. (effective only when the boost regulator is configured in LED operation mode).<br>0 = set the boost regulator to provide the bias voltage for all active LED channels. In this configuration, the boost regulator provides the adaptive headroom regulation according to all active LED current sources.<br>1 = set the boost regulator to provide the bias voltage only to the active LED backlight channels. |
| 5 | FOVR | R/W | 0 | This bit configures the override feature in the backlight fade in and fade out.<br>0 = the fade in and fade out override is disabled.<br>1 = the fade in and fade out override is enabled. |
| 4 | Not used | R | | Not used. |
| [3:2] | BST_OVP | R/W | 00 | This bit sets the overvoltage threshold in the boost output voltage in VOUT4 pin.<br>00 = 18.5 V.<br>01 = 15 V.<br>10 = 10 V.<br>11 = 5.6 V. |
| 1 | Not used | R | | Not used. |
| 0 | BST_IPK | R/W | 0 | This bit sets the peak current limit for boost regulator.<br>0 = 600 mA peak current limit.<br>1 = 300 mA peak current limit. |

**Table 59. IBL_SET, Register Address 0x28 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:6] | Not used | R | | Not used. |
| [5:0] | IBL[5:0] | R/W | 000000 | These bits set the LED current setting for the grouped backlight (LED1). All grouped backlight LED channels follow this current setting. A square law algorithm for 64 levels is used.<br>000000 = 0 mA.<br>000001 = 0.005 mA.<br>000010 = 0.020 mA.<br>…<br>111101 = 18.750 mA.<br>111110 = 19.370 mA.<br>111111 = 20 mA. |

**Table 60. ILED2_SET, Register Address 0x29 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | BL_LED2 | R/W | 0 | This bit sets LED2 as the grouped backlight or individual current sink.<br>0 = set as individual current sink.<br>1 = set as grouped backlight. |
| 6 | Not used | R | | Not used. |
| [5:0] | ILED2[5:0] | R/W | 000000 | These bits set the individual LED current setting for LED2. This setting is not effective if LED2 is configured as the grouped LED backlight. A square law algorithm for 64 levels is used.<br>000000 = 0 mA.<br>000001 = 0.005 mA.<br>000010 = 0.020 mA.<br>…<br>111101 = 18.750 mA.<br>111110 = 19.370 mA.<br>111111 = 20 mA. |

**Table 61. ILED3_SET, Register Address 0x2A Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | BL_LED3 | R/W | 0 | This bit sets LED3 as the grouped backlight or individual current sink.<br>0 = set as individual current sink.<br>1 = set as grouped backlight. |
| 6 | Not used | R | | Not used. |
| [5:0] | ILED3[5:0] | R/W | 000000 | Those bits set the individual LED current setting for LED3. This setting is not effective if LED3 is configured as the grouped LED backlight. A square law algorithm for 64 levels is used.<br>000000 = 0 mA.<br>000001 = 0.005 mA.<br>000010 = 0.020 mA.<br>…<br>111101 = 18.750 mA.<br>111110 = 19.370 mA.<br>111111 = 20 mA. |

**Table 62. ILED4_SET, Register Address 0x2B Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | BL_LED4 | R/W | 0 | This bit sets LED4 as the grouped backlight or individual current sink.<br>0 = set as individual current sink.<br>1 = set as grouped backlight. |
| 6 | Not used | R | | Not used. |
| [5:0] | ILED4[5:0] | R/W | 000000 | Those bits set the individual LED current setting for LED4. This setting is not effective if LED4 is configured as the grouped LED backlight. A square law algorithm for 64 levels is used.<br>000000 = 0 mA.<br>000001 = 0.005 mA.<br>000010 = 0.020 mA.<br>…<br>111101 = 18.750 mA.<br>111110 = 19.370 mA.<br>111111 = 20 mA. |

**Table 63. ILED5_SET, Register Address 0x2C Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | BL_LED5 | R/W | 0 | This bit sets LED5 as the grouped backlight or individual current sink.<br>0 = set as individual current sink.<br>1 = set as grouped backlight. |
| 6 | Not used | R | | Not used. |
| [5:0] | ILED5[5:0] | R/W | 000000 | Those bits set the individual LED current setting for LED5. This setting is not effective if LED5 is configured as the grouped LED backlight. A square law algorithm for 64 levels is used.<br>000000 = 0 mA.<br>000001 = 0.005 mA.<br>000010 = 0.020 mA.<br>…<br>111101 = 18.750 mA.<br>111110 = 19.370 mA.<br>111111 = 20 mA. |

**Table 64. BL_FR, Register Address 0x2D Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | BL_FO[3:0] | R/W | 0000 | These bits set the fade out timer for the grouped LED backlight. The timer setting applies to the specific time starting from the maximum LED current code fade out to zero. Therefore, the real fade out time is shorter if the maximum LED current code is not being used. |
| | | | | 0000 = fade-out disabled.<br>0001 = 0.3 sec.<br>0010 = 0.6 sec.<br>…<br>1101 = 3.9 sec.<br>1110 = 4.2 sec.<br>1111 = 4.5 sec. |
| [3:0] | BL_FI[3:0] | R/W | 0000 | These bits set the fade in timer for the grouped LED backlight. The timer setting applies to the specific time starting from zero fading into the maximum LED current code. Therefore, the real fade in time is shorter if the maximum LED current code is not being used.<br>0000 = fade in disabled.<br>0001 = 0.3 sec.<br>0010 = 0.6 sec.<br>…<br>1101 = 3.9 sec.<br>1110 = 4.2 sec.<br>1111 = 4.5 sec. |

**Table 65. LED3_BLINK, Register Address 0x2E Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | LED3_OFF[3:0] | R/W | 0000 | These bits set the off timer for the LED3 blinking feature (not effective if this LED channel is configured as the grouped LED backlight).<br>0000 = the blinking feature is disabled.<br>0001 = 0.250 sec.<br>0010 = 0.500 sec.<br>0011 = 0.750 sec.<br>…<br>1110 = 3.500 sec.<br>1111 = 3.750 sec. |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [3:0] | LED3_ON[3:0] | R/W | 0000 | These bits set the on timer for the LED3 blinking feature (not effective if this LED channel is configured as the grouped LED backlight).<br>0000 = 0.125 sec.<br>0000 = 0.250 sec.<br>0010 = 0.375 sec.<br>…<br>1110 = 1.875 sec.<br>1111 = 2.000 sec. |

**Table 66. LED4_Blink, Register Address 0x2F Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | LED4_OFF[3:0] | R/W | 0000 | These bits set the off timer for the LED4 blinking feature (not effective if this LED channel is configured as the grouped LED backlight).<br>0000 = the blinking feature is disabled.<br>0001 = 0.250 sec.<br>0010 = 0.500 sec.<br>0011 = 0.750 sec.<br>…<br>1110 = 3.500 sec.<br>1111 = 3.750 sec |
| [3:0] | LED4_ON[3:0] | R/W | 0000 | These bits set the on timer for the LED4 blinking feature (not effective if this LED channel is configured as the grouped LED backlight).<br>0000 = 0.125 sec.<br>0000 = 0.250 sec.<br>0010 = 0.375 sec.<br>…<br>1110 = 1.875 sec.<br>1111 = 2.000 sec. |

**Table 67. LED5_Blink, Register Address 0x30 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | LED5_OFF[3:0] | R/W | 0000 | These bits set the off timer for the LED4 blinking feature (not effective if this LED channel is configured as the grouped LED backlight).<br>0000 = the blinking feature is disabled.<br>0001 = 0.250 sec.<br>0010 = 0.500 sec.<br>0011 = 0.750 sec.<br>…<br>1110 = 3.500 sec.<br>1111 = 3.750 sec. |
| [3:0] | LED5_ON[3:0] | R/W | 0000 | These bits set the on timer for the LED5 blinking feature (not effective if this LED channel is configured as the grouped LED backlight).<br>0000 = 0.125 sec.<br>0000 = 0.250 sec.<br>0010 = 0.375 sec.<br>…<br>1110 = 1.875 sec.<br>1111 = 2.000 sec. |

**Table 68. LED_STATUS, Register Address 0x31 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:5] | Not used | R | | Not used. |
| 4 | LED5_OPEN[1] | R | Not applicable | This bit records the LED5 status<br>0: LED5 channel is not open<br>1: LED5 channel is open |
| 3 | LED4_OPEN[1] | R | Not applicable | This bit records the LED4 status<br>0: LED4 channel is not open<br>1: LED4 channel is open |
| 2 | LED3_OPEN[1] | R | Not applicable | This bit records the LED3 status<br>0: LED3 channel is not open<br>1: LED3 channel is open |
| 1 | LED2_OPEN[1] | R | Not applicable | This bit records the LED2 status<br>0: LED2 channel is not open<br>1: LED2 channel is open |
| 0 | LED1_OPEN[1] | R | Not applicable | This bit records the LED1 status<br>0: LED1 channel is not open<br>1: LED1 channel is open |

[1] To reset any bit in this register, power cycle VBUSx or write the corresponding I²C bit high.

**Table 69. LDO_CTRL, Register Address 0x32 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:3] | Not used | R | | Not used. |
| 2 | EN_LDO3 | R/W | Factory setting | Enable signal for LDO3 (or Load Switch 3)<br>0 = disable LDO3 (or Load Switch 3)<br>1 = enable LDO3 (or Load Switch 3) |
| 1 | EN_LDO2 | R/W | Factory setting | Enable signal for LDO2 (or Load Switch 2)<br>0 = disable LDO2 (or Load Switch 2)<br>1 = enable LDO2 (or Load Switch 2) |
| 0 | EN_LDO1 | R/W | 1 | Enable signal for LDO1 (or Load Switch 1)<br>0 = disable LDO1 (or Load Switch 1)<br>1 = enable LDO1 (or Load Switch 1) |

**Table 70. LDO_CFG, Register Address 0x33 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | Not used | R | | Not used. |
| 6 | DSCG_LDO3 | R/W | 0 | This bit configures the output discharge functionality for LDO3 or Load Switch 3<br>0 = discharge functionality disabled<br>1 = discharge functionality enabled |
| 5 | DSCG_LDO2 | R/W | 0 | This bit configures the output discharge functionality for LDO2 or Load Switch 2<br>0 = discharge functionality disabled<br>1 = discharge functionality enabled |
| 4 | DSCG_LDO1 | R/W | 0 | This bit configures the output discharge functionality for LDO1 or Load Switch 1<br>0 = discharge functionality disabled<br>1 = discharge functionality enabled |
| 3 | Not used | R | | Not used. |
| 2 | MODE_LDO3 | R/W | 0 | This bit sets LDO3 as an LDO or load switch<br>0 = LDO mode<br>1 = load switch mode |
| 1 | MODE_LDO2 | R/W | 0 | This bit sets LDO2 as an LDO or load switch<br>0 = LDO mode<br>1 = load switch mode |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 0 | MODE_LDO1 | R/W | 0 | This bit sets LDO1 as an LDO or load switch<br>0 = LDO mode<br>1 = load switch mode |

**Table 71. VID_LDO12, Register Address 0x34 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | VID_LDO2 | R/W | Factory setting | These bits set the output voltage in LDO2. These bits have no effect when this channel is set as a load switch.<br>0000 = 4.20 V.<br>0001 = 3.60 V.<br>0010 = 3.30 V.<br>0011 = 3.15 V.<br>0100 = 3.00 V.<br>0101 = 2.85 V.<br>0110 = 2.50 V.<br>0111 = 2.30 V.<br>1000 = 2.10 V.<br>1001 = 1.80 V.<br>1010 = 1.50 V.<br>1011 = 1.40 V.<br>1100 = 1.30 V.<br>1101 = 1.20 V.<br>1110 = 1.10 V.<br>1111 = 1.00 V. |
| [3:0] | VID_LDO1 | R/W | Factory setting | These bits set the output voltage in LDO1. These bits have no effect when this channel is set as a load switch.<br>0000 = 4.20 V.<br>0001 = 3.60 V.<br>0010 = 3.30 V.<br>0011 = 3.15 V.<br>0100 = 3.00 V.<br>0101 = 2.85 V.<br>0110 = 2.50 V.<br>0111 = 2.30 V.<br>1000 = 2.10 V.<br>1001 = 1.80 V.<br>1010 = 1.50 V.<br>1011 = 1.40 V.<br>1100 = 1.30 V.<br>1101 = 1.20 V.<br>1110 = 1.10 V.<br>1111 = 1.00 V. |

**Table 72. VID_LDO3, Register Address 0x35 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | Not used | R | | Not used. |
| [3:0] | VID_LDO3 | R/W | Factory setting | These bits set the output voltage in LDO3. These bits have no effect when this channel is set as a load switch.<br>0000 = 4.20 V.<br>0001 = 3.60 V.<br>0010 = 3.30 V.<br>0011 = 3.15 V.<br>0100 = 3.00 V.<br>0101 = 2.85 V.<br>0110 = 2.50 V.<br>0111 = 2.30 V.<br>1000 = 2.10 V.<br>1001 = 1.80 V.<br>1010 = 1.50 V.<br>1011 = 1.40 V.<br>1100 = 1.30 V.<br>1101 = 1.20 V.<br>1110 = 1.10 V.<br>1111 = 1.00 V. |

**Table 73. PGOOD_STATUS, Register Address 0x36 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | Not used | R | | Not used. |
| 3 | VBUSOK | R | Not applicable | This bit shows real-time status of VBUSx voltage.<br>0 = the voltage at the VBUSx pin is below $V_{VBUSOK}$ or above $V_{VBUS\_OV}$.<br>1 = the voltage at the VBUSx pin is above $V_{VBUSOK}$ and below $V_{VBUS\_OV}$. |
| 2 | BATOK | R | Not applicable | This bit shows the real-time status of the battery voltage.<br>0 = battery voltage is lower than $V_{WEAK}$.<br>1 = battery voltage is higher than $V_{WEAK}$. |
| 1 | PG4_BST | R | Not applicable | This bit shows the real-time power-good status for the boost regulator. This bit is effective only in boost standalone fixed output mode.<br>0 = boost regulator power-good status is low.<br>1 = boost regulator power-good status is high. |
| 0 | PG1_LDO1 | R | Not applicable | This bit shows the real-time power good status for LDO1. This bit is not effective if the LDO regulator is configured as a load switch mode.<br>0 = LDO1 power-good status is low.<br>1 = LDO1 power-good status is high. |

**Table 74. PGOOD_MASK, Register Address 0x37 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:4] | Not used | R | | Not used. |
| 3 | VBUSOK_MASK | R/W | Factory setting | This bit configures the external PGOOD pin.<br>0 = do not output the $V_{VBUSx}$ voltage status signal to the external PGOOD pin.<br>1 = output $V_{BUS}$ voltage status signal to the external PGOOD pin. |
| 2 | BATOK_MASK | R/W | 0 | This bit configures the external PGOOD pin.<br>0 = do not output BATOK signal to the external PGOOD pin.<br>1 = output the BATOK signal to the external PGOOD pin. |

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 1 | PG4_BST_MASK | R/W | 0 | This bit configures the external PGOOD pin. This bit is only effective in boost standalone fixed output mode.<br>0 = do not output the boost PGOOD signal to the external PGOOD pin.<br>1 = output the boost PGOOD signal to the external PGOOD pin. |
| 0 | PG1_LDO1_MASK[1] | R/W | Factory setting | This bit configures the external PGOOD pin. This bit is not effective if the LDO regulator is configured as a load switch mode.<br>0 = do not output the LDO1 PGOOD signal to the external PGOOD pin.<br>1 = output the LDO1 PGOOD signal to the external PGOOD pin. |

[1] When the PGOOD pin is selected for PG1_LDO1_MASK, the ADP5350 quiescent current increases to 4 µA typically.

**Table 75. CHARGER_INTERRUPT_ENABLE, Register Address 0x38 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | EN_IND_PEAK_INT | R/W | 0 | When high, the inductor peak current-limit interrupt is enabled. |
| 6 | EN_THERM_LIM_INT | R/W | 0 | When high, the isothermal charging interrupt is allowed. |
| 5 | EN_WD_INT | R/W | 0 | When high, the watchdog alarm interrupt is allowed. |
| 4 | EN_TSD_INT | R/W | 0 | When high, the overtemperature 130°C warning interrupt is allowed. |
| 3 | EN_THR_INT | R/W | 0 | When high, the THR temperature thresholds interrupt is allowed. |
| 2 | EN_BAT_INT | R/W | 0 | When high, the battery voltage thresholds interrupt is allowed. |
| 1 | EN_CHG_INT | R/W | 0 | When high, the charger mode change interrupt is allowed. |
| 0 | EN_VIN_INT | R/W | 0 | When high, the VBUSx pin voltage thresholds interrupt is allowed. |

**Table 76. CHARGER_INTERRUPT_FLAG, Register Address 0x39 Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| 7 | IND_PEAK_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by an inductor peak current limit. |
| 6 | THERM_LIM_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by isothermal charging. |
| 5 | WD_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by the watchdog alarm. The watchdog timer expires within 2 sec or 4 sec depending on the $t_{WD}$ setting of 32 sec or 64 sec, respectively. |
| 4 | TSD_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by an overtemperature fault. |
| 3 | THR_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by THR temperature thresholds. |
| 2 | BAT_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by battery voltage thresholds. |
| 1 | CHG_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by a charger mode change. |
| 0 | VIN_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by VBUSx voltage thresholds. |

[1] These bits reset to 0 automatically when read.

**Table 77. BOOST_LDO_INTERRUPT_ENABLE, Register Address 0x3A Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:3] | Not used | R | | Not used. |
| 2 | EN_LED_OPEN_INT | R/W | 0 | 0 = LED open events does not trigger the interrupt pin.<br>1 = LED open events triggers the interrupt pin. |
| 1 | EN_PG4_BST_INT | R/W | 0 | 0 = power-good warning on the boost regulator does not trigger the interrupt pin.<br>1 = power-good warning on the boost regulator triggers the interrupt pin. |
| 0 | EN_PG1_LDO1_INT | R/W | 0 | 0 = power-good warning on LDO1 does not trigger the interrupt pin.<br>1 = power-good warning on LDO1 triggers the interrupt pin. |

**Table 78. BOOST_LDO_INTERRUPT_FLAG, Register Address 0x3B Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:3] | Not used | R | | Not used. |
| 2 | LED_OPEN_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by LED open-circuit faults. |
| 1 | PG4_BST_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by a power-good warning on the boost regulator. |
| 0 | PG1_LDO1_INT[1] | R | 0 | When high, this bit indicates an interrupt caused by a power-good warning on LDO1. |

[1] These bits reset to 0 automatically when read.

**Table 79. DEFAULT_SET, Register Address 0x3C Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:0] | DEFAULT_SET | W | 0 | Write 0x7F to this bit to reset all register to default values. |

**Table 80. NTC47K_SET, Register Address 0x3D Bit Descriptions**

| Bit No. | Mnemonic | Access | Default | Description |
|---|---|---|---|---|
| [7:1] | Not used | R | | Not used. |
| 0 | NTC_47K | R/W | 1 | Select battery thermistor NTC resistance, effective when R_NTC = 1.<br>0 = 100 kΩ at 25°C.<br>1 = 47 kΩ at 25°C. |

# APPLICATIONS INFORMATION

## EXTERNAL COMPONENTS

### Buck Inductor Selection

The high switching frequency of the ADP5350 buck converter allows the selection of small chip inductors. Suggested buck inductors are shown in Table 81.

The peak-to-peak inductor current ripple, $I_{RIPPLE}$, is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{ISOS} \times (V_{ISOS} - V_{CFL1})}{V_{ISOS} \times f_{SW} \times L1}$$

where:
$V_{ISOS}$ is the ISOS node output voltage.
$V_{CFL1}$ is the converter input voltage at the CFL1 node.
$f_{SW}$ is the switching frequency.
$L1$ is the buck output inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current, $I_{PEAK}$, is calculated using the following equation:

$$I_{PEAK} = I_{CHG} + I_{LOAD\_MAX} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger inductors have smaller DCR values, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the buck regulators are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low electromagnetic interference (EMI).

### Boost Inductor Selection

The inductor is an essential part of the boost switching regulator. It stores energy during the on time, and transfers that energy to the output through the output rectifier during the off time. Use inductance in the range of 2 µH to 10 µH. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. Peak-to-peak inductor ripple current at close to 30% of the maximum dc input current typically yields an optimal compromise. Suggested boost inductors are shown in Table 82.

The input $V_{IN4}$ and output $V_{OUT4}$ voltages determine the switch duty cycle, which in turn determine the inductor ripple current. Calculate the inductor ripple current in a steady state using the following equation:

$$I_{RIPPLE4} = \frac{V_{IN4} \times (V_{OUT4} - V_{IN4})}{V_{OUT4} \times f_{SW4} \times L2}$$

Make sure that the peak inductor current, the maximum input current plus half the inductor ripple current is below the rated saturation current of the inductor. Likewise, make sure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

### VBUSx Capacitor Selection

According to the USB 2.0 specification, USB peripherals have a detectable change in capacitance on VBUSx when VBUSx are attached. The peripheral device VBUSx bypass capacitance must be at least 1 µF but not larger than 10 µF. The combined capacitance for the VBUSx and CFL1 pins must not exceed 10 µF at any temperature or dc bias condition. Suggested VBUSx capacitors are shown in Table 83.

### CFL1 Capacitor Selection

The CFL1 pin serves the ADP5350 as the buck dc-to-dc regulator input capacitor. The rms current rating of the input capacitor current must be larger than the value calculated by the following equation:

$$I_{C\_RMS} = (I_{CHG} + I_{LOAD\_MAX}) \sqrt{\frac{V_{ISOS} \times (V_{CFL1} - V_{ISOS})}{V_{CFL1}}}$$

To minimize supply noise, place the input capacitor as close as possible to the CFL1 pin of the charger. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 2 µF and a maximum of 7 µF. A list of suggested capacitors is shown in Table 84.

**Table 81. Suggested Buck Inductors**

| Vendor | Part Number | L (µH) | Typical DC Current (A) | Maximum DCR (mΩ) | Size |
|---|---|---|---|---|---|
| Wurth | 74479976215 | 1.5 | 1.2 | 125 | 0806 |
| TDK | VLS201612CX-1R5M | 1.5 | 1.9 | 89 | 0806 |

**Table 82. Suggested Boost Inductors**

| Vendor | Part Number | L (µH) | Typical DC Current (A) | Maximum DCR (mΩ) | Size |
|---|---|---|---|---|---|
| Wurth | 74479776247A | 4.7 | 0.9 | 140 | 0806 |
| TDK | VLS201612CX-4R7M | 4.7 | 1.12 | 252 | 0806 |

### CFL2 Capacitor Selection

The CFL2 pin is the internal regulator output that provides the power supply for post stage control circuits, including the fuel gauge, boost LED, and LDOs. To ensure stable performance of the internal regulator, the recommended components for the CFL2 capacitor are given in Table 85.

### ISOS and ISOB Capacitor Selection

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

To guarantee the performance of the charger in various operation modes, including trickle charge, CC charge, and CV charge, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}$$

Capacitors with lower effective series resistance (ESR) are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

**Table 83. Suggested VBUSx Capacitors**

| Vendor | Part Number | Value (µF) | Voltage (V) | Size |
|---|---|---|---|---|
| Murata | GRM188R61E225K | 2.2 | 25 | 0603 |
| TDK | C1608X5R1E225 | 2.2 | 25 | 0603 |

**Table 84. Suggested CFL1 Capacitors**

| Vendor | Part Number | Value (µF) | Voltage (V) | Size |
|---|---|---|---|---|
| Murata | GRM188R60J475K | 4.7 | 6.3 | 0603 |
| TDK | C1608X5R0J475K | 4.7 | 6.3 | 0603 |

**Table 85. Suggested CFL2 Capacitors**

| Vendor | Part Number | Value (µF) | Voltage (V) | Size |
|---|---|---|---|---|
| Murata | GRM188R60J225K | 2.2 | 6.3 | 0603 |
| TDK | C1608X5R0J475K | 2.2 | 6.3 | 0603 |

**Table 86. Suggested ISOS and ISOB Capacitors**

| Vendor | Part Number | Value (µF) | Voltage (V) | Size |
|---|---|---|---|---|
| Murata | GRM188R60J106K | 10 | 6.3 | 0603 |
| TDK | C1608X5R0J106M080AB | 10 | 6.3 | 0603 |

### LDO Capacitor Selection

Connecting a 1 µF capacitor from VIN123 to AGND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered.

The ADP5350 is designed for operation with small, space-saving ceramic capacitors, but functions with most commonly used capacitors as long as care is taken with regard to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP5350. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5350 to large changes in load current.

**Table 87. Suggested LDO Capacitors**

| Vendor | Part Number | Value (µF) | Voltage (V) | Size |
|---|---|---|---|---|
| Murata | GRM155R60J105KE19D | 1 | 6.3 | 0402 |
| TDK | CGB2A3X5R0J105M033BB | 1 | 6.3 | 0402 |

### Boost Capacitor Selection

The ADP5350 requires input and output decoupling capacitors to supply transient currents while maintaining a constant input and output voltage. Use a low ESR input capacitor, 4.7 µF or greater, to prevent noise at the VIN4 node. Place the capacitor between the VIN4 pin and PGND4 as close to the ADP5350 as possible. Ceramic capacitors are preferred because of their low ESR characteristics.

The output capacitor maintains the output voltage and supplies current to the load while the boost switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. Use a low ESR output capacitor; ceramic dielectric capacitors are preferred.

For very low ESR capacitors, such as ceramic capacitors, the ripple current due to the capacitance is calculated as follows. Because the capacitor discharges during the on time the charge removed from the capacitor is the load current multiplied by the on time. Choose the output capacitor based on the following equation:

$$C_{OUT4} \geq \frac{I_{L2} \times \left(V_{OUT4} - V_{IN4}\right)}{f_{SW4} \times V_{OUT4} \times V_{RIPPLE4}}$$

where:
$I_{L2}$ is the average inductor current.
$V_{RIPPLE4}$ is boost output voltage ripple.

**Table 88. Suggested Boost Capacitors**

| Vendor | Part Number | Value (µF) | Voltage (V) | Size |
|---|---|---|---|---|
| Murata | GRM188R61C475ME11 | 4.7 | 25 | 0603 |
| TDK | C1608X5R1E475M080AC | 4.7 | 25 | 0603 |
| Murata | GRM188R61E106MA73 | 10 | 25 | 0603 |
| TDK | C1608X5R1E106M080AC | 10 | 25 | 0603 |

## PCB LAYOUT GUIDELINES

Poor layout can affect ADP5350 performance, causing EMI and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the decoupling capacitor, inductor, input capacitor, and output capacitor close to the IC.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Use a dedicated trace to connect the BSNS pin to the battery pack output node for accurate sensing of the battery voltage.
- Use Size 0603 or Size 0402 resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

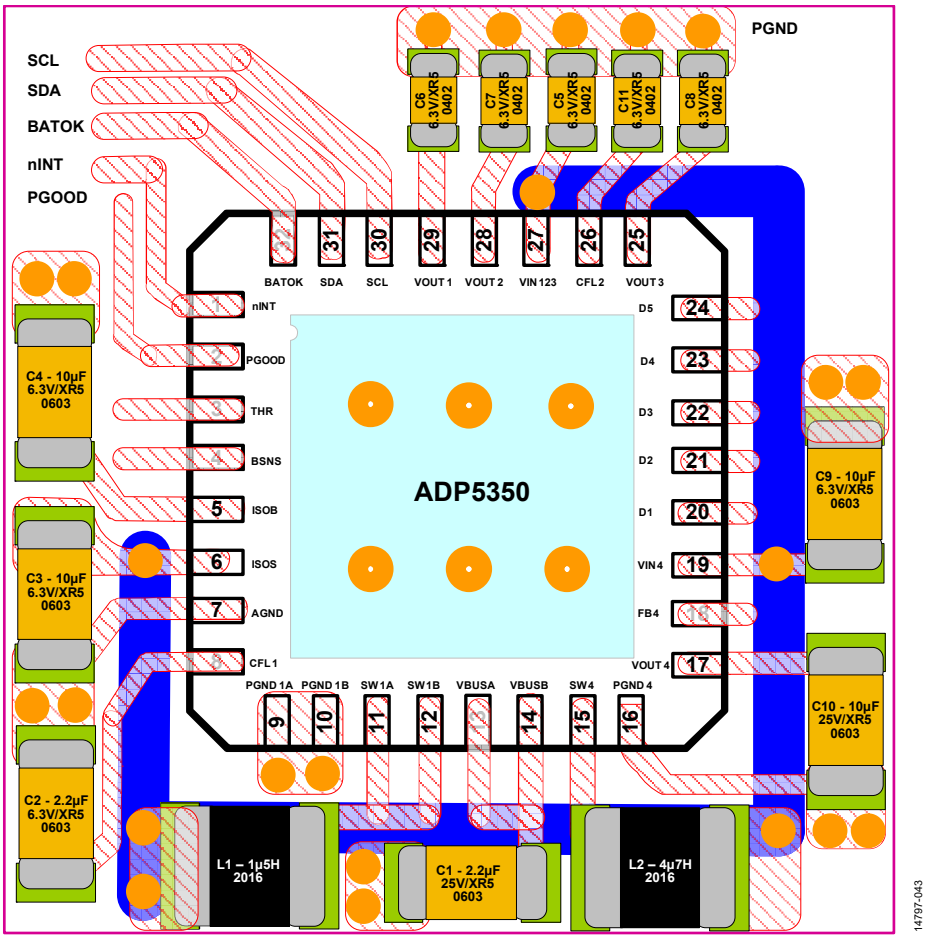



*Figure 59. Recommended Layout*

## TYPICAL APPLICATION CIRCUITS

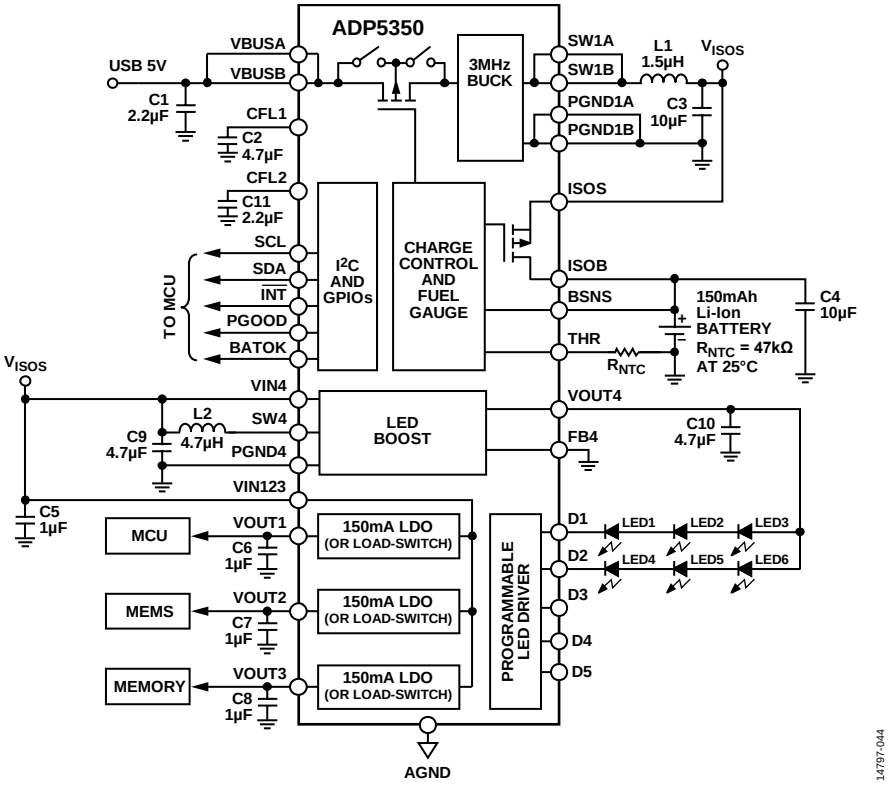



*Figure 60. Li-Ion Battery Charger Application with LED Panel*

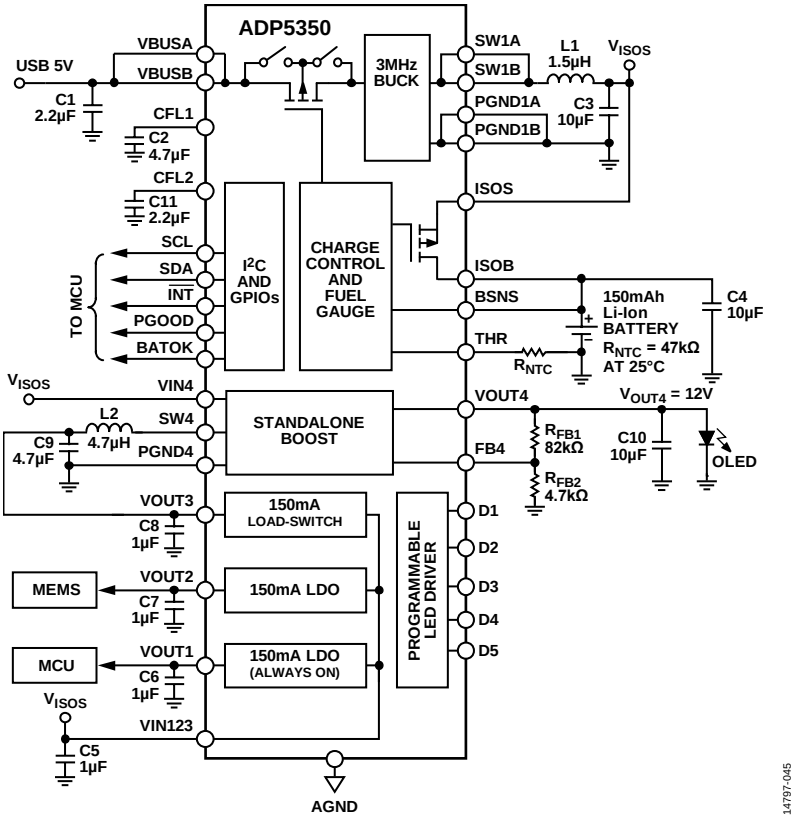



*Figure 61. True Shutdown Standalone Boost for OLED Panel Application*

# FACTORY-PROGRAMMABLE OPTIONS

**Table 89. Fuse-Programmable Trim Options for the ADP5350**

| Parameter | Value | Default Setting |
|---|---|---|
| I²C Address | 0x44<br>0x45<br>0x64<br>0x65 | 0x44 |
| R_NTC | 10 kΩ<br>100 kΩ/47 kΩ | 100 kΩ/47 kΩ |
| BETA_NTC | 2350<br>2600<br>2750<br>3000<br>3150<br>3350<br>3500<br>3600<br>3800<br>4000<br>4200<br>4400<br>4600<br>4800<br>5000<br>5200 | 3800 |
| EN_CHG | Charger is enabled<br>Charger is disabled | Charger is disabled |
| EN_LDO2 | LDO2 is enabled<br>LDO2 is disabled | LDO2 is disabled |
| EN_LDO3 | LDO3 is enabled<br>LDO3 is disabled | LDO3 is disabled |
| VID_LDO1, VID_LDO2, VID_LDO3 | 4.20 V<br>3.60 V<br>3.30 V<br>3.15 V<br>3.00 V<br>2.85 V<br>2.50 V<br>2.30 V<br>2.10 V<br>1.80 V<br>1.50 V<br>1.40 V<br>1.30 V<br>1.20 V<br>1.10 V<br>1.00 V | 3.3 V |
| VBUSOK_MASK | Do not output the $V_{VBUSx}$ voltage status signal to the external PGOOD pin<br>Output the $V_{VBUSx}$ voltage status signal to external PGOOD pin | Output the $V_{VBUSx}$ voltage status signal to the external PGOOD pin |
| PG1_LDO1_MASK | Do not output the LDO1 PGOOD signal to the external PGOOD pin<br>Output the LDO1 PGOOD signal to external PGOOD pin | Do not output the LDO1 PGOOD signal to the external PGOOD pin |

# OUTLINE DIMENSIONS

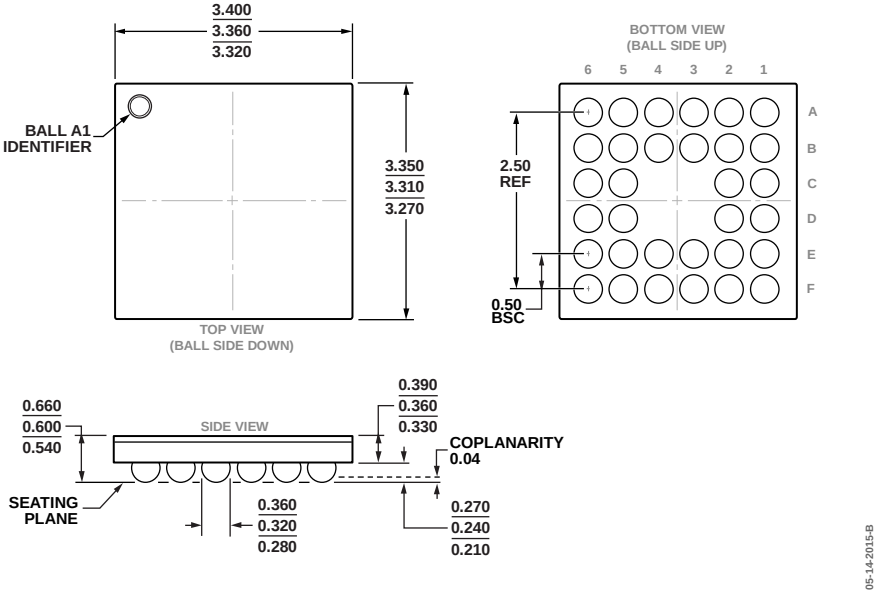
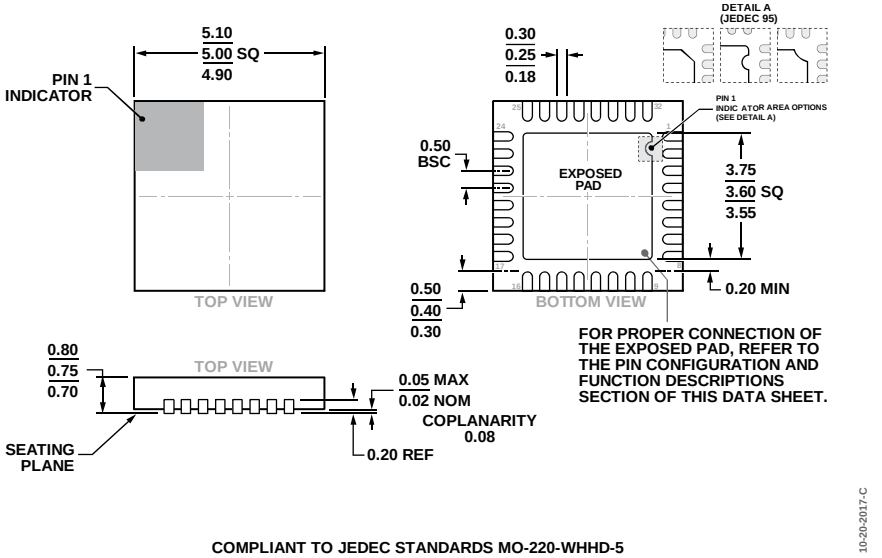



*Figure 62. 32-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-32-1)*
*Dimensions shown in millimeters*




**COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5**

*Figure 63. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.75 mm Package Height*
*(CP-32-12)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADP5350ACBZ-1-R7 | −40°C to +125°C | 32-Ball Wafer Level Chip Scale Package [WLCSP] | CB-32-1 |
| ADP5350ACPZ-1-R7 | −40°C to +125°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-12 |
| ADP5350CB-EVALZ | | Evaluation Board | |
| ADP5350CP-EVALZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.