GaAs, pHEMT, MMIC, Power Amplifier, 2 GHz to 50 GHz

Data Sheet **HMC1126**

FEATURES

Output power for 1 dB compression (P1dB): 17.5 dB typical
Saturated output power (P_{SAT}): 21 dBm typical
Gain: 11 dB typical
Output third-order intercept (IP3): 28 dBm typical
Supply voltage: 5 V at 65 mA
50 Ω matched input/output
Die size: 2.3 mm × 1.45 mm × 0.05 mm

APPLICATIONS

Test instrumentation
Microwave radios and VSATs
Military and space
Telecommunications infrastructure
Fiber optics

FUNCTIONAL BLOCK DIAGRAM

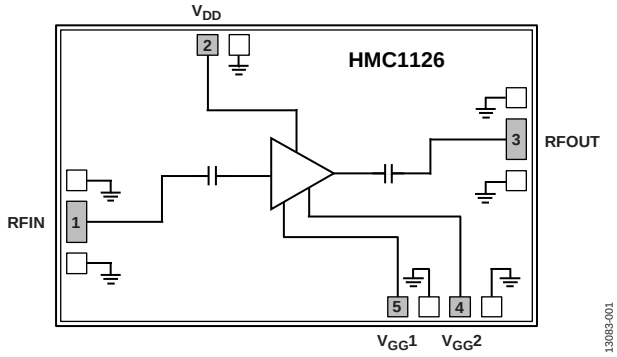

Figure 1.

GENERAL DESCRIPTION

The HMC1126 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from 2 GHz to 50 GHz. The HMC1126 provides 11 dB of gain, 28 dBm output IP3, and 17.5 dBm of output power at 1 dB gain compression, while requiring 65 mA from a 5 V supply.

The HMC1126 amplifier inputs/outputs are internally matched to 50 Ω facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm (1 mil) wire bonds of minimal length 0.31 mm (12 mils).

Rev. C **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

12/2017—Rev. B to Rev. C

Changes to Figure 1 ... 1
Changes to Figure 4 ... 7
Changes to Ordering Guide ... 16

2/2016—Rev. A to Rev. B

Change to Features Section ... 1
Updated Outline Dimensions ... 16

5/2015—Rev. 00.1114 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.
Updated Format ... Universal
Changes to Table 5 ... 5
Added Applications Information Section and Figure 35 ... 13
Added Ordering Guide Section ... 16

ELECTRICAL SPECIFICATIONS

2 GHz TO 10 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1.4 V, I_{DD} = 65 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V to 0 V to achieve I_{DD} = 65 mA typical.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			2		10	GHz
GAIN			8	11		dB
Gain Variation Over Temperature				0.002		dB/°C
RETURN LOSS						
Input				12		dB
Output				14		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		14.5	17.5		dBm
Saturated Output Power	P_{SAT}			21		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		31		dBm
NOISE FIGURE				4.5		
TOTAL SUPPLY CURRENT	I_{DD}	V_{DD} = 4 V, V_{DD} = 5 V, V_{DD} = 6 V, V_{DD} = 7 V, or V_{DD} = 8 V		65		mA

10 GHz TO 26 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1.4 V, I_{DD} = 65 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V to 0 V to achieve I_{DD} = 65 mA typical.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			10		26	GHz
GAIN			8	10.5		dB
Gain Variation Over Temperature				0.005		dB/°C
RETURN LOSS						
Input				14		dB
Output				20		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		14.5	17.5		dBm
Saturated Output Power	P_{SAT}			21		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		28		dBm
NOISE FIGURE				4		
TOTAL SUPPLY CURRENT	I_{DD}	V_{DD} = 4 V, V_{DD} = 5 V, V_{DD} = 6 V, V_{DD} = 7 V, or V_{DD} = 8 V		65		mA

26 GHz TO 40 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1.4 V, I_{DD} = 65 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V to 0 V to achieve I_{DD} = 65 mA typical.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			26		40	GHz
GAIN			8	11		dB
Gain Variation Over Temperature				0.005		dB/°C
RETURN LOSS						
Input				20		dB
Output				218		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		13	16		dBm
Saturated Output Power	P_{SAT}			20.5		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		28		dBm
NOISE FIGURE				4		
TOTAL SUPPLY CURRENT	I_{DD}	V_{DD} = 4 V, V_{DD} = 5 V, V_{DD} = 6 V, V_{DD} = 7 V, or V_{DD} = 8 V		65		mA

40 GHz TO 50 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1.4 V, I_{DD} = 65 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V to 0 V to achieve I_{DD} = 65 mA typical.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			40		50	GHz
GAIN			8	10.5		dB
Gain Variation Over Temperature				0.009		dB/°C
RETURN LOSS						
Input				12		dB
Output				12		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		10	13		dBm
Saturated Output Power	P_{SAT}			18		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		24		dBm
NOISE FIGURE				5		
TOTAL SUPPLY CURRENT	I_{DD}	V_{DD} = 4 V, V_{DD} = 5 V, V_{DD} = 6 V, V_{DD} = 7 V, or V_{DD} = 8 V		65		mA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DD})	8.5 V
Gate Bias Voltage	
$V_{GG}1$	−3 V to 0 V
$V_{GG}2$	
For V_{DD} = 8 V[1]	3.6 V
For V_{DD} = 7 V	3.0 V
For V_{DD} = 6 V	>2.0 V
For V_{DD} = 4 V to 5 V	>1.2 V
RF Input Power (RFIN)	22 dBm
Channel Temperature	175°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 21.3 mW/°C at 85°C)	1.915 W
Thermal Resistance, R_{TH} (Channel to Bottom of Die)	47°C/W[2]
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	Class 1A, passed 250 V

[1] I_{DD} < 105 mA.
[2] Based upon a thermal epoxy of 20 W/°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

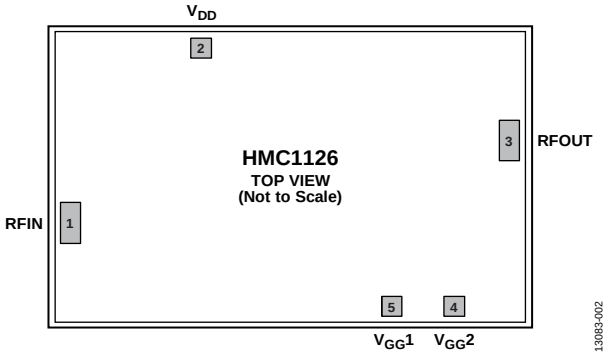

Figure 2. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	RF Input. This pin is ac-coupled and matched to 50 Ω.
2	V_{DD}	Power Supply Voltage with Integrated RF Choke. Connect dc bias to this pin to provide drain current (I_{DD}).
3	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω.
4	$V_{GG}2$	Gate Control 2 for Amplifier. Attach bypass capacitors as shown in Figure 38. For nominal operation, apply 1.4 V to $V_{GG}2$.
5	$V_{GG}1$	Gate Control 1 for Amplifier. Attach bypass capacitors as shown in Figure 38. Adjust this pin to achieve I_{DD} = 65 mA.
Die Bottom	GND	Die bottom must be connected to RF/dc ground.

INTERFACE SCHEMATICS

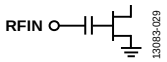

Figure 3. RFIN Interface Schematic

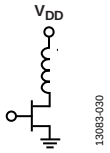

Figure 4. V_{DD} Interface Schematic

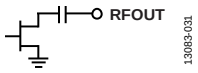

Figure 5. RFOUT Interface Schematic

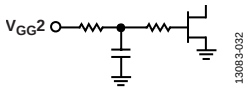

Figure 6. $V_{GG}2$ Interface Schematic

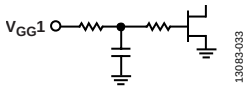

Figure 7. $V_{GG}1$ Interface Schematic

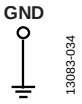

Figure 8. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

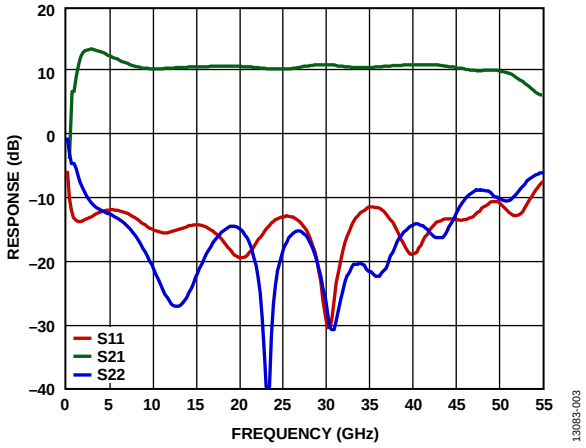

Figure 9. Response (Gain and Return Loss) vs. Frequency

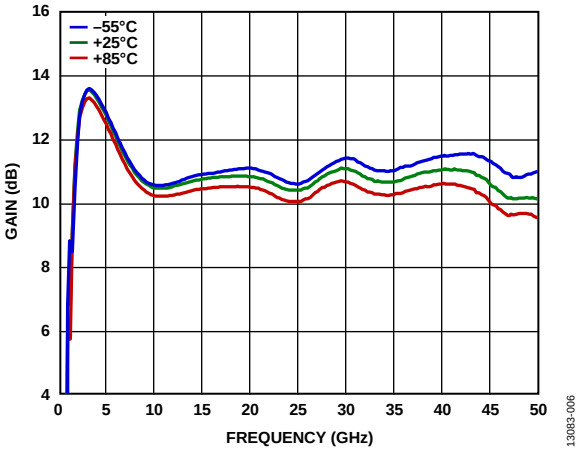

Figure 12. Gain vs. Frequency at Various Temperatures

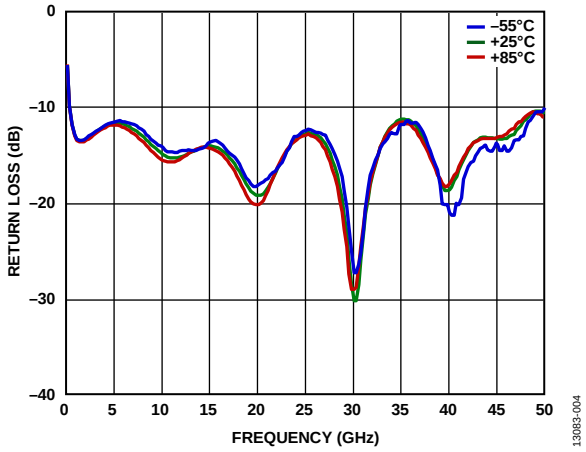

Figure 10. Input Return Loss vs. Frequency at Various Temperatures

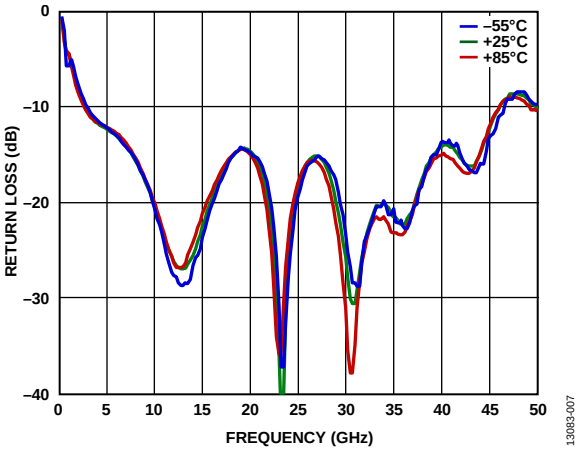

Figure 13. Output Return Loss vs. Frequency at Various Temperatures

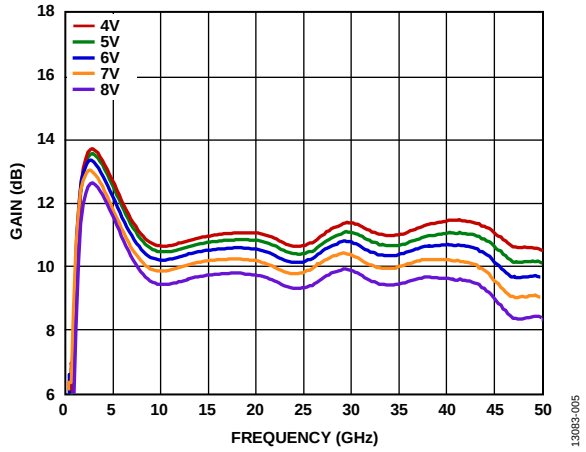

Figure 11. Gain vs. Frequency at Various Supply Voltages (V_{DD})
(For V_{DD} = 4 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 5 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 6 V, $V_{GG}2$ = 2 V; for V_{DD} = 7 V, $V_{GG}2$ = 3 V; for V_{DD} =8 V, $V_{GG}2$ = 3.6 V)

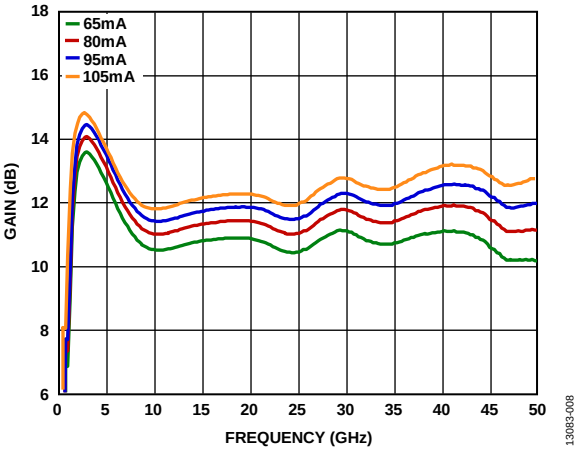

Figure 14. Gain vs. Frequency at Various Supply Currents (I_{DD})
(For V_{DD} = 5 V, $V_{GG}2$ = 1.4 V)

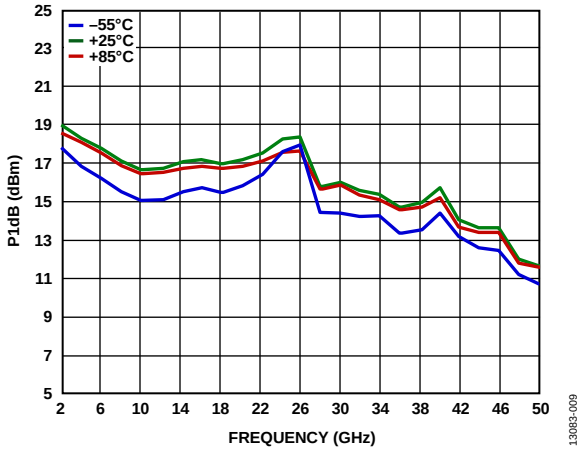

Figure 15. P1dB vs. Frequency at Various Temperatures

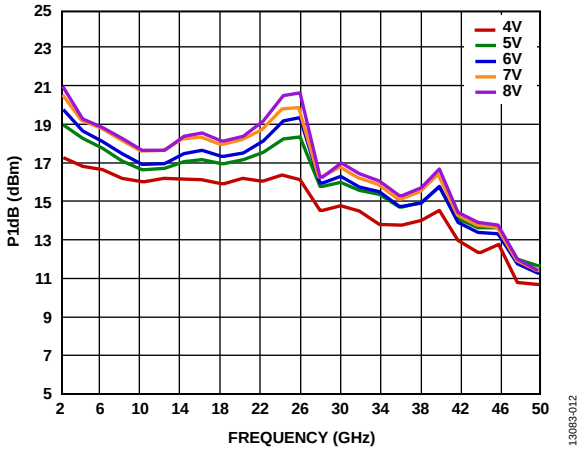

Figure 18. P1dB vs. Frequency at Various Supply Voltages (For V_{DD} = 4 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 5 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 6 V, $V_{GG}2$ = 2 V; for V_{DD} = 7 V, $V_{GG}2$ = 3 V; for V_{DD} =8 V, $V_{GG}2$ = 3.6 V)

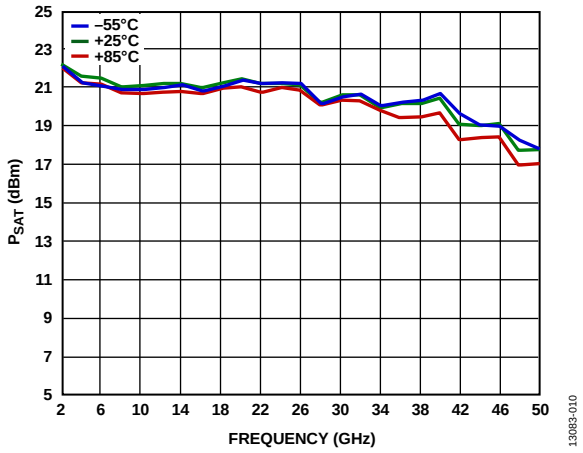

Figure 16. P_{SAT} vs. Frequency at Various Temperatures

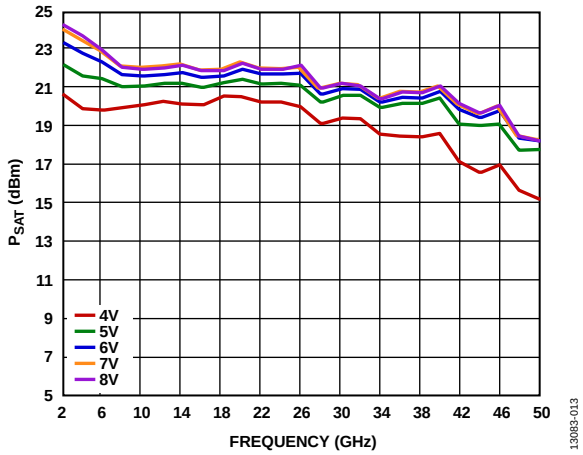

Figure 19. P_{SAT} vs. Frequency at Various Supply Voltages (For V_{DD} = 4 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 5 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 6 V, $V_{GG}2$ = 2 V; for V_{DD} = 7 V, $V_{GG}2$ = 3 V; for V_{DD} =8 V, $V_{GG}2$ = 3.6 V)

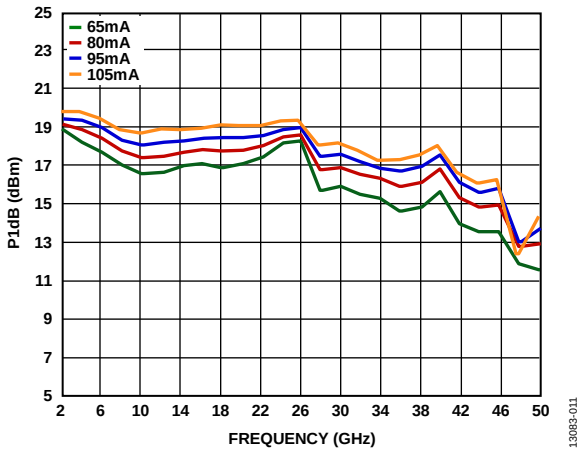

Figure 17. P1dB vs. Frequency at Various Supply Currents (For V_{DD} = 5 V, $V_{GG}2$ = 1.4 V)

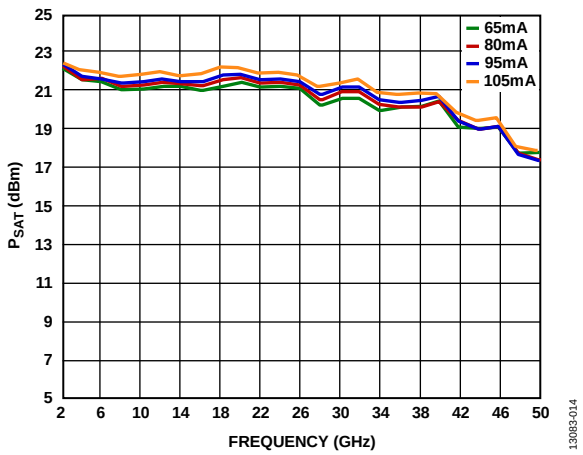

Figure 20. P_{SAT} vs. Frequency at Various Supply Currents (For V_{DD} = 5 V, $V_{GG}2$ = 1.4 V)

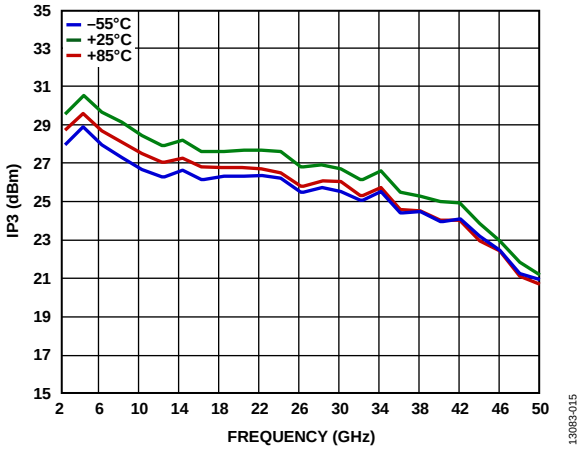

Figure 21. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} = 0 dBm/Tone

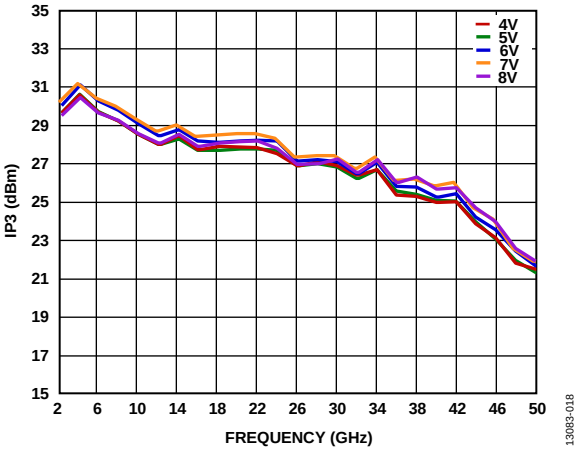

Figure 24. Output IP3 vs. Frequency for Various Supply Voltages, P_{OUT} = 0 dBm/Tone (For V_{DD} = 4 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 5 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 6 V, $V_{GG}2$ = 2 V; for V_{DD} = 7 V, $V_{GG}2$ = 3 V; for V_{DD} =8 V, $V_{GG}2$ = 3.6 V)

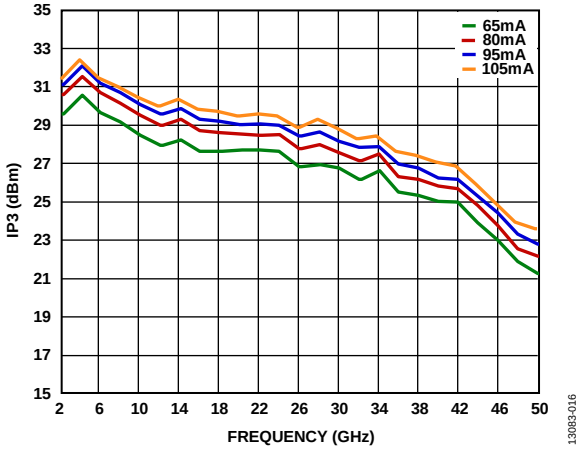

Figure 22. Output IP3 vs. Frequency for Various Supply Currents, P_{OUT} = 0 dBm/Tone (For V_{DD} = 5 V, $V_{GG}2$ = 1.4 V)

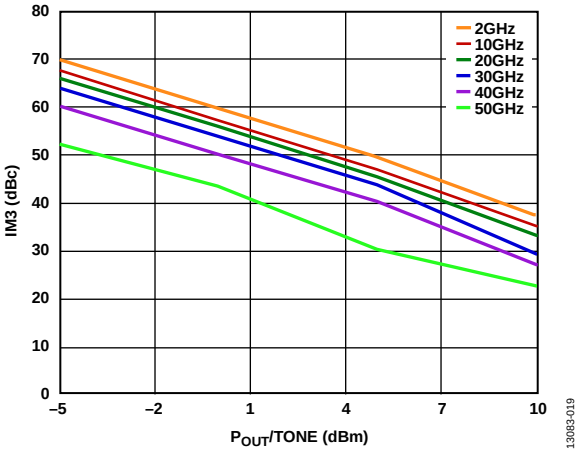

Figure 25. Output IM3 vs. P_{OUT}/Tone at V_{DD} = 4 V, $V_{GG}2$ = 1.4 V

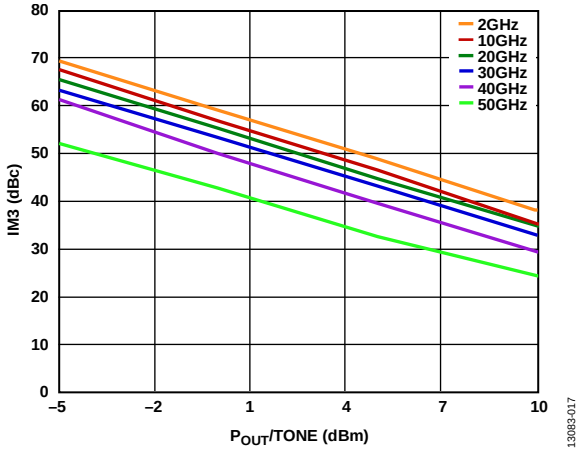

Figure 23. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 5 V, $V_{GG}2$ = 1.4 V

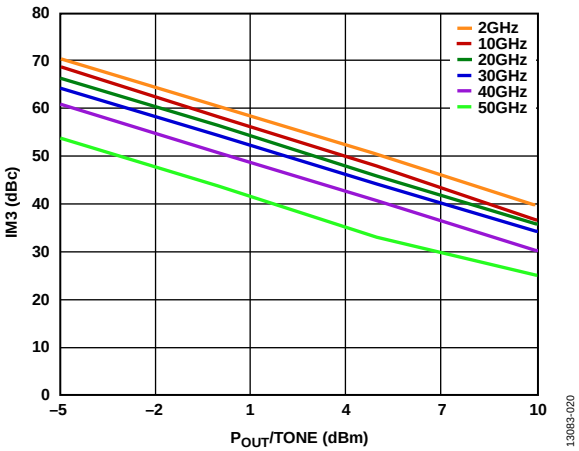

Figure 26. Output IM3 vs. P_{OUT}/Tone at V_{DD} = 6 V, $V_{GG}2$ = 2 V

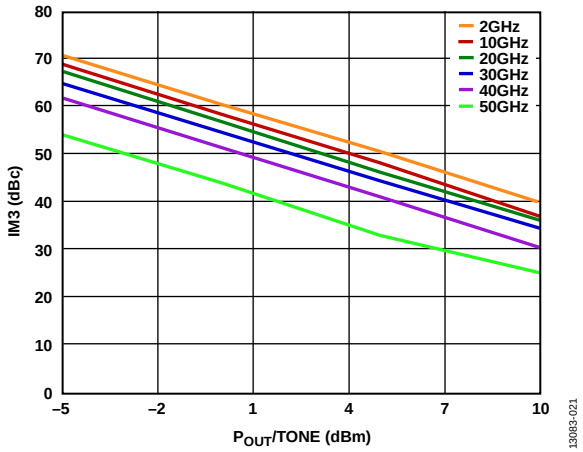

Figure 27. Output IM3 vs. P_{OUT}/Tone at V_{DD} = 7 V, $V_{GG}2$ = 3 V

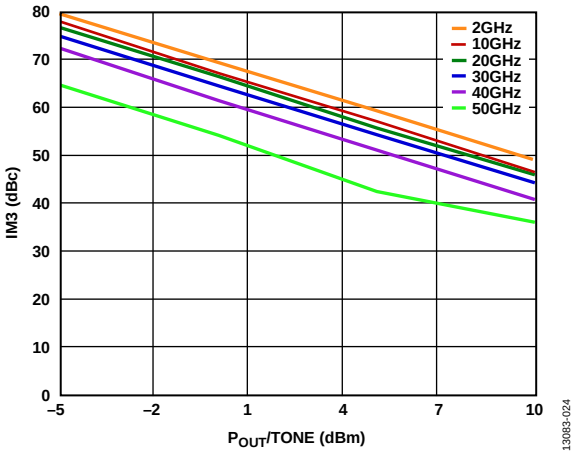

Figure 30. Output IM3 vs. P_{OUT}/Tone at V_{DD} = 8 V, $V_{GG}2$ = 3.6 V

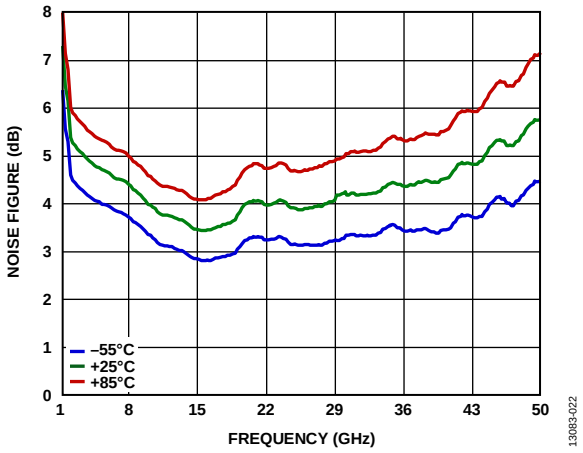

Figure 28. Noise Figure vs. Frequency at Various Temperatures

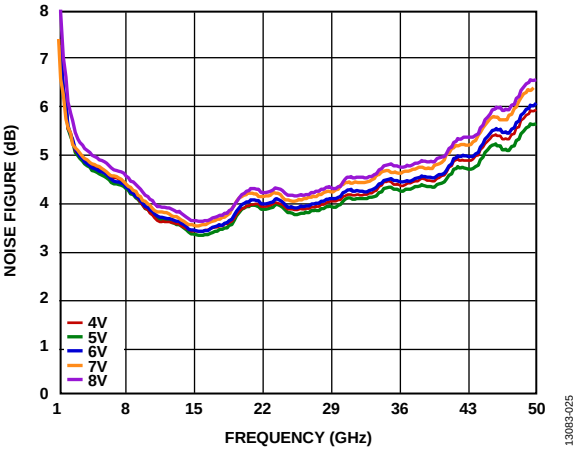

Figure 31. Noise Figure vs. Frequency at Various Supply Voltages (For V_{DD} = 4 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 5 V, $V_{GG}2$ = 1.4 V; for V_{DD} = 6 V, $V_{GG}2$ = 2 V; for V_{DD} = 7 V, $V_{GG}2$ = 3 V; for V_{DD} =8 V, $V_{GG}2$ = 3.6 V)

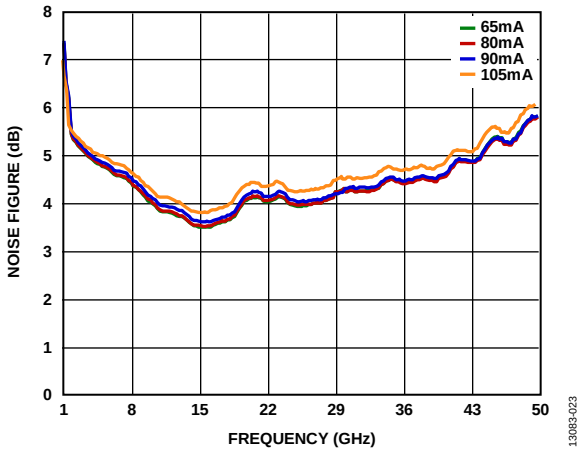

Figure 29. Noise Figure vs. Frequency at Various Supply Currents (For V_{DD} = 5 V, $V_{GG}2$ = 1.4 V)

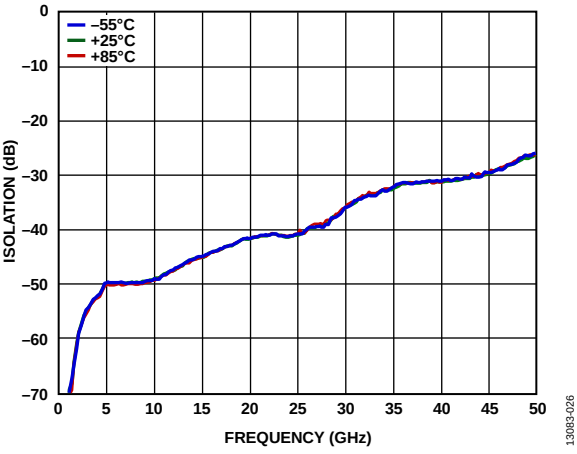

Figure 32. Reverse Isolation vs. Frequency for Various Temperatures (For V_{DD} = 5 V, $V_{GG}2$ = 1.4 V)

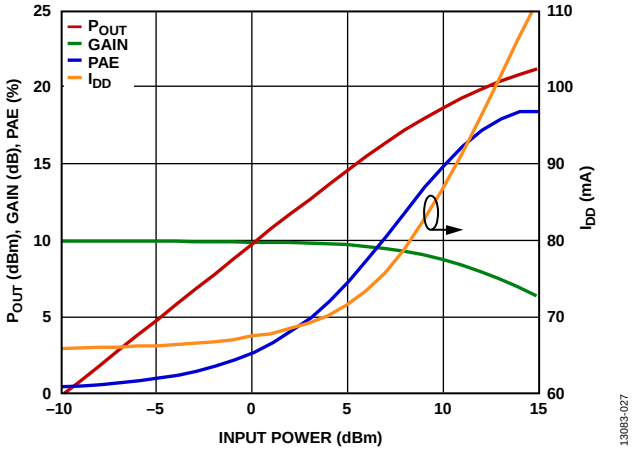

Figure 33. Power Compression at 24 GHz

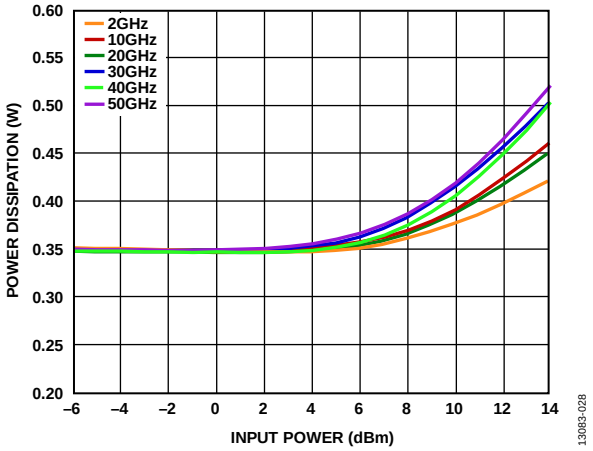

Figure 34. Power Dissipation at 85°C vs. Input Power at Various Frequencies

APPLICATIONS INFORMATION

The HMC1126 is a GaAs, pHEMT, MMIC, cascode distributed power amplifier.

The cascode distributed amplifier uses a fundamental cell of two FETs in series, source to drain. This fundamental cell then duplicates a number of times. The major benefit of this is an increase in the operation bandwidth. The basic schematic for a fundamental cell is given in Figure 35.

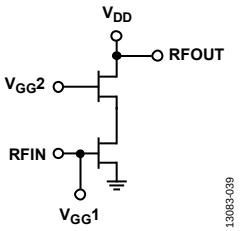

Figure 35. Fundamental Cell Schematic

The recommended bias sequence during power up is the following:

1. Connect GND.
2. Set $V_{GG}1$ to −2 V.
3. Set V_{DD} to 5 V.
4. Set $V_{GG}2$ to 1.4 V.
5. Increase $V_{GG}1$ to achieve a typical quiescent current (I_{DQ}) = 65 mA.
6. Apply the RF signal.

The recommended bias sequence during power down is the following:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −2 V to achieve I_{DQ} = 0 mA.
3. Decrease $V_{GG}2$ to 0 V.
4. Decrease V_{DD} to 0 V.
5. Increase $V_{GG}1$ to 0 V.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω, transmission lines on 0.127 mm (5 mil) thick alumina, thin film substrates are recommended for bringing the radio frequency to and from the chip (see Figure 36). When using 0.254 mm (10 mil) thick alumina, thin film substrates, raise the die 0.150 mm (6 mils) to ensure that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick, molybdenum (Mo) heat spreader (moly tab) which can then be attached to the ground plane (see Figure 36 and Figure 37).

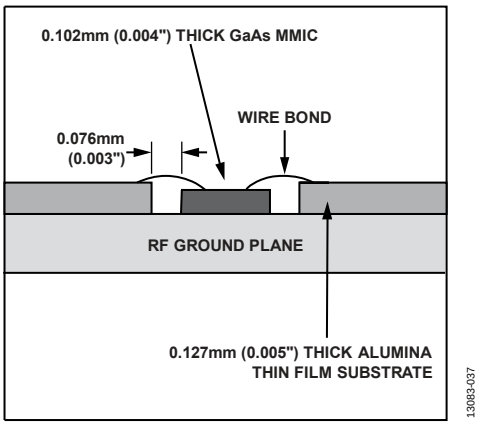

Figure 36. Die Without the Moly Tab

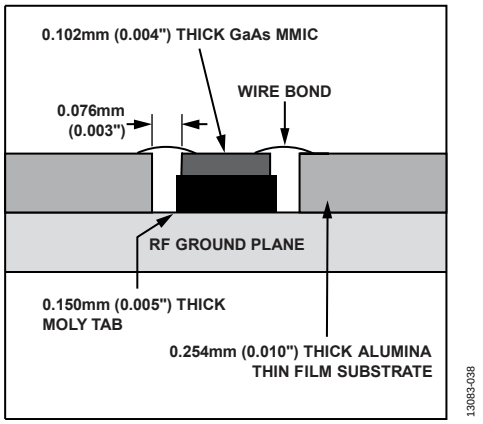

Figure 37. Die With the Moly Tab

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. Once the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pick up.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. Ensure that the mounting surface is clean and flat.

When eutectic die attached, an 80/20 gold tin preform is recommended with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90/10 nitrogen/hydrogen gas is applied, ensure that tool tip temperature is 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 seconds. For attachment, no more than 3 seconds of scrubbing is required.

When epoxy die attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with two 1 mil wires are recommended. Ensure that these bonds are thermosonically bonded with a force of 40 grams to 60 grams. DC bonds of an 0.001" (0.025 mm) diameter, thermosonically bonded, are recommended. Make ball bonds with a force of 40 grams to 50 grams and wedge bonds with a force of 18 grams to 22 grams. Make all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Make all bonds as short as possible, less than 12 mils (0.31 mm).

APPLICATION CIRCUIT

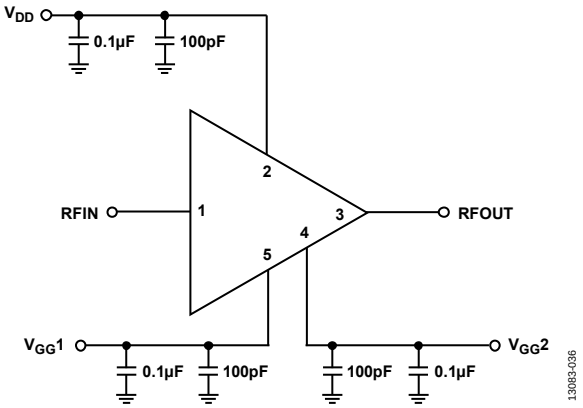

Figure 38. Application Circuit

ASSEMBLY DIAGRAM

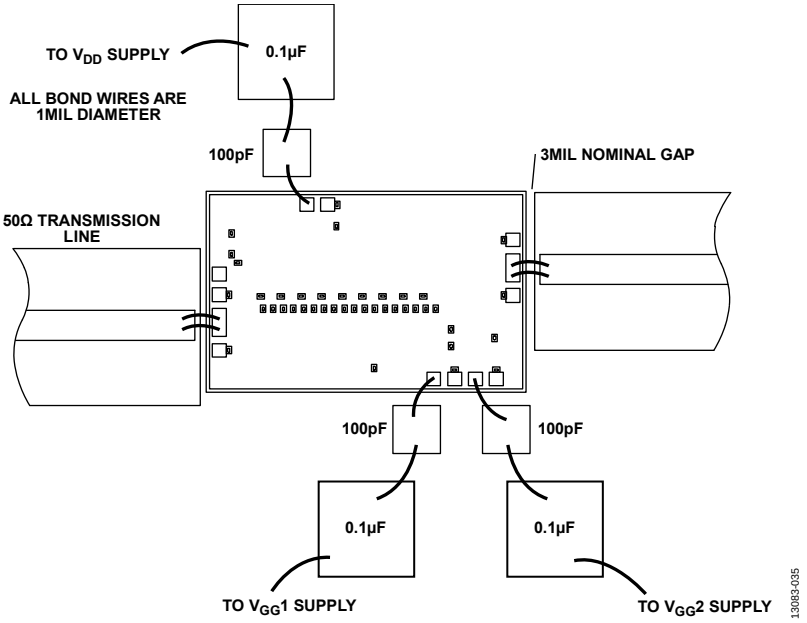

Figure 39. Assembly Diagram

OUTLINE DIMENSIONS

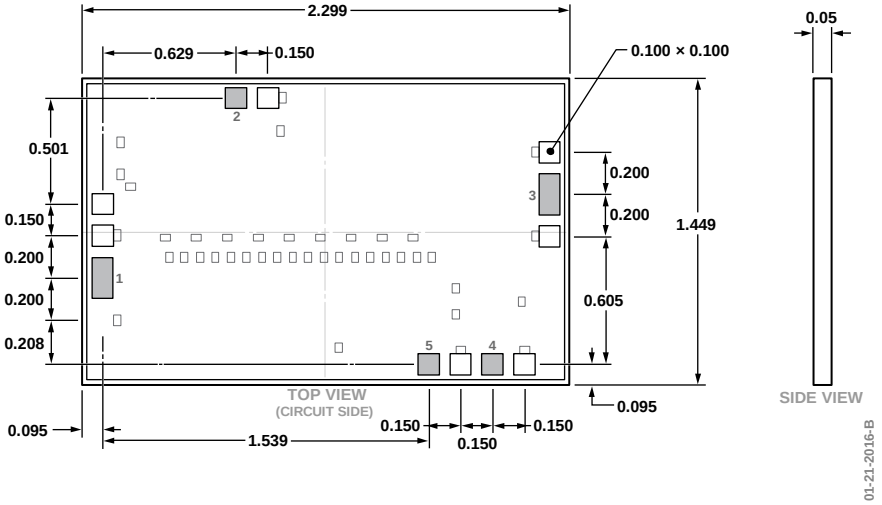

Figure 40. 5-Pad Bare Die [CHIP]
(C-5-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1,2]	Temperature Range	Package Description	Package Option
HMC1126	−55°C to +85°C	5-Pad Bare Die [CHIP]	C-5-4
HMC1126-SX	−55°C to +85°C	5-Pad Bare Die [CHIP]	C-5-4

[1] The HMC1126 is RoHS Compliant.
[2] The HMC1126-SX is a sample order of two devices.