

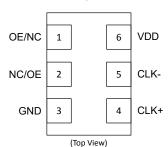
Ultra Series[™] Crystal Oscillator Si545 Data Sheet

Ultra Low Jitter Any-Frequency XO (80 fs), 0.2 to 1500 MHz

The Si545 Ultra Series[™] oscillator utilizes Silicon Laboratories' advanced 4th generation DSPLL® technology to provide an ultra-low litter, low phase noise clock at any output frequency. The device is factory-programmed to any frequency from 0.2 to 1500 MHz with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. The Si545 offers excellent reliability and frequency stability as well as guaranteed aging performance. On-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in industry-standard 3.2x5 mm and 5x7 mm footprints, the Si545 has a dramatically simplified supply chain that enables Silicon Labs to ship custom frequency samples 1-2 weeks after receipt of order. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si545 uses one simple crystal and a DSPLL IC-based approach to provide the desired output frequency. This process also guarantees 100% electrical testing of every device. The Si545 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location/polarity. Specific configurations are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators.

Pin Assignments





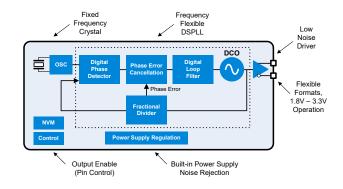
Pin #	Descriptions
1, 2	Selectable via ordering option OE = Output enable; NC = No connect
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output. Not used for CMOS.
6	VDD = Power supply

KEY FEATURES

- Available with any frequency from 0.2 MHz to 1500 MHz
- Ultra low jitter: 80 fs Typ RMS (12 kHz – 20 MHz)
- Excellent PSRR and supply noise immunity: –80 dBc Typ
- 7 ppm stability option (-40 to 85 °C)
- 3.3 V, 2.5 V and 1.8 V V_{DD} supply operation from the same part number
- LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- 3.2×5, 5x7 mm package footprints
- Samples available with 1-2 week lead times

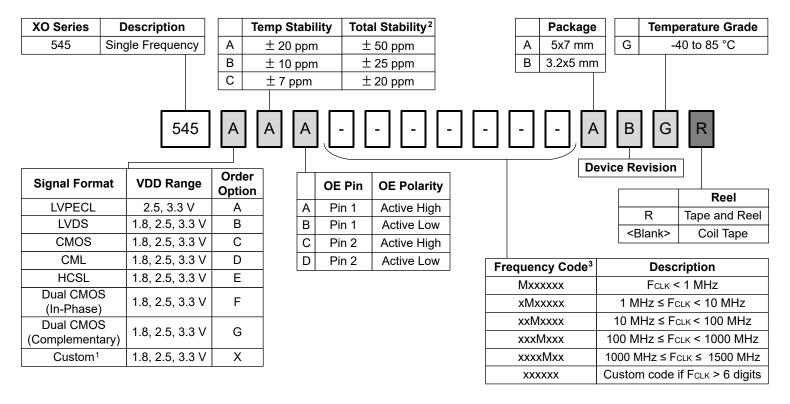
APPLICATIONS

- 100G/200G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Datacenter
- · Test and measurement
- · Clock and data recovery
- · FPGA/ASIC clocking



1. Ordering Guide

The Si545 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.



Notes:

- 1. Contact Silicon Labs for non-standard configurations.
- 2. Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
- 3. For example: 156.25 MHz = 156M250; 25 MHz = 25M0000. Create custom part numbers at www.silabs.com/oscillators.

1.1 Technical Support

Frequently Asked Questions (FAQ)	www.silabs.com/Si545-FAQ		
Oscillator Phase Noise Lookup Utility	www.silabs.com/oscillator-phase-noise-lookup		
Quality and Reliability	www.silabs.com/quality		
Development Kits	www.silabs.com/oscillator-tools		

2. Electrical Specifications

Table 2.1. Electrical Specifications

 V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition/Comment	Min	Тур	Max	Unit
Temperature Range	T _A		-40	_	85	°C
Frequency Range	F _{CLK}	LVPECL, LVDS, CML	0.2	_	1500	MHz
		HCSL	0.2	_	400	MHz
		CMOS, Dual CMOS	0.2	_	250	MHz
Supply Voltage	V _{DD}	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	I _{DD}	LVPECL (output enabled)	_	107	153	mA
		LVDS/CML (output enabled)	_	83	121	mA
		HCSL (output enabled)	_	86	126	mA
		CMOS (output enabled)	_	87	127	mA
		Dual CMOS (output enabled)	_	92	141	mA
		Tristate Hi-Z (output disabled)	_	73	112	mA
Temperature Stability		Frequency stability Grade A	-20	_	20	ppm
		Frequency stability Grade B	-10	_	10	ppm
		Frequency stability Grade C	-7	_	7	ppm
Total Stability ¹	F _{STAB}	Frequency stability Grade A	-50	_	50	ppm
		Frequency stability Grade B	-25	_	25	ppm
		Frequency stability Grade C	-20	_	20	ppm
Rise/Fall Time	T _R /T _F	LVPECL/LVDS/CML	_	_	350	ps
(20% to 80% V _{PP})		CMOS / Dual CMOS, (C _L = 5 pF)	_	0.5	1.5	ns
		HCSL, F _{CLK} >50 MHz	_	_	550	ps
Duty Cycle	D _C	All formats	45	_	55	%
Output Enable (OE) ²	V _{IH}		0.7 × V _{DD}	_	_	V
	V _{IL}		_	_	0.3 × V _{DD}	V
	T _D	Output Disable Time, F _{CLK} > 10 MHz	_	_	3	μs
	T _E	Output Enable Time, F _{CLK} > 10 MHz	_		20	μs
Powerup Time	tosc	Time from 0.9 × V _{DD} until output frequency (F _{CLK}) within spec	_	_	10	ms
LVPECL Output Option ³	V _{OC}	Mid-level	V _{DD} – 1.42	_	V _{DD} – 1.25	V
	Vo	Swing (diff)	1.1		1.9	V_{PP}

Parameter	Symbol	Test Condition/Comment	Min	Тур	Max	Unit
LVDS Output Option ⁴	V _{oc}	Mid-level (2.5 V, 3.3 V VDD)		1.20	1.275	V
		Mid-level (1.8 V VDD)	0.8	0.9	1.0	V
	Vo	Swing (diff)	0.5	0.7	0.9	V_{PP}
HCSL Output Option ⁵		Output voltage high	660	750	850	mV
	V _{OL}	Output voltage low	-150	0	150	mV
	V _C	Crossing voltage	250	350	550	mV
CML Output Option (AC-Coupled)	Vo	Swing (diff)	0.6	0.8	1.0	V _{PP}
CMOS Output Option	V _{OH}	I _{OH} = 8/6/4 mA for 3.3/2.5/1.8 V VDD	0.85 × V _{DD}	_	_	V
	V _{OL}	I _{OL} = 8/6/4 mA for 3.3/2.5/1.8 V VDD	_	_	0.15 × V _{DD}	V

Notes:

- 1. Total Stability includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 °C.
- 2. OE includes a 50 k Ω pull-up to VDD for OE active high. Includes a 50 k Ω pull-down to GND for OE active low.
- 3.50 Ω to $V_{DD}-2.0~V_{\cdot}$
- 4. R_{term} = 100 Ω (differential).
- $5.50\;\Omega$ to GND.

Table 2.2. Clock Output Phase Jitter and PSRR

 V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 °C

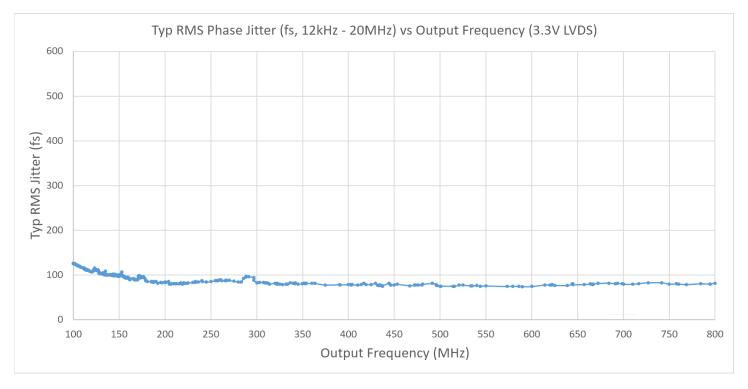
Parameter	Symbol	mbol Test Condition/Comment		Тур	Max	Unit	
Phase Jitter (RMS, 12kHz - 20MHz) ¹	фЈ	F _{CLK} ≥ 200 MHz	_	80	110	fs	
3.2 x 5 mm, All Differential Formats		100 MHz ≤ F _{CLK} < 200 MHz	_	100	150	fs	
		LVPECL @ 156.25 MHz	_	90	125	fs	
Phase Jitter (RMS, 12kHz - 20MHz) ¹		F _{CLK} ≥ 200 MHz	_	80	130	fs	
5 x 7 mm, All Differential Formats		100 MHz ≤ F _{CLK} < 200 MHz	_	100	150	fs	
		LVPECL @ 156.25 MHz	_	90	125	fs	
Phase Jitter (RMS, 12kHz - 20MHz) ¹ CMOS / Dual CMOS Formats	фЈ	10 MHz ≤ F _{CLK} ≤ 250 MHz	_	200	_	fs	
Spurs Induced by External Power Supply	PSRR	100 kHz sine wave	_	-83	_		
Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output		200 kHz sine wave	_	-83	_	dBo	
		500 kHz sine wave	_	-82	_	- dBc	
		1 MHz sine wave	_	-85	_		

Note:

1. Guaranteed by characterization. Jitter inclusive of any spurs.

Table 2.3. 3.2 x 5 mm Clock Output Phase Noise (Typical)

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	-106	-102	-92	
1 kHz	-133	–129	–119	
10 kHz	-140	-138	-127	
100 kHz	–145	-142	-132	dBc/Hz
1 MHz	–152	–150	-139	
10 MHz	-160	-160	-154	
20 MHz	-161	-161	–155	
Offset Frequency (f)	156.25 MHz LVPECL	200 MHz LVPECL	644.53125 MHz LVPECL	Unit
100 Hz	-103	-104	– 91	
1 kHz	-130	-128	–118	
10 kHz	-140	-138	–127	
100 kHz	–145	-142	-132	dBc/Hz
1 MHz	–152	–150	-140	
10 MHz	-162	-162	–155	
20 MHz	-163	-163	-156	



Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.

Figure 2.1. Phase Jitter vs. Output Frequency

Table 2.4. Environmental Compliance and Package Information

MIL-STD-883, Method 2002 MIL-STD-883, Method 2007
MIL-STD-883, Method 2007
MIL-STD-883, Method 2003
MIL-STD-883, Method 1014
MIL-STD-883, Method 2036
1
Gold over Nickel
_

Note:

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/quality/Pages/RoHSInformation.aspx.

Table 2.5. Thermal Conditions

Package	Parameter	Symbol	Test Condition	Value	Unit
	Thermal Resistance Junction to Ambient	ΘЈΑ	Still Air, 85 °C	80.3	°C/W
3.2 × 5 mm 6-pin CLCC	Thermal Resistance Junction to Board	Θ _{JB}	Still Air, 85 °C	50.8	°C/W
	Max Junction Temperature	TJ	Still Air, 85 °C	125	°C
5 × 7 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	ОЈА	Still Air, 85 °C	68.4	°C/W
	Thermal Resistance Junction to Board	Θ _{JB}	Still Air, 85 °C	52.9	°C/W
	Max Junction Temperature	TJ	Still Air, 85 °C	125	°C

Table 2.6. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	T _{AMAX}	95	°C
Storage Temperature	T _S	-55 to 125	°C
Supply Voltage	V_{DD}	-0.5 to 3.8	°C
Input Voltage	V _{IN}	-0.5 to V _{DD} + 0.3	V
ESD HBM (JESD22-A114)	НВМ	2.0	kV
Solder Temperature ²	T _{PEAK}	260	°C
Solder Time at T _{PEAK} ²	T _P	20–40	sec

Notes:

- 1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2. The device is compliant with JEDEC J-STD-020.

3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single Si545 device.

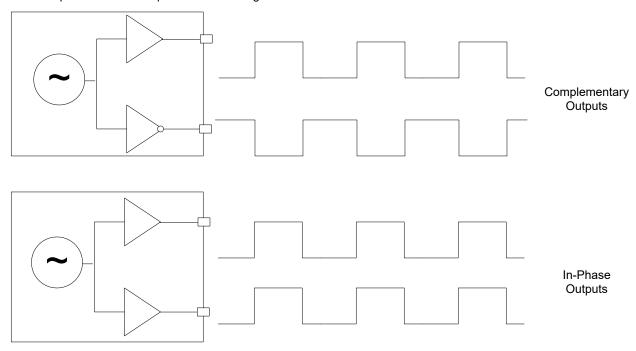


Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

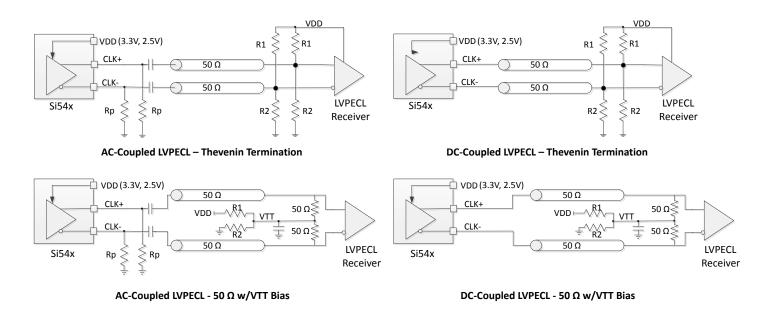


Figure 4.1. LVPECL Output Terminations

AC Coupled LVPECL Termination Resistor Values					DC Coupled LVPECL mination Resistor Va	
VDD	R1	R2	Rp	VDD	R1	R2
3.3 V	127 Ω	82.5 Ω	130 Ω	3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω	90 Ω	2.5 V	250 Ω	62.5 Ω

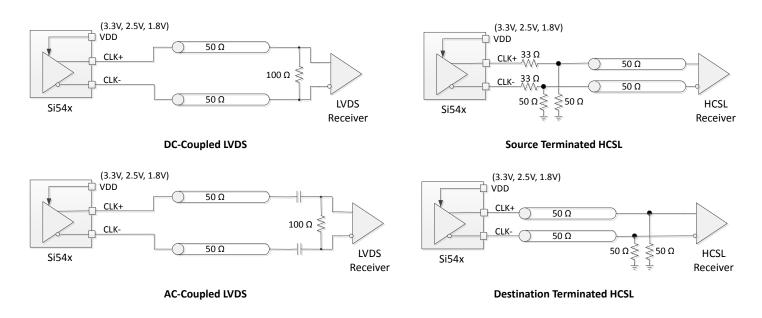


Figure 4.2. LVDS and HCSL Output Terminations

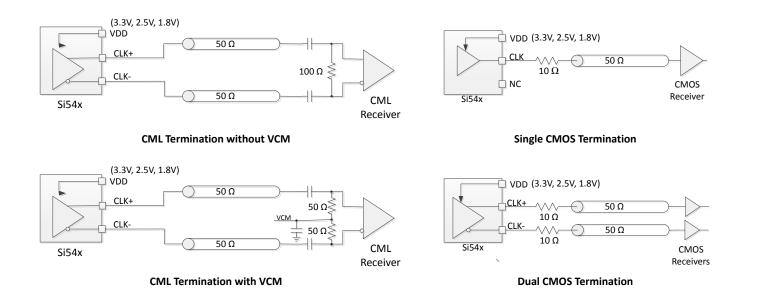


Figure 4.3. CML and CMOS Output Terminations

5. Package Outline

5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si545. The table below lists the values for the dimensions shown in the illustration.

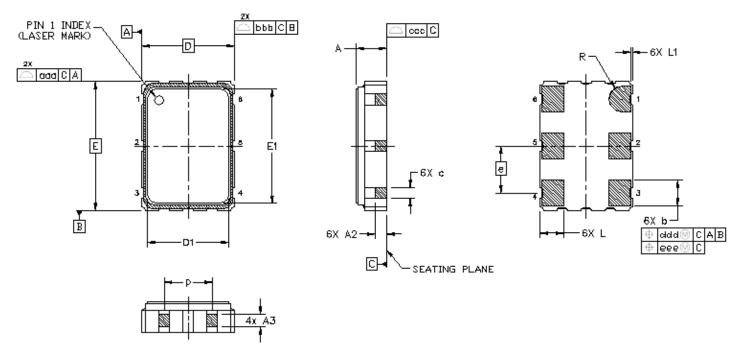


Figure 5.1. Si545 (5×7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max	
А	1.13	1.28	1.43	L	1.17 1.27 1.37			
A2	0.50	0.55	0.60	L1	0.05	0.05 0.10 0.15		
A3	0.50	0.55	0.60	р	1.70 — 1.9			
b	1.30	1.40	1.50	R	0.70 REF			
С	0.50	0.60	0.70	aaa	0.15			
D	5.00 BSC			bbb	b 0.15			
D1	4.30	4.40	4.50	ccc		0.08		
е		2.54 BSC		ddd		0.10		
E		7.00 BSC		eee		0.05		
E1	6.10	6.20	6.30					
		•						

Notes:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si545. The table below lists the values for the dimensions shown in the illustration.

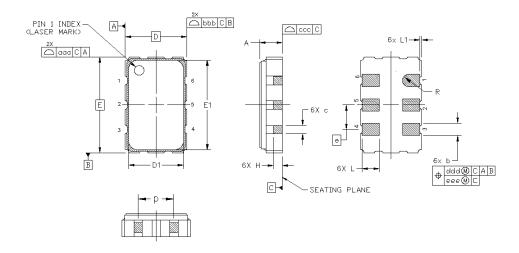


Figure 5.2. Si545 (3.2×5 mm) Outline Diagram

Table 5.2. Package Diagram Dimensions (mm)

Dimension	Min Nom Max						
A	1.06	1.17	1.33				
b	0.54	0.64	0.74				
С	0.35	0.35 0.45 0.56					
D		3.20 BSC					
D1	2.55 2.60 2.65						
е		1.27 BSC					
E	5.00 BSC						
E1	4.35 4.40 4.45						
Н	0.45	0.65					
L	0.80	0.90	1.00				
L1	0.05	0.10	0.15				
р	1.36	1.46	1.56				
R		0.32 REF					
aaa		0.15					
bbb		0.15					
ccc		0.08					
ddd		0.10					
eee		0.05					

Notes:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6. PCB Land Pattern

6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si545. The table below lists the values for the dimensions shown in the illustration.

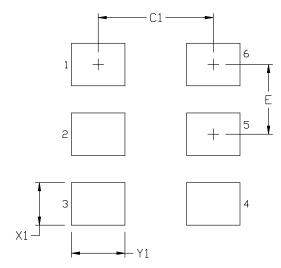


Figure 6.1. Si545 (5×7 mm) PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.
- 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

- 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si545. The table below lists the values for the dimensions shown in the illustration.

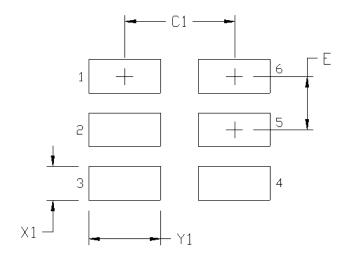


Figure 6.2. Si545 (3.2×5 mm) PCB Land Pattern

Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.
- 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

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Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Top Marking

The figure below illustrates the mark specification for the Si545. The table below lists the line information.

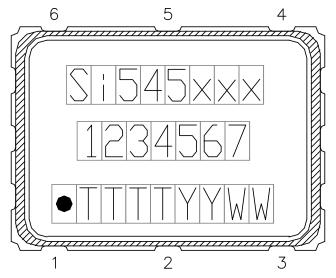


Figure 7.1. Mark Specification

Table 7.1. Si545 Top Mark Description

Line	Position	Description
1	1–8	"Si545", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si545AAA)
2	1–7	Frequency Code (e.g. 100M000 or 6-digit custom code as described in the Ordering Guide)
3	Trace Code	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (B)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

8. Revision History

Revision 1.0

July, 2018

• Added 20 ppm total stability option.

Revision 0.75

March, 2018

• Added 25 ppm total stability option.

Revision 0.71

December 11, 2017

• Added 5x7 package and land pattern.

Revision 0.7

June 27, 2017

· Initial release.









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