

Freescale Semiconductor Data Sheet: Technical Data

Document Number: MC9S08SC4

Rev. 4, 6/2010



MC9S08SC4 8-Bit Microcontroller Data Sheet

MC9S08SC4



948F-01

8-Bit HCS08 Central Processor Unit (CPU)

- Up to 40 MHz HCS08 CPU (central processor unit); up to 20 MHz bus frequency
- HC08 instruction set with added BGND instruction

On-Chip Memory

- 4 KB of FLASH with read/program/erase over full operating voltage and temperature
- 256 bytes of Random-access memory (RAM)

Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode

Clock Source Options

- Oscillator (XOSC) Loop-control Pierce oscillator; Crystal or ceramic resonator range of 32 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2 % resolution and 2.0 % deviation over temperature and voltage; supports bus frequencies from 2 MHz to 20 MHz.

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect
- Reset on loss of clock

Development Support

Single-wire background debug interface

during in-circuit debugging

Breakpoint capability to allow single breakpoint setting

Peripherals

- **SCI** Serial Communication Interface
 - Full-duplex non-return to zero (NRZ)
 - LIN master extended break generation
 - LIN slave extended break detection
 - Wake-up on active edge
- **TPMx** Two 2-channel Timer/PWM modules (TPM1 and TPM2)
 - 16-bit modulus or up/down counters
 - Input capture, output compare, buffered edge-aligned or center-aligned PWM
- **ADC** Analog to Digital Converter
 - 8-channel, 10-bit resolution
 - 2.5 μs conversion time
 - Automatic compare function
 - Temperature sensor
 - Internal bandgap reference channel

Input/Output

- 12 general purpose I/O pins (GPIOs)
- 8 interrupt pins with selectable polarity
- Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.

Package Options

16-TSSOP

Operating Parameters

- 4.5-5.5 V operation
- C,V, M temperature ranges available, covering -40 125 °C operation

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

© Freescale Semiconductor, Inc., 2009-2010. All rights reserved.





Table of Contents

Chapter 1	3.9 Internal Clock Source (ICS) Characteristics	18
Device Overview	3.10 ADC Characteristics	19
1.1 MCU Block Diagram	3.11 AC Characteristics	21
Chapter 2	3.11.1 Control Timing	21
Pins and Connections5	3.11.2 TPM Module Timing	22
2.1 Device Pin Assignment	3.12 Flash Specifications	23
Chapter 3	3.13 EMC Performance	24
Electrical Characteristics	3.13.1 Radiated Emissions	24
3.1 Introduction	Chapter 4	
3.2 Parameter Classification	Ordering Information and Mechanical Drawings	25
3.3 Absolute Maximum Ratings	4.1 Ordering Information	25
3.4 Thermal Characteristics	4.1.1 Device Numbering Scheme	25
3.5 ESD Protection and Latch-Up Immunity	4.2 Package Information	25
3.6 DC Characteristics	4.3 Mechanical Drawings	25
3.7 Supply Current Characteristics	Chapter 5	
3.8 External Oscillator (XOSC) Characteristics	Revision History	29



Chapter 1 Device Overview

The MC9S08SC4 is a member of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). The MC9S08SC4 uses the enhanced HCS08 core.

1.1 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08SC4 MCU.

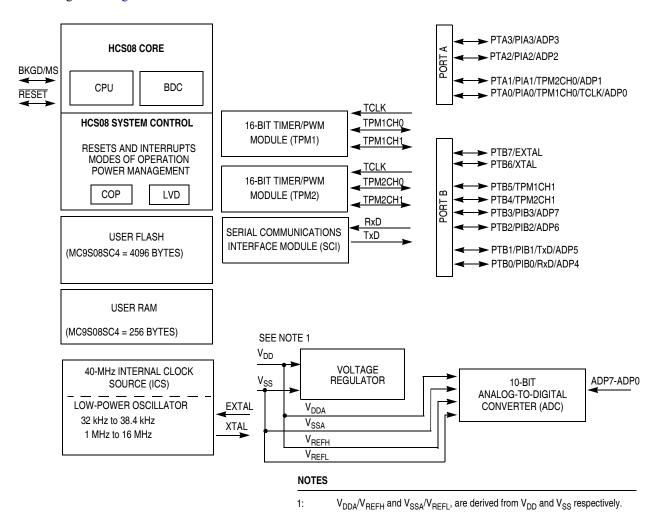


Figure 1-1. MC9S08SC4 Block Diagram



Chapter 1 Device Overview



Chapter 2 Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

The following figure shows the pin assignments for the MC9S08SC4 device.

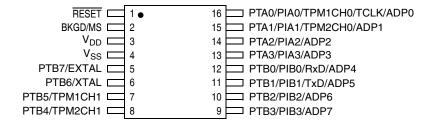


Table 2-1. Pin Function Priority

Pin	_		Priority		
Number	Lowest				Highest
16-pin	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1					RESET
2				BKGD	MS
3					V_{DD}
4					V _{SS}
5	PTB7		EXTAL		
6	PTB6		XTAL		
7	PTB5	TPM1CH1			
8	PTB4	TPM2CH1			
9	PTB3	PIB3			ADP7
10	PTB2	PIB2			ADP6
11	PTB1	PIB1	TxD		ADP5



Chapter 2 Pins and Connections

Table 2-1. Pin Function Priority (continued)

Pin	_		Priority		
Number	Lowest				Highest
16-pin	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
12	PTB0	PIB0	RxD		ADP4
13	PTA3	PIA3			ADP3
14	PTA2	PIA2			ADP2
15	PTA1	PIA1	TPM2CH0		ADP1
16	PTA0	PIA0	TPM1CH0	TCLK	ADP0



3.1 Introduction

This section contains electrical and timing specifications for the MC9S08SC4 Series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3-1. Parameter Classifications

Р	Those parameters are guaranteed during production testing on each individual device.
С	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
Т	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.



Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to +5.8	V
Maximum current into V _{DD}	I _{DD}	120	mA
Digital input voltage	V _{In}	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I _D	± 25	mA
Storage temperature range	T _{stg}	-55 to 150	°C

Table 3-2. Absolute Maximum Ratings

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

С Num Rating **Symbol** Value Unit 1 Operating temperature range (packaged) T_I to T_H С -40 to 85 T_A °C ٧ -40 to 105 Μ -40 to 125 Maximum junction temperature 2 D С T_{JM} 95 ٥С ٧ 115 M 135 Thermal resistance 1,2 Single-layer board θ_{JA} 3 D 16-pin TSSOP 130 °C/W Thermal resistance^{1,2} Four-layer board 4 D 16-pin TSSOP 87 °C/W θ_{JA}

Table 3-3. Thermal Characteristics

MC9S08SC4 MCU Series Data Sheet, Rev. 4

Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

 $^{^2}$ $\,$ All functional non-supply pins are internally clamped to $\rm V_{SS}$ and $\rm V_{DD}$

Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).



- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- ² Junction to Ambient Natural Convection

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_{.1} = T_{\Delta} + (P_{D} \times \theta_{.1\Delta})$$
 Eqn. 3-1

where:

 $T_A = Ambient temperature, °C$

 θ_{IA} = Package thermal resistance, junction-to-ambient, °C/W

$$P_D = P_{int} + P_{I/O}$$

 $P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

 $P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_A + 273^{\circ}C)$$
 Eqn. 3-2

Solving Equation 3-1 and Equation 3-2 for K gives:

$$K = P_D \times (T_A + 273^{\circ}C) + \theta_{JA} \times (P_D)^2$$
 Eqn. 3-3

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 3-1 and Equation 3-2 iteratively for any value of T_A

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Model Description **Symbol** Value Unit Human Series resistance R1 1500 Ω Body Storage capacitance С 100 pF Number of pulses per pin 3 ٧ Minimum input voltage limit -2.5Latch-up Maximum input voltage limit 7.5 ٧

Table 3-4. ESD and Latch-up Test Conditions

MC9S08SC4 MCU Series Data Sheet, Rev. 4



Table 3-5. ESD and Latch-Up Protection Characteristics

No.	Rating ¹	Symbol	Min	Max	Unit
1	1 Human body model (HBM)		± 2000	_	V
2	2 Charge device model (CDM)		± 500	_	V
3	Latch-up current at T _A = 125°C	I _{LAT}	± 100	_	mA

Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 3-6. DC Characteristics

Num	С	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit	
4	_	Operating voltage	V_{DD}	_	4.5	_	5.5	V	
	С	All I/O pins,		5 V, I _{Load} = -4 mA	V _{DD} – 1.5	_	_		
5	Р	Output high low-drive strength	V _{OH}	5 V, I _{Load} = –2 mA	V _{DD} – 0.8	_	_	V	
	С	voltage All I/O pins,		5 V, I _{Load} = -20 mA	V _{DD} – 1.5	_	_		
	Р	high-drive strength		5 V, $I_{Load} = -10 \text{ mA}$	V _{DD} – 0.8	_	_		
6	С	Output high Max total I _{OH} for current all ports		V _{OUT} < V _{DD}	0	_	-100	mA	
	С	All I/O pins		5 V, I _{Load} = 4 mA	_	_	1.5		
7	Р	Output low low-drive strength	V _{OL}	5 V, I _{Load} = 2 mA	_	_	0.8		
'	С	voltage All I/O pins		5 V, I _{Load} = 20 mA	_	_	1.5	V	
	Р	high-drive strength		5 V, I _{Load} = 10 mA	_	_	0.8		
8	С	Output low Max total I _{OL} for all ports current	I _{OLT}	V _{OUT} > V _{SS}	0	_	100	mA	
9	Р	Input high voltage; all digital inputs	V _{IH}	5V	0.65 x V _{DD}	_	_	V	
10	Р	Input low voltage; all digital inputs	V _{IL}	5V	_	_	0.35 x V _{DD}	V	
11	С	Input hysteresis	V _{hys}	_	0.06 x V _{DD}	_	_	V	
12	Р	Input leakage current (per pin)	I _{In}	$V_{In} = V_{DD}$ or V_{SS}	_	0.1	1	μΑ	
	Р	Hi-Z (off-state) leakage current (per pin)							
13		input/output port pins	$ I_{OZ} $	$V_{In} = V_{DD}$ or V_{SS} ,	_	0.1	1	μΑ	
		PTB6/XTAL,RESET		$V_{In} = V_{DD}$ or V_{SS}	_	0.2	2	μΑ	
		Pull-up or Pull-down ² resistors; when enabled							
14	Р	I/O pins	R _{PU} ,R _{PD}	_	17	37	52	kΩ	
	С	RESET ³	R _{PU}		17	37	52	kΩ	

11



Table 3-6. DC Characteristics (continued)

Num	С	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit
	D	DC injection current ^{4, 5, 6, 7}						
		Single pin limit		$V_{IN} > V_{DD}$	0	_	2	mA
15			I _{IC}	$V_{IN} < V_{SS}$	0	_	-0.2	mA
		Total MCU limit, includes		$V_{IN} > V_{DD}$	0	_	25	mA
		sum of all stressed pins		$V_{IN} < V_{SS}$	0	_	- 5	mA
16	D	Input Capacitance, all pins	C _{In}	_	_	_	8	pF
17	D	RAM retention voltage	V_{RAM}	_	_	0.6	1.0	V
18	D	POR re-arm voltage ⁸	V _{POR}	_	0.9	1.4	2.0	V
19	D	POR re-arm time ⁹	t _{POR}	_	10	_	_	μS
20	Р	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V _{LVD1}	_	3.85 3.95	4.0 4.1	4.15 4.25	V
21	Р	Low-voltage warning threshold — high range 1 V _{DD} falling V _{DD} rising	V _{LVW3}	_	4.45 4.55	4.6 4.7	4.75 4.85	V
22	Р	Low-voltage warning threshold — high range 0 V _{DD} falling V _{DD} rising	V _{LVW2}	_	4.15 4.25	4.3 4.4	4.45 4.55	V
23	Т	Low-voltage inhibit reset/recover hysteresis	V_{hys}	_	_	100	_	mV
24	Р	Bandgap Voltage Reference ¹⁰	V_{BG}	_	1.17	1.20	1.22	V

¹ Typical values are measured at 25°C. Characterized, not tested.

When a pin interrupt is configured to detect rising edges, pull-down resistors are used in place of pull-up resistors.

³ The specified resistor value is the actual value internal to the device. The pull-up value may measure higher when measured externally on the pin.

Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

 $^{^{5}}$ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁶ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁷ The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD} . Do not drive this pin above V_{DD} .

⁸ Maximum is highest voltage that POR will occur.

⁹ Simulated, not tested

 $^{^{10}}$ Factory trimmed at $V_{DD} = 5.0 \text{ V}$, Temp = 25°C



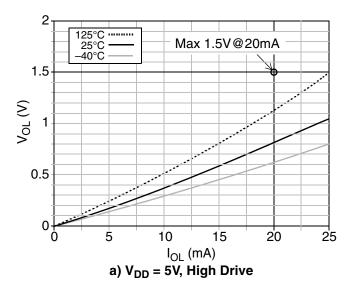


Figure 3-1. Typical V_{OL} vs I_{OL} , High Drive Strength

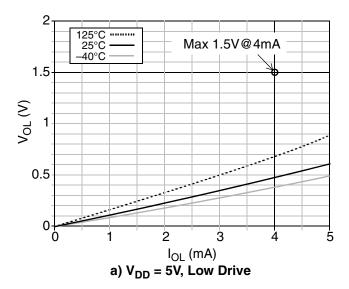


Figure 3-2. Typical $\rm V_{OL}$ vs $\rm I_{OL},$ Low Drive Strength



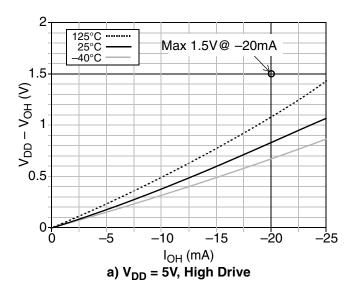


Figure 3-3. Typical $V_{DD} - V_{OH}$ vs I_{OH} , High Drive Strength

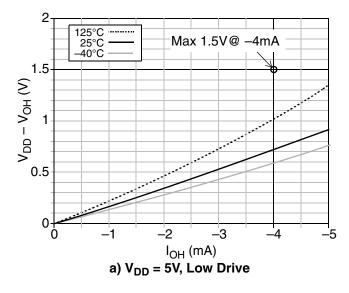


Figure 3-4. Typical $V_{DD} - V_{OH}$ vs I_{OH} , Low Drive Strength

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 3-7. Supply Current Characteristics

Num	С	Р	Parameter		V _{DD} (V)	Typ ¹	Max ²	Unit
1	С	Run supply current ³ measured at (CPU clock = 4 MHz, f _{Bus} = 2 MHz)		RI _{DD}	5	1.9	2.4	mA
2	Р	Run supply curren (CPU clock = 16	nt ³ measured at 6 MHz, f _{Bus} = 8 MHz)	RI _{DD}	5	4.6	5.6	mA
3	С	Run supply curren (CPU clock = 32	nt ⁴ measured at 2 MHz, f _{Bus} = 16 MHz)	RI _{DD}	5	7.8	8.9	mA
	С		-40 °C (C & M suffix)			0.71	_	
	Р	Stop3 mode	25 °C (All parts)			0.93	_	
4	C ⁵	supply current	85 °C (C suffix only)	S3I _{DD}	5	4	11	μΑ
	C ⁵		105 °C (V suffix only)			9	30	
	P ⁵		125 °C (M suffix only)			28	60	
5	С		-40 °C (C & M suffix)			0.70	_	
	Р	Stop2 mode	25 °C (All parts)			0.89	_	
	C ⁵	supply current	85 °C (C suffix only)	S2I _{DD}	5	3	8	μΑ
	C ⁵		105 °C (V suffix only)			6	22	
	P ⁵		125 °C (M suffix only)			17	41	1
6	С	LVD adder to stop3 (LVDE = LVDSE = 1)		S3I _{DDLVD}	5	110	165	μА
7	С	Adder to stop3 for (EREFSTEN =1)	oscillator enabled ⁶	S3I _{DDOSC}	5	5	8	μА

Typical values are based on characterization data at 25 °C. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

² Max values in this column apply for the full operating temperature range of the device unless otherwise noted.

³ All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins.

⁴ All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins.

⁵ Stop currents are tested in production for 25 °C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

Values given under the following conditions: low range operation (RANGE = 0) with a 32.768 kHz crystal and low power mode (HGO = 0).

15



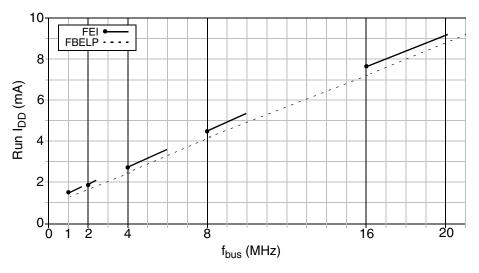
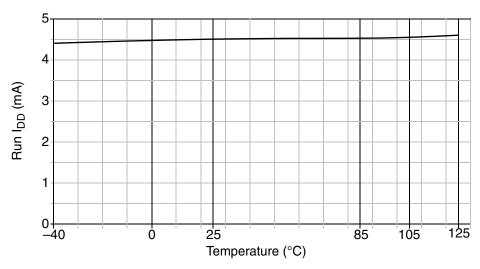


Figure 3-5. Typical Run I_{DD} vs. Bus Frequency ($V_{DD} = 5V$)



Note: ICS is configured to FEI.

Figure 3-6. Typical Run I_{DD} vs. Temperature (V_{DD} = 5V; f_{bus} = 8MHz)

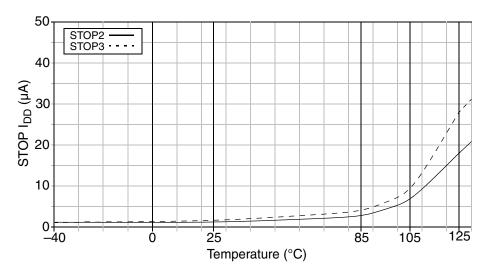


Figure 3-7. Typical Stop I_{DD} vs. Temperature ($V_{DD} = 5V$)

3.8 External Oscillator (XOSC) Characteristics

NOTE

The MC9S08SC4 series supports a narrower low frequency external reference range than the standard ICS specification. All references to range "31.25 kHz to 39.0625 kHz" in this section should be limited to " 32.0 kHz to 38.4 kHz".



Table 3-8. Oscillator Electrical Specifications (Temperature Range = −40 to 125°C Ambient)

Num	С	Rating	Symbol	Min	Typ ¹	Max	Unit
		Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f _{lo}	32	_	38.4	kHz
1	С	High range (RANGE = 1) FEE or FBE mode ²	f _{hi}	1	_	5	MHz
		High range (RANGE = 1, HGO = 1) FBELP mode	f _{hi-hgo}	1	_	16	MHz
		High range (RANGE = 1, HGO = 0) FBELP mode	f _{hi-lp}	1	_	8	MHz
2	_	Load capacitors	C _{1,} C ₂			r resonato	
		Feedback resistor					
3	_	Low range (32 kHz to 100 kHz)	R_{F}	_	10	_	$M\Omega$
		High range (1 MHz to 16 MHz)			1	1	
		Series resistor					
		Low range, low gain (RANGE = 0, HGO = 0)		_	0	_	
		Low range, high gain (RANGE = 0, HGO = 1)		_	100	_	
4	_	High range, low gain (RANGE = 1, HGO = 0)	R _S		0		kΩ
7		High range, high gain (RANGE = 1, HGO = 1)	5				NSZ
		≥ 8 MHz		_	0	0	
		4 MHz		_	0	10	
		1 MHz			0	20	
		Crystal start-up time ³					
		Low range, low gain (RANGE = 0, HGO = 0)	t CSTL-LP	_	200	_	
5	Т	Low range, high gain (RANGE = 0, HGO = 1)	t CSTL-HGO	_	400	_	ms
		High range, low gain (RANGE = 1, HGO = 0) ⁴	t CSTH-LP	_	5	_	
		High range, high gain (RANGE = 1, HGO = 1) ⁴	t CSTH-HGO	_	15	_	
		Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					
6	Т	FEE or FBE mode ²	f _{extal}	0.03125	_	5	MHz
		FBELP mode		0	_	40	MHz

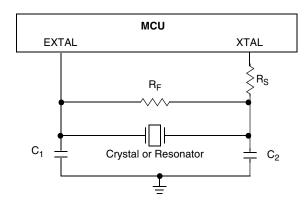
¹ Typical data was characterized at 5.0 V, 25°C or is recommended value.

 $^{^2}$ The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.

⁴ 4 MHz crystal.





3.9 Internal Clock Source (ICS) Characteristics

Table 3-9. ICS Frequency Specifications (Temperature Range = -40 to 125°C Ambient)

Num	С	Rating	Symbol	Min	Typical	Max	Unit
1	Р	Internal reference frequency - factory trimmed at V _{DD} = 5 V and temperature = 25°C	f _{int_ft}	_	31.25	_	kHz
2	Т	Internal reference frequency - untrimmed ¹	f _{int_ut}	25	36	41.66	kHz
3	Р	Internal reference frequency - user trimmed	f _{int_t}	31.25	_	39.0625	kHz
4	T	Internal reference startup time	t _{irefst}	_	_	6	μS
5	_	DCO output frequency range - untrimmed ¹ value provided for reference assumes: fdco_ut = 1024 x f _{int_ut}	f _{dco_ut}	25.6	36.86	42.66	MHz
6	D	DCO output frequency range - trimmed	f _{dco_t}	32	_	40	MHz
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	Δf _{dco_res_t}	_	± 0.1	± 0.2	%f _{dco}
8	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	Δf _{dco_res_t}	_	± 0.2	± 0.4	%f _{dco}
9	D	Total deviation from actual trimmed DCO output frequency over voltage and temperature	Δf _{dco_t}	_	+ 0.5 – 1.0	± 2.0	%f _{dco}
10	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	_	± 0.5	± 1	%f _{dco}
11	D	FLL acquisition time ²	t _{acquire}	_	_	1	ms
12	D	DCO output clock long term jitter (over 2mS interval) 3	C _{Jitter}	_	0.02	0.2	%f _{dco}

¹ TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

MC9S08SC4 MCU Series Data Sheet, Rev. 4

This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.



3.10 ADC Characteristics

Table 3-10. ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V _{DDA} ²	2.7	_	5.5	V	_
Input Voltage	_	V _{ADIN}	V _{REFL} ²	_	V _{REFH} ²	V	_
Input Capacitance	_	C _{ADIN}	_	4.5	5.5	pF	_
Input Resistance	_	R _{ADIN}	_	3	5	kΩ	_
Analog Source Resistance	10 bit mode f _{ADCK} > 4MHz f _{ADCK} < 4MHz	R _{AS}	_	_ _	5 10	kΩ	External to MCU
	8 bit mode (all valid f _{ADCK})		_	_	10		
ADC	High Speed (ADLPC=0)	f _{ADCK}	0.4	_	8.0	MHz	_
Conversion Clock Frequency	Low Power (ADLPC=1)		0.4	_	4.0		

Typical values assume VDDA = 5.0 V, Temp = 25°C, fADCK=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

 $^{^2~\}rm V_{DDA}/\rm V_{REFH}$ and $\rm V_{SSA}/\rm V_{REFL},$ are derived from $\rm V_{DD}$ and $\rm V_{SS}$ respectively.

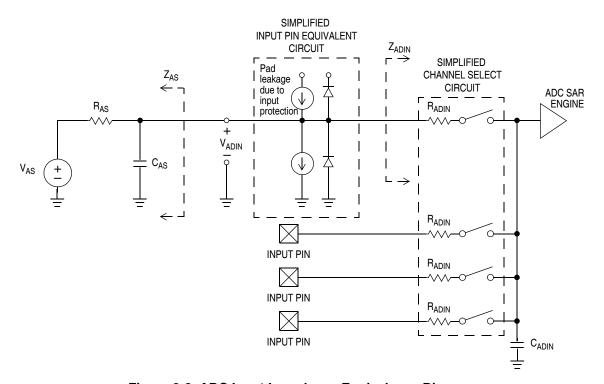


Figure 3-8. ADC Input Impedance Equivalency Diagram



Table 3-11. ADC Characteristics

Characteristic	Conditions	С	Symb	Min	Typ ¹	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1	_	Т	I _{DDA}	_	133	_	μА	_
Supply Current ADLPC=1 ADLSMP=0 ADCO=1	_	Т	I _{DDA}	_	218	_	μА	_
Supply Current ADLPC=0 ADLSMP=1 ADCO=1	_	Т	I _{DDA}	_	327	_	μА	_
Supply Current ADLPC=0 ADLSMP=0 ADCO=1	_	Т	I _{DDA}	_	0.582	1	mA	_
ADC	High Speed (ADLPC=0)	Р	f _{ADACK}	2	3.3	5	MHz	t _{ADACK} =
Asynchronous Clock Source	Low Power (ADLPC=1)			1.25	2	3.3		1/f _{ADACK}
Conversion Time	Short Sample (ADLSMP=0)	Р	t _{ADC}	_	20	_	ADCK cycles	See ADC chapter in
(Including sample time)	Long Sample (ADLSMP=1)			_	40	_		MC9S08SC4 Reference Manual for
Sample Time	Short Sample (ADLSMP=0)	Р	t _{ADS}	_	3.5	_	ADCK cycles	conversion time variances
	Long Sample (ADLSMP=1)			_	23.5	_		
Total	10 bit mode	Р	E _{TUE}	_	±1.5	±3.5	LSB	Includes
Unadjusted Error	8 bit mode			_	±0.7	±1.5		quantization
Differential	10 bit mode	Р	DNL	_	±0.5	±1.0	LSB	
Non-Linearity	8 bit mode			_	±0.3	±0.5		
		Monot	onicity and	No-Missin	g-Codes gua	ranteed		<u> </u>
Integral	10 bit mode	С	INL	_	±0.5	±1.0	LSB	
Non-Linearity	8 bit mode			_	±0.3	±0.5	1	
Zero-Scale	10 bit mode	Р	E _{ZS}	_	±1.5	±2.5	LSB	V _{ADIN} = V _{SSA}
Error	8 bit mode			_	±0.5	±0.7		
Full-Scale	10 bit mode	Р	E _{FS}	_	±1	±1.5	LSB	$V_{ADIN} = V_{DDA}$
Error	8 bit mode				±0.5	±0.5		

MC9S08SC4 MCU Series Data Sheet, Rev. 4



Table	0 44		Chara	cteristics
Table	.3- I I .	AUG	Cnara	cieristics

Characteristic	Conditions	С	Symb	Min	Typ ¹	Max	Unit	Comment
Quantization	10 bit mode	D	EQ	_	_	±0.5	LSB	_
Error	8 bit mode			_	_	±0.5		
Input Leakage	10 bit mode	D	E _{IL}	_	±0.2	±2.5	LSB	Pad leakage ²
Error	8 bit mode			_	±0.1	±1		* R _{AS}
Temp Sensor Slope	−40°C− 25°C	D	m	_	3.266	_		
	25°C– 125°C			_	3.638	_	mV/°C	_
Temp Sensor Voltage	25°C	D	V _{TEMP2}	_	1.396	_	V	_

Typical values assume V_{DDA} = 5.0V, Temp = 25C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3.11 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.11.1 Control Timing

Table 3-12. Control Timing

Num	С	Rating	Symbol	Min	Typ ¹	Max	Unit
1	D	Bus frequency (t _{cyc} = 1/f _{Bus})	f _{Bus}	dc	_	20	MHz
2	Р	Internal low power oscillator period	t _{LPO}	700	975	1500	μS
3	D	External reset pulse width ²	t _{extrst}	100	_	_	ns
4	D	Reset low drive ³	t _{rstdrv}	66 x t _{cyc}	_	_	ns
5	D	Pin interrupt pulse width Asynchronous path ² Synchronous path ⁴	t _{ILIH} , t _{IHIL}	100 1.5 x t _{cyc}	_	_	ns
6	С	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t _{Rise} , t _{Fall}		40 75	_ _	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) ⁶ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t _{Rise} , t _{Fall}		11 35		ns

Typical values are based on characterization data at $V_{DD} = 5.0V$, 25°C unless otherwise stated.

MC9S08SC4 MCU Series Data Sheet, Rev. 4

² Based on input pad leakage current. Refer to pad electricals.



- ² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources. Refer to Figure 3-9.
- When any reset is initiated, internal circuitry drives the reset pin low for about 66 cycles of t_{cyc} . After POR reset the bus clock frequency changes to the untrimmed DCO frequency ($f_{reset} = (f_{dco_ut})/4$) because TRIM is reset to 0x80 and FTRIM is reset to 0, and there is an extra divide-by-two because BDIV is reset to 0:1. After other resets trim stays at the pre-reset value.
- ⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 5 Timing is shown with respect to 20% $\rm V_{DD}$ and 80% $\rm V_{DD}$ levels. Temperature range –40°C to 125°C.

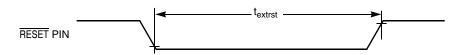


Figure 3-9. Reset Timing

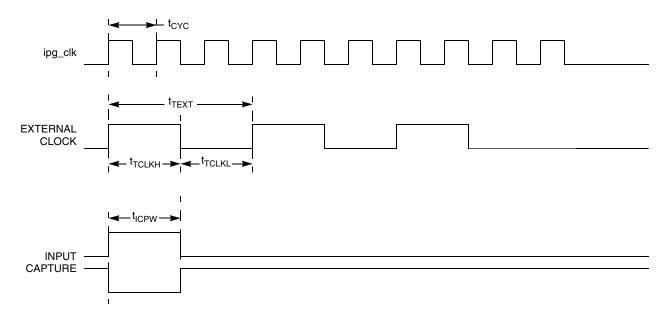
3.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Num	С	Rating	Symbol	Min	Max	Unit
1	_	External clock frequency	f _{TEXT}	dc	1/4 f _{op}	MHz
2	_	External clock period	t _{TEXT}	4	_	t _{CYC}
3	_	External clock high time	t _{TCLKH}	1.5	_	t _{CYC}
4	_	External clock low time	t _{TCLKL}	1.5	_	t _{CYC}
5	_	Input capture pulse width	f _{ICPW}	1.5	_	t _{CYC}

Table 3-13. TPM Input Timing





3.12 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Num	С	Characteristic	Symbol	Min	Typical	Max	Unit
1	_	Supply voltage for program/erase	V _{prog/erase}	4.5	_	5.5	V
2	_	Supply voltage for read operation	V _{Read}	4.5	_	5.5	V
3	_	Internal FCLK frequency ¹	f _{FCLK}	150	_	200	kHz
4	_	Internal FCLK period (1/f _{FCLK})	t _{Fcyc}	5	_	6.67	μS
5	_	Byte program time (random location) ²	t _{prog}		9		t _{Fcyc}
6	_	Byte program time (burst mode) ²	t _{Burst}	4			t _{Fcyc}
7	_	Page erase time ²	t _{Page}		4000		t _{Fcyc}
8	_	Mass erase time ²	t _{Mass}		20,000		t _{Fcyc}
9	С	Program/erase endurance ³ T_L to $T_H = -40$ °C to +125°C $T = 25$ °C	n _{FLPE}	10,000 —	— 100,000		cycles
10	С	Data retention ⁴	t _{D_ret}	15	100	_	years

Table 3-14. FLASH Characteristics

MC9S08SC4 MCU Series Data Sheet, Rev. 4

¹ The frequency of this clock is controlled by a software setting.

These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

Typical endurance for FLASH is based on the intrinsic bit cell performance. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, Typical Endurance for Nonvolatile Memory.

Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, Typical Data Retention for Nonvolatile Memory.



3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Parameter	Symbol	Conditions	Frequency	f _{osc} /f _{Bus}	Levei ¹ (Max)	Unit
	V _{RE_TEM}	$V_{DD} = 5 V$	0.15 – 50 MHz	4 MHz crystal	-7	dBμV
		T _A = +25°C package type 16-TSSOP	50 – 150 MHz	8 MHz bus	-11	
Radiated emissions,			150 – 500 MHz		-11	
electric field			500 – 1000 MHz		-10	
			IEC Level		N	_

SAE Level

Table 3-15. Radiated Emissions, Electric Field

MC9S08SC4 MCU Series Data Sheet, Rev. 4

Data based on qualification test results.



Chapter 4 Ordering Information and Mechanical Drawings

4.1 Ordering Information

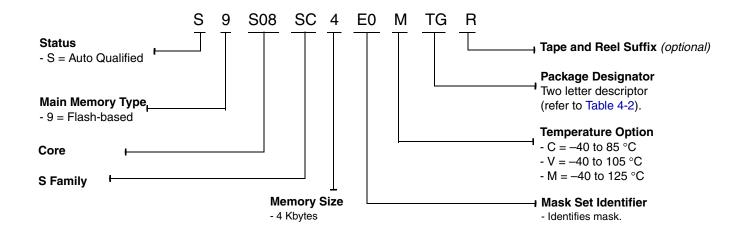
This section contains ordering information for MC9S08SC4 device.

Table 4-1. Device Numbering System

Device Number ¹	Men	Memory				
Device Number	FLASH	RAM	Packages ²			
S9S08SC4E0MTG	4K	256	16 TSSOP			

See MC9S08SC4 Reference Manual for a complete description of modules. included on each device.

4.1.1 Device Numbering Scheme



4.2 Package Information

Table 4-2. Package Information

Pin Count	Туре	Designator	Case Number	Document No.
16	TSSOP	TG	948F-01	98ASH70247A

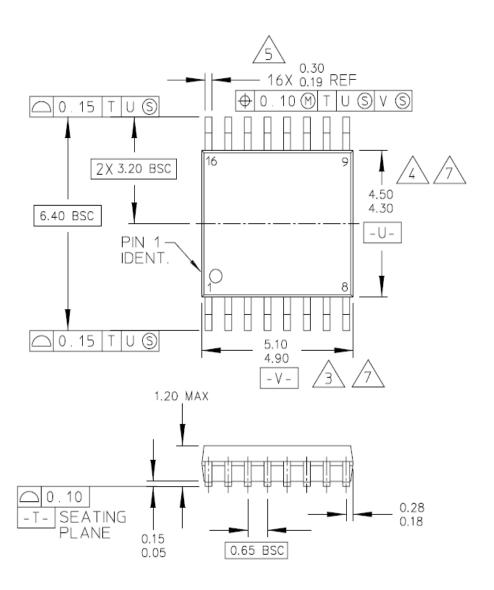
4.3 Mechanical Drawings

The following pages are mechanical drawings for the package described in Table 4-2.

² See Table 4-2 for package information.



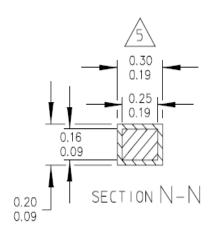
Chapter 4 Ordering Information and Mechanical Drawings

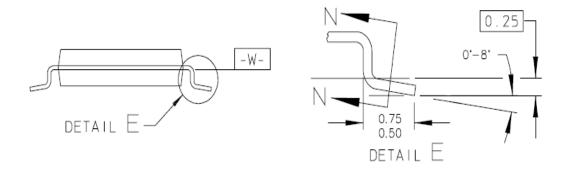


© FREESCALE SEMICONDUCTOR, INC. MECHANICAL ALL RIGHTS RESERVED.		L OUTLINE	PRINT VERSION NO	TO SCALE
TITLE:		DOCUMENT NO	: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM		CASE NUMBER	948F-01	19 MAY 2005
		STANDARD: JE	DEC	

MC9S08SC4 MCU Series Data Sheet, Rev. 4







© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. MECHANICAL		L OUTLINE	PRINT VERSION NO	T TO SCALE
16 LD TSSOP, PITCH 0.65MM		DOCUMENT NO	: 98ASH70247A	REV: B
		CASE NUMBER	: 948F-01	19 MAY 2005
		STANDARD: JE	DEC	

MC9S08SC4 MCU Series Data Sheet, Rev. 4



Chapter 4 Ordering Information and Mechanical Drawings

NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER
- 2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.



DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE



DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE



DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

	Λ	
/	7	\
/	/	١

/7\ DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -w-

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICA	L OUTLINE	PRINT VERSION NO	T TO SCALE
TITLE: 16 LD TSSOP, PITCH 0.65MM		DOCUMENT NO	: 98ASH70247A	REV: B
		CASE NUMBER	948F-01	19 MAY 2005
		STANDARD: JE	DEC	

MC9S08SC4 MCU Series Data Sheet, Rev. 4



Chapter 5 Revision History

To provide the most up-to-date information, the version of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to: http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	9/2008	Initial Release.
2	7/2009	 Incorporated editing updates. Added C and V temperature ranges at page 1. Updated Section 3.10, "ADC Characteristics". Updated Table 3-3, Table 3-6, Table 3-7, Table 3-9, Table 3-12, Table 3-15 and Section 4.1.1, "Device Numbering Scheme". Added actual package mechanical drawings. Updated Figure 3-5, Figure 3-6. Removed Transient Susceptibilty Section. Updated disclaimer page.
3	3/2010	 Updated TSSOP-16 package diagram, clarified ICS deviation, SCI LIN features at page 1. Updated Table 3-6, Table 3-7, Table 3-9, Table 3-12, Table 4-1. Updated Figure 3-5 and Figure 3-7.
4	6/2010	 Document changed from Advance Information to Technical Data Updated footnotes in Table 3-7 Updated Figure 3-5



Chapter 5 Revision History



How to Reach Us:

Home Page:

www.freescale.com

Web Support:

http://www.freescale.com/support

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc. Technical Information Center, EL516 2100 East Elliot Road Tempe, Arizona 85284 1-800-521-6274 or +1-480-768-2130 www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH **Technical Information Center** Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd. Exchange Building 23F No. 118 Jianguo Road Chaoyang District Beijing 100022 China China +86 10 5879 8000 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center 1-800-441-2447 or +1-303-675-2140 Fax: +1-303-675-2150 LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners

© Freescale Semiconductor, Inc. 2010. All rights reserved.

MC9S08SC4 Rev.4 6/2010