

LB8503V



ON Semiconductor®

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Monolithic Digital IC

DC Fan Motor Speed Control IC

Overview

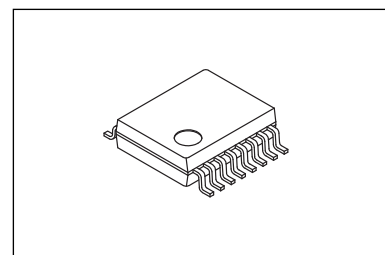
The LB8503V is an improved functionality version of the LB8500 and LB8502 products that features the added functions listed below. The LB8503V supports both single-phase and three-phase applications.

Added Functions

- Supports origin shifting in the speed control function
- Adds a dedicated pin for setting the soft start time
This allows a longer start time to be set without reducing the response time when changing speed.
- FG output pin added

Functions and Features

- Achieves linear speed control
Applications can set the slope of the change in motor speed with change in the input duty.
- Minimized speed fluctuations in the presence of line or load variations
- Allows a minimum speed to be set
- Soft start function
- Settings using external capacitors and resistors (to support easier mass production of end products)
- Supports both PWM duty and analog voltage control inputs



SSOP16 (225 mil)

ORDERING INFORMATION

See detailed ordering and shipping information on page 21 of this data sheet.

LB8503V

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------|--------------|------------------------------------|-------------|------------------|
| Supply voltage | V_{CC} max | V_{CC} pin | 18 | V |
| Output current | I_O max | E0 pin | 3 | mA |
| FG output pin output voltage | V_{FG} max | FGOUT pin | 18 | V |
| FG output pin output current | I_{FG} max | FGOUT pin | 10 | mA |
| Allowable power dissipation | P_d max | When mounted on a circuit board *1 | 0.8 | W |
| Operating temperature | T_{opr} | | -30 to +95 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

*1 Specified circuit board : $114.3 \times 76.1 \times 1.6\text{mm}^3$, glass epoxy.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------------|-----------|--|------------|------|
| Supply voltage range 1 | V_{CC1} | V_{CC} pin | 7.5 to 17 | V |
| Supply voltage range 2 | V_{CC2} | V_{CC} pin, with V_{CC} shorted to 6VREG | 5.5 to 6.5 | V |
| Output current | I_O | E0 pin | 2.5 | mA |
| 6V constant voltage output current | I_{REG} | | -5 | mA |
| CTL pin voltage | V_{CTL} | | 0 to 6VREG | V |
| LIM pin voltage | V_{LIM} | | 0 to 6VREG | V |
| VC1 pin voltage | V_{CI} | | 0 to 6VREG | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------|---------------------------|------------|------------|------|----------------------|
| | | | min | typ | max | |
| Supply current | I_{CC} | | | 5.5 | 6.5 | mA |
| 6V constant voltage output (VREG pin) | | | | | | |
| Output voltage | VREG | | 5.8 | 6.0 | 6.2 | V |
| Line regulation | ΔV_{REG1} | $V_{CC} = 8$ to 17V | | 40 | 100 | mV |
| Load regulation | ΔV_{REG2} | $I_O = -5$ to 5mA | | 10 | 100 | mV |
| Temperature coefficient | ΔV_{REG3} | Design target* | | 0 | | mV/ $^\circ\text{C}$ |
| Integrating Amplifier Block (E01) | | | | | | |
| Common-mode input voltage range | VICM | | 2.0 | | VREG | V |
| High-level output voltage | $V_{OH}(E01)$ | $I_{EO1} = -0.2\text{mA}$ | VREG - 1.2 | VREG - 0.8 | | V |
| Low-level output voltage | $V_{OL}(E01)$ | $I_{EO1} = 0.2\text{mA}$ | | 0.8 | 1.0 | V |
| Integrating Amplifier Block (E03) | | | | | | |
| High-level output voltage | $V_{OH}(E03)$ | $I_{EO1} = -0.2\text{mA}$ | VREG - 1.2 | VREG - 0.8 | | V |
| Low-level output voltage | $V_{OL}(E03)$ | $I_{EO1} = 0.2\text{mA}$ | | 0.8 | 1.0 | V |
| FGIN pin | | | | | | |
| High-level input voltage | VFGH | | 3.0 | | VREG | V |
| Low-level input voltage | VFGL | | 0 | | 1.5 | V |
| Input open voltage | VFGO | | VREG - 0.5 | | VREG | V |
| Hysteresis | VFGS | | 0.2 | 0.3 | 0.4 | V |
| High-level input current | IFGH | VFGIN = 6VREG | -10 | 0 | 10 | μA |
| Low-level input current | IFGL | VFGIN = 0V | -140 | -110 | | μA |
| FGOUT pin | | | | | | |
| Output low saturation voltage | VFG | | | 0.2 | 0.3 | V |
| Output leakage current | IFGL | | | | 10 | μA |

Continued on next page.

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Continued from preceding page.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------------|---------------|---------------|------------|------------|------|---------|
| | | | min | typ | max | |
| RC pin | | | | | | |
| High-level output voltage | $V_{OH(RC)}$ | | 3.2 | 3.45 | 3.7 | V |
| Low-level output voltage | $V_{OL(RC)}$ | | 0.8 | 0.95 | 1.05 | V |
| Clamp voltage | $V_{CLP(RC)}$ | | 1.5 | 1.65 | 1.8 | V |
| CTL pin | | | | | | |
| High-level input voltage | V_{CTH} | | 2.0 | | VREG | V |
| Low-level input voltage | V_{CTL} | | 0 | | 1.0 | V |
| Input open voltage | V_{CTO} | | VREG - 0.5 | | VREG | V |
| High-level input current | I_{CTH} | VFGIN = 6VREG | -10 | 0 | 10 | μA |
| Low-level input current | I_{CTL} | VFGIN = 0V | -140 | -110 | | μA |
| C pin | | | | | | |
| High-level input voltage | $V_{OH(C)}$ | | VREG - 0.3 | VREG - 0.1 | | V |
| Low-level input voltage | $V_{OL(C)}$ | | 1.8 | 2.0 | 2.2 | V |
| LIM pin | | | | | | |
| Input bias current | $I_{B(LIM)}$ | | -1 | | 1 | μA |
| Common-mode input voltage range | V_{ILIM} | | 2.0 | | VREG | V |
| SOFT pin | | | | | | |
| Charge current | $I_{C(SOFT)}$ | | | 1.4 | | μA |
| Operation voltage range | V_{ISOFT} | | 2.0 | | VREG | V |
| VCI pin | | | | | | |
| Input bias current | $I_{B(VCI)}$ | | -1 | | 1 | μA |
| Common-mode input voltage range | V_{IVCI} | | 2.0 | | VREG | V |
| VCO pin | | | | | | |
| High-level output voltage | $V_{OH(VCO)}$ | | | VREG - 0.2 | | V |
| Low-level output voltage | $V_{OL(VCO)}$ | | | 2.0 | | V |

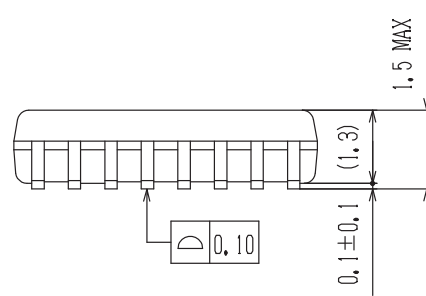
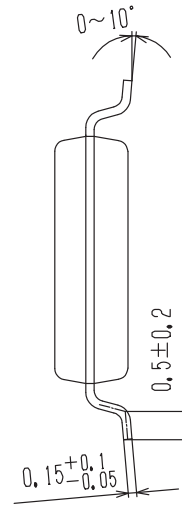
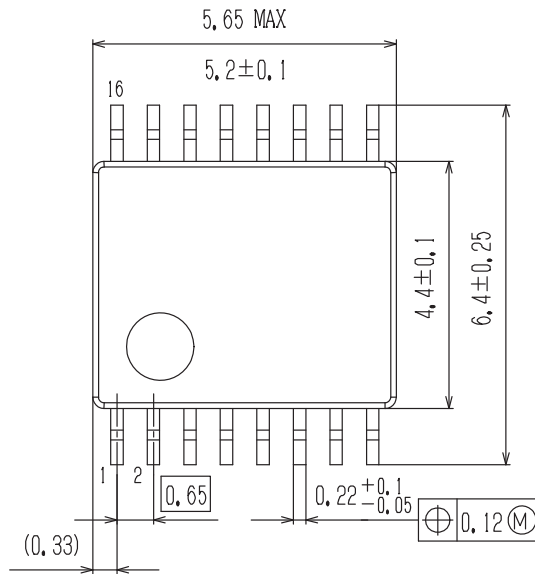
* The design specification items are design guarantees and are not measured.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

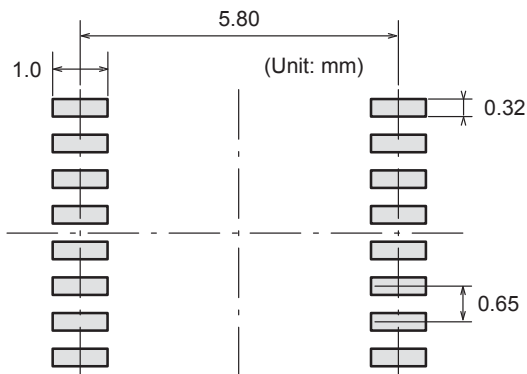
Package Dimensions

unit : mm (typ)

SSOP16 (225mil)
CASE 565AM
ISSUE A



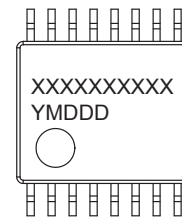
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

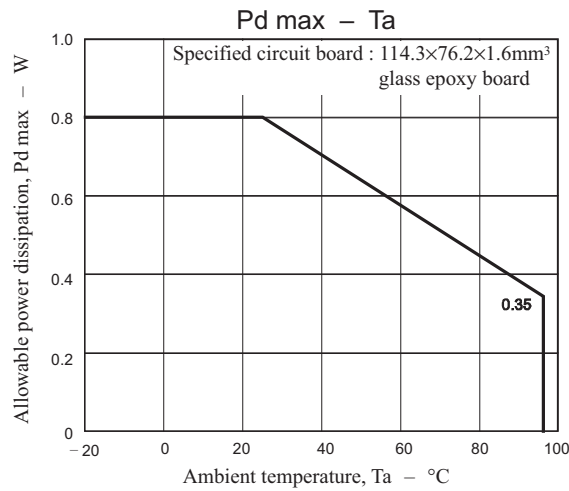
GENERIC MARKING DIAGRAM*



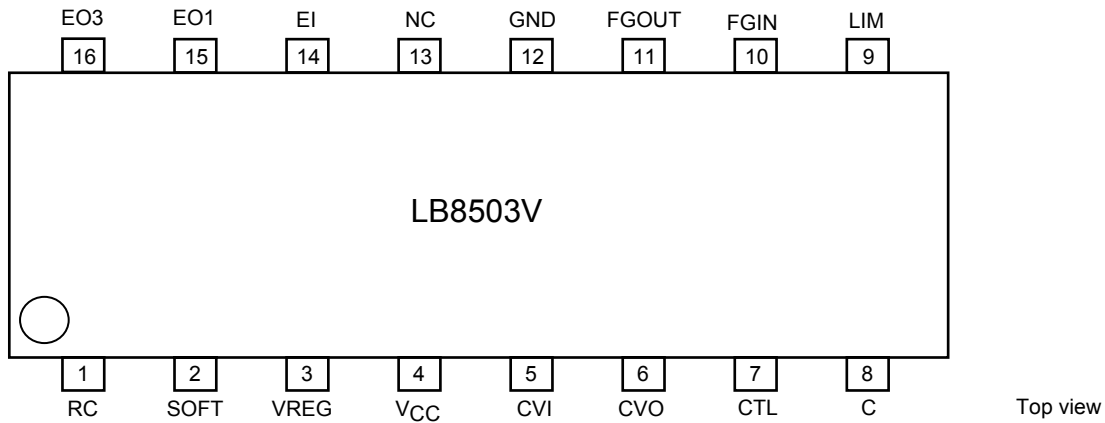
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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Pin Assignment



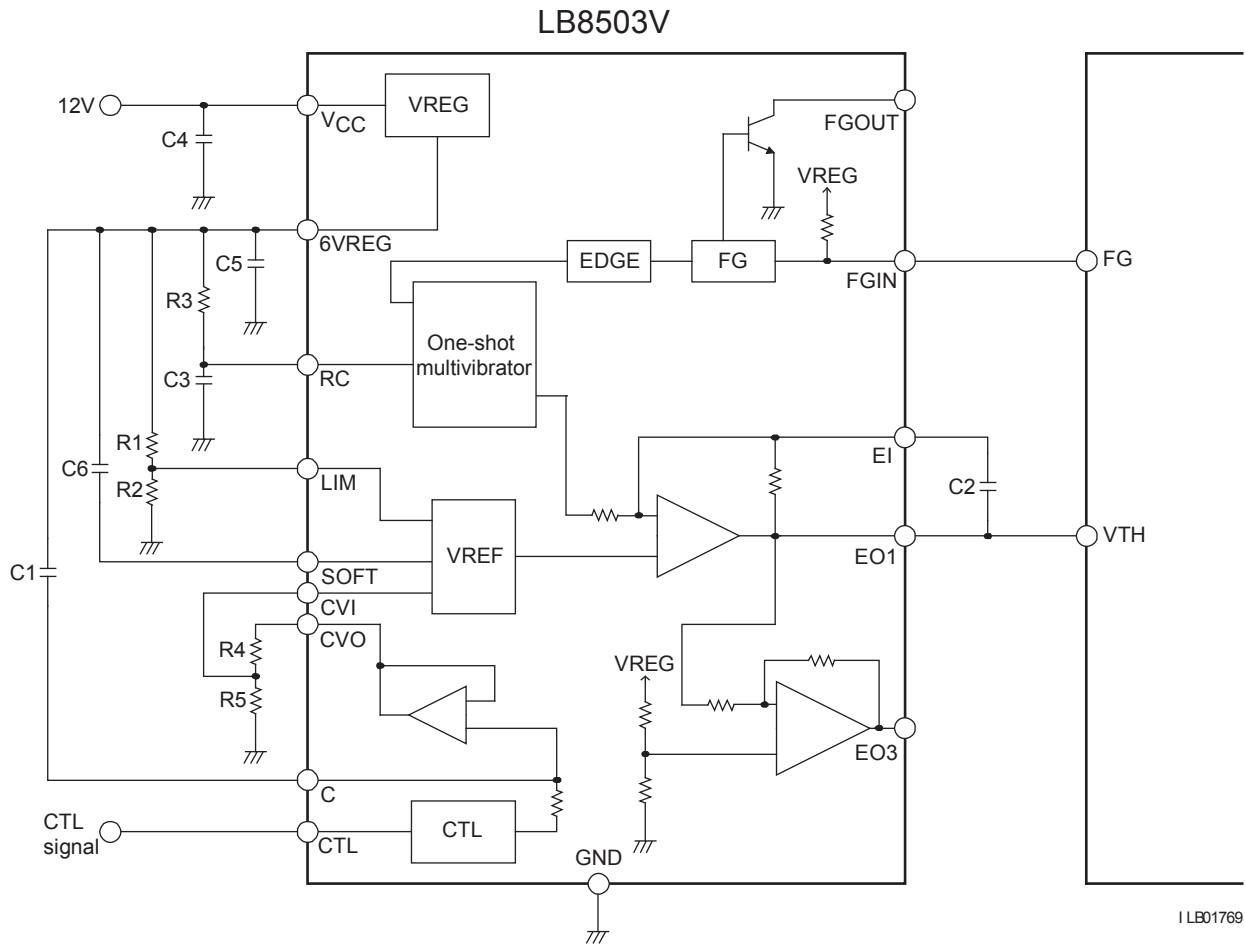
Pin Functions

| Pin No. | Pin | Description |
|-----------------|-----|---|
| RC | 1 | One-shot multivibrator pulse width setting. Connect a resistor between this pin and VREG, and a capacitor between this pin and ground. |
| SOFT | 2 | Soft start time setting. Connect a capacitor between this pin and VREG. |
| VREG | 3 | 6V regulator output. Connect a capacitor between this pin and ground for stabilization. |
| V _{CC} | 4 | Power supply. Connect a capacitor between this pin and ground for stabilization. |
| CVI | 5 | Control voltage input |
| CVO | 6 | Duty pulse signal smoothed voltage output |
| CTL | 7 | Duty pulse signal input. The speed is controlled by the duty of this pulse signal. |
| C | 8 | Duty pulse signal smoothing. Connect a capacitor between this pin and VREG. |
| LIM | 9 | Minimum speed setting. Normally, the 6V regulator level is resistor divided to set this pin's input level. |
| FGIN | 10 | FG pulse input |
| FGOUT | 11 | FG pulse output |
| GND | 12 | Grand pin |
| NC | 13 | NC pin |
| EI | 14 | One-shot multivibrator output and integrating amplifier input. A capacitor must be connected between this pin and EO for this integration. |
| EO1 | 15 | Integrating amplifier output. (For use with an accelerating driver IC if the command voltage becomes low (single-phase systems).) |
| EO3 | 16 | Integrating amplifier inverting output. (For use with an accelerating driver IC if the command voltage becomes high (three-phase systems).) |

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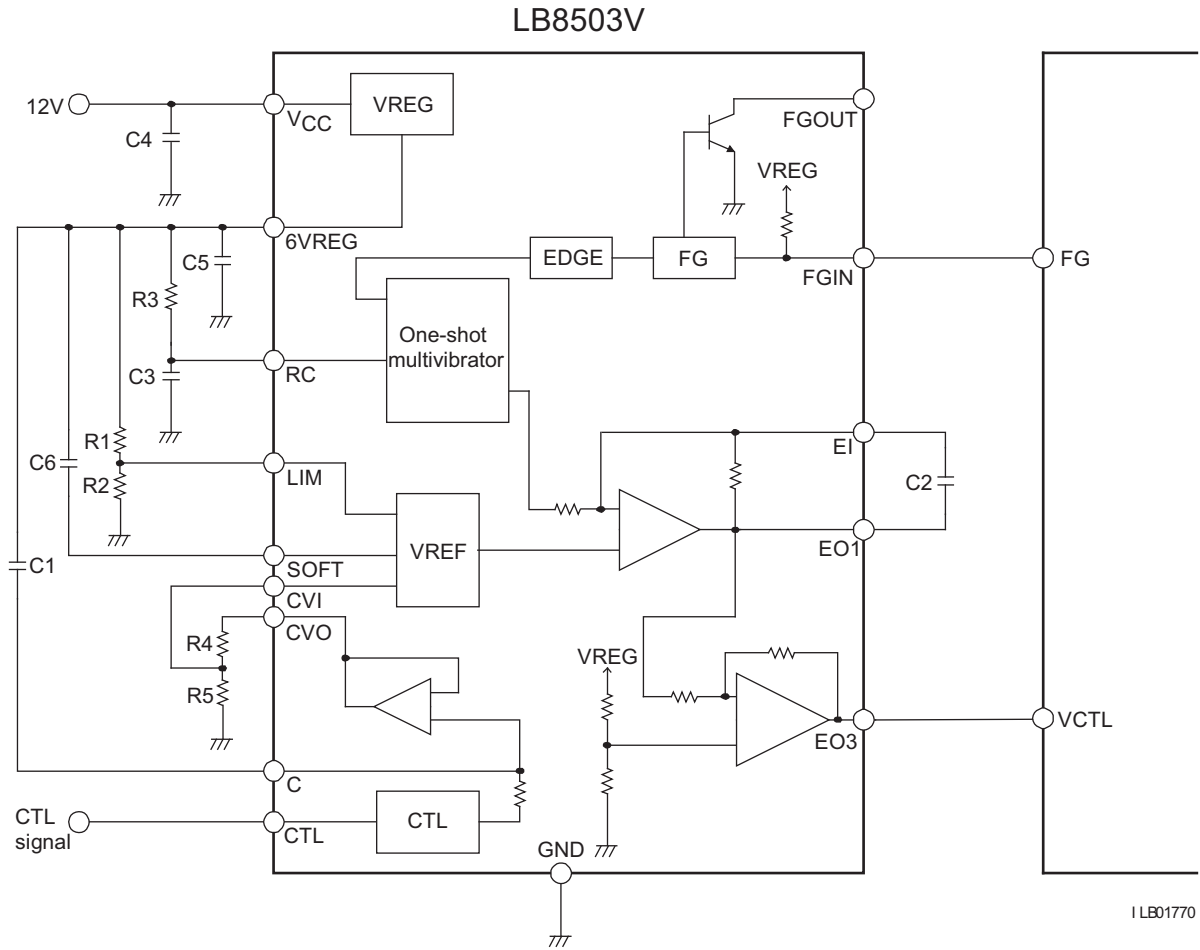
Block Diagrams and Application Examples

Combination with an accelerating driver IC when the command voltage goes low (single-phase systems)



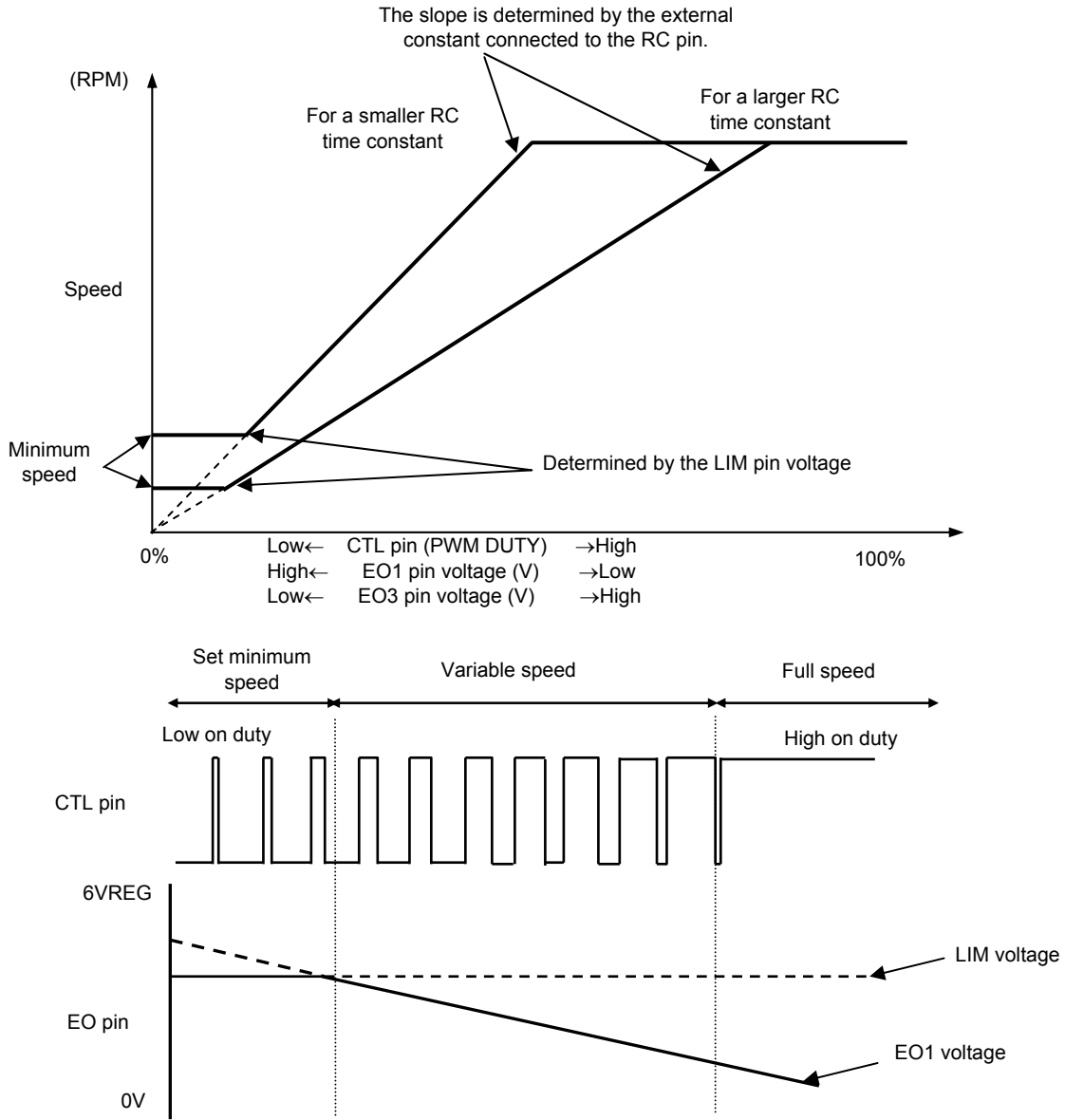
LB8503V

Combination with an accelerating driver IC when the command voltage goes high (three-phase systems)

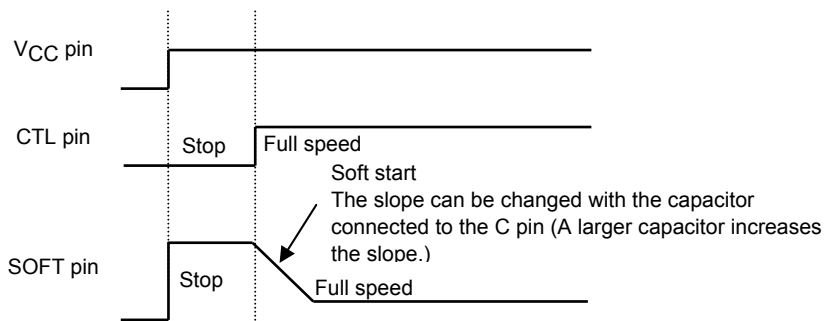


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Speed Control Diagrams

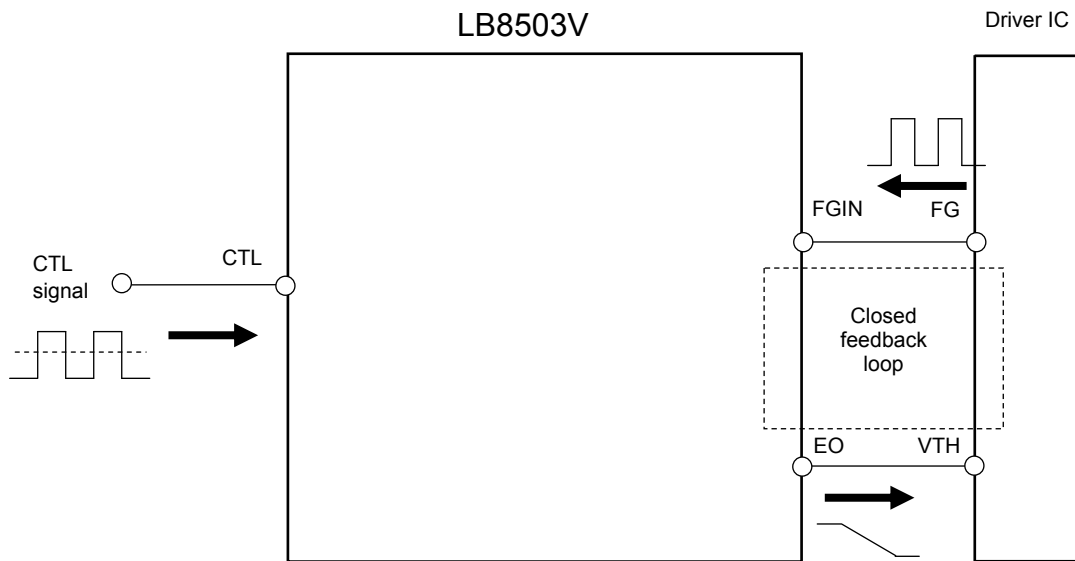


Startup Timing (soft start)

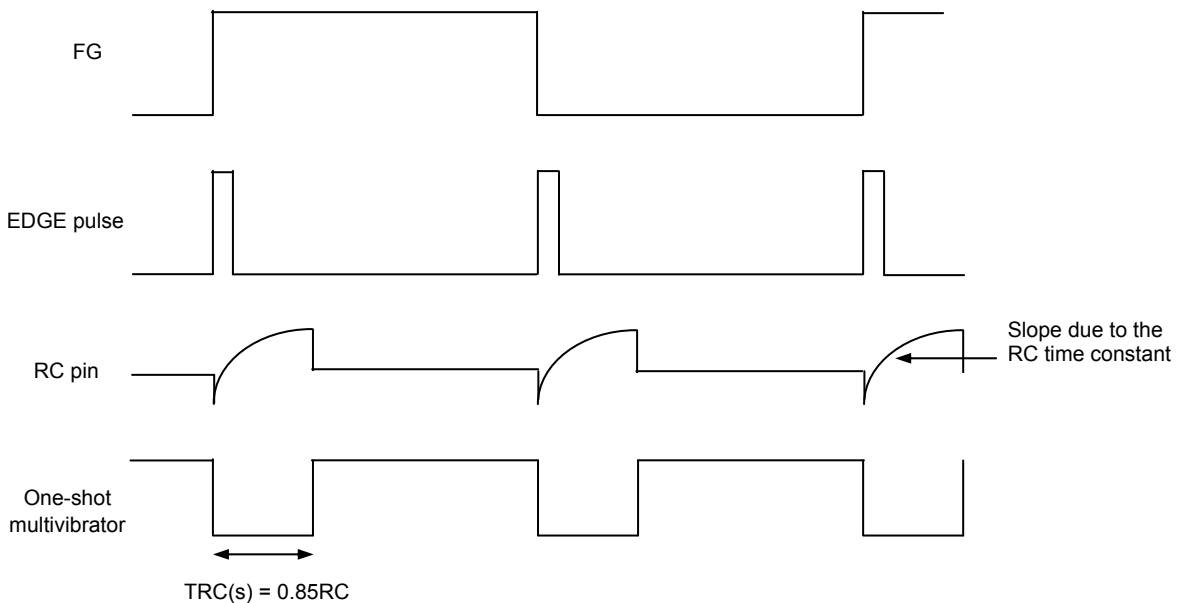


Supplementary Operational Descriptions

The LB8503V accepts a duty pulse input and an FG signal from the driver IC, and generates the driver IC control voltage so that the FG period (motor speed) becomes proportional to the control voltage.



As shown in the figure below, the LB8503V generates a pulse signal from edges on the FG signal and then generates a pulse width waveform determined by the RC time constant in a one-shot multivibrator. The LB8503V then integrates that pulse waveform to create the output driver IC control voltage (a DC voltage).

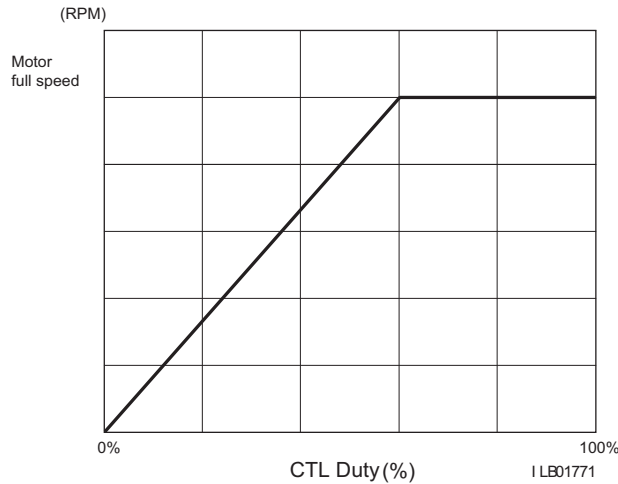


It is also possible to change the slope of the VCTL/speed relationship as shown in the speed control diagram in the previous section by changing the pulse width with the RC time constant. Note, however, that since pulses determined by this RC time constant are used, variation in the RC components will appear as speed control errors.

Pin Setting Procedures (Provided for reference purposes)

[RC pin]

The slope in the speed control diagram is determined by the RC pin time constant.



1. Determine the FG signal frequency (f_{FG} (Hz)) at the motor's highest speed.
 (When 2 FG pulses are created on each motor revolution.)
 $f_{FG}(\text{Hz}) = 2\text{rpm}/60 \dots\dots\dots(1)$

2. Determine the time constant for the RC pin.
 (Let DUTY be the control duty at the highest motor speed. For example, 100% = 1.0, 60% = 0.6)
 $R \times C = \text{DUTY} / (3 \times 0.85 \times f_{FG}) \dots\dots\dots(2)$

3. Determine the resistor and capacitor values
 The range of capacitors that can be used is from 0.01 to 0.015 μF due to the charge capabilities of the RC pin circuit. Therefore, an appropriate resistor value can be determined from either (3) or (4) below from the result obtained in step 2 above.
 $R = (R \times C) / 0.01 \mu\text{F} \dots\dots\dots(3)$
 $R = (R \times C) / 0.015 \mu\text{F} \dots\dots\dots(4)$

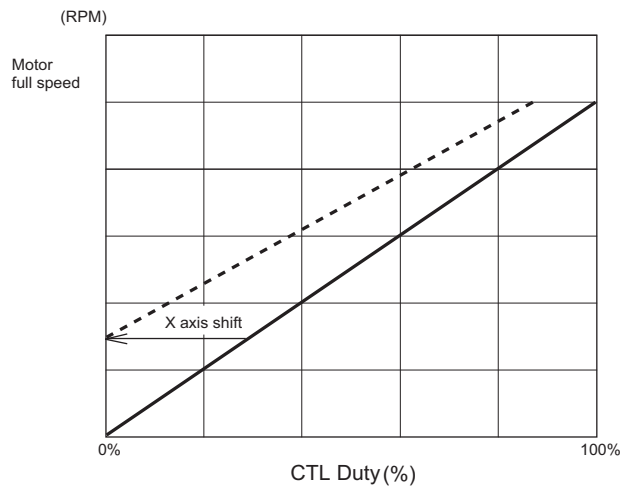
Note that the temperature characteristics of the curve are determined by the temperature characteristics of the capacitor connected to the RC pin.

A capacitor with excellent temperature characteristics must be used to minimize motor speed variation with temperature.

[CVO and CVI Pins]

These pins determine the origin of the slope. (To set the origin to 0% at 0 rpm, short CVO to CVI.)

1. X axis shift (Resistor dividing the CVO to ground potential)



To shift the characteristics from a 0% = 0 rpm origin to a situation where the speed at a duty of 30% is shifted to 0%: First, determine the required CVI pin input voltage at 0%.

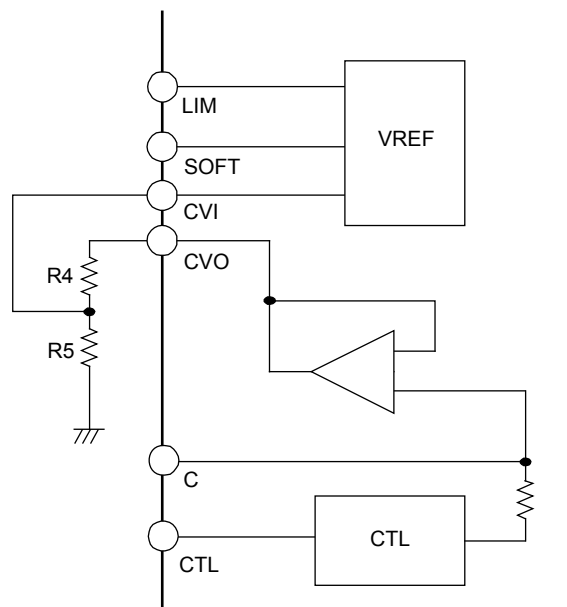
$$CVI = 6 - (4 \times DUTY) = 6 - (4 \times 0.3) = 6 - 1.2 = 4.8V$$

Next, when CVO is 6V, determine the resistor values for the resistor divider between CVO and ground such that the midpoint becomes 4.8V.

$$CVO - CVI : CVI - \text{ground} = 1.2V : 4.8V = \text{a ratio of } 1 : 4.$$

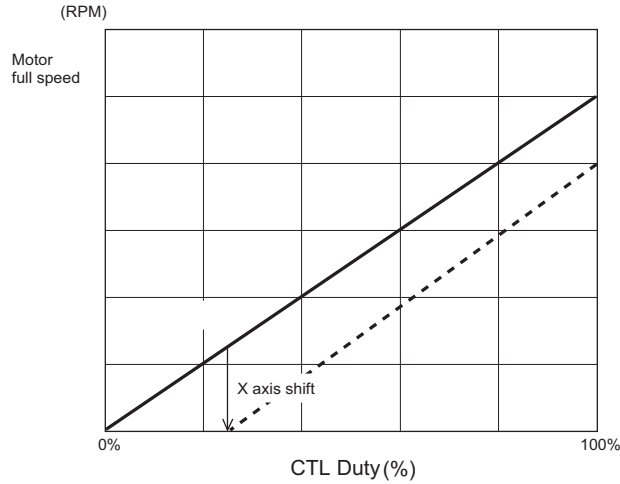
From the above, the desired resistor values will be 20kΩ between CVO and CVI and 80kΩ between CVI and ground. Note that the slope will change. (In this case, since the resistor ratio is 1:4, the result will be 4/5 of (or 0.8 times) the original slope.)

If required, the RC pin resistor value must be changed to correct the slope.



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2. Y axis shift (Resistor dividing the CVO to V_{CC} potential)



To shift the characteristics from a 0% = 0 rpm origin to a situation where the speed is 0 rpm at a duty of 30%:

First, determine the required CVO pin input voltage at 0%.

$$CVO = 6 - (4 \times DUTY) = 6 - (4 \times 0.25) = 6 - 1 = 5V$$

Determine the resistor values such that at CVO = 5 V, CVI becomes 6V.

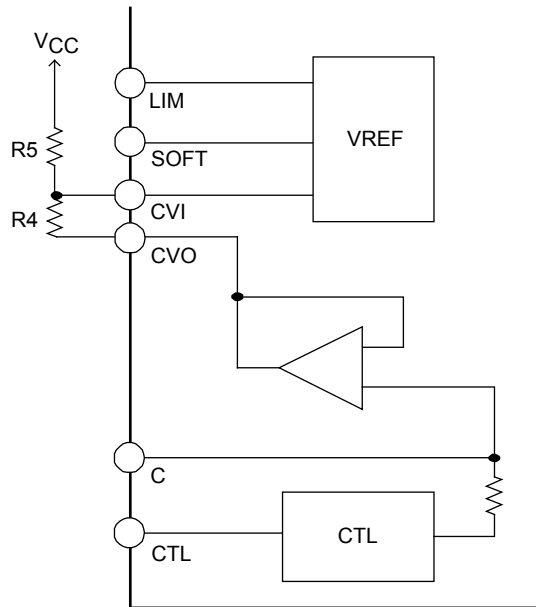
$$CVO - CVI : CVI - V_{CC} = 1 V : 6V = \text{a ratio of } 1:6.$$

From the above, the desired resistor values will be 20kΩ between CVO and CVI and 80kΩ between CVI and ground.

(Due to the current capability of the CVO pin, the total resistor value must exceed 100kΩ.)

Note that the slope will change. (In this case, since the resistor ratio is 1:6, the result will be 6/7 of (or 0.86 times) the original slope.)

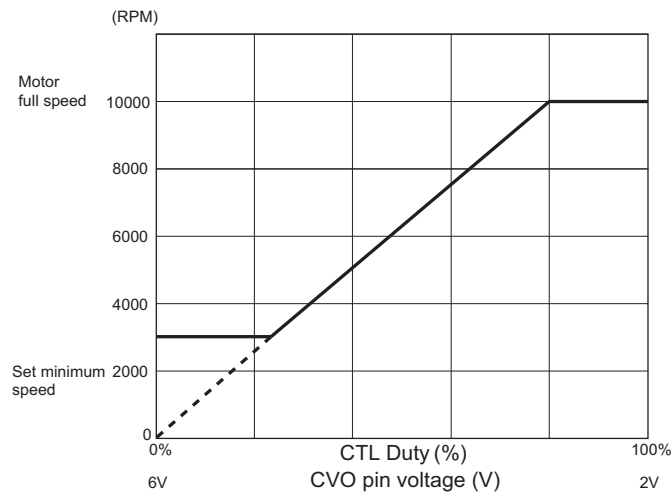
If required, the RC pin resistor value must be changed to correct the slope.



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[LIM Pin]

The minimum speed is determined by the LIM pin voltage.

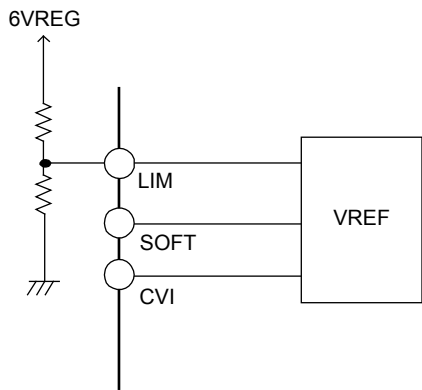


1. Determine the ratio of the required minimum speed and the maximum speed.
 $R_a = \text{minimum speed}/\text{maximum speed} \dots\dots\dots (1)$
 In the example in the figure above, $R_a = \text{minimum speed}/\text{maximum speed} = 3000/10000 = 0.3$

2. Determine the product of the duty that produces the maximum speed and the value from equation 1.
 $C_a = \text{maximum speed duty} \times R_a \dots\dots\dots (2)$
 For example, $C_a = \text{maximum speed duty} \times R_a = 0.8 \times 0.3 = 0.24$

3. Determine the required LIM pin voltage
 $LIM = 6 - (4 \times C_a) \dots\dots\dots (3)$
 For example, $LIM = 6 - (4 \times C_a) = 6 - (4 \times 0.24) \approx 5V$

4. Generate the LIM voltage by resistor dividing the 6 V regulator voltage.
 For example, the resistor ratio to create a 5V level will be 1:5.
 Thus the resistor values will be 10kΩ between 6VREG and LIM and 51kΩ between LIM and ground.



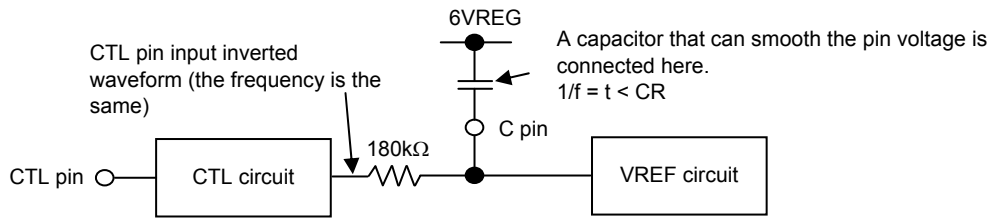
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[C Pin]

Since a capacitor that can smooth the pin voltage is connected to the C pin, if the CTL pin input signal frequency is f (Hz), then the capacitor must meet the following condition. (Here, R is the IC internal resistance of 180Ω (typical).)

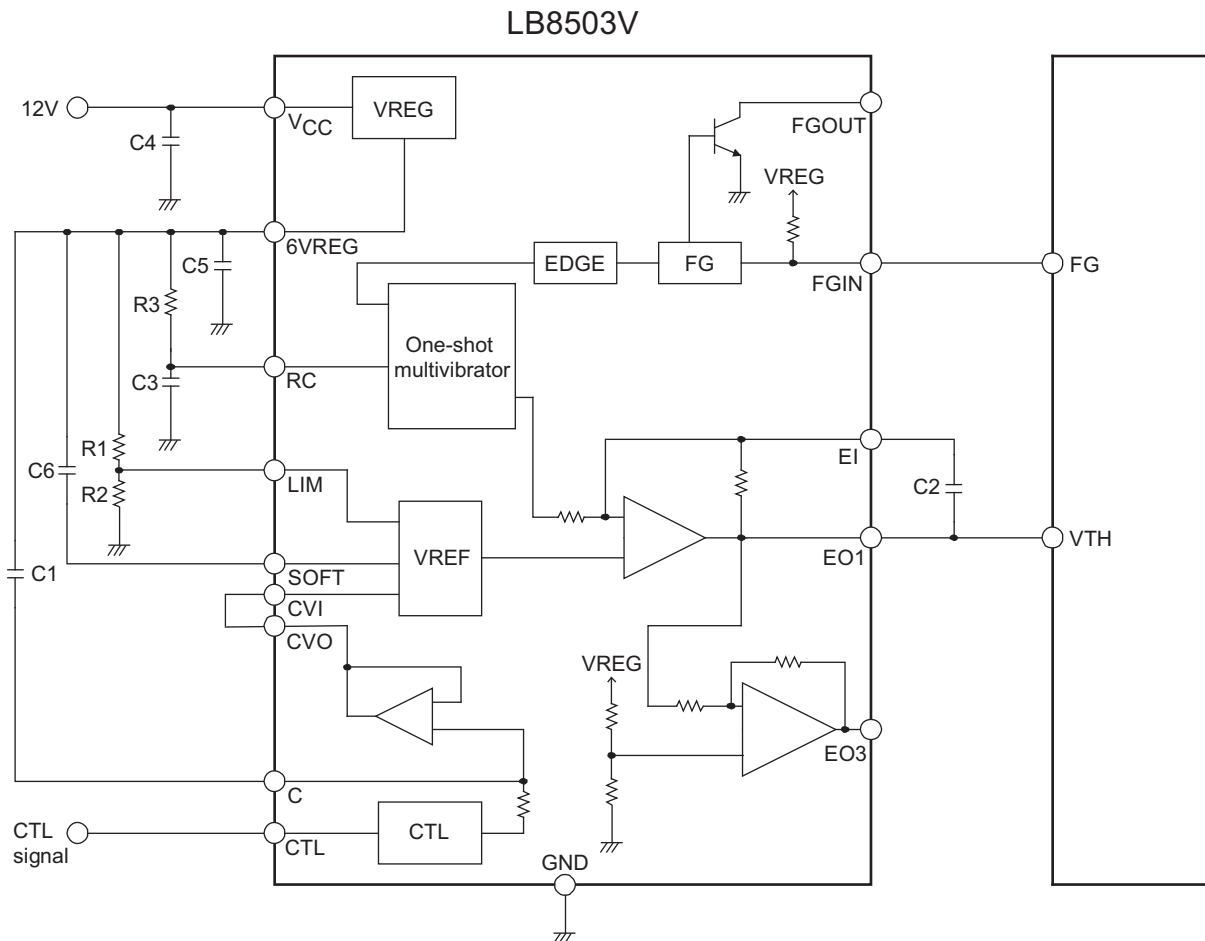
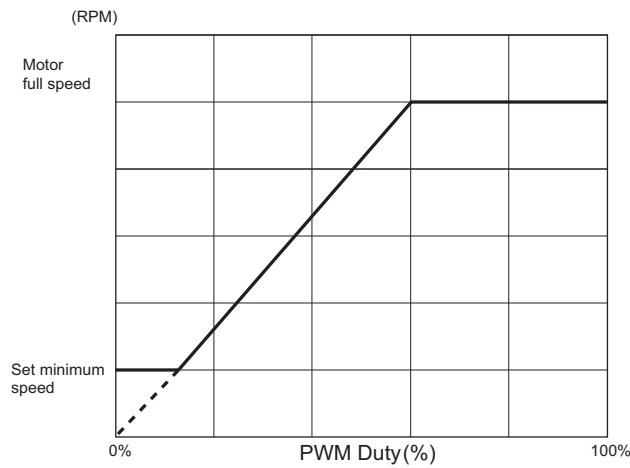
$$1/f = t < RC$$

Note that the larger the capacitor, the slower its response to changes in the input signal will be.



Application Example 2

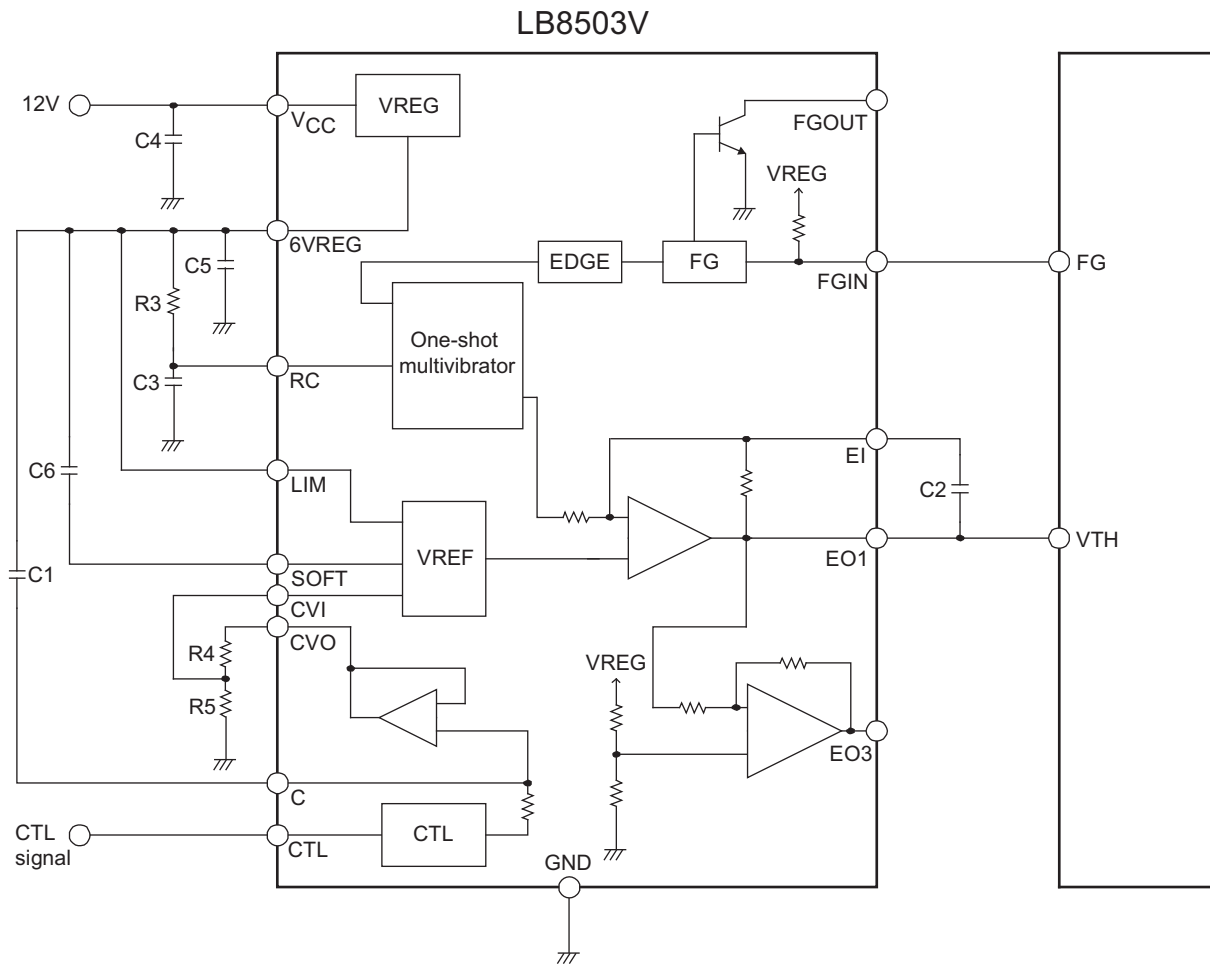
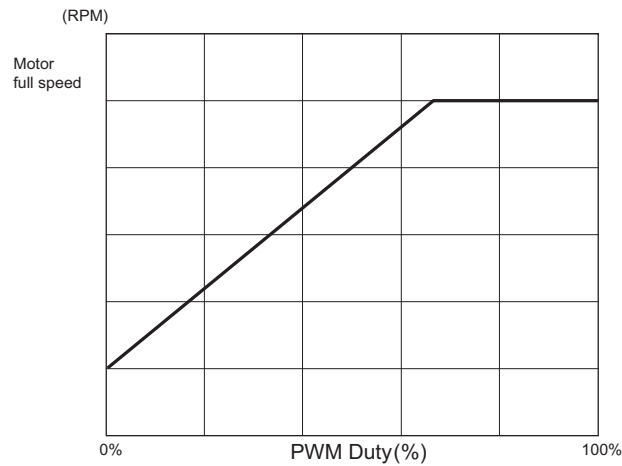
[Setting the minimum speed for an origin of 0% = 0 rpm]



When the speed control diagram origin is 0% = 0 rpm, the CVO pin is connected to the CVI pin.
 If the minimum speed is not set, connect the LIM pin to the 6VREG pin.

Application Example 3

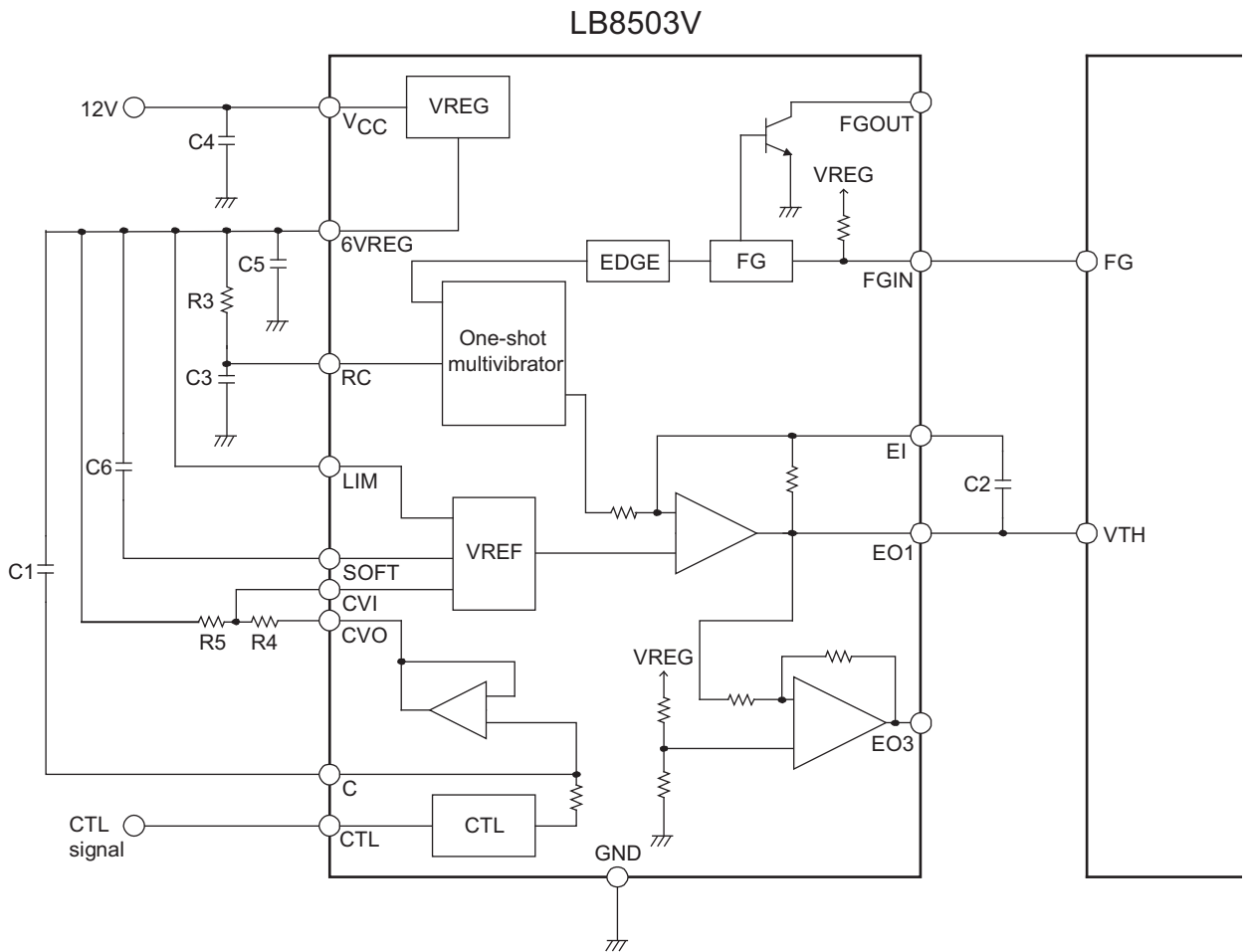
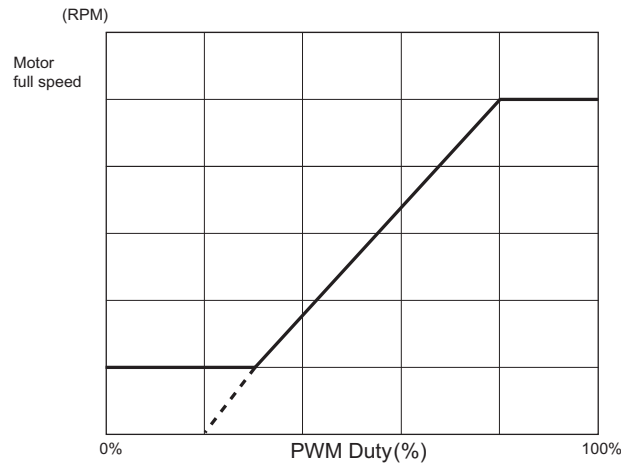
[Origin shift in the Y direction (the motor turns at 0%)]



When the speed control diagram origin is set so the motor turns at 0%, the CVO pin to ground potential difference is resistor divided and the midpoint is input to the CVI pin.
The speed at 0% can be changed with the resistor ratio.

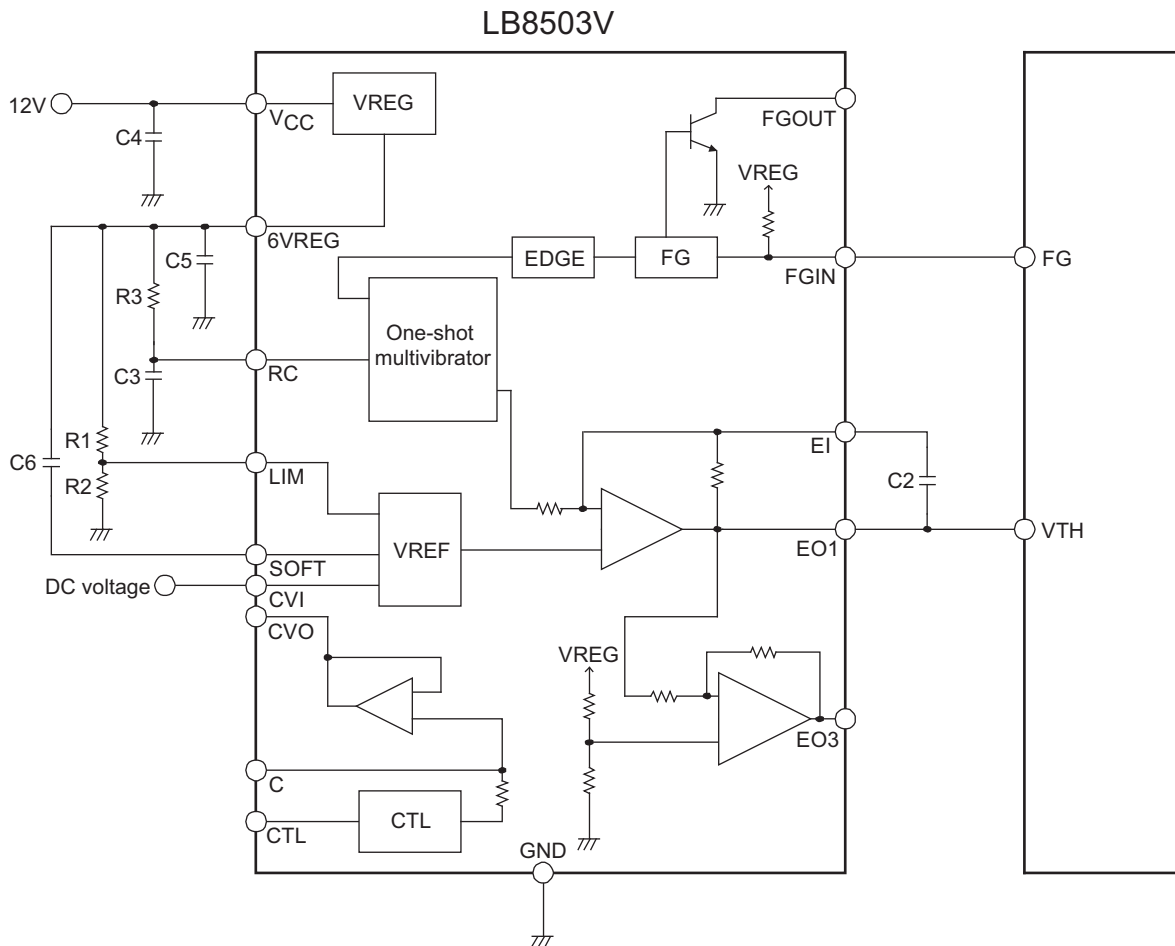
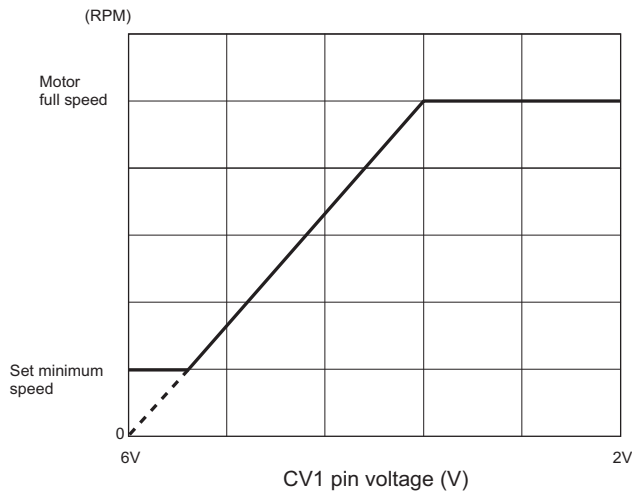
Application Example 4

[Origin shift in the X axis direction (The motor turns at a duty of 10% or higher) plus a minimum speed setting]



When the origin in the speed control diagram is set so that the motor starts turning when the duty is above 0%, the potential difference between the CVO pin and VCC is resistor divided, and that divided level is input to the CVI pin. The duty at which rotation starts can be changed by changing the resistor ratio. Note that the total value of the resistors R4 and R5 must exceed 100kΩ.

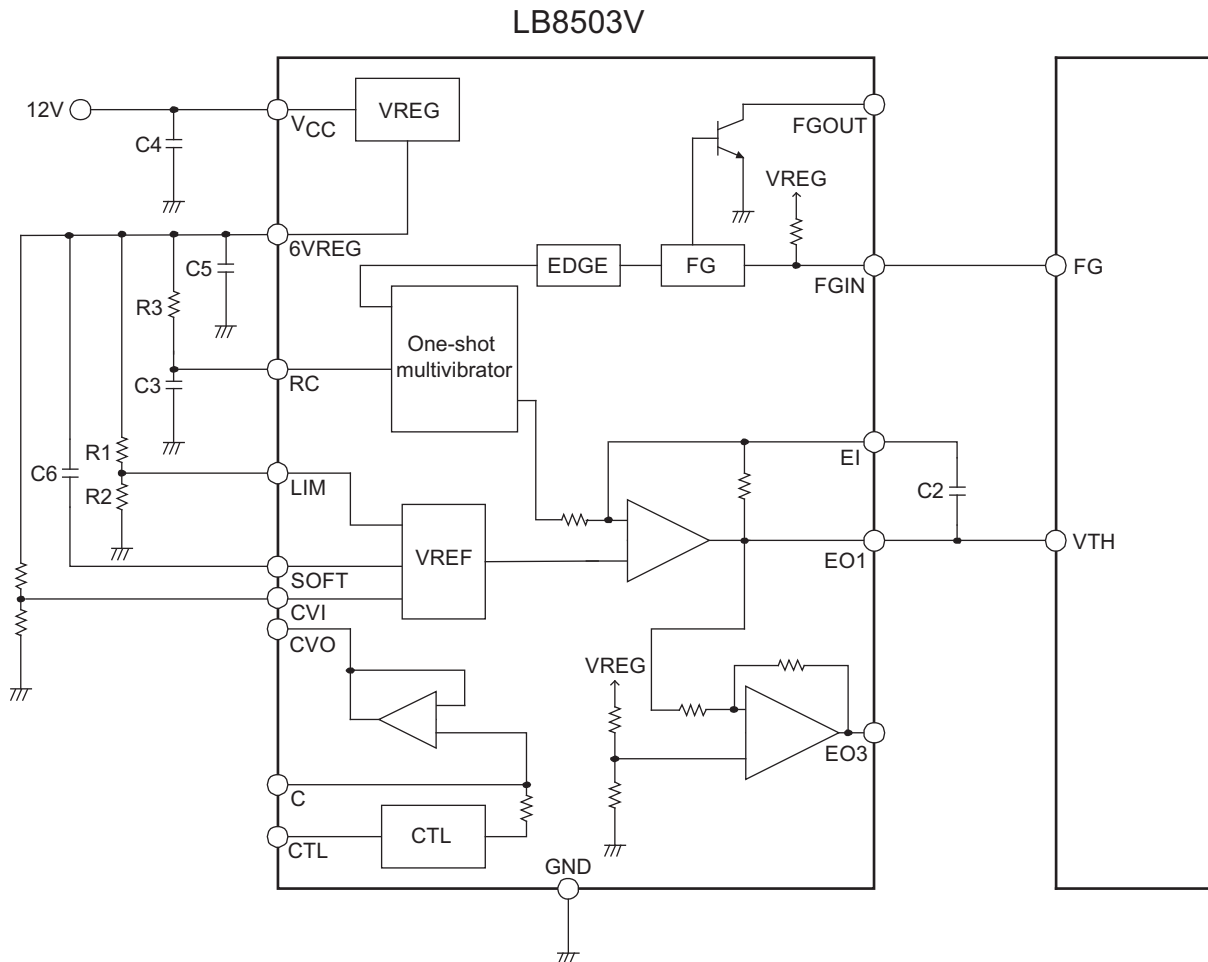
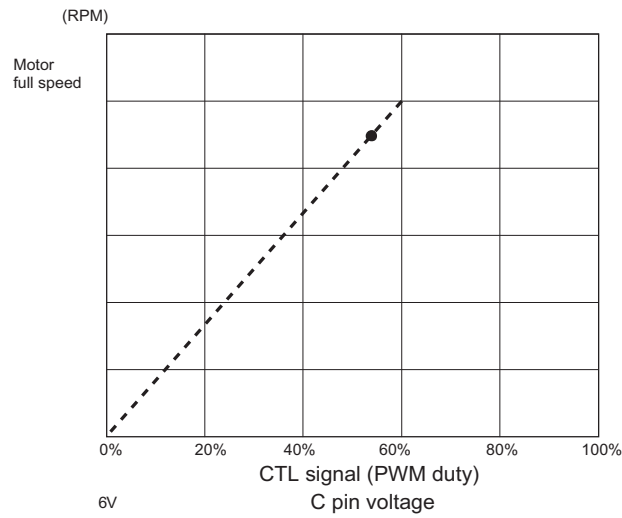
Application Example 5
[DC Voltage Speed Control]



When the motor speed is controlled by a DC voltage, that voltage must be in the range from 2V to 6VREG. Note that the motor stops when the control voltage is at 6VREG, and the motor speed increases as the voltage falls.

Application Example 6

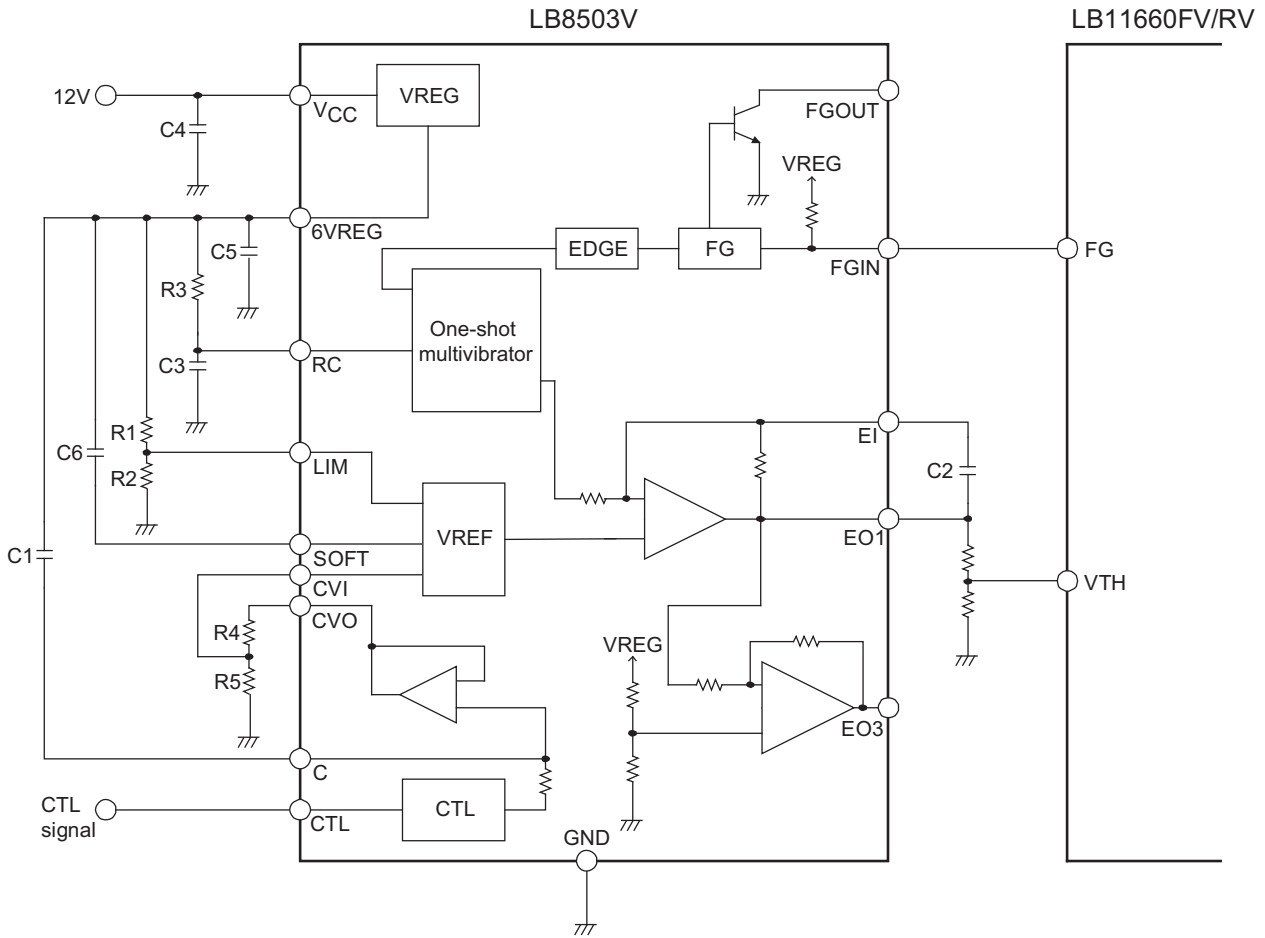
[Fixed Speed + Soft Start]



With this circuit, the motor speed remains constant even if there are fluctuations in the supply voltage or static voltage. It is also possible to input a fixed-duty signal to the CTL pin signal input as an input signal for which soft start is enabled at startup.

Application Example 7

[Used in Combination with the LB11660FV]



In this circuit, the dynamic range of the LB8503V EO pin (the range from the amplifier block output high to output low levels) must be wider than the dynamic range (from the high to low levels of the PWM signal) of VTH pin of driver IC with which this IC is combined.

However, since the LB11660FV PWM low-level voltage is lower than the LB8503V amplifier output low-level voltage, it must be resistor divided.

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|---|--------------------------|
| LB8503V-TLM-E | SSOP16 (225mil) (Pb-Free) | 2000 / Tape & Reel |
| LB8503V-W-AH | SSOP16 (225mil) (Pb-Free / Halogen Free) | 2000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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