



VND5025AK-E

Double channel high side driver with analog current sense for automotive applications

Features

| | | |
|-----------------------------------|------------|--------------------------|
| Max transient supply voltage | V_{CC} | 41V |
| Operating voltage range | V_{CC} | 4.5 to 36V |
| Max on-state resistance (per ch.) | R_{ON} | 25 m Ω |
| Current limitation (typ) | I_{LIMH} | 41 A |
| Off-state supply current | I_S | 2 μ A ⁽¹⁾ |

1. Typical value with all loads connected.

- Main
 - In-rush current active management by power limitation
 - Very low standby current
 - 3.0V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC European directive
 - Package: ECOPACK®
- Diagnostic functions Doc ID 12581
 - Proportional load current sense
 - High current sense precision for wide range currents
 - Current sense disable
 - Thermal shutdown indication
 - Very low current sense leakage
- Protection
 - Undervoltage shut-down
 - Overvoltage clamp
 - Load current limitation
 - Self-limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Thermal shutdown
 - Reverse battery protection (see [Application schematic on page 21](#))



- Electrostatic discharge protection

Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5025AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology, intended for driving resistive or inductive loads with one side connected to ground, and suitable for driving LEDs. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1. Device summary

| Package | Order codes | |
|--------------|-------------|---------------|
| | Tube | Tape and reel |
| PowerSSO-24™ | VND5025AK-E | VND5025AKTR-E |

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1 Block diagram and pin description

Figure 1. Block diagram

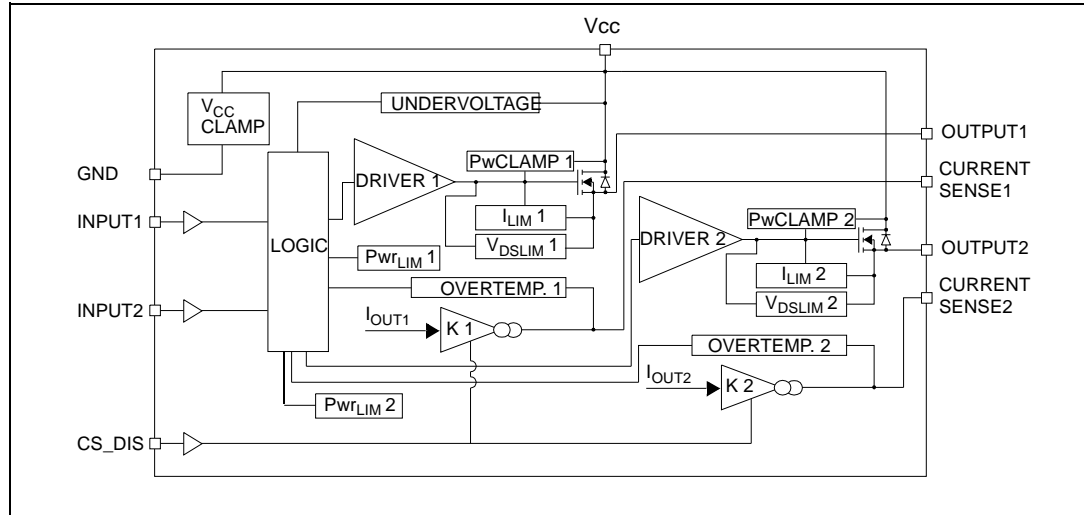


Table 2. Pin functions

| Name | Function |
|------------------------------|--|
| V _{CC} | Battery connection. |
| OUTPUT _{1,2} | Power output. |
| GND | Ground connection; must be reverse battery protected by an external diode/resistor network. |
| INPUT _{1,2} | Voltage controlled input pin with hysteresis, CMOS compatible; controls output switch state. |
| CURRENT SENSE _{1,2} | Analog current sense pin; delivers a current proportional to the load current. |
| CS_DIS | Active high CMOS compatible pin to disable the current sense pin. |

Figure 2. Configuration diagram (top view)

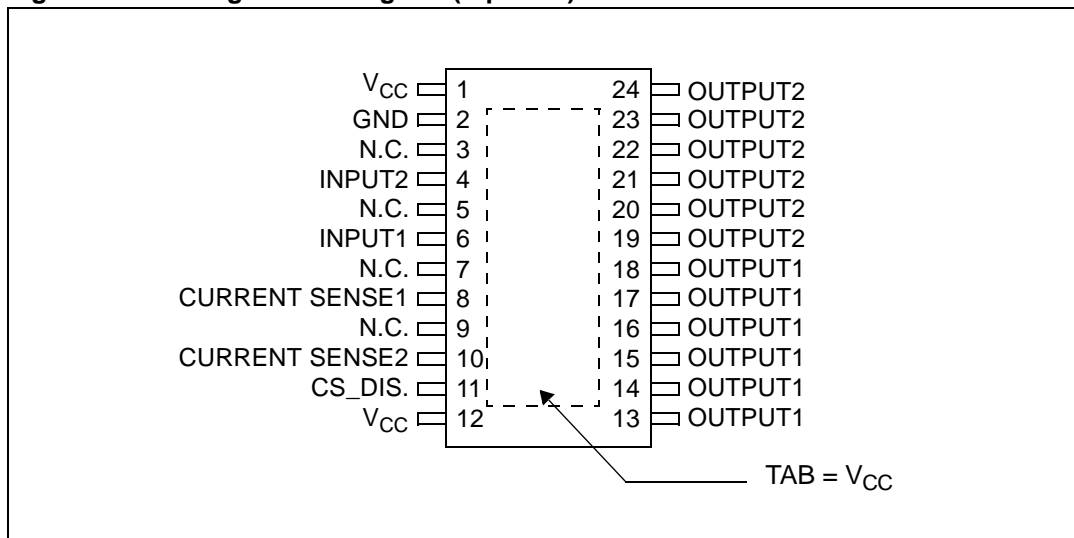


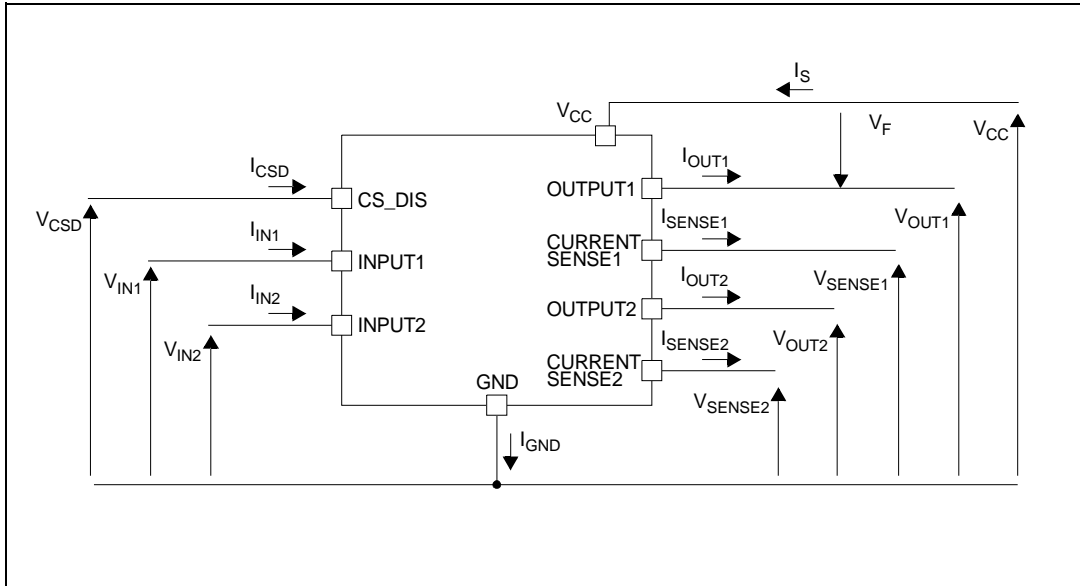
Table 3. Suggested connections for unused and not connected pins

| Connection / pin | Current sense | N.C. | Output | Input | CS_DIS |
|------------------|----------------------|------|--------|-----------------------|-----------------------|
| Floating | N.R. ⁽¹⁾ | X | X | X | X |
| To Ground | Through 1kΩ resistor | X | N.R. | Through 10kΩ resistor | Through 10kΩ resistor |

1. Not recommended.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|--|----------------------------|------|
| V_{CC} | DC supply voltage | 41 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 0.3 | |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 24 | |
| I_{IN} | DC input current | -1 to 10 | mA |
| I_{CSD} | DC current sense disable input current | | |
| $-I_{CSENSE}$ | DC reverse CS pin current | 200 | |
| V_{CSENSE} | Current sense maximum voltage | $V_{CC} - 41$ to $+V_{CC}$ | V |

Table 4. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|-----------|--|------------|------|
| E_{MAX} | Maximum switching energy (single pulse) ($L = 0.8\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5\text{V}$; $T_{jstart} = 150^\circ\text{C}$; $I_{OUT} = I_{limL}(\text{Typ.})$) | 140 | mJ |
| V_{ESD} | Electrostatic discharge (Human Body Model: $R = 1.5\text{k}\Omega$; $C = 100\text{pF}$) | | |
| | - Input | 4000 | V |
| | - Current sense | 2000 | V |
| | - CS_DIS | 4000 | V |
| | - Output | 5000 | V |
| | - V_{CC} | 5000 | V |
| V_{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T_j | Junction operating temperature | -40 to 150 | °C |
| T_{stg} | Storage temperature | -55 to 150 | |

2.2 Thermal data

Table 5. Thermal data

| Symbol | Parameter | Max Value | Unit |
|----------------|--|-------------------------------|------|
| $R_{thj-case}$ | Thermal resistance junction-case (MAX) (with one channel ON) | 1.35 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (MAX) | See Figure 29 | |

2.3 Electrical characteristics

$8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise specified.

Table 6. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------------------|------------------|------------|
| V_{CC} | Operating supply voltage | | 4.5 | 13 | 36 | V |
| V_{USD} | Undervoltage shutdown | | | 3.5 | 4.5 | |
| $V_{USDhyst}$ | Undervoltage shut-down hysteresis | | | 0.5 | | |
| R_{ON} | On-state resistance ⁽¹⁾ | $I_{OUT} = 3A$; $T_j = 25^{\circ}C$ | | | 25 | m Ω |
| | | $I_{OUT} = 3A$; $T_j = 150^{\circ}C$ | | | 50 | |
| | | $I_{OUT} = 3A$; $V_{CC} = 5V$; $T_j = 25^{\circ}C$ | | | 35 | |
| V_{clamp} | Clamp voltage | $I_S = 20\text{ mA}$ | 41 | 46 | 52 | V |
| I_S | Supply current | Off-state; $V_{CC} = 13V$; $T_j = 25^{\circ}C$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0V$ | | 2 ⁽²⁾ | 5 ⁽²⁾ | μA |
| | | On-state; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$ | | 3 | 6 | mA |
| $I_{L(off)}$ | Off-state output current ⁽¹⁾ | $V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$ | 0 | 0.01 | 3 | μA |
| | | $V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$ | 0 | | 5 | |
| V_F | Output - V_{CC} diode voltage ⁽¹⁾ | $-I_{OUT} = 4A$; $T_j = 150^{\circ}C$ | | | 0.7 | V |

1. For each channel.

2. PowerMOS leakage included.

Table 7. Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|--|------|-------------------------------|------|------------|
| $t_{d(on)}$ | Turn-on delay time | $R_L = 4.3\Omega$ (see Figure 6) | | 35 | | μs |
| $t_{d(off)}$ | Turn-off delay time | | | 50 | | |
| $(dV_{OUT}/dt)_{on}$ | Turn-on voltage slope | $R_L = 4.3\Omega$ | | See Figure 21 | | V/ μs |
| $(dV_{OUT}/dt)_{off}$ | Turn-off voltage slope | | | See Figure 22 | | |
| W_{ON} | Switching energy losses during t_{WON} | $R_L = 4.3\Omega$ (see Figure 6) | | 0.45 | | mJ |
| W_{OFF} | Switching energy losses during t_{WOFF} | | | 0.35 | | |

Table 8. Logic input

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|---------------------------|------------------|------|------|------|---------|
| V_{IL} | Input low level voltage | | | | 0.9 | V |
| I_{IL} | Low level input current | $V_{IN} = 0.9V$ | 1 | | | μA |
| V_{IH} | Input high level voltage | | 2.1 | | | V |
| I_{IH} | High level input current | $V_{IN} = 2.1V$ | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.25 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN} = 1mA$ | 5.5 | | 7 | |
| | | $I_{IN} = -1mA$ | | -0.7 | | |
| V_{CSDL} | CS_DIS low level voltage | | | | 0.9 | μA |
| I_{CSDL} | Low level CS_DIS current | $V_{CSD} = 0.9V$ | 1 | | | |
| V_{CSDH} | CS_DIS high level voltage | | 2.1 | | | V |
| I_{CSDH} | High level CS_DIS current | $V_{CSD} = 2.1V$ | | | 10 | μA |
| $V_{CSD(hyst)}$ | CS_DIS hysteresis voltage | | 0.25 | | | V |
| V_{CSCL} | CS_DIS clamp voltage | $I_{CSD} = 1mA$ | 5.5 | | 7 | |
| | | $I_{CSD} = -1mA$ | | -0.7 | | |

Table 9. Protection and diagnostics⁽¹⁾

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--|---|---------------|---------------|---------------|------|
| I_{LIMH} | DC short circuit current | $V_{CC} = 13V$ | 29 | 41 | 57 | A |
| | | $5V < V_{CC} < 36V$ | | | | |
| I_{LIML} | Short circuit current during thermal cycling | $V_{CC} = 13V$; $T_R < T_j < T_{TSD}$ | | 16 | | |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | °C |
| T_R | Reset temperature | | $T_{RS} + 1$ | $T_{RS} + 5$ | | |
| T_{RS} | Thermal reset of STATUS | | 135 | | | |
| T_{HYST} | Thermal hysteresis ($T_{TSD} - T_R$) | | | 7 | | |
| V_{DEMAG} | Turn-off output voltage clamp | $I_{OUT} = 2A$; $V_{IN} = 0$; $L = 6mH$ | $V_{CC} - 41$ | $V_{CC} - 46$ | $V_{CC} - 52$ | V |
| V_{ON} | Output voltage drop limitation | $I_{OUT} = 0.20.1A$; $T_j = -40^\circ C$ to $+150^\circ C$ (see Figure 9) | | 25 | | mV |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V < V_{CC} < 16V)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|--|--|--------------|--------------|--------------|----------------|
| K _{LED} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.05A; V _{SENSE} = 0.5V; V _{CSD} = 0V; T _j = -40°C to 150°C | 1450 | 3300 | 5180 | |
| K ₀ | I _{OUT} /I _{SENSE} | I _{OUT} = 0.5 A; V _{SENSE} = 0.5V; V _{CSD} = 0V; T _j = -40°C to 150°C | 1720 | 3020 | 4360 | |
| dK ₀ /K ₀ ⁽¹⁾ | Current Sense ratio drift | I _{OUT} = 0.5A; V _{SENSE} = 0.5V; V _{CSD} = 0V; T _j = -40°C to 150°C | -12 | | +12 | % |
| K ₁ | I _{OUT} /I _{SENSE} | I _{OUT} = 2A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C T _j = 25°C to 150°C | 1940 2230 | 2810 2810 | 3740 3390 | |
| dK ₁ /K ₁ ⁽¹⁾ | Current Sense ratio drift | I _{OUT} = 2A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C | -10 | | +10 | % |
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} = 3A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C T _j = 25°C to 150°C | 2250 2400 | 2790 2790 | 3450 3180 | |
| dK ₂ /K ₂ ⁽¹⁾ | Current Sense ratio drift | I _{OUT} = 3A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C | -7 | | +7 | % |
| K ₃ | I _{OUT} /I _{SENSE} | I _{OUT} = 10A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C T _j = 25°C to 150°C | 2610 2650 | 2760 2760 | 2970 2870 | |
| dK ₃ /K ₃ ⁽¹⁾ | Current Sense ratio drift | I _{OUT} = 10A; V _{SENSE} = 4V; V _{CSD} = 0V; T _j = -40°C to 150°C | -4 | | +4 | % |
| I _{SENSE0} | Analog Sense leakage current | I _{OUT} = 0A; V _{SENSE} = 0V; V _{CSD} = 5V; V _{IN} = 0V; T _j = -40°C to 150°C V _{CSD} = 0V; V _{IN} = 5V; T _j = -40°C to 150°C I _{OUT} = 2A; V _{SENSE} = 0V; V _{CSD} = 5V; V _{IN} = 5V; T _j = -40°C to 150°C | 0 0 0 | | 1 2 1 | μA μA μA |
| I _{OL} | Openload on-state current detection threshold | V _{IN} = 5V, I _{SENSE} = 5 μA | 5 | | 30 | mA |
| V _{SENSE} | Max analog Sense output voltage | I _{OUT} = 3 A; V _{CSD} = 0V | 5 | | | V |
| V _{SENSEH} | Analog Sense output voltage in overtemperature condition | V _{CC} = 13V; R _{SENSE} = 3.9kΩ | | 9 | | |

Table 10. Current sense (8V < V_{CC} < 16V) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------|--|---|------|------|------|------|
| I _{SENSEH} | Analog Sense output current in overtemperature condition | V _{CC} = 13V; V _{SENSE} = 5V | | 8 | | mA |
| t _{DSENSE1H} | Delay response time from falling edge of CS_DIS pin | V _{SENSE} < 4V, 0.5 < I _{OUT} < 10A I _{SENSE} = 90% of I _{SENSEMAX} (see Figure 4) | | 50 | 100 | μs |
| t _{DSENSE1L} | Delay response time from rising edge of CS_DIS pin | V _{SENSE} < 4V, 0.5 < I _{OUT} < 10A I _{SENSE} = 10% of I _{SENSEMAX} (see Figure 4) | | 5 | 20 | |
| t _{DSENSE2H} | Delay response time from rising edge of INPUT pin | V _{SENSE} < 4V, 0.5 < I _{OUT} < 10A I _{SENSE} = 90% of I _{SENSEMAX} (see Figure 4) | | 70 | 300 | |
| Δt _{DSENSE2H} | Delay response time between rising edge of output current and rising edge of current sense | V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} , I _{OUTMAX} = 3A (see Figure 5) | | | 200 | |
| t _{DSENSE2L} | Delay response time from falling edge of INPUT pin | V _{SENSE} < 4V, 0.5 < I _{OUT} < 10A I _{SENSE} = 10% of I _{SENSEMAX} (see Figure 4) | | 100 | 250 | |

1. Parameter guaranteed by design; it is not tested.

Figure 4. Current sense delay characteristics

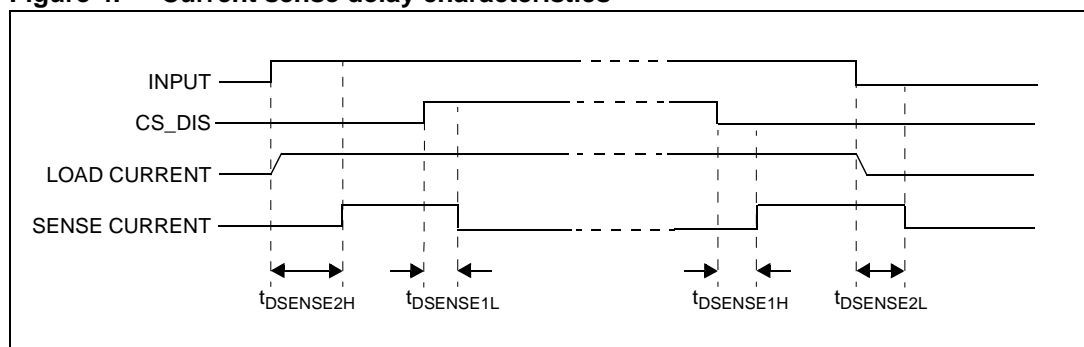


Figure 5. Delay response time between rising edge of output current and rising edge of Current Sense (CS enabled)

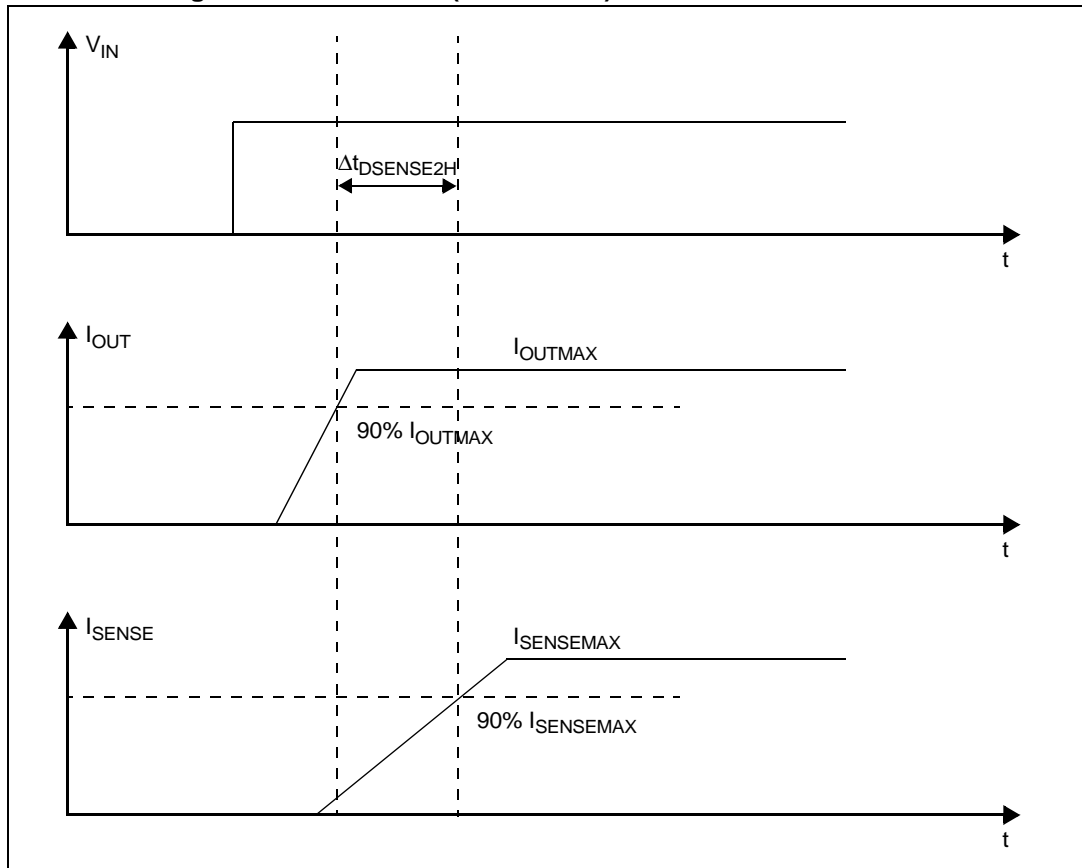


Figure 6. Switching characteristics

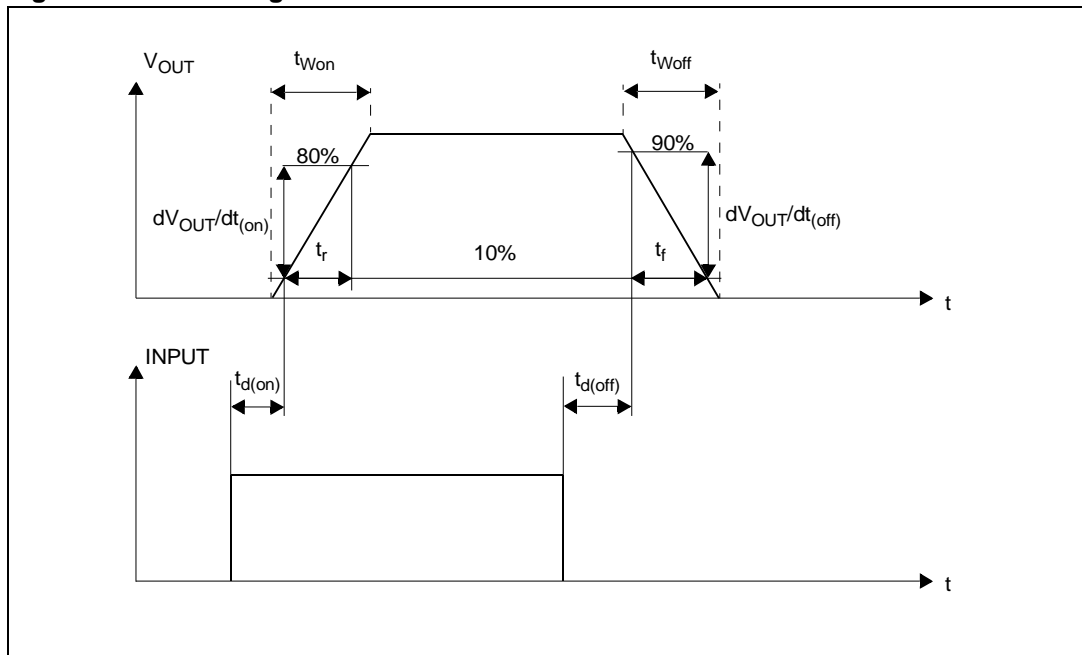
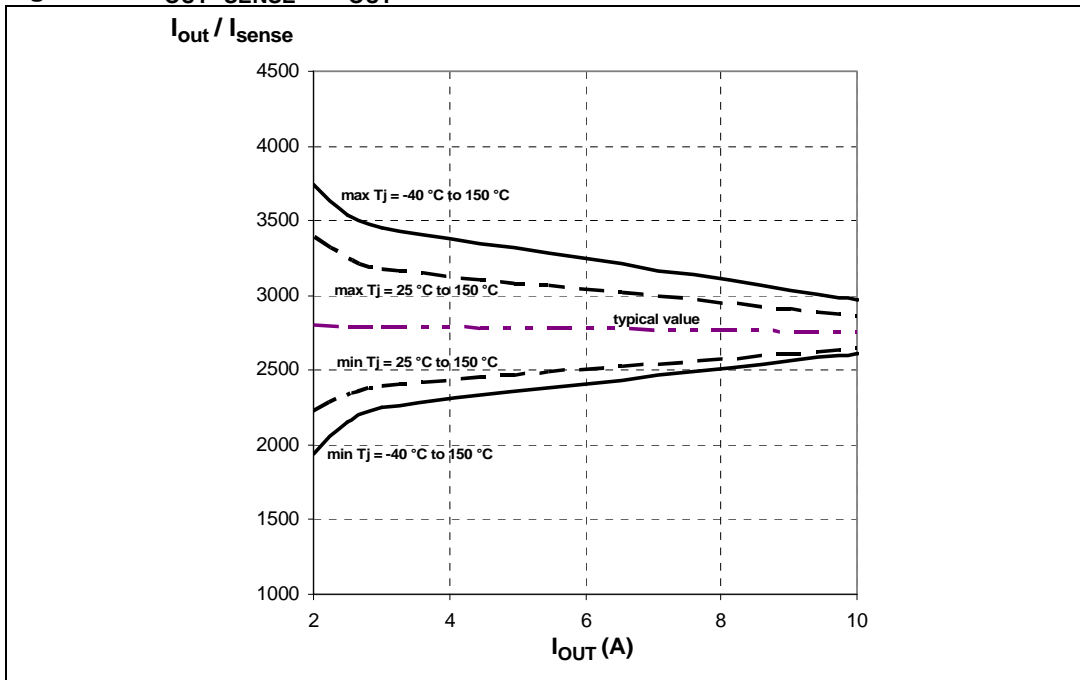
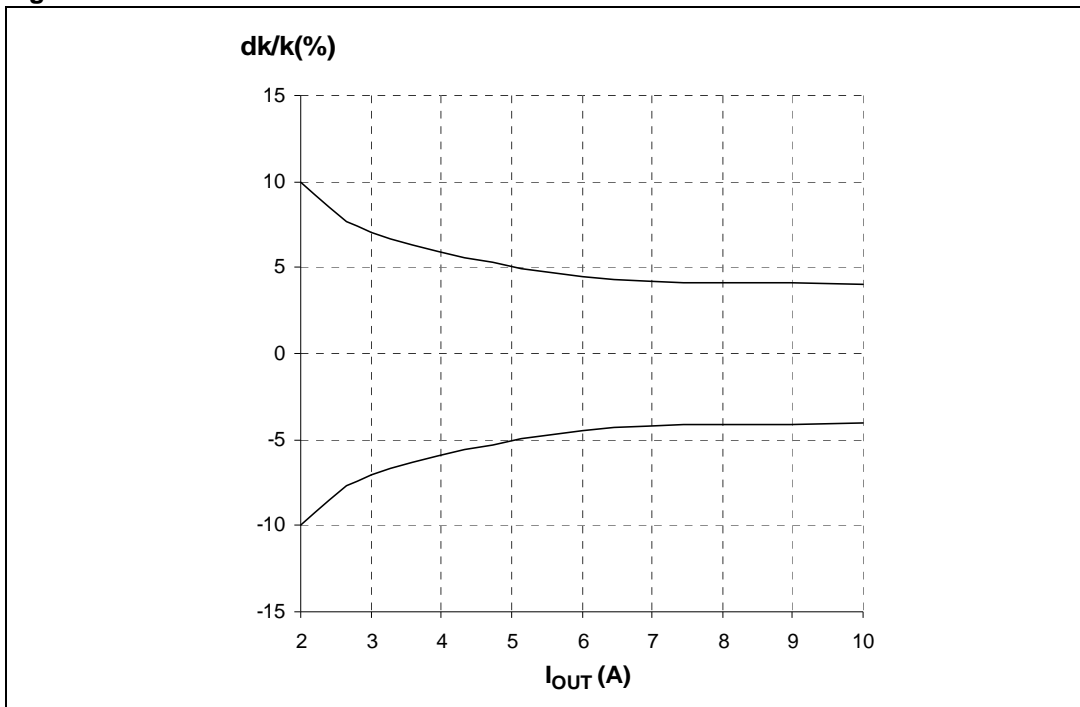


Figure 7. I_{OUT}/I_{SENSE} vs I_{OUT} (1)



1. See [Table 10](#) for details.

Figure 8. Maximum current sense ratio drift vs load current(1)



1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

| Conditions | Input | Output | Sense ($V_{CSD} = 0V$) ⁽¹⁾ |
|--|-------|--------|---|
| Normal operation | L | L | 0 |
| | H | H | Nominal |
| Over temperature | L | L | 0 |
| | H | | V_{SENSEH} |
| Undervoltage | L | L | 0 |
| | H | | |
| Short circuit to GND ($R_{SC} \leq 10m\Omega$) | L | L | 0 |
| | H | | 0 if $T_j < T_{TSD}$ |
| | | | V_{SENSEH} if $T_j > T_{TSD}$ |
| Short circuit to V_{CC} | L | H | 0 |
| | H | | < Nominal |
| Negative output voltage clamp | L | L | 0 |

1. If the V_{CSD} is high, the SENSE output is at a high impedance; its potential depends on leakage currents and external circuit.

Figure 9. Output voltage drop limitation

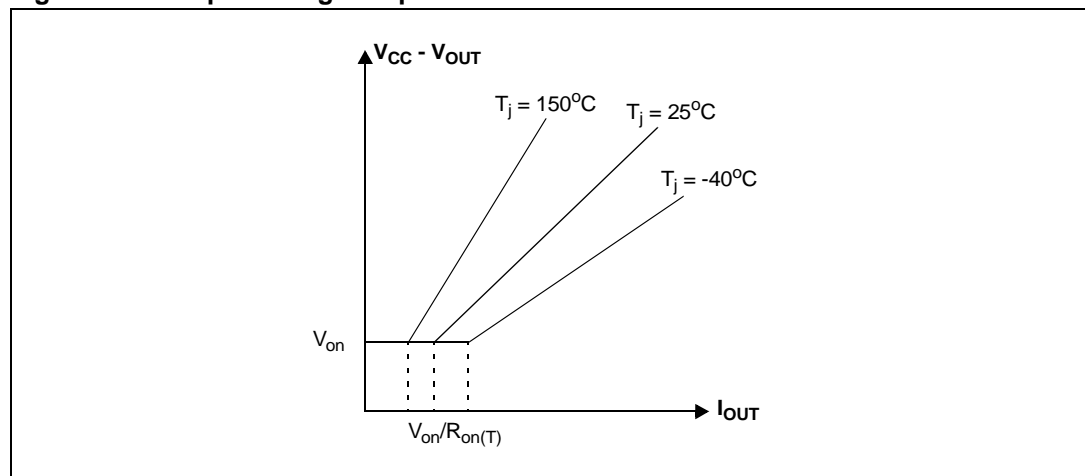


Table 12. Electrical transient requirements (part 1/3)

| ISO 7637-2: 2004(E) Test pulse | Test levels ⁽¹⁾ | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and Impedance |
|--------------------------------------|----------------------------|-------|--------------------------------------|--------------------------------------|-------|-------------------------|
| | III | IV | | Min. | Max. | |
| 1 | -75V | -100V | 5000 pulses | 0.5s | 5s | 2 ms, 10Ω |
| 2a | +37V | +50V | 5000 pulses | 0.2s | 5s | 50μs, 2Ω |
| 3a | -100V | -150V | 1h | 90ms | 100ms | 0.1μs, 50Ω |
| 3b | +75V | +100V | 1h | 90ms | 100ms | 0.1μs, 50Ω |
| 4 | -6V | -7V | 1 pulse | | | 100ms, 0.01Ω |
| 5b ⁽²⁾ | +65V | +87V | 1 pulse | | | 400ms, 2Ω |

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2/3)

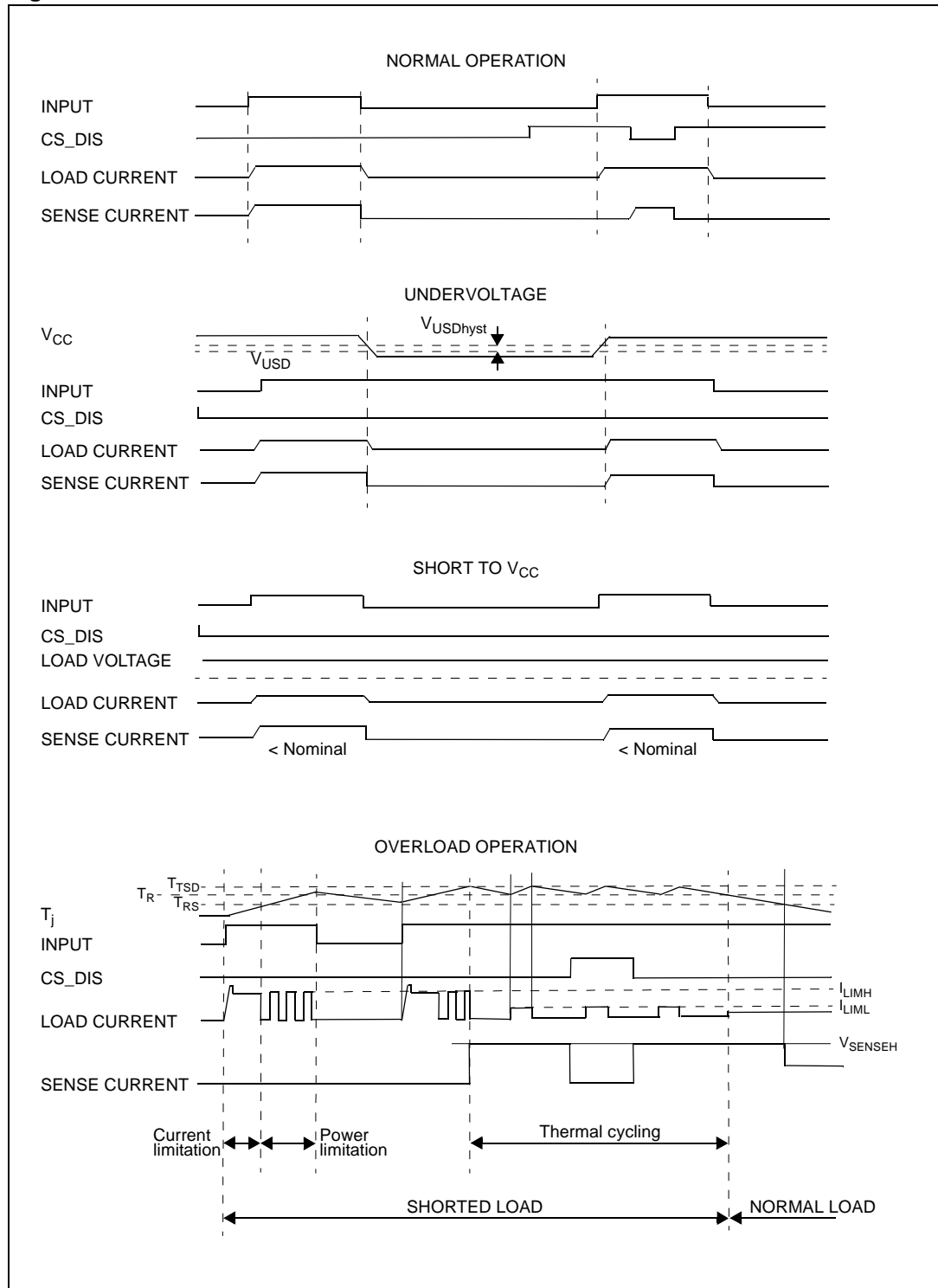
| ISO 7637-2: 2004E Test pulse | Test level results | |
|------------------------------------|--------------------|----|
| | III | VI |
| 1 | C | C |
| 2a | C | C |
| 3a | C | C |
| 3b | C | C |
| 4 | C | C |
| 5b ⁽¹⁾ | C | C |

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

| Class | Contents |
|-------|---|
| C | All functions of the device performed as designed after exposure to disturbance. |
| E | One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure 10. Waveforms



2.4 Electrical characteristics curves

Figure 11. Off-state output current

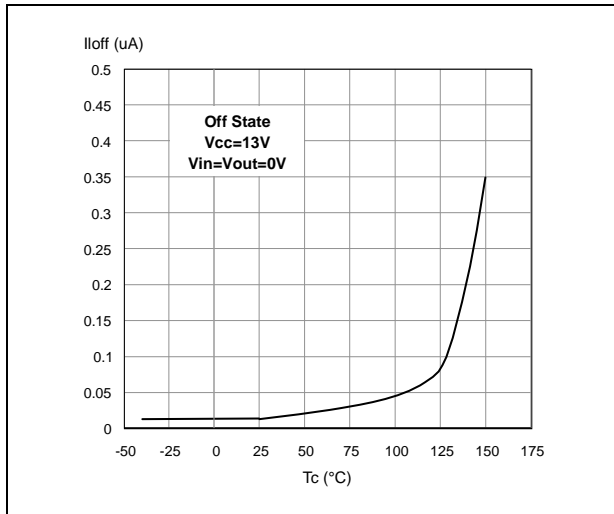


Figure 12. High level input current

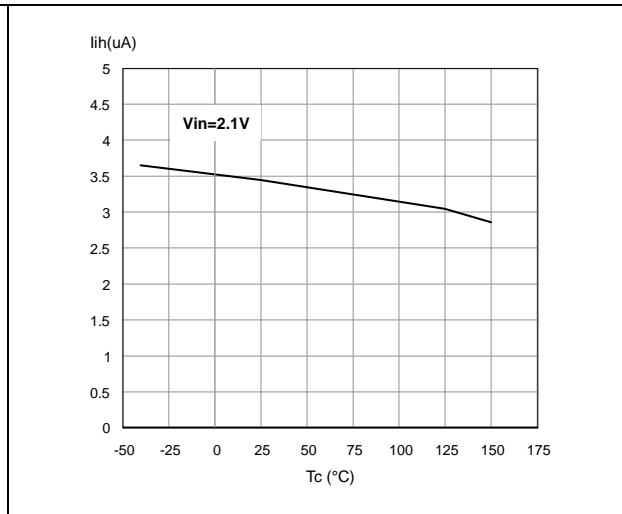


Figure 13. Input clamp voltage

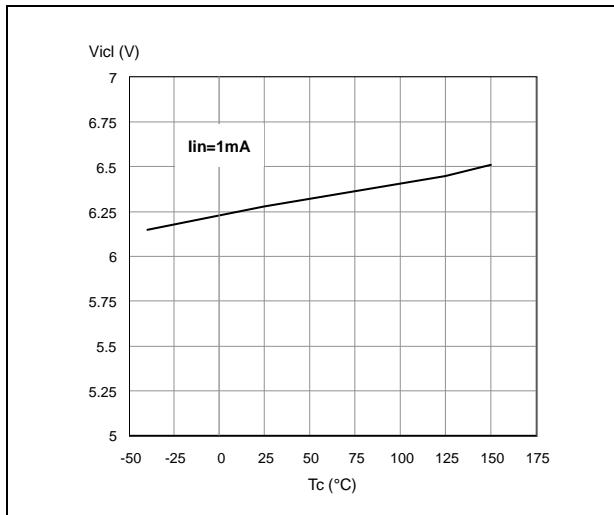


Figure 14. Input high level

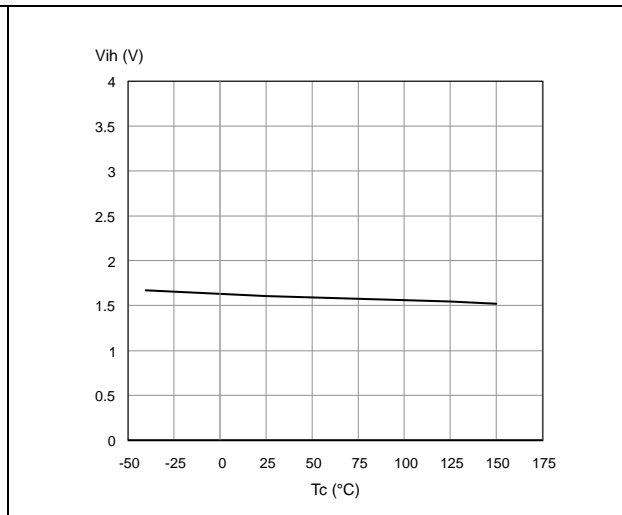


Figure 15. Input low level

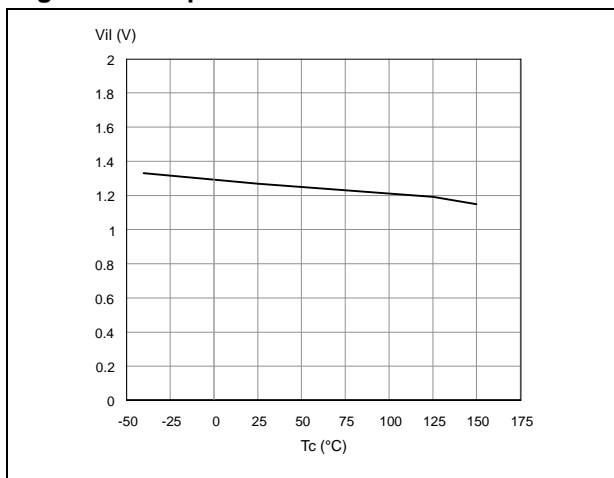


Figure 16. Input hysteresis voltage

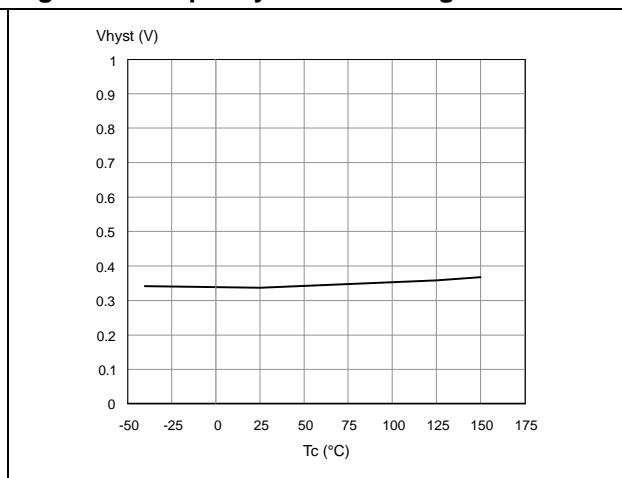


Figure 17. On-state resistance vs T_{case}

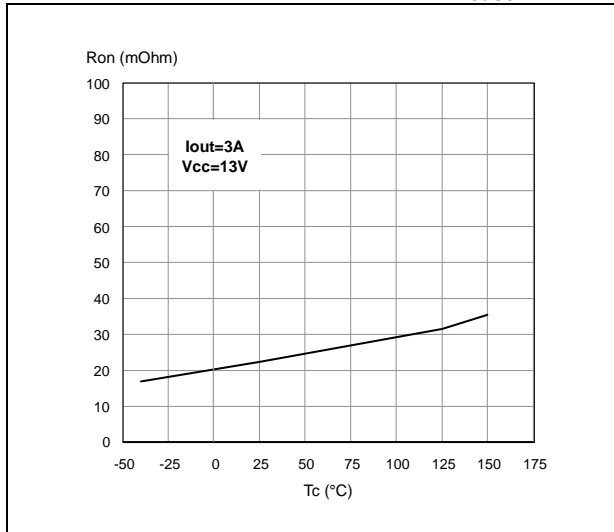


Figure 18. On-state resistance vs V_{CC}

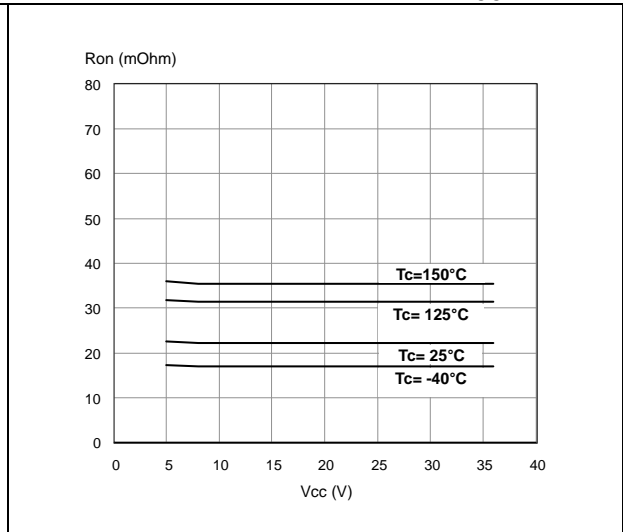


Figure 19. Undervoltage shutdown

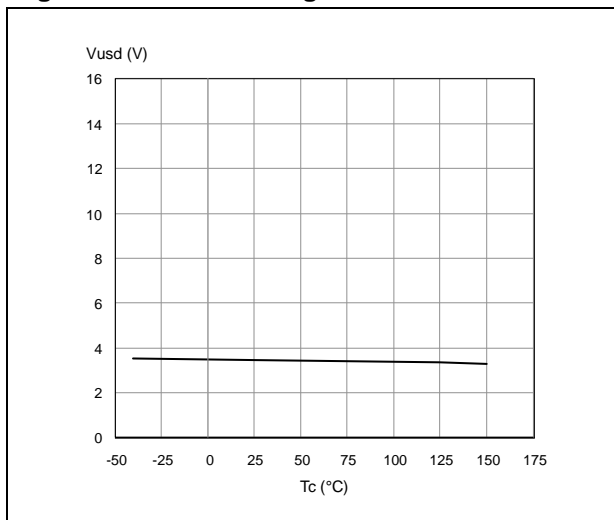


Figure 20. I_{LIMH} vs T_{case}

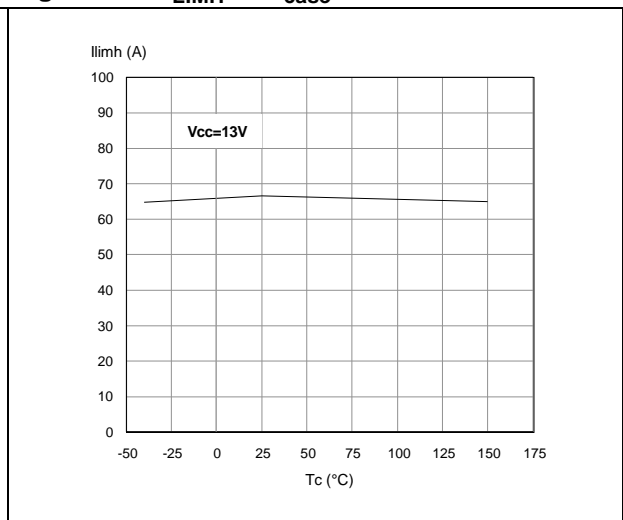


Figure 21. Turn-on voltage slope

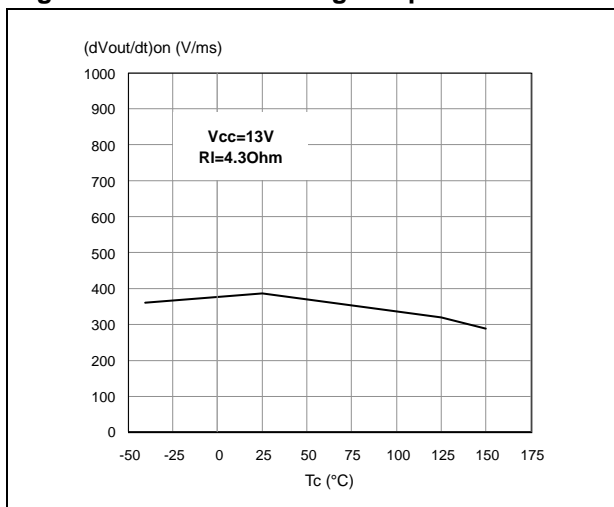


Figure 22. Turn-off voltage slope

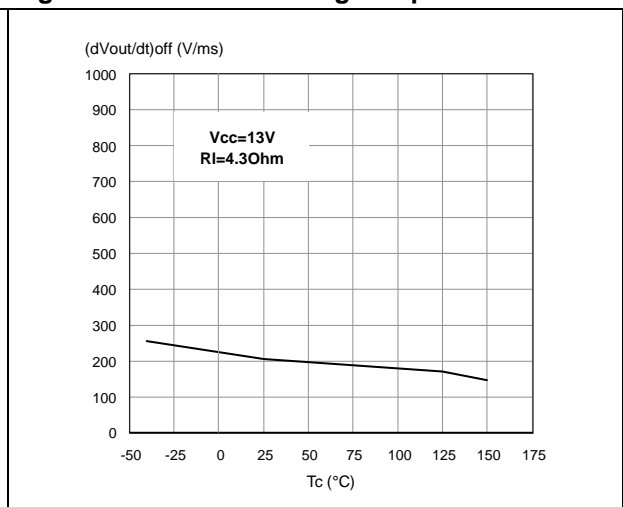


Figure 23. CS_DIS high level voltage

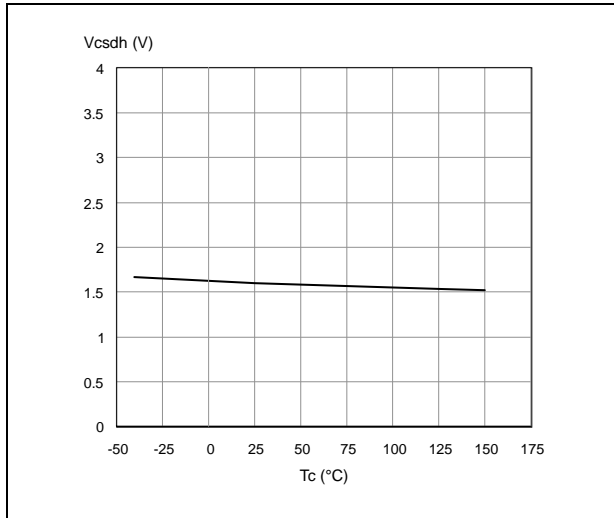


Figure 24. CS_DIS low level voltage

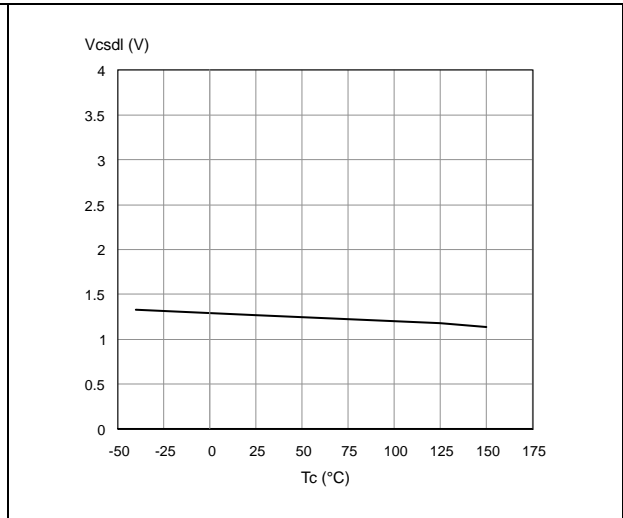
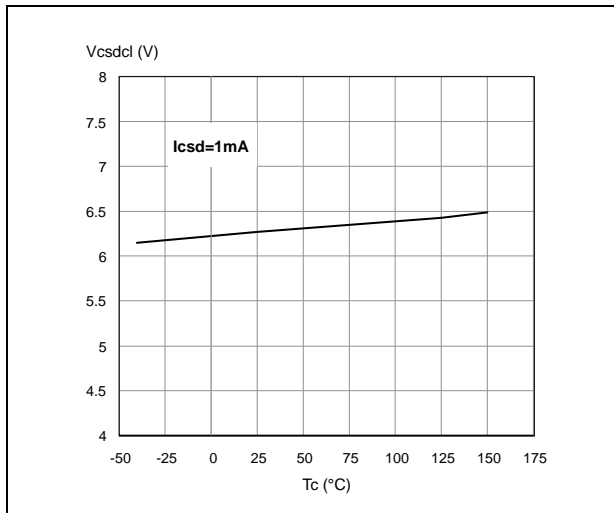
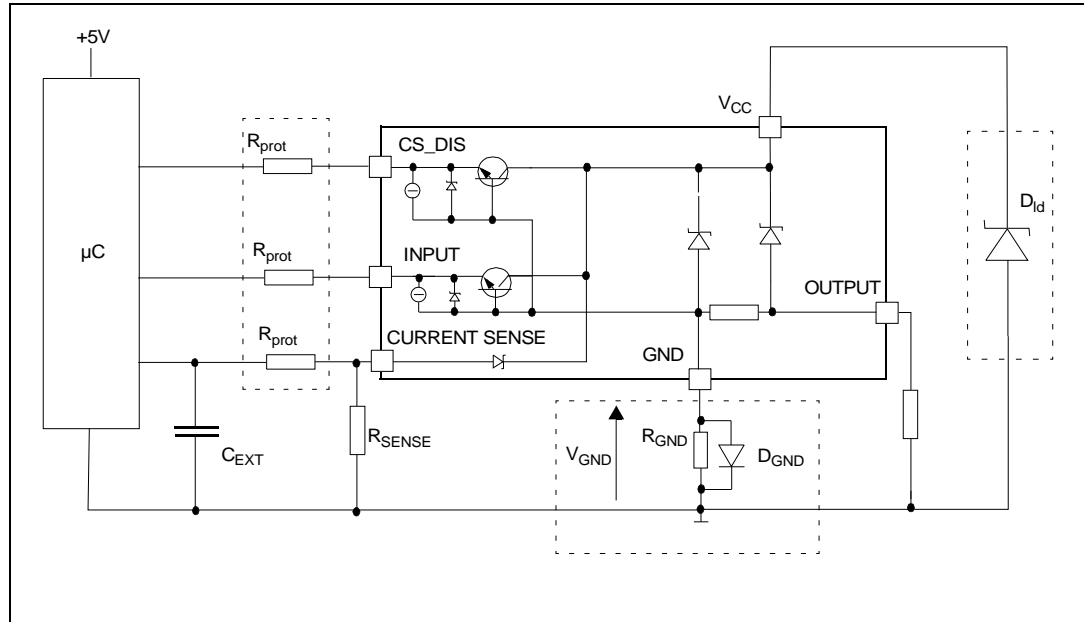


Figure 25. CS_DIS clamp voltage



3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This first solution can be used with any type of load.

The following formulas indicate how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC} < 0 during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared among several different HSDs. Please note that the value of this resistor is calculated with formula (1), where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground, the R_{GND} produces a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor, then ST suggests to utilize the following Solution 2.

3.1.2 Solution 2: diode (D_{GND}) in the ground line

If the device drives an inductive load, insert a resistor ($R_{GND} = 1k\Omega$) in parallel to D_{GND} .

This small signal diode can be safely shared among several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2:2004E table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert an in-line resistor (R_{prot}) to prevent the μC I/Os pins from latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

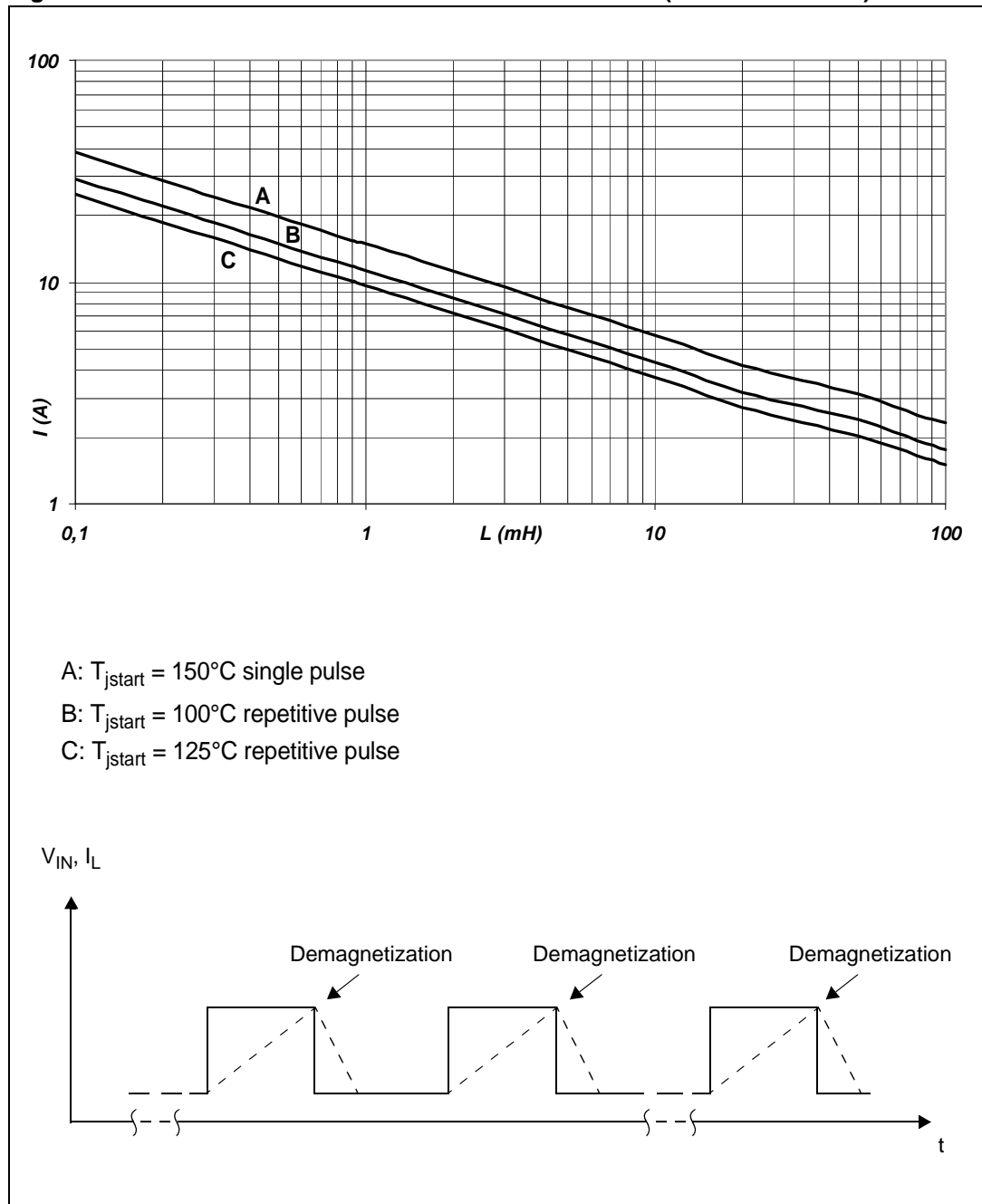
$$\text{For } V_{CCpeak} = -100V \text{ and } I_{latchup} \geq 20mA; V_{OH\mu C} \geq 4.5V$$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$.

3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 27. Maximum turn-off current versus inductance (for each channel)

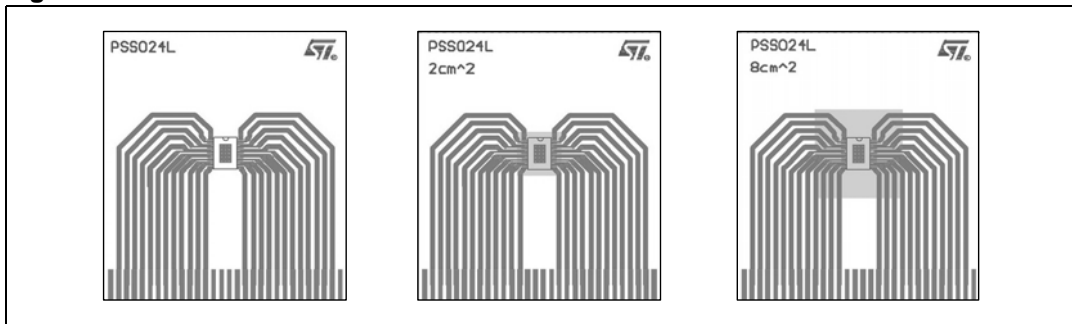


Note: Values are generated with $R_L = 0 \Omega$.
 In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and thermal data

4.1 PowerSSO-24™ thermal data

Figure 28. PowerSSO-24™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 77mm x 86mm, PCB thickness = 1.6mm, Cu thickness = 70µm (front and back side), Copper areas: from minimum pad layout to 8cm²).

Figure 29. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

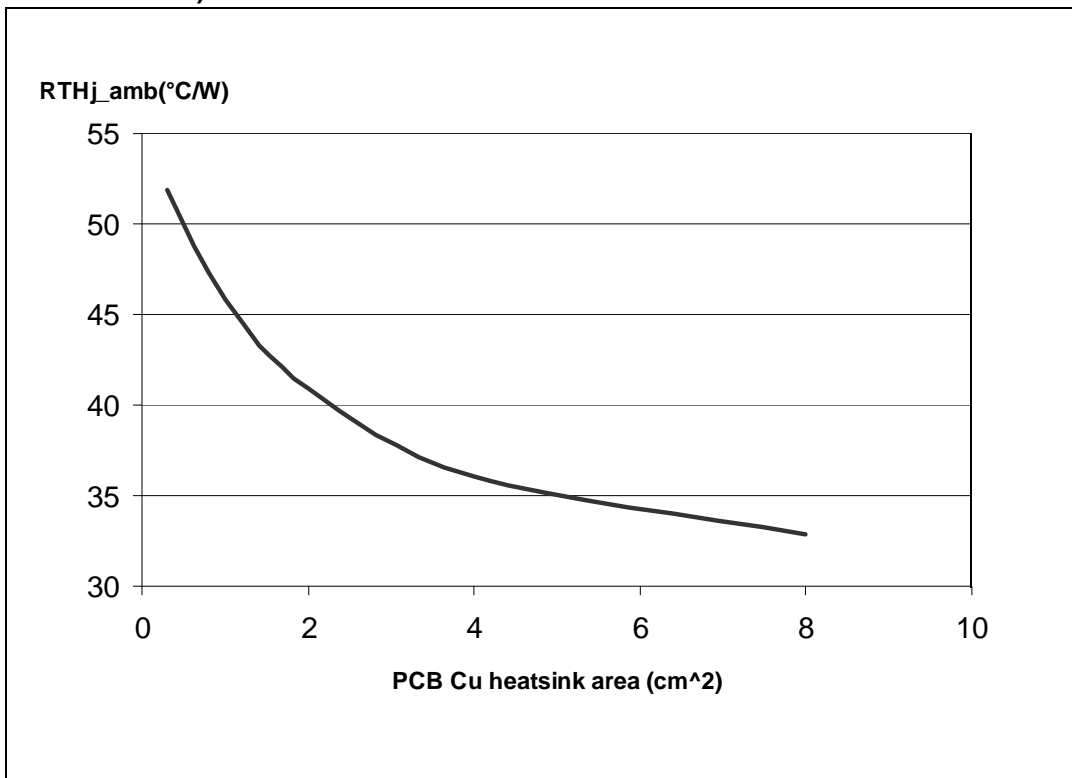
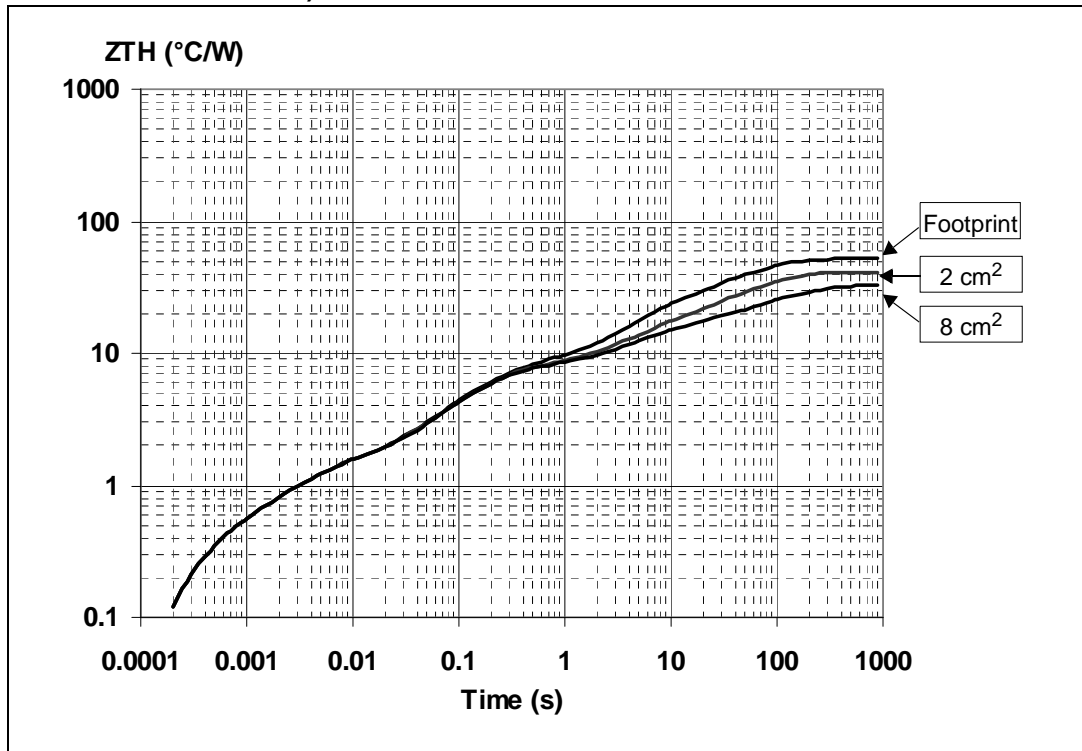


Figure 30. PowerSSO-24™ thermal impedance junction to ambient single pulse (one channel ON)

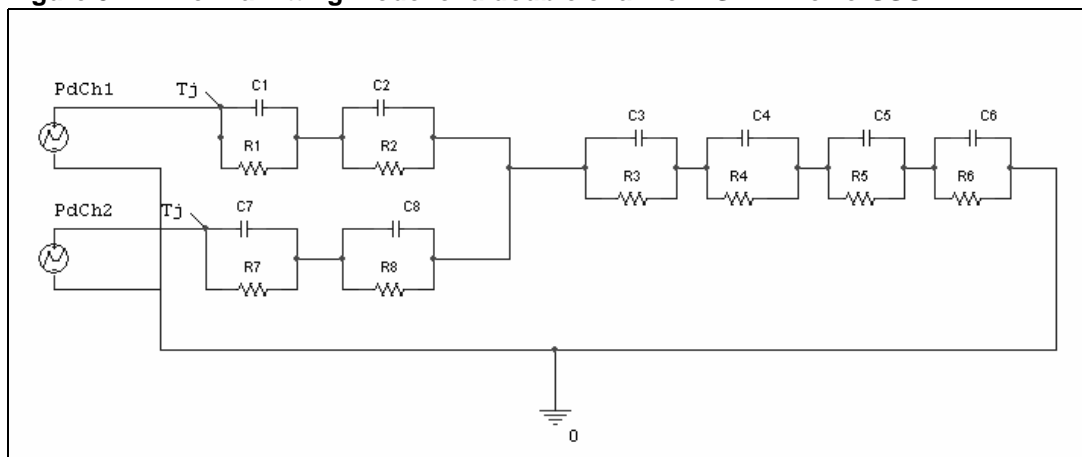


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24™(1)



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

| Area/Island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|----|----|
| R1 (°C/W) | 0.28 | | |
| R2 (°C/W) | 0.9 | | |
| R3 (°C/W) | 6 | | |
| R4 (°C/W) | 7.7 | | |
| R5 (°C/W) | 9 | 9 | 8 |
| R6 (°C/W) | 28 | 17 | 10 |
| R7 (°C/W) | 0.28 | | |
| R8 (°C/W) | 0.9 | | |
| C1 (W.s/°C) | 0.001 | | |
| C2 (W.s/°C) | 0.003 | | |
| C3 (W.s/°C) | 0.025 | | |
| C4 (W.s/°C) | 0.75 | | |
| C5 (W.s/°C) | 1 | 4 | 9 |
| C6 (W.s/°C) | 2.2 | 5 | 17 |
| C7 (W.s/°C) | 0.001 | | |
| C8 (W.s/°C) | 0.003 | | |

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 32. PowerSSO-24™ package dimensions

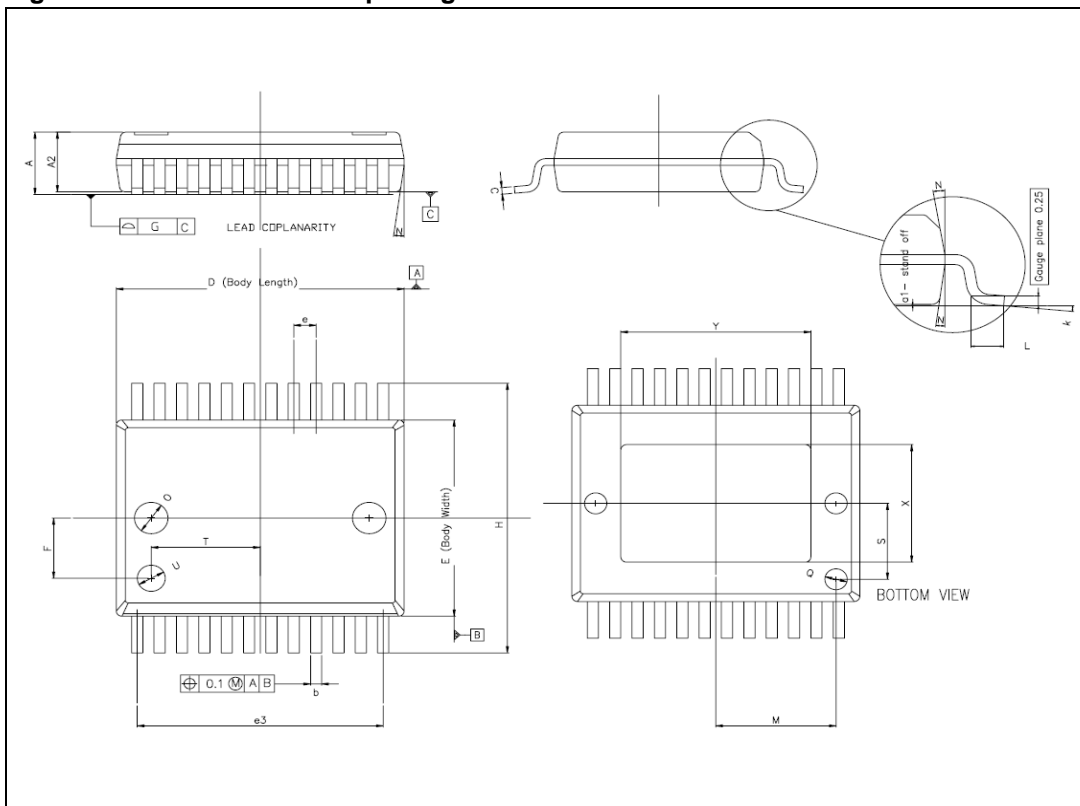


Table 16. PowerSSO-24™ mechanical data

| Symbol | Millimeters | | |
|--------|-------------|------|-------|
| | Min | Typ | Max |
| A | | | 2.45 |
| A2 | 2.15 | | 2.35 |
| a1 | 0 | | 0.1 |
| b | 0.33 | | 0.51 |
| c | 0.23 | | 0.32 |
| D | 10.10 | | 10.50 |
| E | 7.4 | | 7.6 |
| e | | 0.8 | |
| e3 | | 8.8 | |
| F | | 2.3 | |
| G | | | 0.1 |
| H | 10.1 | | 10.5 |
| h | | | 0.4 |
| k | 0° | | 8° |
| L | 0.55 | | 0.85 |
| O | | 1.2 | |
| Q | | 0.8 | |
| S | | 2.9 | |
| T | | 3.65 | |
| U | | 1.0 | |
| N | | | 10° |
| X | 4.1 | | 4.7 |
| Y | 6.5 | | 7.1 |

5.3 Packing information

Figure 33. PowerSSO-24™ tube shipment (no suffix)

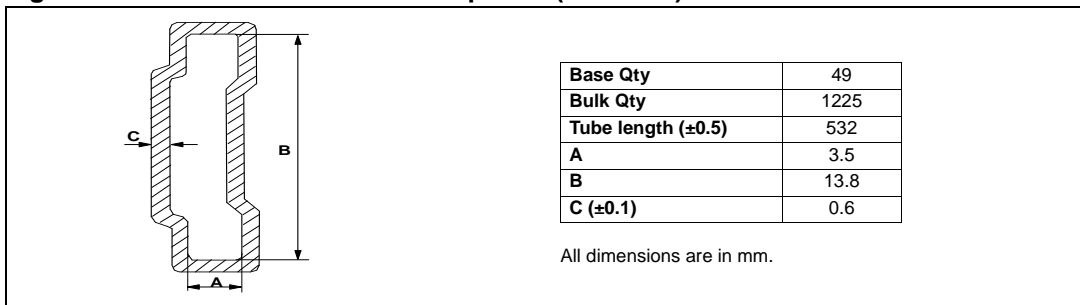
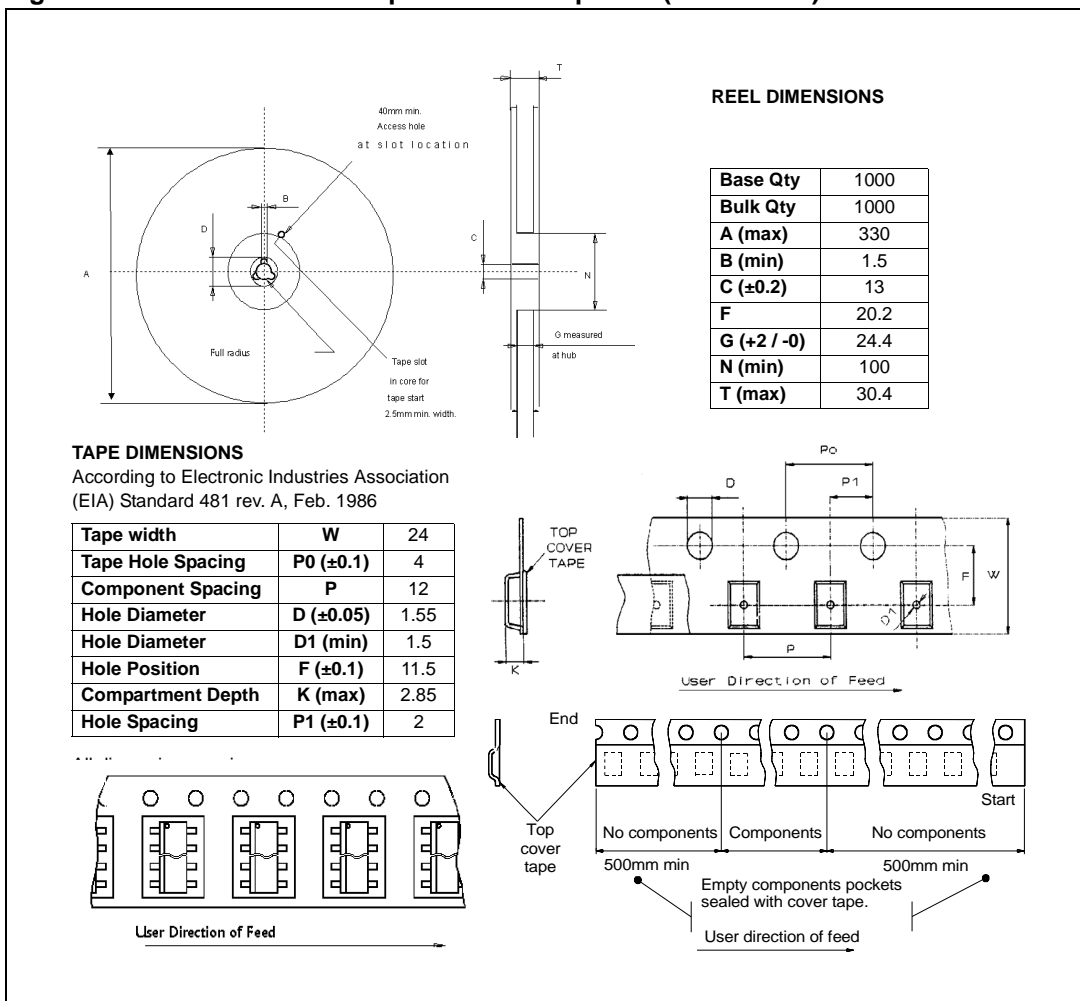


Figure 34. PowerSSO-24™ tape and reel shipment (suffix “TR”)



6 Revision history

Table 17. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 11-Apr-2006 | 1 | Initial release |
| 30-Mar-2007 | 2 | Reformatted. <i>Table 4 on page 7</i> : updated E_{MAX} entries. <i>Table 6 on page 9</i> : updated V_F test conditions. <i>Table 7 on page 9</i> : set T_j condition to 25°C” <i>Table 10 on page 11</i> : added dK_1/K_1 , dK_2/K_2 , dK_3/K_3 , $\Delta t_{DSENSE2H}$, $t_{DSENSE2H}$ values and note. Added <i>Figure 5: Delay response time between rising edge of output current and rising edge of Current Sense (CS enabled) on page 13</i> . Updated <i>Figure 7: IOUT/ISENSE vs IOUT⁽¹⁾ on page 14</i> . Added <i>Figure 8: Maximum current sense ratio drift vs load current⁽¹⁾ on page 14</i> . <i>Table 12 on page 16</i> : Updated Test Level values III and IV for test pulse 5b and notes. Added <i>Section 3.4: Maximum demagnetization energy (VCC = 13.5V) on page 23</i> . Added <i>ECOPACK® packages</i> information. |
| 01-Jun-2007 | 3 | <i>Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-24™⁽¹⁾</i> : added note. |
| 03-Jul-2007 | 4 | Updated <i>Figure 1: Block diagram</i> and <i>Figure 2: Configuration diagram (top view)</i> . |
| 24-Jul-2007 | 5 | Updated <i>Table 16: PowerSSO-24™ mechanical data</i> . |
| 12-Dec-2007 | 6 | Updated <i>Table 10: Current sense (8V < VCC < 16V)</i> : – added dK_0/K_0 values – changed dK_3/K_3 values from ± 3 to $\pm 4\%$ – changed $\Delta t_{DSENSE2H}$ value from 110 to 200 μs – added I_{OL} parameter Updated <i>Figure 8: Maximum current sense ratio drift vs load current⁽¹⁾</i> with new dK/K values. |
| 12-Feb-2008 | 7 | Corrected typing error in <i>Table 10: Current sense (8V < VCC < 16V)</i> : changed I_{OL} test condition from $V_{IN} = 0V$ to $V_{IN} = 5V$. |
| 10-Apr-2008 | 8 | Corrected <i>Figure 27: Maximum turn-off current versus inductance (for each channel)</i> |
| 02-Jul-2009 | 9 | <i>Table 16: PowerSSO-24™ mechanical data</i> : – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F row – Updated k values |

Table 17. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 23-Jul-2009 | 10 | Updated Figure 32: PowerSSO-24™ package dimensions . Updated Table 16: PowerSSO-24™ mechanical data : – Deleted G1 row – Added O, Q, S, T and U rows |
| 23-Sep-2013 | 11 | Updated Disclaimer. |

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