PRELIMINARY

Analog Signal Input Class-D Amplifier with DC-DC Converter for Piezo Speaker

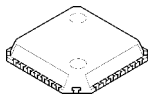
■ GENERAL DESCRIPTION

The **NJU8753** is an analog signal input monaural class D power amplifier with DC-DC converter for Piezo speaker. Input part operates on 2.85V(typ) and a built-in DC-DC converter generates variable output voltage(up to 12V) with input voltage(2.6 to 4.2V). Therefore, it drives Piezo speaker with louder sound and high efficiency.

The **NJU8753** incorporates BTL amplifier, which eliminate AC coupling capacitors, capable of driving Piezo speaker with simple external LC low-pass filters.

Class D operation achieves lower power operation for Piezo speaker, thus the **NJU8753** is suited for battery- powered applications.

■ PACKAGE OUTLINE

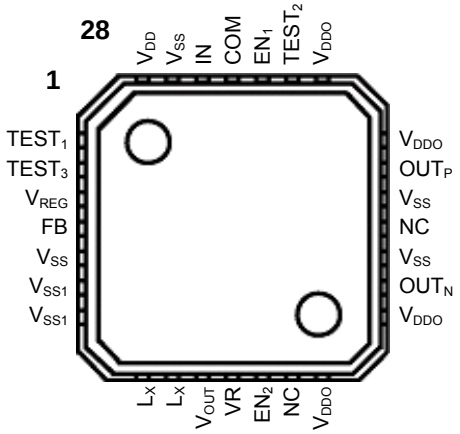


NJU8753KN1

■ FEATURES

- Operating Voltage :2.6 to 3.6V(V_{DD}, V_{REG})
  :2.6 to 4.2V(V_{BAT})
- Output voltage :8Vrms(Typ.) @V_{DDO}=10.0V
- Piezo Speaker Driving
- 1-channel Analog Signal Input, 1-channel BTL output
- Standby(Hi-Z),
- Built-in DC-DC Converter
- Built-in Low Voltage Detector
- Built-in Short Protector
- CMOS Technology
- Package Outline :QFN28

■ TERMINAL CONFIGURATION



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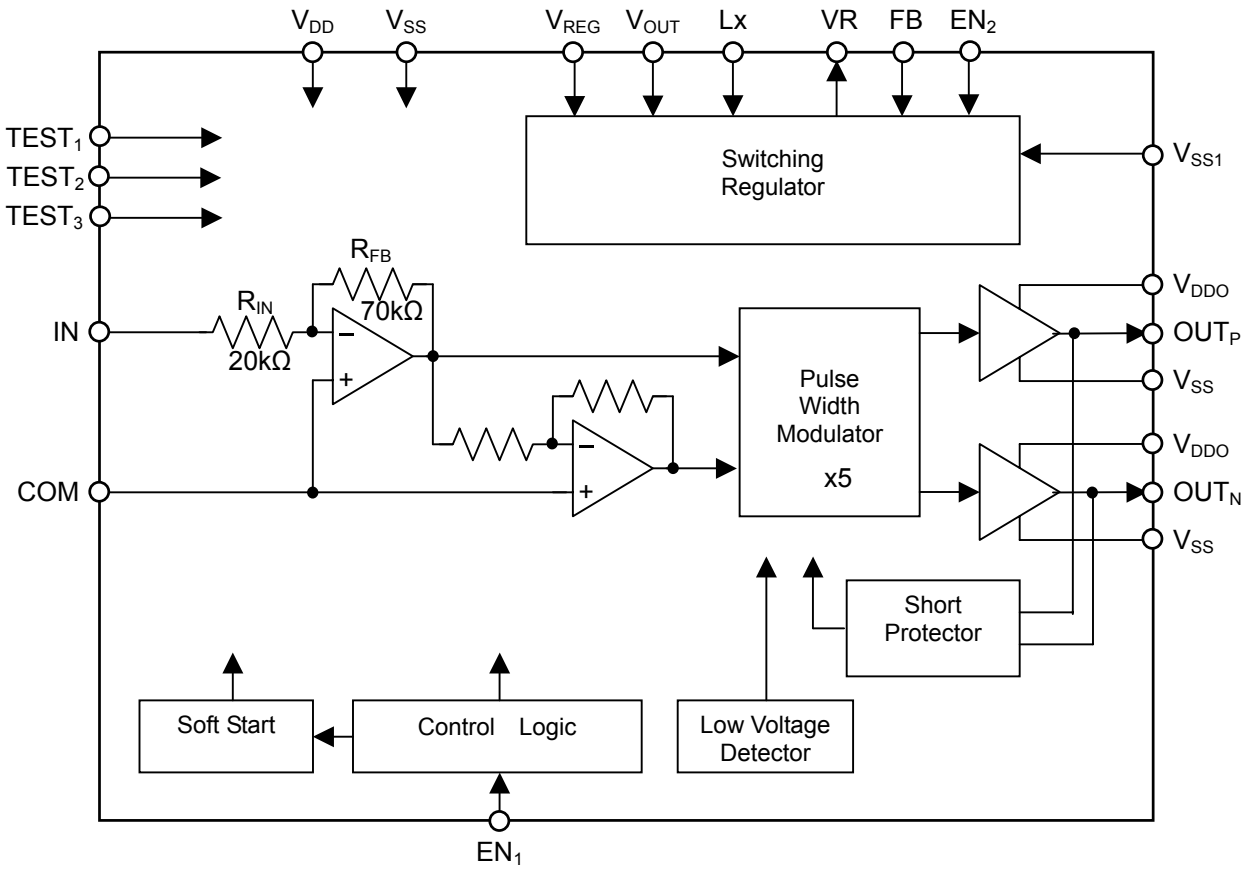
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
1, 2, 23	$TEST_1$ $TEST_3$ $TEST_2$	I	Maker test These terminals must be connected to GND.
3	V_{REG}	–	Switching regulator Power Supply : V_{REG}=2.85V
4	FB	I	Switching regulator Feedback resistor connection
5, 17, 19, 27	V_{SS}	–	Power GND : V_{SS}=0V
6,7	V_{SS1}	–	Switching regulator Power GND: V_{SS1}=0V
8,9	Lx	I	Switching regulator coil connection
10	V_{OUT}	–	Switching regulator Power Supply : V_{OUT}=10.0V
11	VR	O	Switching regulator step-up voltage setting resistor connection
12	EN_2	I	Switching regulator Standby Control High : Step-up ON Low : Standby ON This terminal must be connected to V_{REG} when step-up ON.
13, 18	NC	–	Non connection
14, 15, 21, 22	V_{DDO}	–	Output Power supply
16	OUT_N	O	Negative Output
20	OUT_P	O	Positive Output
24	EN_1	I	Power Amplifier Standby Control High : Standby OFF Low : Standby ON This terminal must be connected to V_{DD} when Standby OFF.
25	COM	–	Analog common
26	IN	I	Audio Signal Input
28	V_{DD}	–	Power Supply: V_{DD}=2.85V

* V_{SS} terminals(pins 5 and 17 and 19 and 27), V_{SS1} terminals(pins 6 and 7) should be connected at the nearest point to the IC.
* V_{DDO} terminals(pins 14 and 15 and 21 and 22) should be connected at the nearest point to the IC.
* OUT_P terminal(pin 20), OUT_N terminal(pin 16) require Schottky barrier diodes. (Refer to the “TYPICAL APPLICATION CIRCUIT”)
* Lx terminals(pins 8 and 9) require caution to the extraneous noise including the ESD(electrical static discharge) because the ESD protection can't be designed as well as other terminals.
Require extra caution when the input voltage (V_{BAT}: Refer to the “TYPICAL APPLICATION CIRCUIT”) to the Lx terminal is supplied directly from the external because the extraneous noise including the ESD appears easily.

■ FUNCTIONAL DESCRIPTION

(1) Input signal

The amount of current passing through a capacitive load increases proportionately with frequency of audio signal. Input filters should be put in the input line to reduce load current at high frequency-band.

The 1st–order RC type HPF(High Pass Filter) and the 1st-order RC type LPF(Low Pass Filter) are composed of input filters.

f_{CH1}(Cut-off frequency of HPF) and f_{CL1}(Cut-off frequency of LPF) are determined by input resistance(R_{IN}), resistor for LPF(R_{LPF}), capacitor for LPF(C_{LPF}) and AC coupling capacitor(C_C). (R_{LPF}, C_{LPF}, C_C: Refer to the "TYPICAL APPLICATION CIRCUIT")

When R_{IN}=20kΩ, R_{LPF}=2.4kΩ and C_{LPF}=0.022μF, C_C=2.2μF, f_{CH1} and f_{CL1} are roughly calculated as following expressions.

$$f_{CH1} = \frac{1}{2\pi(R_{IN} + R_{LPF})C_C} = \frac{1}{2 \times 3.14 \times (20 \times 10^3 + 2.4 \times 10^3) \times 2.2 \times 10^{-6}} \cong 5[\mathrm{Hz}]$$

$$f_{CL1} = \frac{1}{2\pi(R_{IN} // R_{LPF})C_{LPF}} = \frac{1}{2 \times 3.14 \times (20 \times 10^3 // 2.4 \times 10^3) \times 0.022 \times 10^{-6}} \cong 3[\mathrm{kHz}]$$

When SBDs are added between OUT_P and V_{SS}, OUT_N and V_{SS}, the f_{CL1}(Cut-off frequency of LPF) must be less than 7KHz. When SBDs are not added, the f_{CL1} must be less than 3KHz.

Input amplitude impressed to IN terminal of IC (V_{IC}) must be less than V_{DD}[Vpp].
When V_{DD}=2.85V, R_{LPF}=2.4kΩ , Audio signal maximum input level V_{INMAX} for considering as VIC<=VDD [Vpp] V_{INMAX} are roughly calculated as following expressions.

$$V_{INMAX} = \frac{(R_{LPF} + R_{IN}) \times V_{IC}}{R_{IN}} = \frac{(2.4 \times 10^3 + 20 \times 10^3) \times 2.85}{20 \times 10^3} \cong 3.1[Vpp]$$

(2) Output signal

The OUT_P and OUT_N generate PWM output signals, which will be converted to analog signal via external 2nd-order or higher LC filter.

LC type LPF is composed of the coil (L) and Piezo Speaker (C_L).

The dump resistance (R_{DAMP}) is connected between the OUT_N terminal and the coil between the OUT_P terminal and the coil to reduce the cut off frequency (fc) of LPF consumption electric current neighborhood signal input.

Set it up so that the value of L, C_L and R_{DAMP} may become Gain(Q) <1 of LPF in fc. (L, C_L, C_{OUT}, R_{DAMP} : Refer to the "TYPICAL APPLICATION CIRCUIT")

When L=47μH, C_L=2.0μF, C_{OUT}=0.1μF, R_{DAMP} =4.7Ω, R_{DCR}=0.2Ω, LPF(f_c) and Q are roughly calculated as following expressions.

$$fc = \frac{1}{2\pi\sqrt{L(2C_L + C_{OUT})}} = \frac{1}{2 \times 3.14 \times \sqrt{47 \times 10^{-6} \times (2 \times 2.0 \times 10^{-6} + 0.1 \times 10^{-6})}} \cong 11[\mathrm{kHz}]$$

$$Q = \frac{1}{(R_{DAMP} + R_{DCR})}\sqrt{\frac{L}{(2C_L + C_{OUT})}} = \frac{1}{(4.7 + 0.2)} \times \sqrt{\frac{47 \times 10^{-6}}{(2 \times 2.0 \times 10^{-6} + 0.1 \times 10^{-6})}} \cong 0.7$$

(3) Power Amplifier Standby

By setting the EN_1 terminal to "L", the standby mode is enabled. In the standby mode, the entire functions of the **NJU8753** enter a low-power state, and the output terminals (OUT_P and OUT_N) are high impedance.

(4) Low Voltage Detector

When the power supply voltage drops down to below V_{DD}(MIN), the internal oscillation is halted for prevention to generate unwanted frequency, and the output terminals (OUT_P, OUT_N) become in high impedance.

(5) Step-up switching regulator

The switching regulator is used as power supply(V_{DDO}) for power amplifier of class-D. The PFM controlled switching regulator works with external components, which are coil, capacitor, Schottky barrier diode and step-up voltage setting resistance.

By setting the EN_2 terminal to "H", the step-up operation is enabled, and in case of "L", standby mode is enabled.

Step-up voltage is set by internal reference voltage(V_{REG} / 2) and external resistors.

The step-up voltage can be calculated by the following methods:

<Calculation of the step-up voltage>

The step-up voltage is determined by internal reference voltage(V_{REF}), R_1 and R_2. (See Figure.2)

example: V_{DD}=2.85V, Internal reference voltage(V_{REF}) = V_{REG} / 2=1.425[V], R_1=2MΩ, R_2=330kΩ"
Step-up voltage[V] = $V_{REF}\times((R_1+R_2)/R_2)$ = 1.425×((2M + 330k)/330k) = 10.06[V] "

Note)

*1 Apply V_{REG} first, next V_{BAT}. Otherwise, the voltage stress may cause a permanent damage to the IC.

*2 The kickback voltage by the step-up voltage operation varies with the fixed number of the external components and the PCB patterns. Output power supply(V_{DDO}) must not exceed the absolute maximum rating.

(6) Short Circuit Protection

The short protector, which protects the **NJU8753** against high short-circuit current, turns off the output driver. After about 5 seconds from the protection, the **NJU8753** returns to normal operation. The short protector functions at the following accidents.

-Short between OUT_P and OUT_N
-Short between OUT_P and V_{SS}
-Short between OUT_N and V_{SS}

Note)

*1 The detectable current and the period for the protection depend on the power supply voltage, chip temperature and ambient temperature.

*2 The short protector is not effective for a long term short-circuit current but for an instantaneous accident. Continuous high-current may cause permanent damage to the **NJU8753**.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT	Note
Supply Voltage	V_{DD}		-0.3 to +4.0	V	
	V_{REG}		-0.3 to +4.0	V	
	V_{DDO}	With SBDs	-0.3 to +14.0	V	6
		Without SBDs	-0.3 to +9.5		
L_X Input Voltage	V_{LX}	With SBDs	-0.3 to +14.0	V	6
		Without SBDs.	-0.3 to +9.5		
FB Input Voltage	V_{FB}		-0.3 to +4.0	V	
Input Voltage	Vin		-0.3 to V_{DD}+0.3	V	
Operating Temperature	Topr		-40 to +85	°C	
Storage Temperature	Tstg		-40 to +125	°C	
Power Dissipation	P_D		640 *	mW	

* : Mounted on two-layer board of based on the JEDEC.

Note 1) All voltage are relative to “VSS= 0V” reference.

Note 2) The LSI must be used inside of the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

■ ELECTRICAL CHARACTERISTIC

(Ta=25°C, V_{DD}=V_{REG}=2.85V, V_{BAT}=3.7V, V_{DDO}=10V, V_{SS}=V_{SS1}=0V,
$TEST_1$=$TEST_2$=$TEST_3$=0V, EN_1=EN_2=2.85V,
Input Signal=1kHz, Input Signal Level=150mVrms,Frequency Band=20Hz to 20kHz,
Load Impedance=2.0μF, 2nd-order 11kHz LC Filter(Q=0.7),
When the SBDs are connected between OUT_P and V_{SS}, OUT_N and V_{SS}.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
V_{DD} Supply Voltage	V_{DD}		2.6	2.85	3.6	V	
V_{REG} Supply Voltage	V_{REG}		2.6	2.85	3.6	V	
V_{BAT} Input Voltage	V_{BAT}		2.6	3.7	4.2	V	
V_{DDO} Supply Voltage	V_{DDO}	With SBDs	6.5	10.0	12.0	V	6
		Without SBDs.	6.5	7.5	8.5		
Input Impedance	Z_{IN}	IN terminal	-	20	-	KΩ	
Voltage Gain	A_V		-	31	-	dB	
THD+N	THD	Input Signal Level =200mVrms	-	0.05	0.08	%	4
Maximum Output	Vo	Output THD+N=10%	-	8.0	-	Vrms	
S/N	SN	A weight	-	80	-	dB	4
Operating Current(Standby)	I_{ST}	EN_1=EN_2=0V	-	-	1	μA	
Operating Current (No signal input)	I_{SS}	No-load operating No Signal Input	-	10	15	mA	
Input Voltage	V_{IH}	EN_1, EN_2 terminals	0.7V_{DD}	-	V_{DD}	V	
	V_{IL}	EN_1, EN_2 terminals	0	-	0.3V_{DD}	V	
Input Leakage Current	I_{LK}	EN_1, EN_2 terminals	-	-	±1.0	μA	
Switching regulator Oscillating Frequency	f_{OSC}		220	300	380	kHz	
Switching regulator Maximum Load Current	I_{OUT}	Step-up Voltage =10.0V V_{OUT}= 10.0V X 95%	50	-	-	mA	
Switching regulator Load Stability	ΔV_{OUT}	Step-up Voltage =10.0V I_{OUT} =10mA to 50mA	-	100	-	mV	

*The LSI must be used within the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

Note 3) Test system of the THD+N and S/N

The THD+N and S/N are tested in the system shown in Figure 1, where a 2nd-order LC LPF and another filter incorporated in an audio analyzer are used.

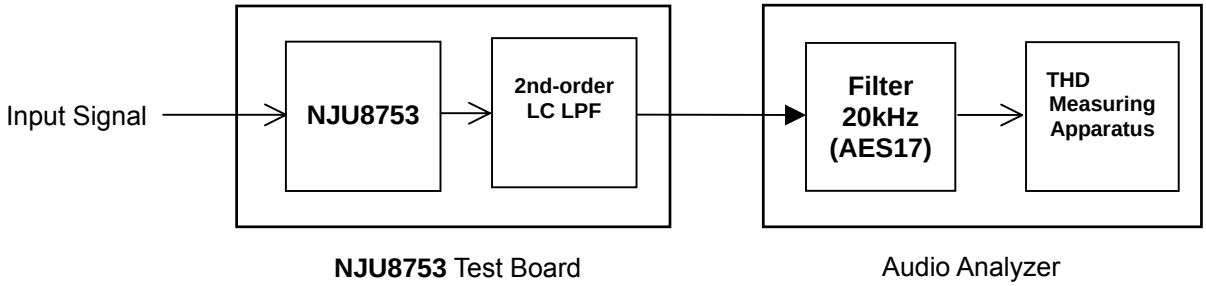


Figure 1. Output THD+N and S/N Test System

2nd-order LC LPF : Refer to “Typical Application Circuit”
Filters : 22Hz HPF + 20kHz LPF(AES17)
(with the A-Weight filter for S/N test)

■ TYPICAL APPLICATION CIRCUIT

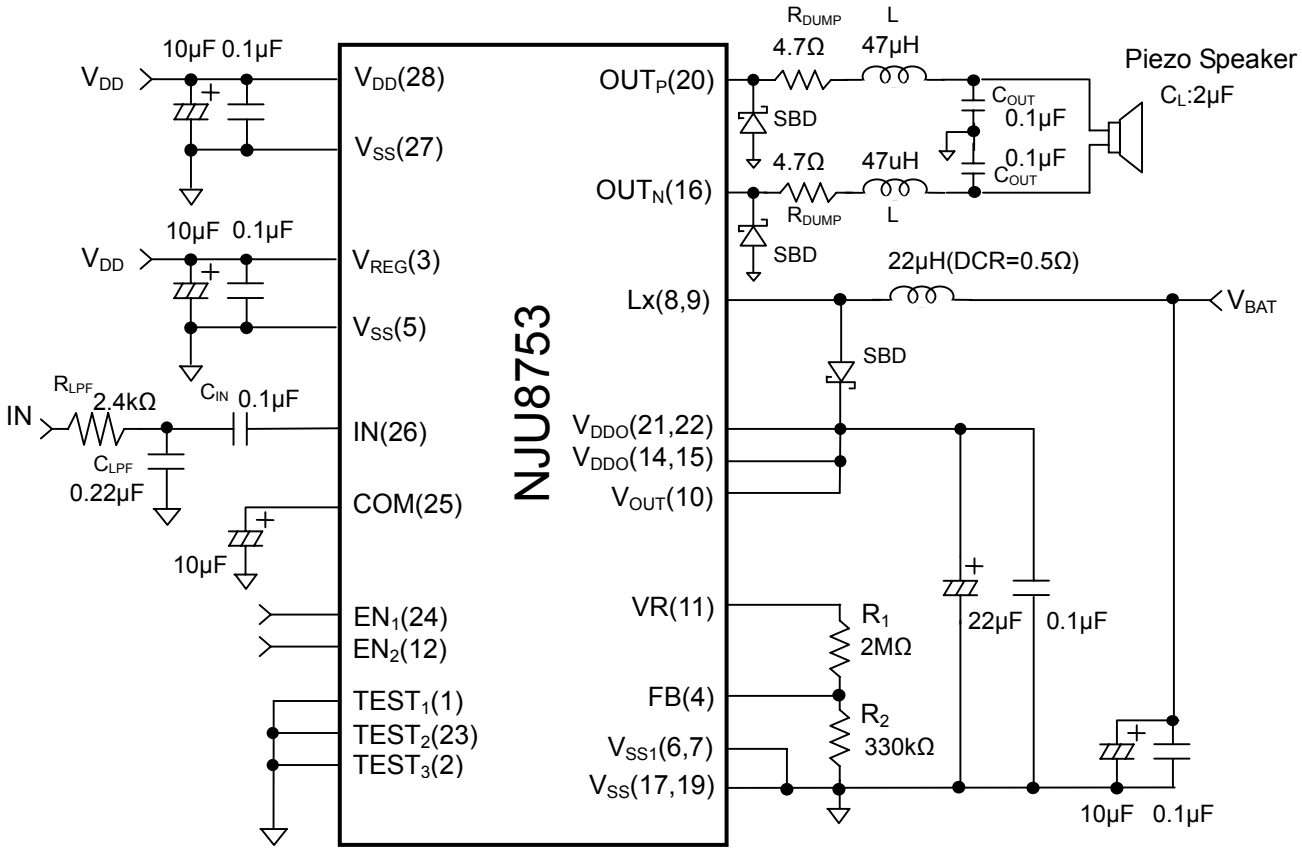


Figure 2. Application Circuit example

Note 4) De-coupling capacitors must be connected between each power supply terminal and GND.

Note 5) The LC filter and the schottky barrier diodes should be laid out nearest to the IC.
OUT_P terminal(pin 20), OUT_N terminal(pin 16) require schottky barrier diodes for terminal protection. When SBDs is not used, the V_{DDO} supply voltage maximum is 8.5V. (SBD: When Tj=125°C, IR=less than 10mA at reverse voltage12V*[1]. When Tj=25°C, Forward voltage (V_F) =0.45V, Forward current (I_F) =more than1A at more than 12V)
*1 Absolute maximum ratings is more than 20V.

Note 6) The LSI must be used inside of the following ratings. Otherwise, a stress may cause permanent damage to the regulator.

	SBDs are added	No SBDs
V_{DDO} (Supply Voltage)	MAX=12V	MAX=8.5V
Input cut-off frequency	MAX=7kHz	MAX=3kHz
Output cut-off frequency	MAX=15kHz	
Q (The gain of LPFat fc)	MAX=1	
Piezo Speaker	MAX=2.2μF	
The capacitor between V_{DDO} and V_{SS}	MAX=22μF	
The coil for Lx terminal	MIN=22μH	
Input voltage	MAX=V_{DD}[Vpp]	

Note 7) The transition time for EN_1 and EN_2 signals must be less than 100μs. Otherwise, a malfunction may be occurred.

Note 8) Apply V_{REG} first, next V_{BAT}. Otherwise, the voltage stress may cause a permanent damage to the IC. The V_{DDO} is not able to accept from external power supply. Therefore use the DC-DC converter of the NJU8753.

Note 9) The Lx terminals require caution to the extraneous noise including the ESD(electrical static discharge) because the ESD protection can't be designed as well as other terminals. Require extra caution when the input voltage (V_{BAT}) to the Lx terminal is supplied directly from the external because the extraneous noise including the ESD appears easily.

Note 10) The kickback voltage by the step-up voltage operation varies with the fixed number of the external components and the PCB patterns. Output power supply(V_{DDO}) must not exceed the absolute maximum rating.

Note 11) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please test the circuit carefully to fit your application. The cut off frequency of the LC filter influences the quality of sound. The Q factor of the LC filter must be less than “1”. Otherwise, the operating current increase when the frequency of input signal is closed to the cut off frequency.

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