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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR 2SJ673

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ673 is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ673	Isolated TO-220 (MP-45F)

FEATURES

• Super low on-state resistance

 $R_{DS(on)1}$ = 20 $m\Omega$ MAX. (VGS = -10 V, ID = -18 A)

 $R_{DS(on)2} = 31 \text{ m}\Omega \text{ MAX.} (V_{GS} = -4.0 \text{ V}, I_{D} = -18 \text{ A})$

- Low Ciss: Ciss = 4600 pF TYP.
- Built-in gate protection diode

(Isolated TO-220)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	-60	V
Gate to Source Voltage (V _{DS} = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓36	Α
Drain Current (pulse) Note1	D(pulse)	∓144	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	32	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	-36	Α
Single Avalanche Energy Note2	Eas	130	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

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ELECTRICAL CHARACTERISTICS (TA = 25°C)

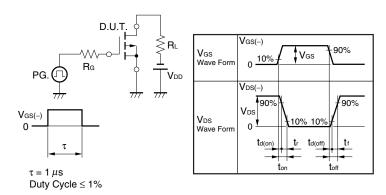
	•	•				
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -60 V, V _{GS} = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.5	-2.0	-2.5	V
Forward Transfer Admittance Note	y fs	V _{DS} = -10 V, I _D = -18 A	22			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = -10 V, I _D = -18 A		17	20	mΩ
	RDS(on)2	V _{GS} = -4.0 V, I _D = -18 A		22	31	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		4600		pF
Output Capacitance	Coss	V _{GS} = 0 V		820		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		330		pF
Turn-on Delay Time	t _{d(on)}	$V_{DD} = -30 \text{ V}, I_{D} = -18 \text{ A}$		14		ns
Rise Time	tr	V _{GS} = -10 V		14		ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		130		ns
Fall Time	t _f			50		ns
Total Gate Charge	Q _G	V _{DD} = -48 V		87		nC
Gate to Source Charge	Qgs	V _{GS} = -10 V		15		nC
Gate to Drain Charge	Q _{GD}	I _D = -36 A		22		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = -36 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	trr	I _F = -36 A, V _{GS} = 0 V		52		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		84		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

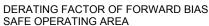
$V_{GS} = -20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

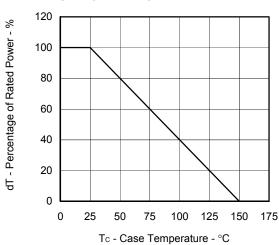
TEST CIRCUIT 2 SWITCHING TIME



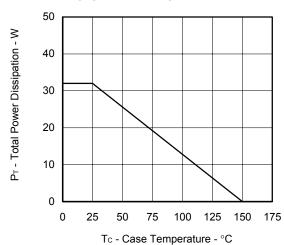
TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

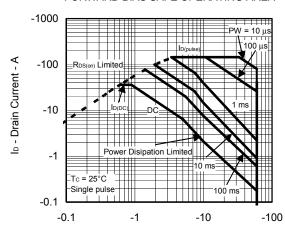




TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

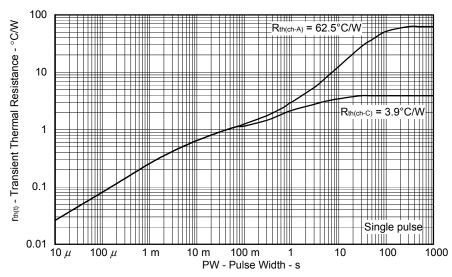


FORWARD BIAS SAFE OPERATING AREA



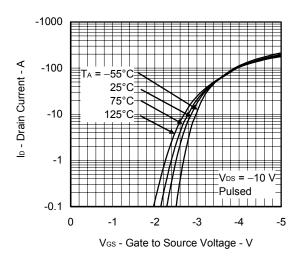
$V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

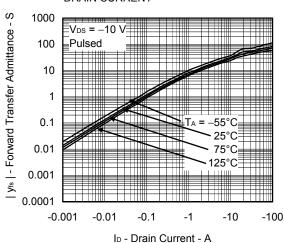


Data Sheet D17210EJ1V0DS 3

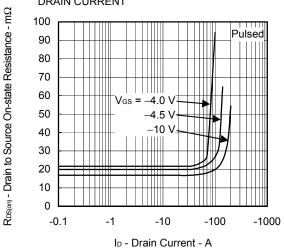
FORWARD TRANSFER CHARACTERISTICS



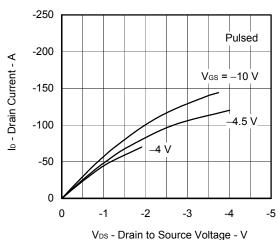
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



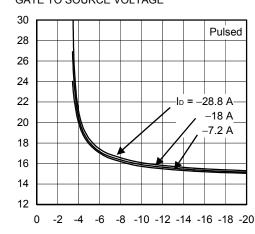
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

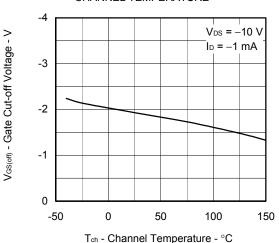


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

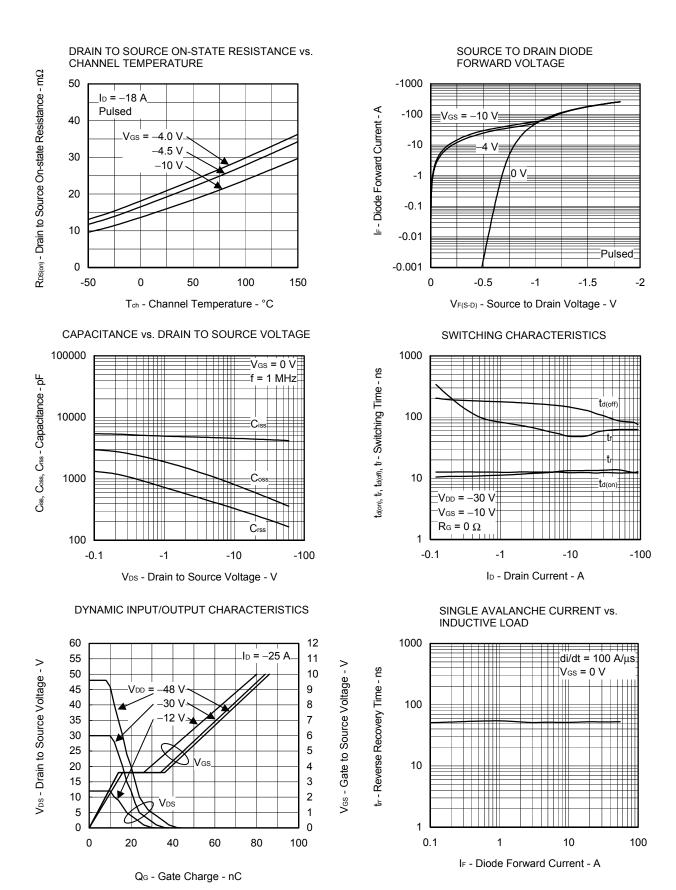


GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

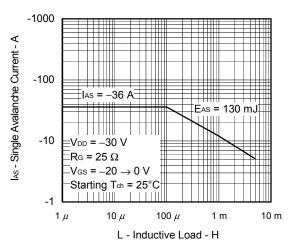
V_{GS} - Gate to Source Voltage - V



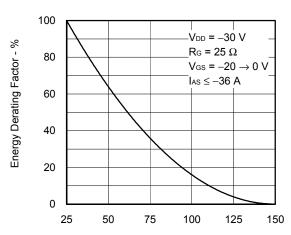
R_{DS(m)} - Drain to Source On-state Resistance - mΩ



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

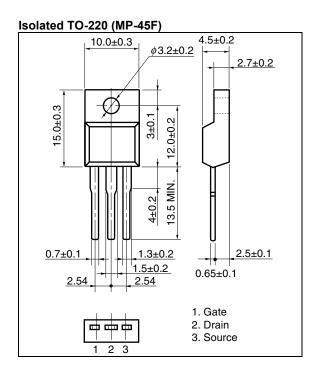


SINGLE AVALANCHE ENERGY DERATING FACTOR

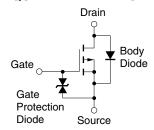


Starting Tch - Starting Channel Temperature - °C

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this debice.

Data Sheet D17210EJ1V0DS 7

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