CS3001
CS3002

Precision Low Voltage Amplifier; DC to 2 kHz

Features

- Low Offset: 10 μV Max
- Low Drift: 0.05 μV/°C Max
- Low Noise
  - 6 nV/√Hz @ 0.5 Hz
  - 0.1 to 10 Hz = 125 nVp-p
  - 1/f corner @ 0.08 Hz
- Open-Loop Voltage Gain
  - 1000 Trillion Typ
  - 10 Billion Min
- Rail-to-Rail Output Swing
- 1.8 mA Supply Current
- Slew rate: 5 V/μs

Applications

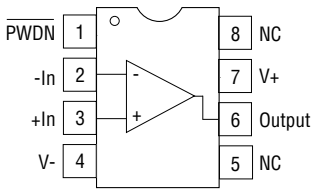
- Thermocouple/Thermopile Amplifiers
- Load Cell and Bridge Transducer Amplifiers
- Precision Instrumentation
- Battery-Powered Systems

Description

The CS3001 single amplifier and the CS3002 dual amplifier are designed for precision amplification of low level signals and are ideally suited to applications that require very high closed loop gains. These amplifiers achieve excellent offset stability, super high open loop gain, and low noise over time and temperature. The devices also exhibit excellent CMRR and PSRR. The common mode input range includes the negative supply rail. The amplifiers operate with any total supply voltage from 2.7 V to 6.7 V (±1.35 V to ±3.35 V).

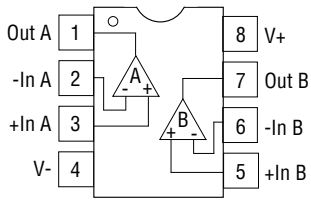
Pin Configurations

CS3001



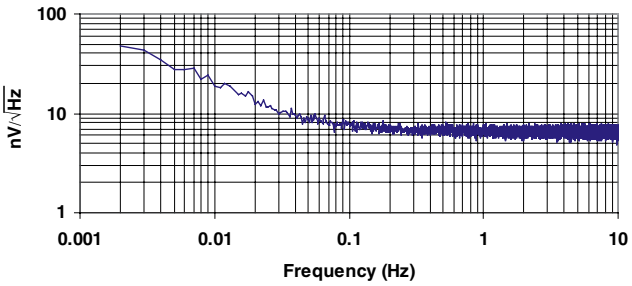
8-lead SOIC

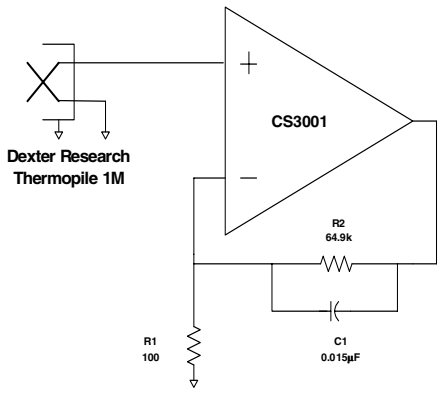
CS3002



8-lead SOIC

Noise vs. Frequency (Measured)





Thermopile Amplifier with a Gain of 650 V/V

Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
http://www.cirrus.com

TABLE OF CONTENTS

LIST OF FIGURES

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **<http://www.cirrus.com/corporate/contacts/sales.cfm>**

1. CHARACTERISTICS AND SPECIFICATIONS

1.1 Electrical Characteristics

V+ = +5 V, V- = 0V, VCM = 2.5 V (Note 1)

Parameter			CS3001/CS3002 Min	Typ	Max	Unit
Input Offset Voltage	(Note 2)	•	-	-	±10	µV
Average Input Offset Drift	(Note 2)	•	-	±0.01	±0.05	µV/ºC
Long Term Input Offset Voltage Stability				(Note 3)		
Input Bias Current	T_A = 25º C	 •	-	±100	±200 ±1000	pA pA
Input Offset Current	T_A = 25º C	 •	-	±200	±400 ±2000	pA pA
Input Noise Voltage Density	R_S = 100 Ω, f_0 = 1 Hz R_S = 100 Ω, f_0 = 1 kHz		- -	6 6		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Input Noise Voltage	0.1 to 10 Hz		-	125		nV_{p-p}
Input Noise Current Density	f_0 = 1 Hz		-	2		$pA/\sqrt{Hz}$
Input Noise Current	0.1 to 10 Hz		-	40		pA_{p-p}
Input Common Mode Voltage Range		•	-0.1	-	(V+)-1.25	V
Common Mode Rejection Ratio (dc)	(Note 4)	•	115	120	-	dB
Power Supply Rejection Ratio		•	120	136	-	dB
Large Signal Voltage Gain	R_L = 2 kΩ to V+/2 (Note 5)	•	200	300	-	dB
Output Voltage Swing	R_L = 2 kΩ to V+/2 R_L = 100 kΩ to V+/2	•	+4.7	- +4.99	-	V V
Slew Rate	R_L = 2 k, 100 pF			5	-	V/µs
Overload Recovery Time			-	100	-	µs
Supply Current per Amplifier $\overline{PWDN}$ active (CS3001 Only)	(Note 6)	• •	-	1.8	2.4 15	mA µA
$\overline{PWDN}$ Threshold	(Note 6)	•	(V+) -1.0	-	-	V
Start-up Time	(Note 7)	•	-	9	12	ms

Notes:
1. Symbol "•" denotes specification applies over -40 to +85 ° C.
2. This parameter is guaranteed by design and laboratory characterization. Thermocouple effects prohibit accurate measurement of these parameters in automatic test systems.
3. 1000-hour life test data @ 125 °C indicates randomly distributed variation approximately equal to measurement repeatability of 1 µV.
4. Measured within the specified common mode range limits.
5. Guaranteed within the output limits of (V+ -0.3 V) to (V- +0.3 V). Tested with proprietary production test method.
6. $\overline{PWDN}$ input has an internal pullup resistor to V+ of approximately 800 kΩ and is the major source of current consumption when $\overline{PWDN}$ is active low.
7. The device has a controlled start-up behavior due to its complex open loop gain characteristics. Start-up time applies when supply voltage is applied or when $\overline{PDWN}$ is released.

1.2 Absolute Maximum Ratings

Parameter		Min	Typ	Max	Unit
Supply Voltage	[(V+) - (V-)]			6.8	V
Input Voltage		V- -0.3		V+ +0.3	V
Storage Temperature Range		-65		+150	ºC

2. PERFORMANCE PLOTS

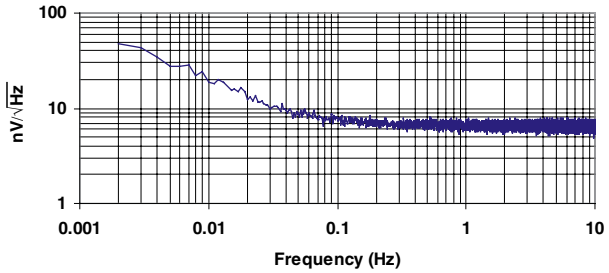


Figure 1. Noise vs Frequency (Measured)

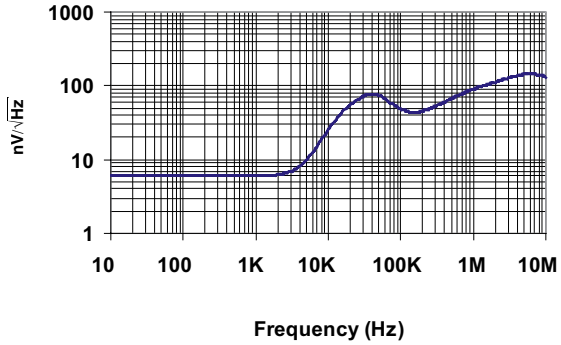


Figure 3. Noise vs Frequency

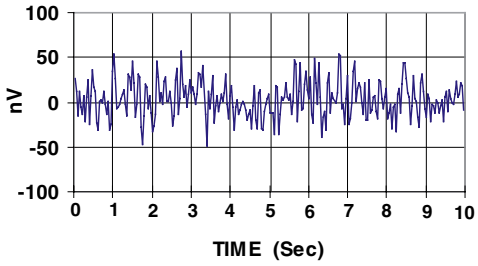


Figure 2. 0.01 Hz to 10 Hz Noise

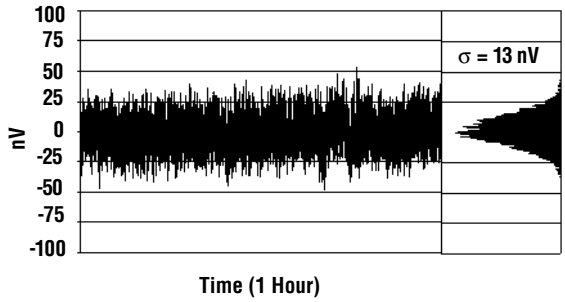


Figure 4. Offset Voltage Stability (DC to 3.2 Hz)

Performance Plots (Cont.)

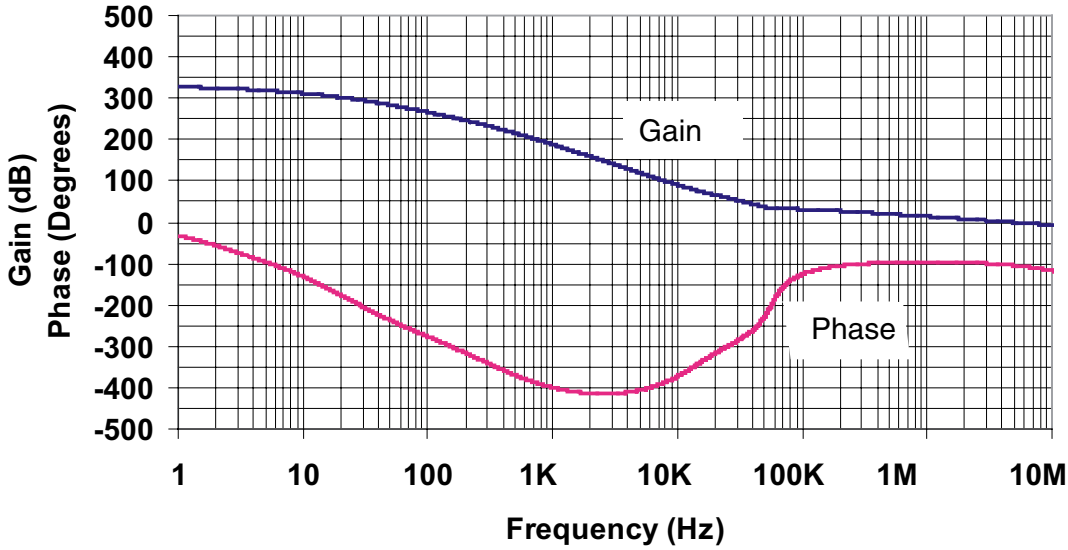


Figure 5. Open Loop Gain and Phase vs Frequency

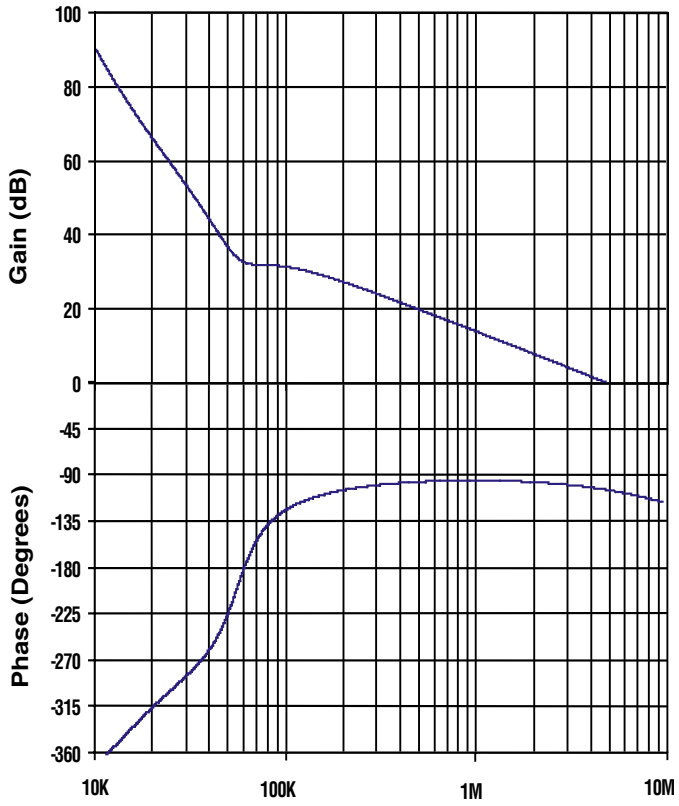


Figure 6. Open Loop Gain and Phase vs Frequency (Expanded)

Performance Plots (Cont.)

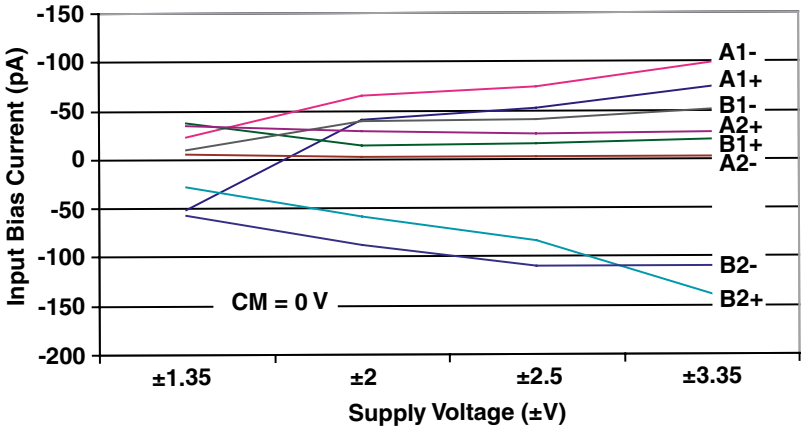


Figure 7. Input Bias Current vs Supply Voltage (CS3002)

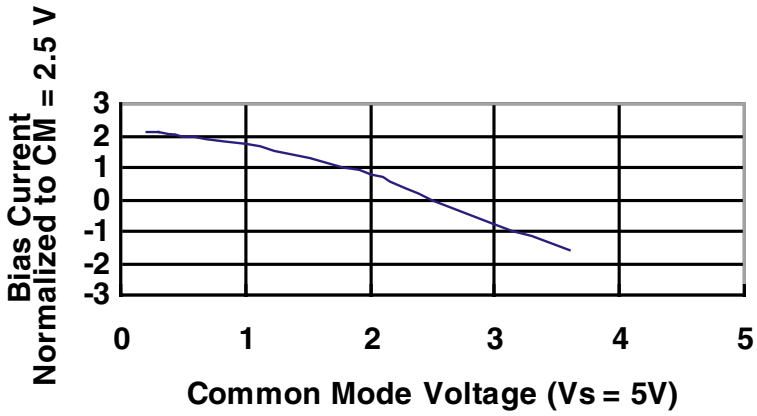


Figure 8. Input Bias Current vs Common Mode Voltage

3. CS3001/CS3002 OVERVIEW

The CS3001/CS3002 amplifiers are designed for precision measurement of signals from DC to 2 kHz when operating from a supply voltage of +2.7 V to +6.7 V (± 1.35 to ± 3.35 V). The amplifiers are designed with a patented architecture that utilizes multiple amplifier stages to yield very high open loop gain at frequencies of 10 kHz and below. The amplifiers yield low noise and low offset drift while consuming relatively low supply current. An increase in noise floor above 2 kHz is the result of intermediate stages of the amplifier being operated at very low currents. The amplifiers are intended for amplifying small signals with large gains in applications where the output of the amplifier can be band-limited to frequencies below 2 kHz.

3.1 Open Loop Gain and Phase Response

Figure 9 illustrates the open loop gain and phase response of the CS3001/CS3002. The gain slope of the amplifier is about –100 dB/decade between 500 Hz and 60 kHz and transitions to –20 dB/decade between 60 kHz and its unity gain crossover frequency at about 4.8 MHz. Phase margin at unity gain is about 70 degrees; gain margin is about 20 dB.

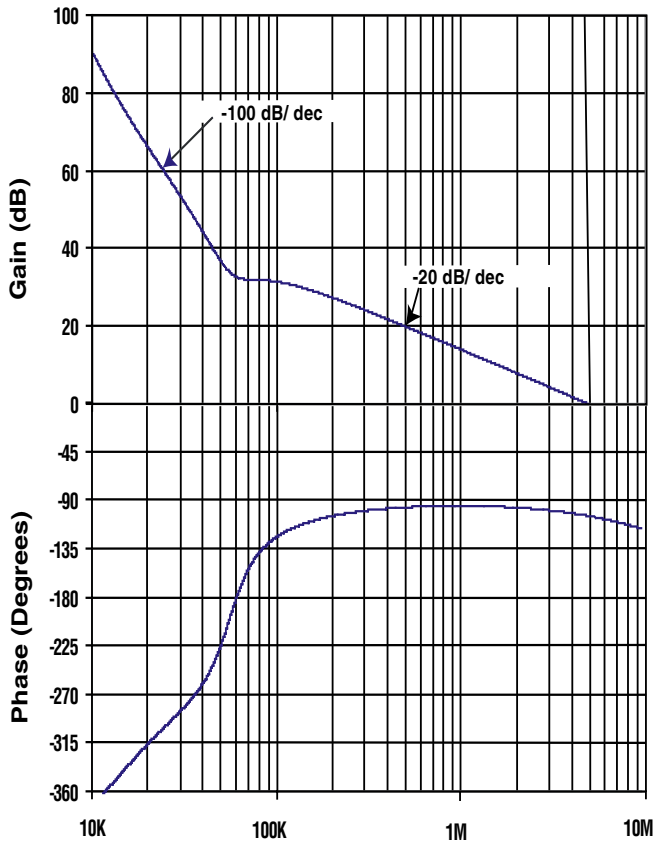


Figure 9. CS3001/CS3002 Open Loop Gain and Phase Response

3.2 Open Loop Gain and Stability Compensation

The CS3001 and CS3002 achieve ultra-high open loop gain. Figure 10 illustrates the amplifier in a non-inverting gain configuration. The open loop gain and phase plots indicate that the amplifier is stable for closed-loop gains less than 50 V/V. For a gain of 50, the phase margin is between 40° and 60° depending upon the loading conditions. As shown in Figure 11 on page 9, the op amp has an input capacitance at the + and – signal inputs of typically 50 pF. This capacitance adds an additional pole in the loop gain transfer function at a frequency of $f = 1/(2\pi R^{*}C_{in})$ where R is the parallel combination of R1 and R2 (R1 || R2). A higher value for R produces a pole at a lower frequency, thus reducing the phase margin. R1 is recommended to be less than or equal to 100 ohms, which results in a pole at 30 MHz or higher. If a higher value of R1 is desired, a compensation capacitor (C2) should be added in parallel with R2. C2 should be chosen such that $R2^{*}C2 \geq R1^{*}C_{in}$.

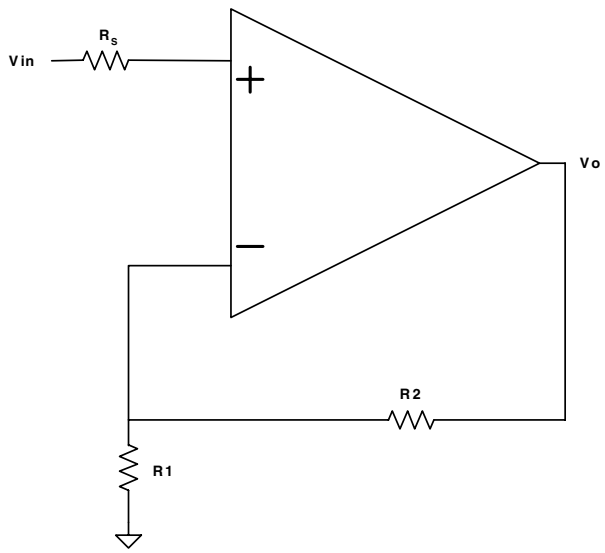


Figure 10. Non-Inverting Gain Configuration

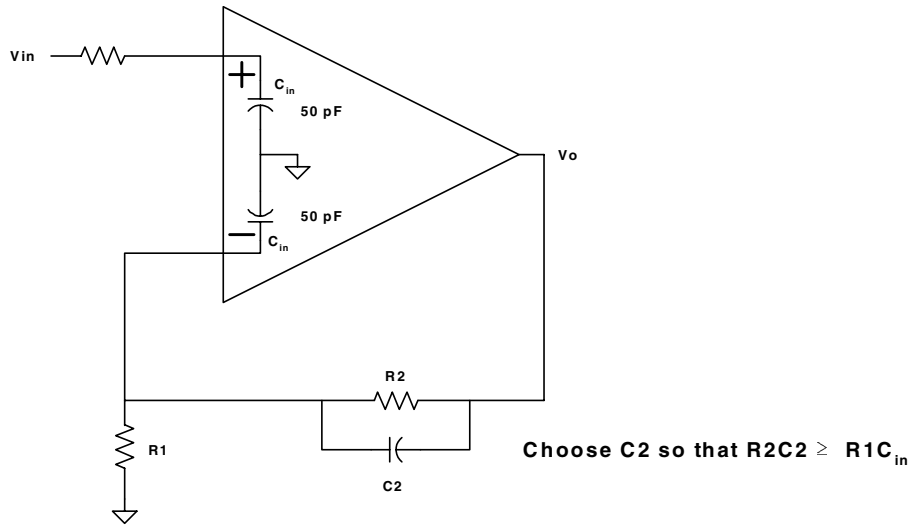


Figure 11. Non-Inverting Gain Configuration with Compensation

The feedback capacitor C2 is required for closed-loop gains greater than 50 V/V. The capacitor introduces a pole and a zero in the loop gain transfer function,

$$T = \frac{-\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)}A_{ol}$$

$$P_1 = \frac{1}{2\pi(R_1 \parallel R_2)C_2} \cong \frac{1}{2\pi(R_1C_2)} \qquad \text{for} \qquad R_2 \gg R_1$$

$$Z_1 = \frac{1}{2\pi(A \times R_1)C_2} \qquad \text{where} \qquad |A| = \frac{R_2}{R_1}$$

This indicates that the separation of the pole and the zero is governed by the closed loop gain. It is required that the zero falls on the steep slope (–100 dB/decade) of the loop gain plot so that there is some gain higher than 0 dB (typically 20 dB) at the hand-over frequency (the frequency at which the slope changes from – 100 dB/decade to –20 dB/decade).

The loop gain plot shown in Figure 12 illustrates the unity gain configuration, and indicates how this is modified when using the amplifier in a higher gain configuration with compensation. If it is configured for higher gain, for example, 60 dB, the x–axis will move up by 60 dB (line B). Capacitor C2 adds a zero and a pole. The modified plot indicates the effects of introducing the pole and zero due to capacitor C2. The pole can be located at any frequency higher than the hand-over frequency, the zero has to be at a frequency lower than the hand-over frequency so as to provide adequate gain margin. The separation between the pole and the zero is governed by the closed loop gain. The zero (z_1) occurs at the intersection of the –100 dB/decade and –80 dB/decade slopes. The point X in the figure should be at closed loop gain plus 20 dB gain margin. The value for C2 = 1/(2πR1p1). Using p1 = 1 MHz works very well and is independent of gain. As the closed loop gain is changed, the zero location is also modified if R1 remains fixed. Capacitor C2 can be increased in value to limit the amplifier's rising noise above 2 kHz.

3.3 Powerdown ($\overline{\text{PDWN}}$)

The CS3001 single amplifier provides a powerdown function on pin 1. If this pin is left open the amplifier will operate normally. If the powerdown is asserted low, the amplifier will go into a low power state. There is a pull-up resistor (approximately 800 k ohm) inside the amplifier from pin 1 to the V+ supply. The current through this pull-up resistor is the main source of current drain in the powerdown state.

3.4 Applications

The CS3001 and CS3002 amplifiers are optimum for applications that require high gain and low drift. Figure 13 illustrates a thermopile amplifier with a gain of 650 V/V. The thermopile outputs only a few millivolts when subjected to infrared radiation. The amplifier is compensated and bandlimited by C1 in combination with R2.

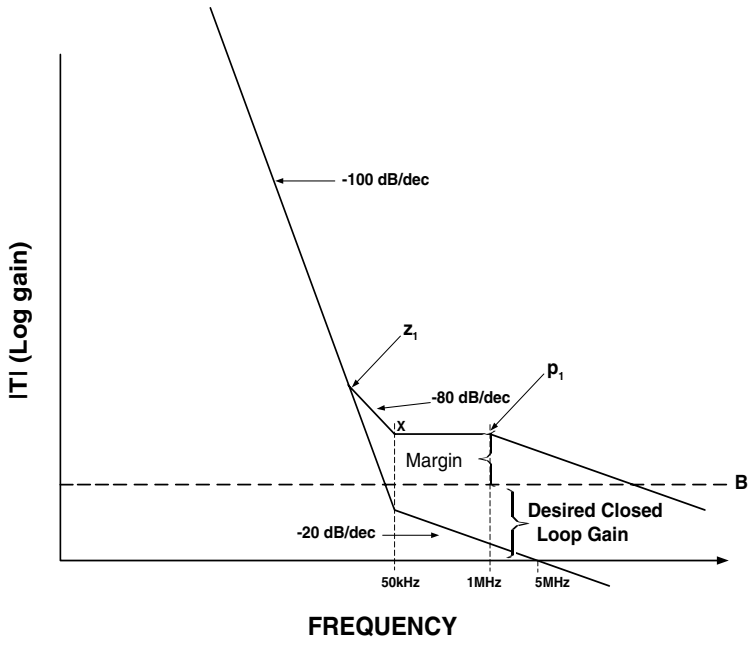


Figure 12. Loop Gain Plot: Unity Gain and with Pole-Zero Compensation

Figure 14 on page 12 illustrates a load cell bridge amplifier with a gain of 768 V/V. The load cell is excited with +5 V and has a 1 mV/V sensitivity. Its full scale output signal is amplified to produce a fully differential ± 3.8 V into the CS5510/12 A/D converter. This circuit operates from +5 V.

A similar circuit operating from +3 V can be constructed using the CS5540/CS5541 A/D converters.

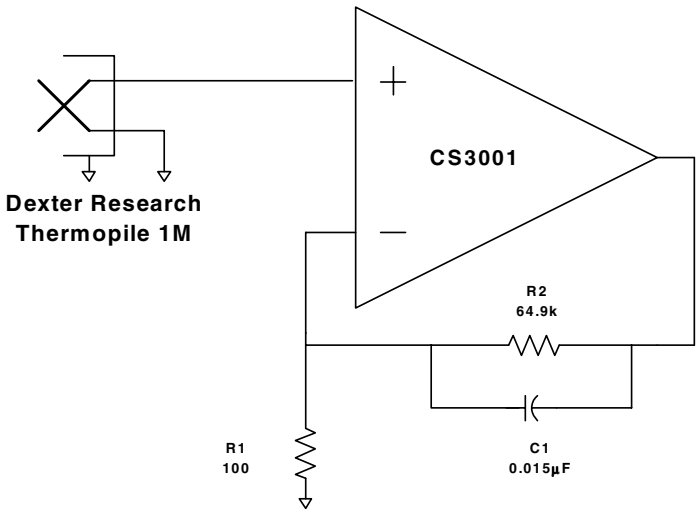


Figure 13. Thermopile Amplifier with a Gain of 650 V/V

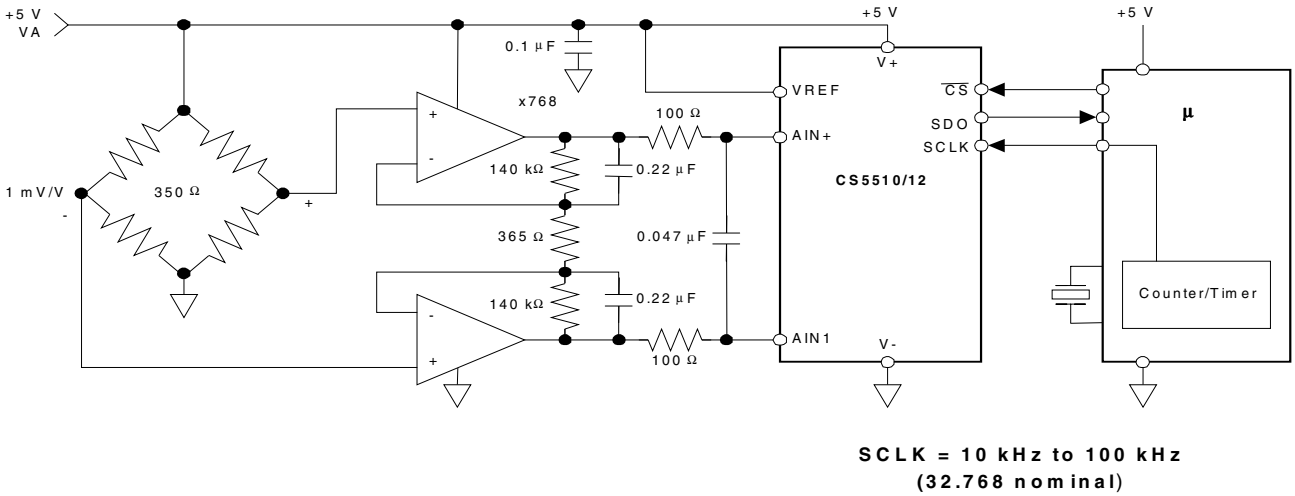
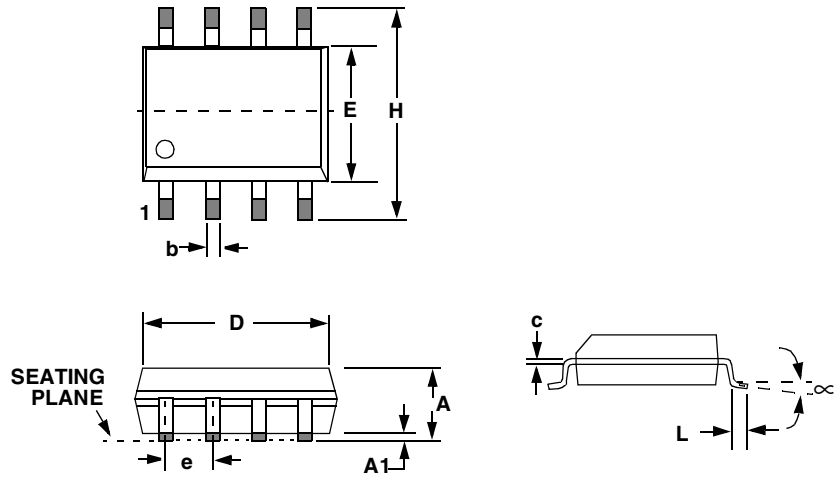


Figure 14. Load Cell Bridge Amplifier and A/D Converter

4. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # : MS-012

5. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS3001-IS	-40 °C to +85 °C	8-lead SOIC
CS3002-IS	-40 °C to +85 °C	8-lead SOIC

Note: Add the letter R to the Part # to order reels. There are 2000 pieces per reel.

• Notes •


CIRRUS LOGIC®