

74LVT640

3.3 V Octal transceiver with direction pin; inverting; 3-state

Rev. 3 — 10 April 2017

Product data sheet

1 General description

The 74LVT640 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable (\overline{OE}) input for easy cascading and a direction (DIR) input for direction control.

2 Features and benefits

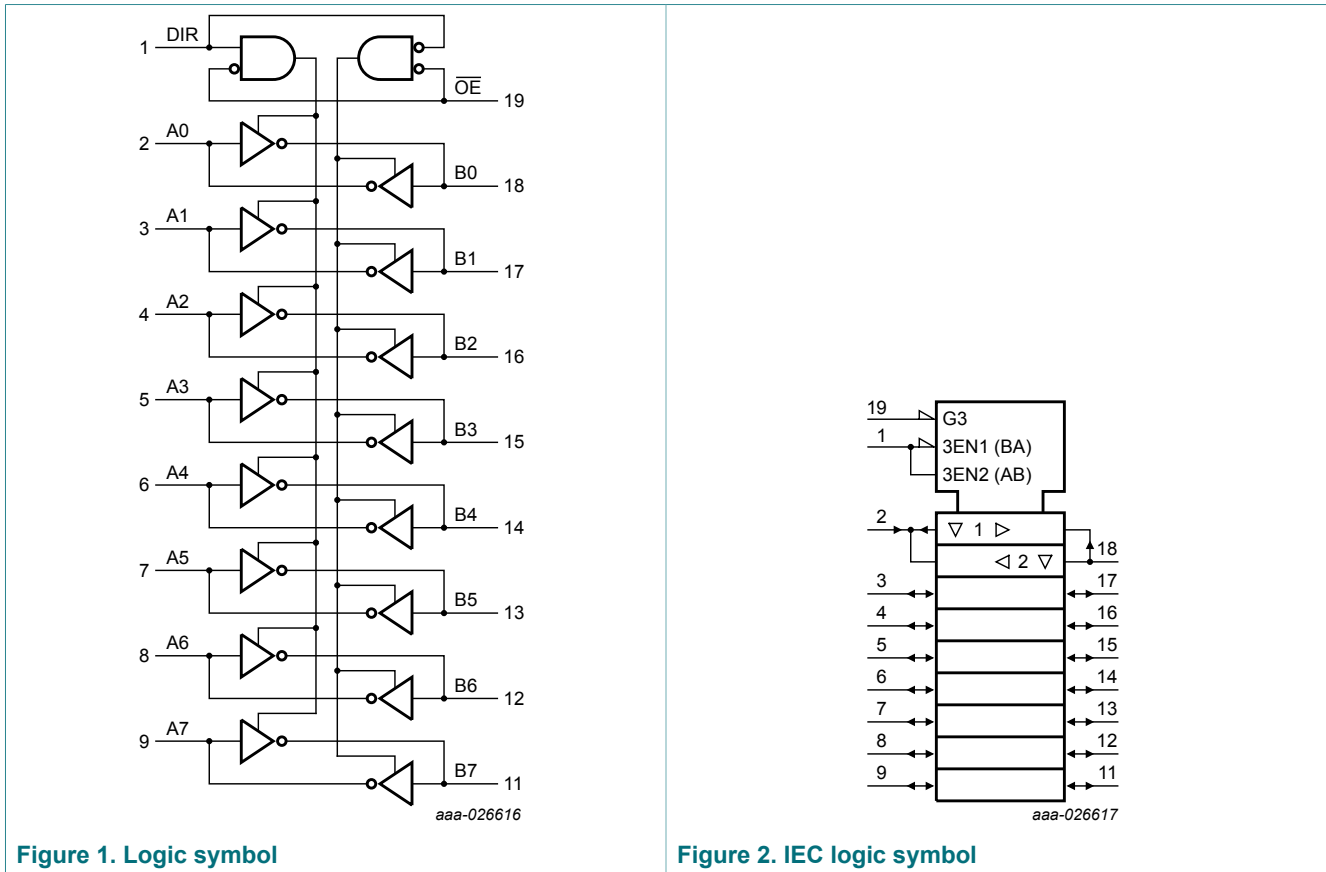
- 3-state buffers
- Octal bidirectional bus interface
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Output capability: +64 mA and -32 mA
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
 - JESD78: exceeds 500 mA
- ESD protection:
 - MIL STD 883 method 3015: exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVT640D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT640DB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT640PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4 Functional diagram



5 Pinning information

5.1 Pinning

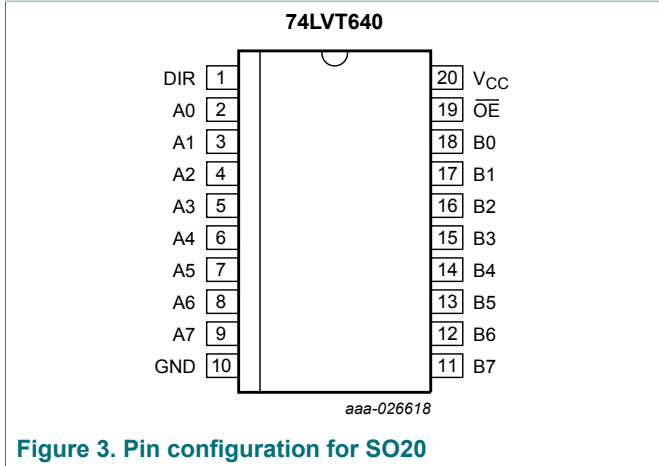


Figure 3. Pin configuration for SO20

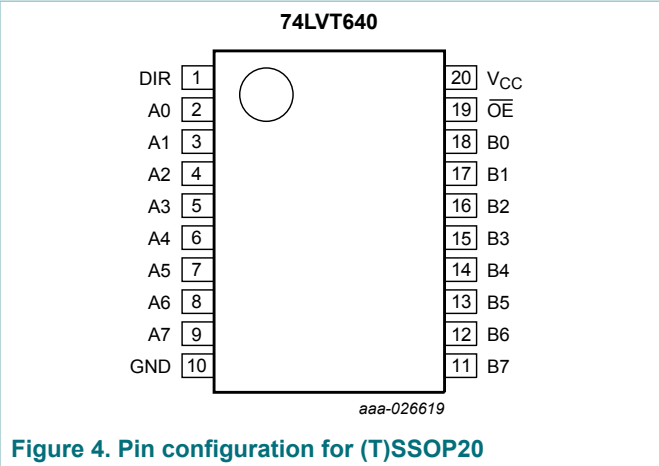


Figure 4. Pin configuration for (T)SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control input
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data inputs/outputs
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data inputs/outputs
\overline{OE}	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6 Functional description

Table 3. Function selection ^[1]

Inputs		Inputs/outputs	
OE	DIR	A _n	B _n
L	L	$\overline{B_n}$	inputs
L	H	inputs	$\overline{A_n}$
H	X	Z	Z

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output in OFF or HIGH state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
I _{OK}	output clamping current	V _O < 0	-50	-	mA
I _O	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[2]	-	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C [3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.7	3.6	V
V _I	input voltage		0	5.5	V
I _{OH}	HIGH-level output current		-	-32	mA
I _{OL}	LOW-level output current		-	32	mA
		current duty cycle ≤ 50 %; f _i ≥ 1 kHz	-	64	mA
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.9	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 µA	V _{CC} - 0.2	V _{CC} - 0.1	-	V
		V _{CC} = 2.7 V; I _{OH} = -8 mA	2.4	2.5	-	V
		V _{CC} = 3.0 V; I _{OH} = -32 mA	2.0	2.2	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 µA	-	0.1	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	control pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	1	10	µA
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±1	µA
		I/O data pins ^[2]				
		V _{CC} = 3.6 V; V _I = 5.5 V	-	1	20	µA
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.1	1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	±100	µA
		V _{CC} = 3.6 V; V _I = 0 V	-5	-1	-	µA
I _{CEX}	output high leakage current	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	60	125	µA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; \overline{OE} = don't care ^[3]	-	15	±100	µA
I _{BHL}	bus hold LOW current	V _{CC} = 3.0 V; V _I = 0.8 V ^[4]	75	150	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 3.0 V; V _I = 2.0 V	-75	-150	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V	-	-	-500	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled	-	0.13	0.19	mA

3.3 V Octal transceiver with direction pin; inverting; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0 \text{ V}$ to 3.6 V ; one input = $V_{CC} - 0.6 \text{ V}$; other inputs = V_{CC} or GND ^[5]	-	0.1	0.2	mA
C_I	input capacitance	DIR and \overline{OE} inputs; $V_I = 0 \text{ V}$ or 3.0 V	-	4	-	pF
$C_{I/O}$	input/output capacitance	at input/output data pins, outputs disabled; $V_{I/O} = 0 \text{ V}$ or 3.0 V	-	7	-	pF

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ (unless stated otherwise) and $T_{amb} = 25 \text{ °C}$.

[2] Unused pins at V_{CC} or GND.

[3] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms . From $V_{CC} = 1.2 \text{ V}$ to $V_{CC} = 3.0 \text{ V}$ to 3.6 V a transition time of 100 ms is permitted. This parameter is valid for $T_{amb} = +25 \text{ °C}$ only.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10 Dynamic characteristics

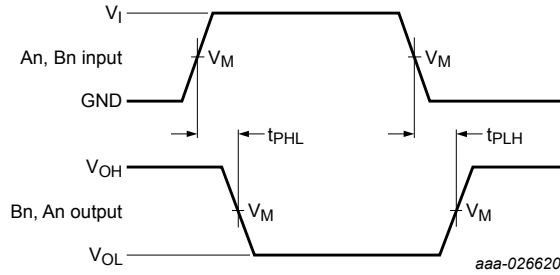
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Figure 5				
		$V_{CC} = 2.7 \text{ V}$	-	-	4.5	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.0	2.3	3.7	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An, see Figure 5				
		$V_{CC} = 2.7 \text{ V}$	-	-	3.1	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.0	2.4	3.3	ns
t_{PZH}	OFF-state to HIGH propagation delay	\overline{OE} to An or Bn; see Figure 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.9	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.1	3.5	5.3	ns
t_{PZL}	OFF-state to LOW propagation delay	\overline{OE} to An or Bn; see Figure 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.2	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	3.6	5.3	ns
t_{PHZ}	HIGH to OFF-state propagation delay	\overline{OE} to An or Bn; see Figure 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	5.6	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2.2	3.7	5.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	\overline{OE} to An or Bn; see Figure 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	4.5	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2.0	3.1	4.5	ns

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and $V_{CC} = 3.3 \text{ V}$

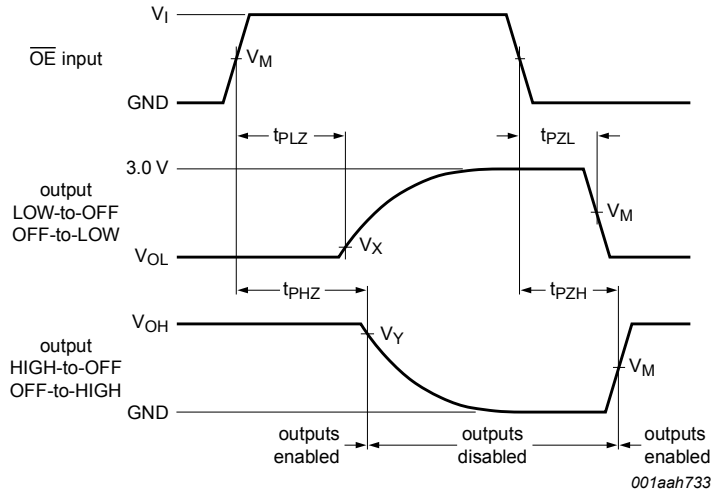
10.1 Waveforms and test circuit



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. Input (An, Bn) to output (\overline{Bn} , \overline{An}) propagation delays



See Table 8 for measurement points.

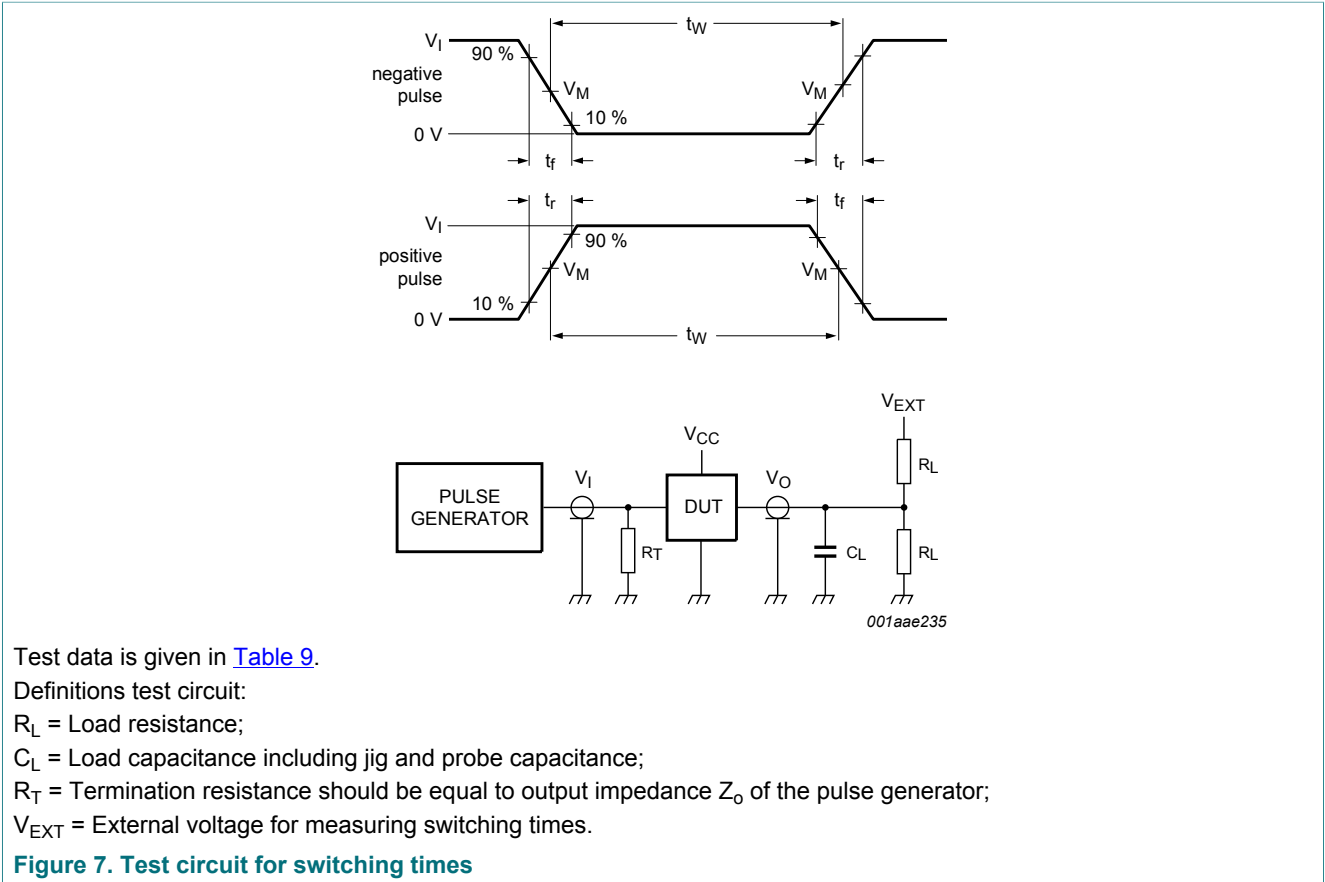
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. 3-state output enable and disable times

Table 8. Measurement points

Input		Output		
V_I	V_M	V_M	V_x	V_y
GND to 2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

3.3 V Octal transceiver with direction pin; inverting; 3-state



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure 7. Test circuit for switching times

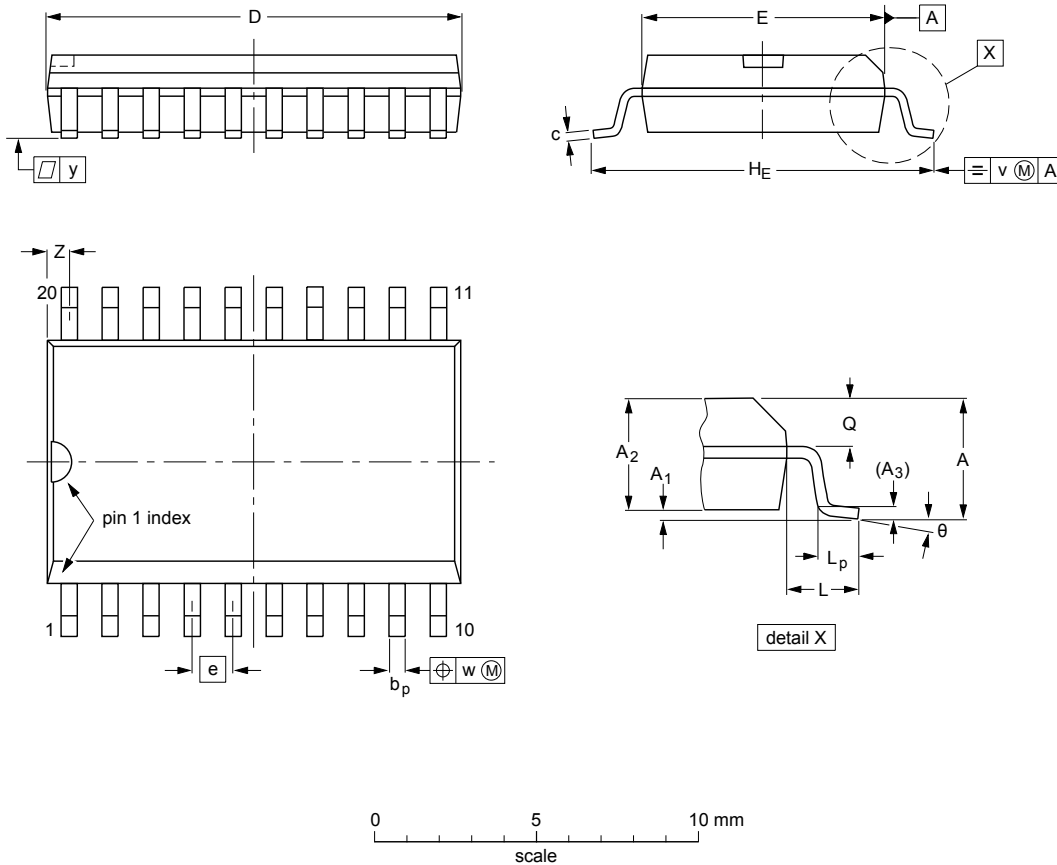
Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

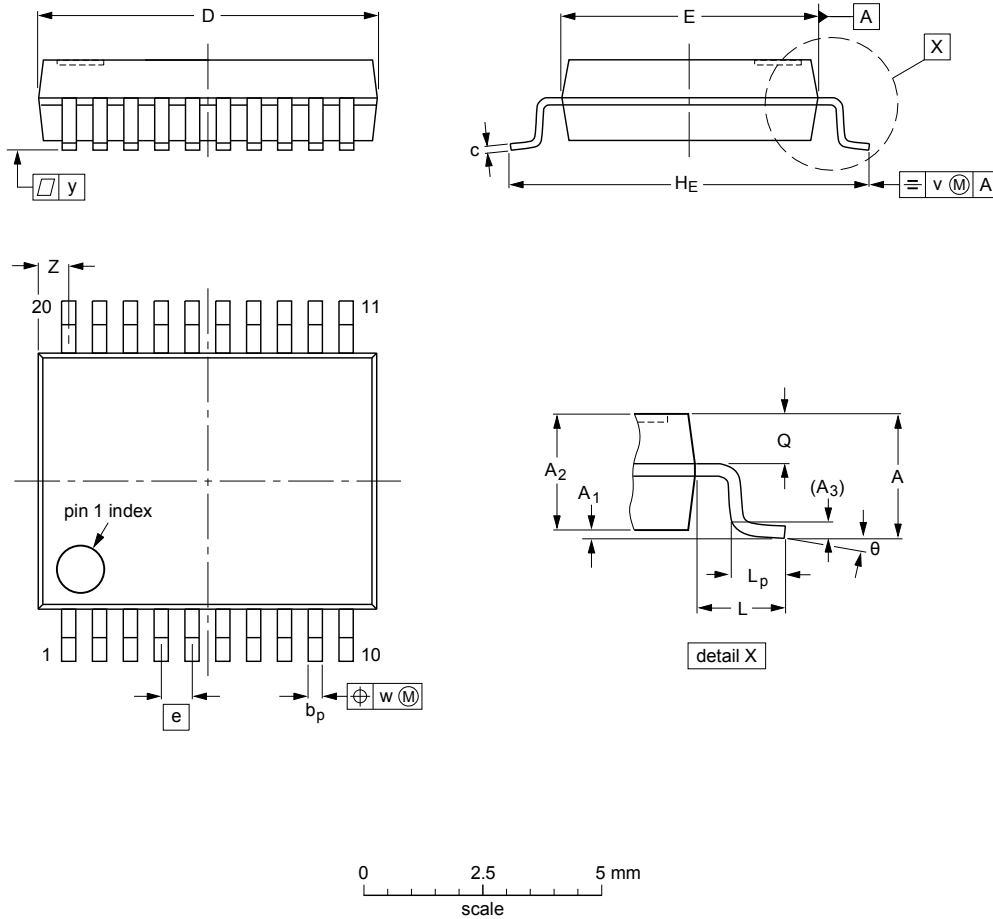
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Figure 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

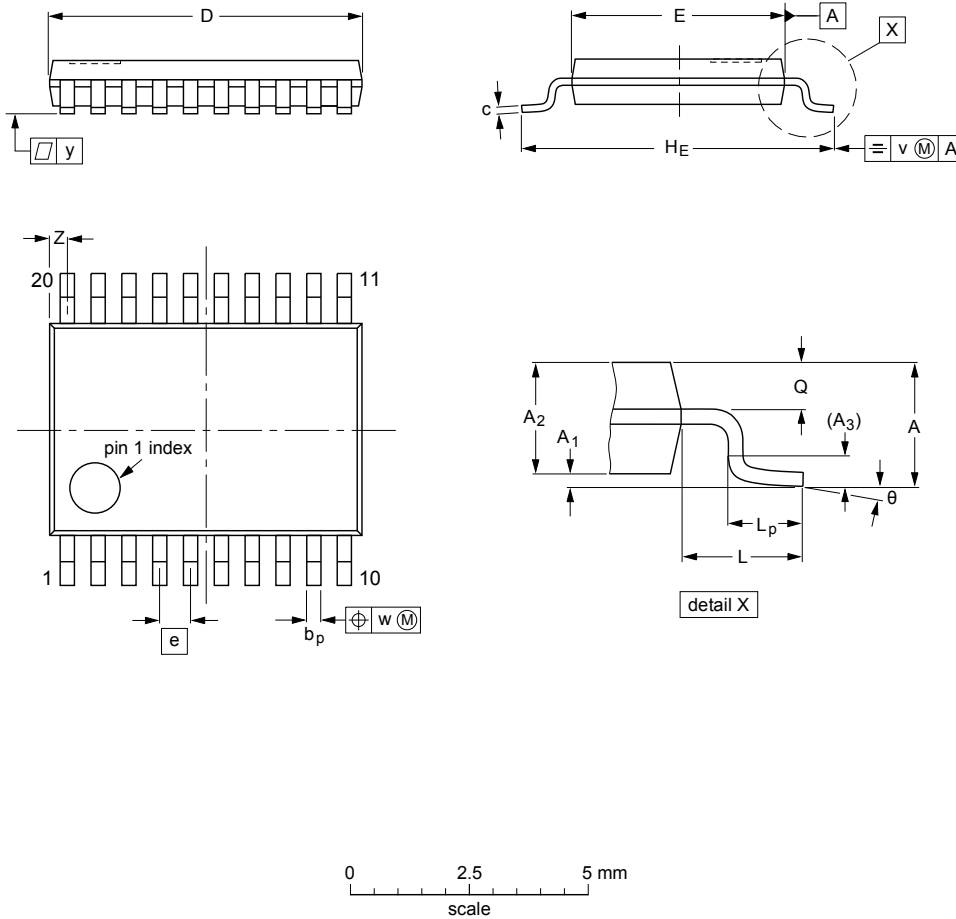
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Figure 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				-99-12-27 03-02-19

Figure 10. Package outline SOT360-1 (TSSOP20)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT640 v.3	20170410	Product data sheet	-	74LVT640 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVT640 v.2	19980219	Product specification	-	74LVT640 v.1
74LVT640 v.1	19961001	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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3.3 V Octal transceiver with direction pin; inverting; 3-state

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