Freescale Semiconductor
Technical Data

Document Number: MML25231HT1
Rev. 0, 4/2016

RoHS

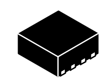
Enhancement Mode pHEMT Technology (E-pHEMT)

Low Noise Amplifier

The MML25231H is a single-stage low noise amplifier (LNA) with active bias and high isolation for use in cellular infrastructure applications. It is designed for a range of low noise, high linearity applications such as picocell, femtocell, tower mounted amplifiers (TMA) and receiver front-end circuits. It operates from a single voltage supply and is suitable for applications with frequencies from 1000 to 4000 MHz such as CDMA, W-CDMA and LTE.

MML25231HT1

1000–4000 MHz, 15.2 dB
23 dBm, 0.36 NF
E-pHEMT LNA



DFN 2 × 2

Features

- Ultra Low Noise Figure: 0.39 dB @ 1900 MHz, 0.54 dB @ 2500 MHz
- High Linearity: 34.7 dBm OIP3 @ 1900 MHz, 35.2 dBm @ 2500 MHz
- Frequency: 1000–4000 MHz
- Unconditionally Stable Over Temperature
- P1dB: 22.6 dBm @ 1900 MHz, 22.5 dBm @ 2500 MHz
- Small-Signal Gain: 17.2 dB @ 1900 MHz, 15.2 dB @ 2500 MHz
- Single 5 V Supply
- Power-down Pin
- Supply Current: 60 mA (adjustable externally)
- 50 Ohm Operation (some external matching required)
- Cost-effective 8-pin, 2 mm DFN Surface Mount Plastic Package

Table 1. Typical Performance (1)

Characteristic	Symbol	1750 MHz	1920 MHz	2350 MHz	2600 MHz	3600 MHz	Unit
Noise Figure	NF	0.38	0.39	0.50	0.57	0.98	dB
Input Return Loss (S11)	IRL	–12.0	–12.8	–15.1	–15.9	–10.7	dB
Output Return Loss (S22)	ORL	–14.4	–14.4	–14.8	–15.3	–20.7	dB
Small-Signal Gain (S21)	GP	17.8	17.2	15.6	14.8	11.7	dB
Power Output @ 1dB Compression	P1dB	22.9	22.6	22.6	22.5	22.8	dBm
Third Order Input Intercept Point	IIP3	16.5	17.5	19.3	20.7	25.1	dBm
Third Order Output Intercept Point	OIP3	34.4	34.7	35.0	35.7	37.0	dBm

1. V_{DD} = 5 Vdc, T_A = 25°C, 50 ohm system, application circuit tuned for specified frequency.

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Supply Current	I_{DD}	150	mA
RF Input Power	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	175	°C

Table 3. Thermal Characteristics

Characteristic	Symbol	Value (3)	Unit
Thermal Resistance, Junction to Case Case Temperature 87°C, 5 Vdc, 65 mA, no RF applied	$R_{\theta JC}$	134	°C/W

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 4. Electrical Characteristics (V_{DD} = 5 Vdc, 2600 MHz, T_A = 25°C, 50 ohm system, in Freescale Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small-Signal Gain (S21)	G_p	14.2	14.8	—	dB
Input Return Loss (S11)	IRL	—	–16.0	—	dB
Output Return Loss (S22)	ORL	—	–15.3	—	dB
Power Output @ 1dB Compression	P1dB	—	22.5	—	dBm
Third Order Input Intercept Point	IIP3	—	20.7	—	dBm
Reverse Isolation (S12)	|S12|	—	–20.9	—	dB
Noise Figure	NF	—	0.56	—	dB
Supply Current (1)	I_{DD}	55	60	65	mA
Supply Voltage	V_{DD}	—	5	—	V
Supply Current in Power Down Mode	I_{PD}	—	2.8	—	mA
Logic Voltage for Power Down (2) Input High Voltage Input Low Voltage	V_{PD}	 1.8 0	 — —	 V_{DD} 0.4	V

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD 22-A114)	1C
Machine Model (per EIA/JESD 22-A115)	A
Charge Device Model (per JESD 22-C101)	IV

Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	1	260	°C

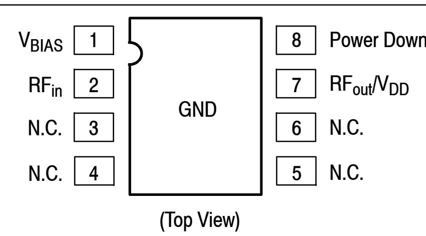
Table 7. Ordering Information

Device	Tape and Reel Information	Package
MML25231HT1	T1 Suffix = 1,000 Units, 12 mm Tape Width, 7-inch Reel	DFN 2 × 2

1. DC current measured with no RF signal applied.
2. Limits derived from device characterization.

Table 8. Functional Pin Description

Pin Number	Pin Function
1	V_{BIAS}
2	RF_{in}
3	No Connection
4	No Connection
5	No Connection
6	No Connection
7	RF_{out}/Supply Voltage
8	Power Down (Active High)



Note: Exposed backside of the package is DC and RF ground. N.C. can be connected to GND.

Figure 1. Pin Connections

50 OHM APPLICATION CIRCUIT: 2500 MHz

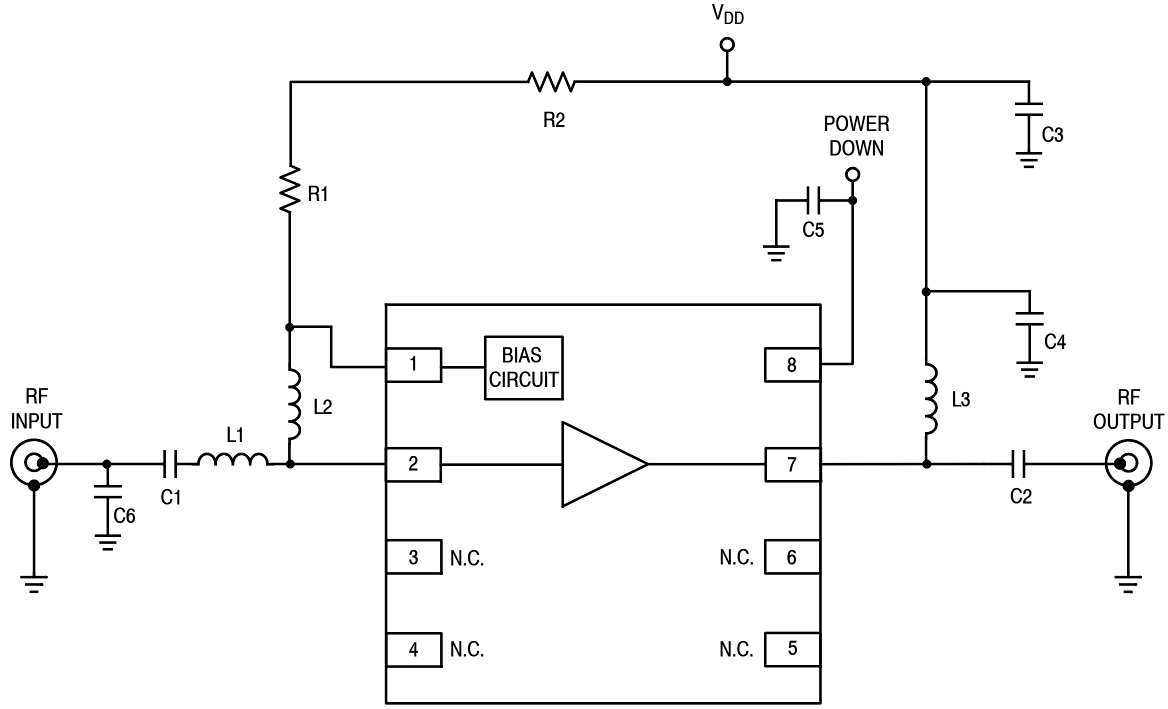
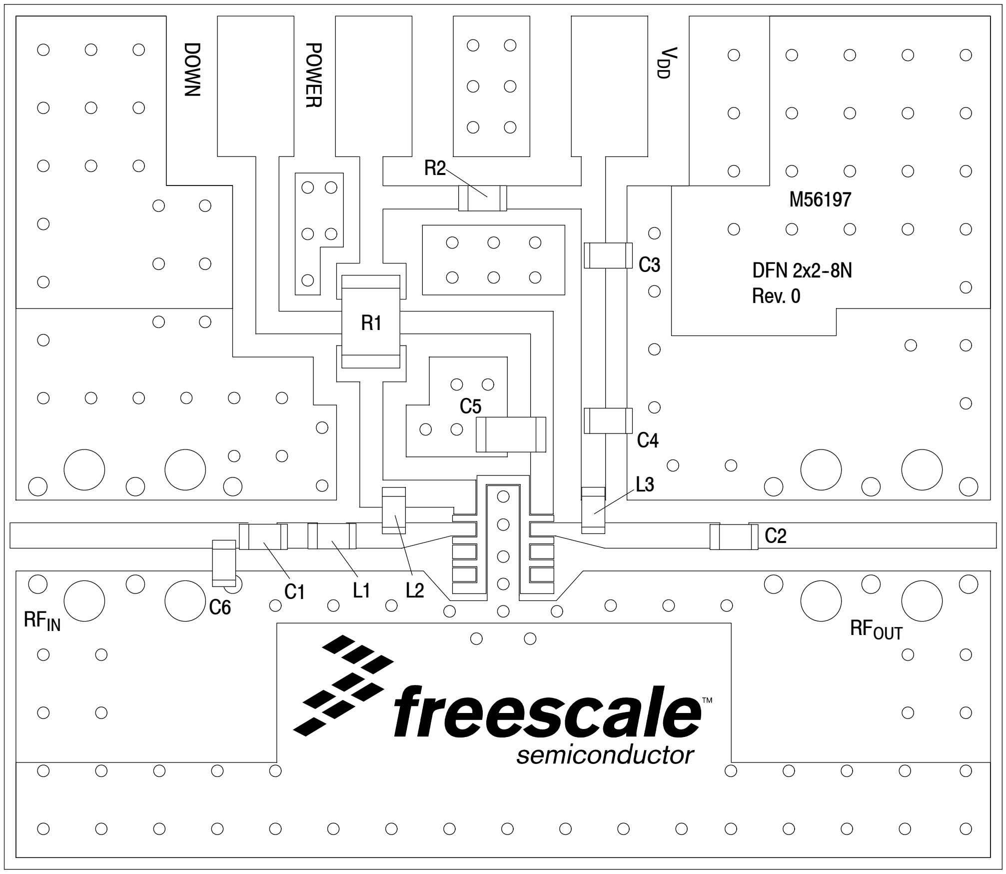


Figure 2. MML25231HT1 Test Circuit Schematic

Table 9. MML25231HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	82 pF Chip Capacitor	GRM1555C1H820JA01	Murata
C2	9 pF Chip Capacitor	GJM1555C1H9R0CB01	Murata
C3	10 pF Chip Capacitor	GJM1555C1H100JB01	Murata
C4	0.01 μF Chip Capacitor	GRM155R71E103KA01	Murata
C5	1000 pF Chip Capacitor	GRM155R71H102KA01	Murata
C6	0.4 pF Chip Capacitor	04023U0R4BBW	AVX
L1	1.0 nH Chip Inductor	0402CS-1N0XJLW	Coilcraft
L2	68 nH Chip Inductor	0402HPH-68NXGL	Coilcraft
L3	40 nH Chip Inductor	0402HP-40NXGL	Coilcraft
R1	1800 Ω, 1/4 W Chip Resistor	RK73B2ATTD182J	KOA
R2	0 Ω, 1.5 A Chip Resistor	CR0402-J/-000GLFCT-ND	Bourns
PCB	Rogers RO4350B, 0.010″, ε_r = 3.66	M56197	MTL



PCB actual size: 0.75″ × 0.86″.

NOTE: To achieve optimal noise performance, it is critical that proper biasing, input matching, supply decoupling and grounding are employed.

Figure 3. MML25231HT1 Test Circuit Component Layout

Table 9. MML25231HT1 Test Circuit Component Designations and Values

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C6	0.4 pF Chip Capacitor	04023U0R4BBW	AVX
L1	1.0 nH Chip Inductor	0402CS-1N0XJLW	Coilcraft
L2	68 nH Chip Inductor	0402HPH-68NXGL	Coilcraft
L3	40 nH Chip Inductor	0402HP-40NXGL	Coilcraft
R1	1800 Ω, 1/4 W Chip Resistor	RK73B2ATTD182J	KOA
R2	0 Ω, 1.5 A Chip Resistor	CR0402-J/-000GLFCT-ND	Bourns
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(Test Circuit Component Designations and Values repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 2500 MHz

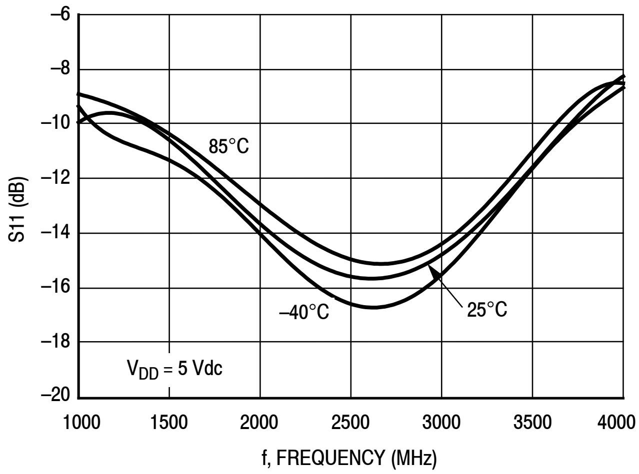

Figure 4. S11 versus Frequency and Temperature

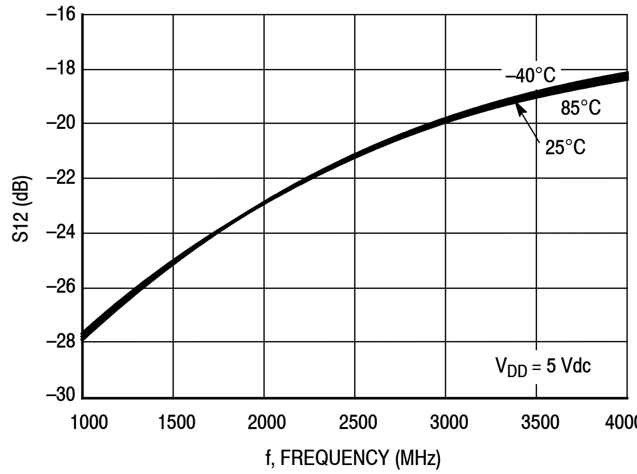

Figure 5. S12 versus Frequency and Temperature

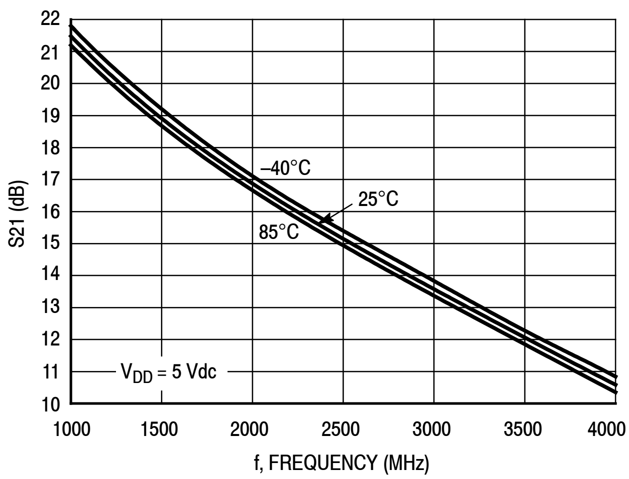

Figure 6. S21 versus Frequency and Temperature

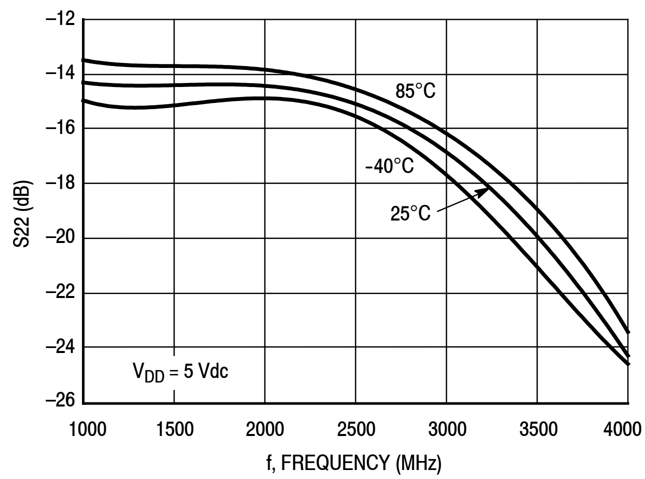

Figure 7. S22 versus Frequency and Temperature

50 OHM TYPICAL CHARACTERISTICS: 2500 MHz

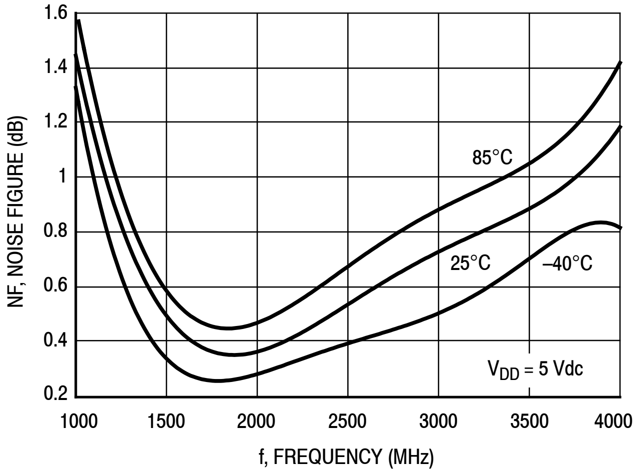

Figure 8. Noise Figure versus Frequency and Temperature

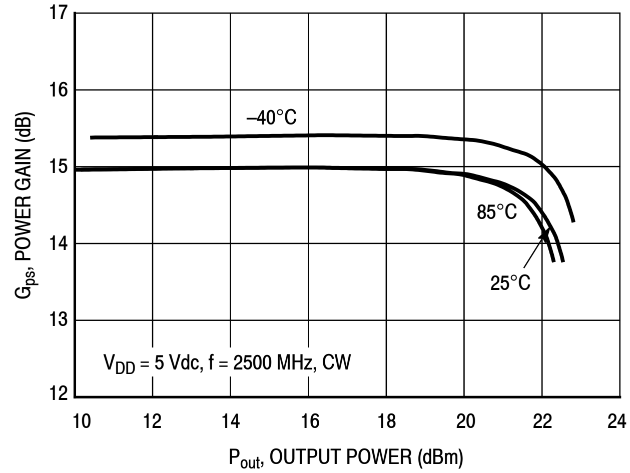

Figure 9. Power Gain versus Output Power and Temperature

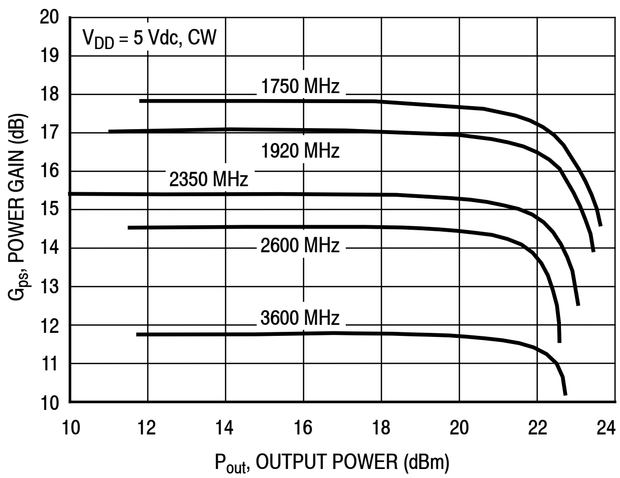

Figure 10. Power Gain versus Output Power and Frequency

Power Gain versus Temperature

f (MHz)	Temperature (°)	Gain (dB)	P1dB (dBm)
1750	25	17.86	22.9
1750	–40	18.09	23
1750	85	17.68	22.2
1920	25	17.16	22.6
1920	–40	17.37	23
1920	85	16.98	22.25
2350	25	15.64	22.6
2350	–40	15.84	22.9
2350	85	15.47	22.2
2500	25	15.13	22.5
2500	–40	15.38	22.75
2500	85	14.96	22.18
2600	25	14.89	22.45
2600	–40	15.11	22.75
2600	85	14.74	22.3
3600	25	11.83	22.8
3600	–40	12	23
3600	85	11.67	22.4

50 OHM TYPICAL CHARACTERISTICS: 2500 MHz

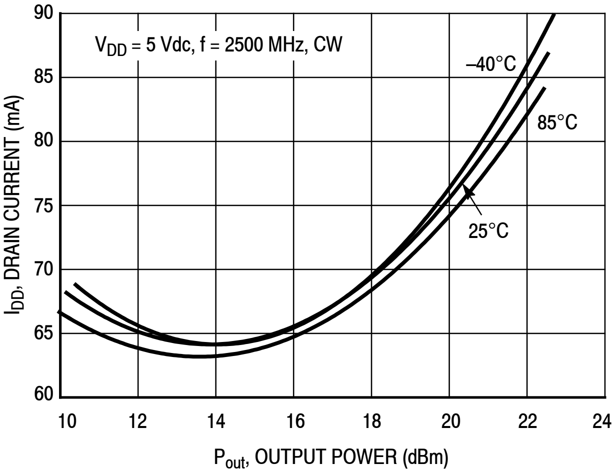

Figure 11. Drain Current versus Output Power and Temperature

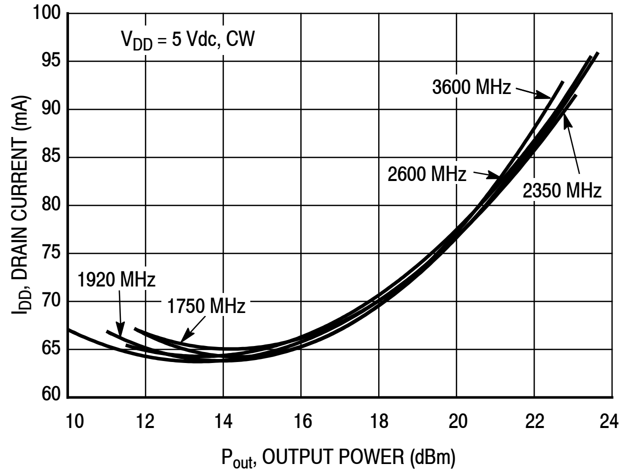

Figure 12. Drain Current versus Output Power and Frequency

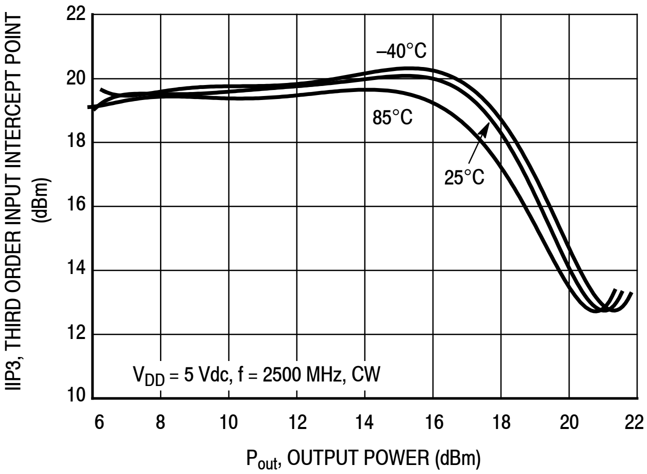

Figure 13. Third Order Input Intercept Point versus Output Power and Temperature

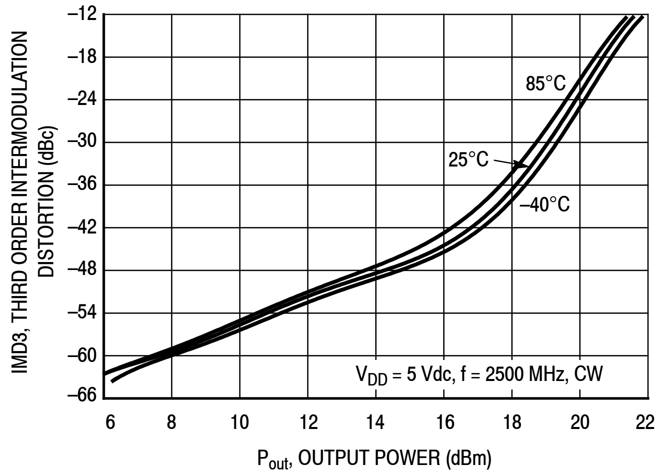

Figure 14. Third Order Intermodulation Distortion versus Output Power and Temperature

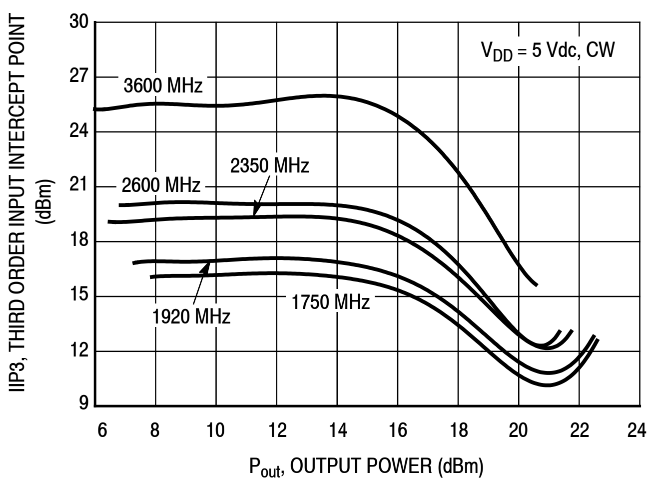

Figure 15. Third Order Input Intercept Point versus Output Power and Frequency

50 OHM TYPICAL CHARACTERISTICS: 2500 MHz

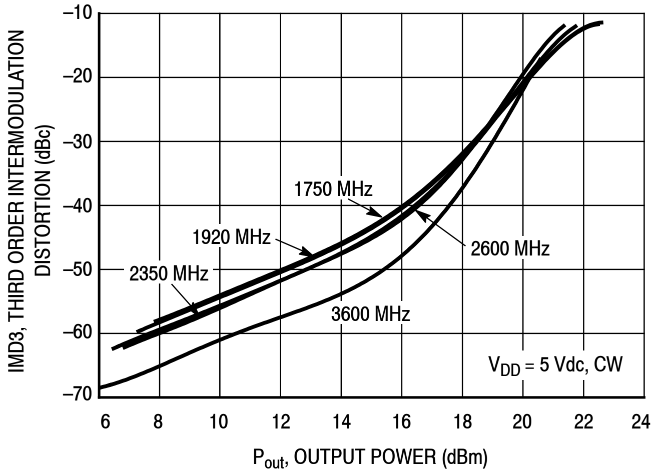

Figure 16. Third Order Intermodulation Distortion versus Output Power

IMD3 and IIP3 versus Temperature

f (GHz)	Temperature (°)	P_{out} (dBm)	Gain (dB)	IIP3 (dBm)	IMD3 (dBc)
1750	25	13.9	17.9	16.5	–47.0
1750	–40	14.1	18.1	16.7	–47.4
1750	85	13.7	17.7	16.0	–46.0
1920	25	14.2	17.2	17.6	–47.1
1920	–40	14.4	17.4	17.7	–47.4
1920	85	14.0	17.0	17.0	–47.9
2350	25	13.7	15.7	19.3	–48.7
2350	–40	13.9	15.9	19.6	–49.1
2350	85	13.5	15.5	19.2	–47.3
2500	25	14.2	15.2	20.0	–48.1
2500	–40	14.4	15.4	20.2	–48.5
2500	85	14.0	15.0	19.7	–47.3
2600	25	13.9	14.9	20.7	–49.5
2600	–40	14.2	15.2	20.9	–49.9
2600	85	13.8	14.8	20.4	–48.7
3600	25	13.9	11.9	25.1	–52.3
3600	–40	14.1	12.1	25.4	–52.9
3600	85	13.7	11.7	25.0	–52.0

50 OHM APPLICATION CIRCUIT: 2000 MHz

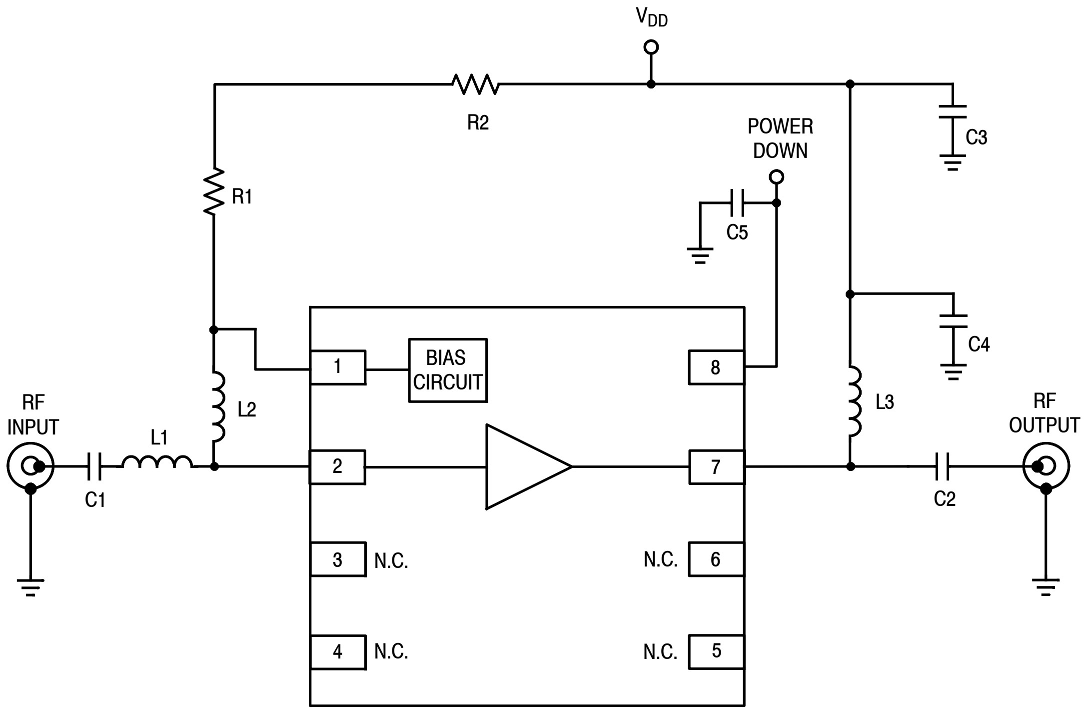

Figure 17. MML25231HT1 Test Circuit Schematic

Table 10. MML25231HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
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C2	12 pF Chip Capacitor	GRM1555C1H120GA01	Murata
C3	10 pF Chip Capacitor	GJM1555C1H100JB01	Murata
C4	0.01 μF Chip Capacitor	GRM155R71E103KA01	Murata
C5	1000 pF Chip Capacitor	GRM155R71H102KA01	Murata
L1	1.0 nH Chip Inductor	0402CS-1N0XJLW	Coilcraft
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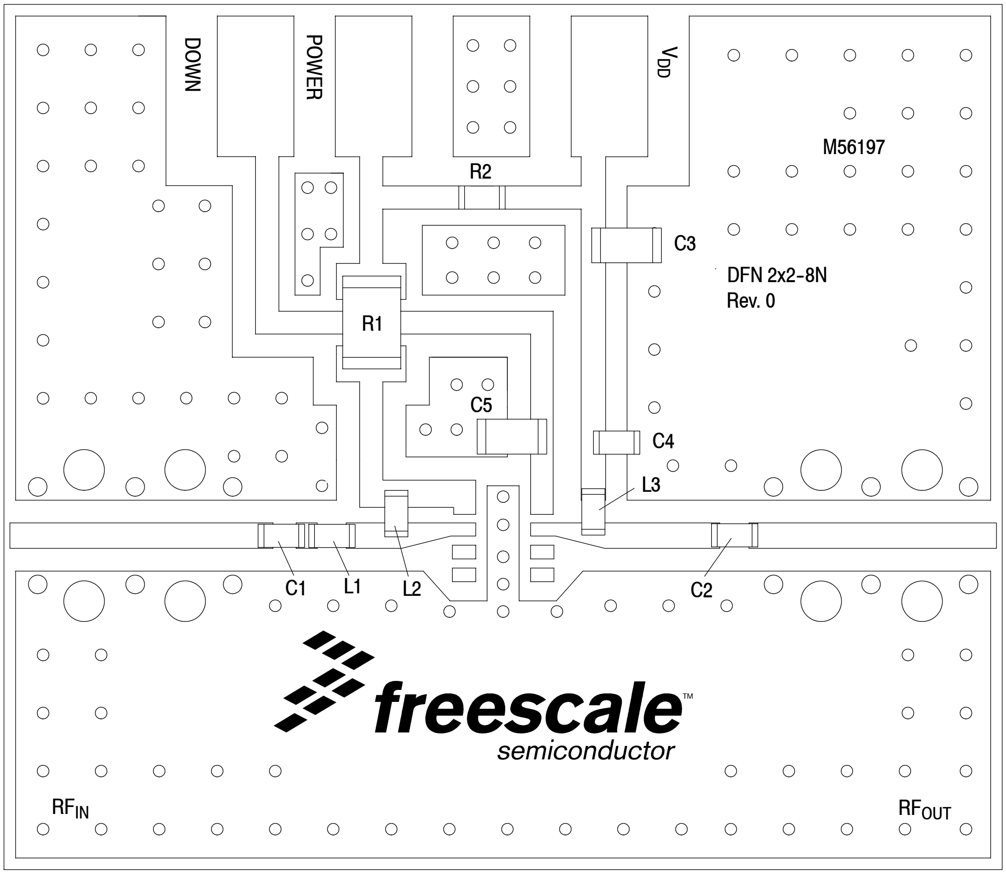
PCB	Rogers RO4350B, 0.010″, ε_r = 3.66	M56197	MTL



PCB actual size: 0.75″ × 0.86″.

NOTE: To achieve optimal noise performance, it is critical that proper biasing, input matching, supply decoupling and grounding are employed.

Figure 18. MML25231HT1 Test Circuit Component Layout

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C4	0.01 μF Chip Capacitor	GRM155R71E103KA01	Murata
C5	1000 pF Chip Capacitor	GRM155R71H102KA01	Murata
L1	1.0 nH Chip Inductor	0402CS-1N0XJLW	Coilcraft
L2	68 nH Chip Inductor	0402HPH-68NXGL	Coilcraft
L3	40 nH Chip Inductor	0402HP-40NXGL	Coilcraft
R1	1800 Ω, 1/4 W Chip Resistor	RK73B2ATTD182J	KOA
R2	0 Ω, 1.5 A Chip Resistor	CR0402-J/-000GLFCT-ND	Bourns
PCB	Rogers RO4350B, 0.010″, ε_r = 3.66	M56197	MTL

(Test Circuit Component Designations and Values repeated for reference.)

50 OHM TYPICAL CHARACTERISTICS: 2000 MHz

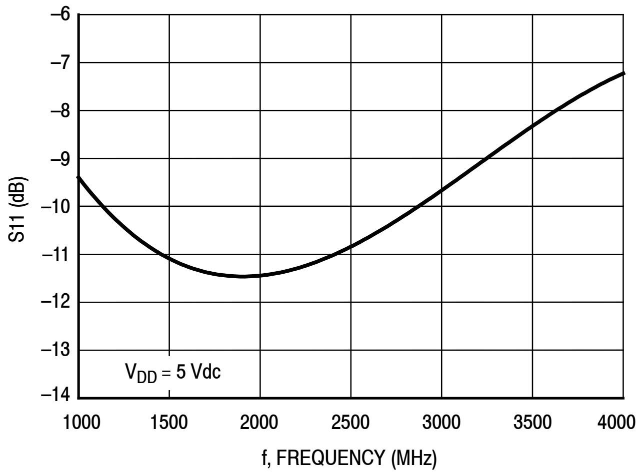


Figure 19. S11 versus Frequency

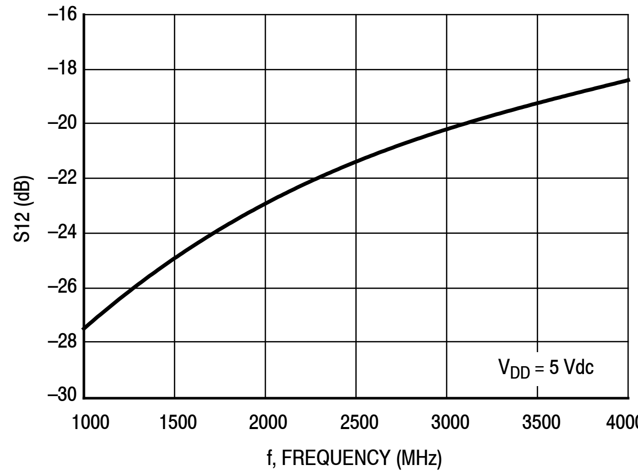


Figure 20. S12 versus Frequency

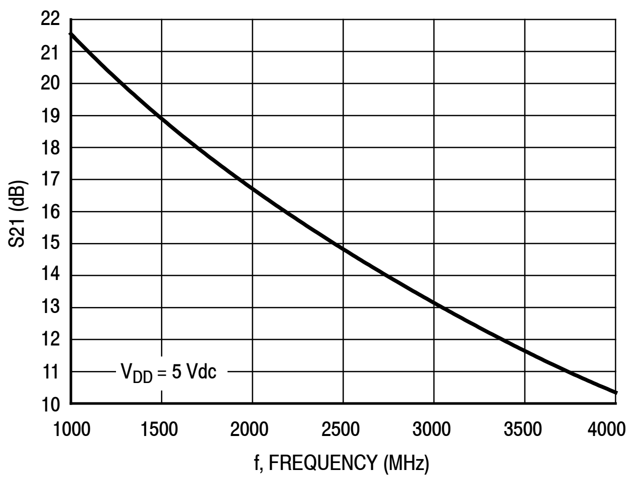


Figure 21. S21 versus Frequency

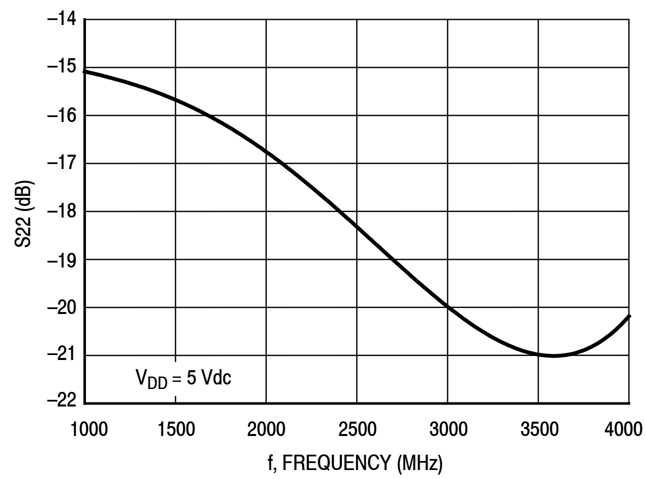


Figure 22. S22 versus Frequency

50 OHM TYPICAL CHARACTERISTICS: 2000 MHz

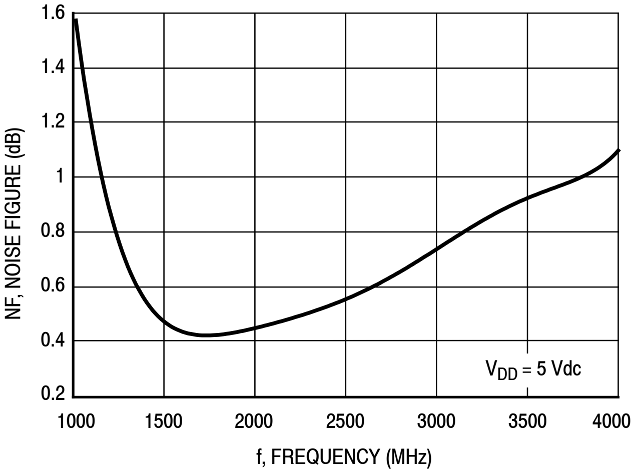


Figure 23. Noise Figure versus Frequency

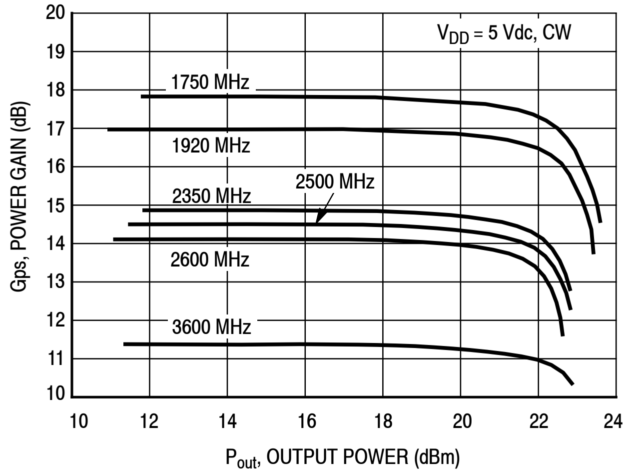


Figure 24. Power Gain versus Output Power and Frequency

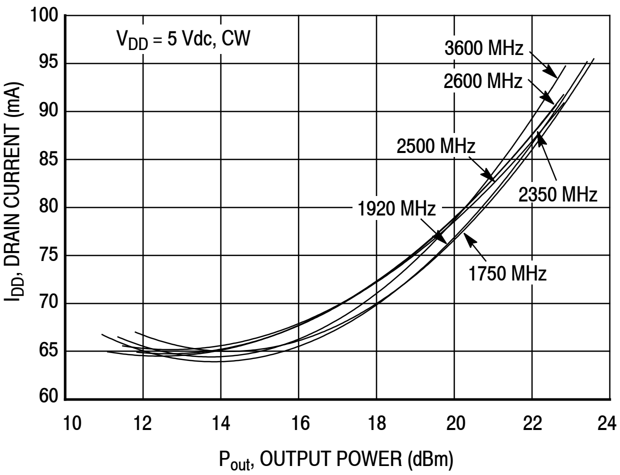


Figure 25. Drain Current versus Output Power and Frequency

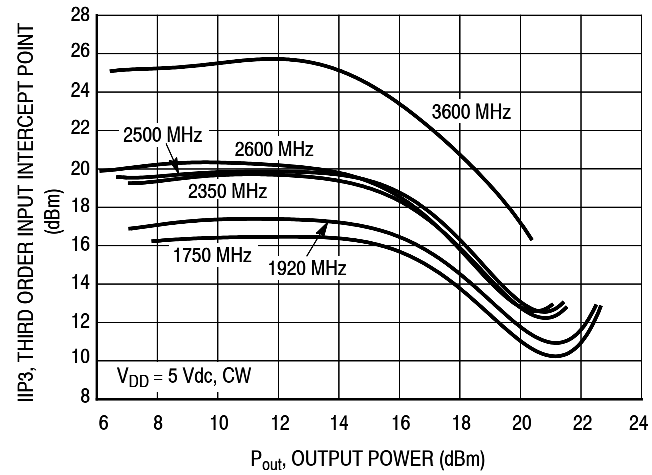


Figure 26. Third Order Input Intercept Point versus Output Power and Frequency

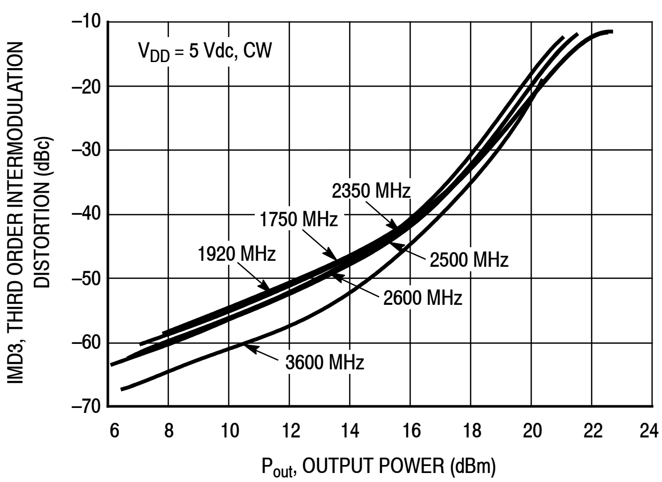


Figure 27. Third Order Intermodulation Distortion versus Output Power and Frequency

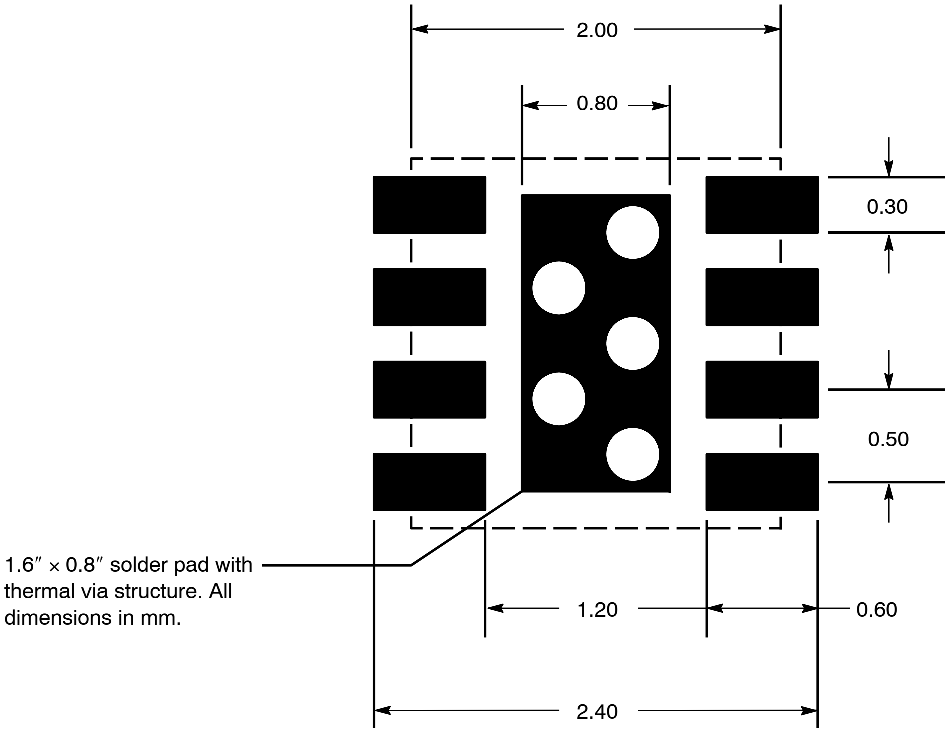


Figure 28. PCB Pad Layout for DFN 2 × 2

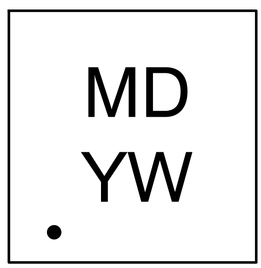
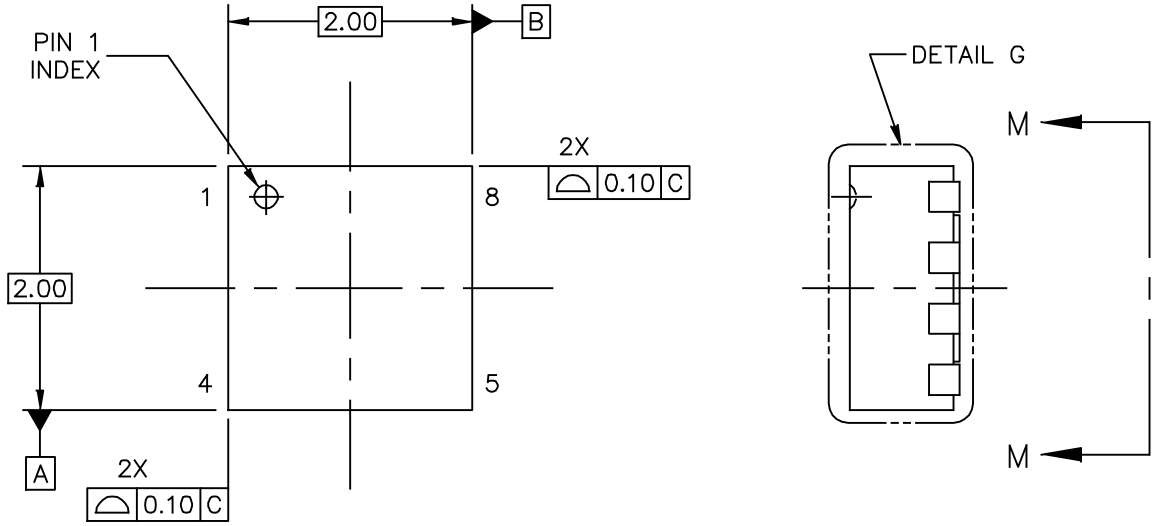
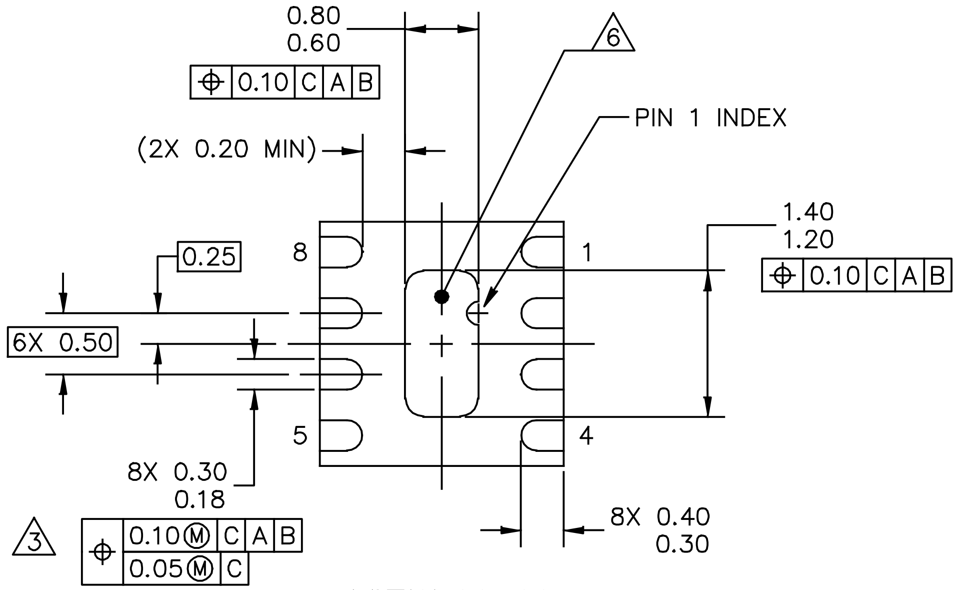


Figure 29. Product Marking

PACKAGE DIMENSIONS





VIEW M–M

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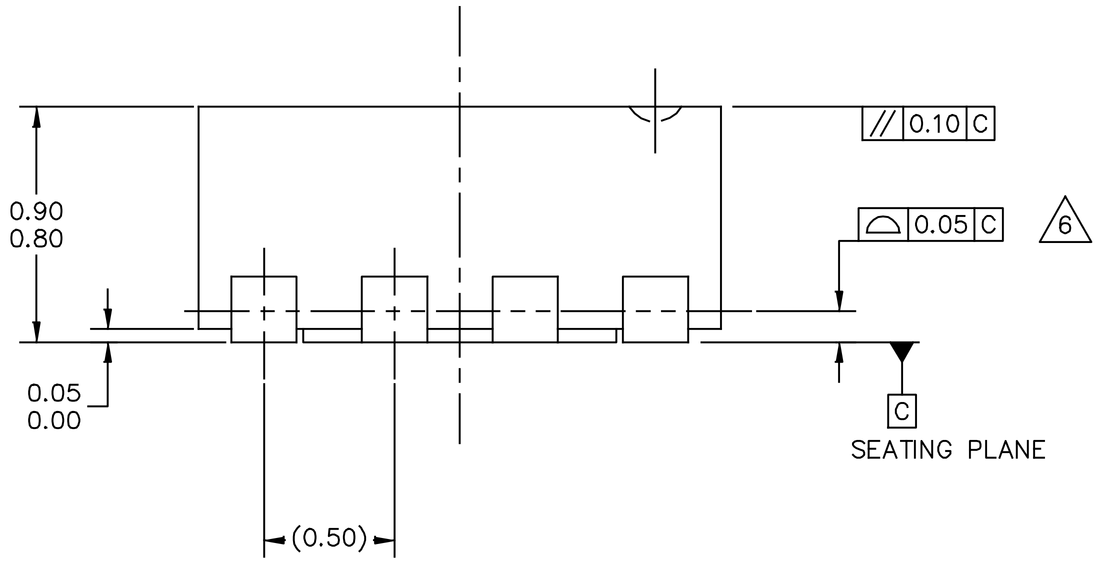
	STANDARD: NON–JEDEC	
	SOT908–4	06 JAN 2016



DETAIL G
VIEW ROTATED 90° CW

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TITLE: THERMALLY ENHANCED DUAL FLAT NON–LEADED PACKAGE (DFN) 8 TERMINAL, 0.5 PITCH (2 X 2 X 0.85)	DOCUMENT NO: 98ASA00228D REV: A	
	STANDARD: NON–JEDEC	
	SOT908–4 06 JAN 2016	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 – 2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMIMAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

4. MAX. PACKAGE WARPAGE IS 0.05 mm.

5. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

6. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED DUAL FLAT NON–LEADED PACKAGE (DFN) 8 TERMINAL, 0.5 PITCH (2 X 2 X 0.85)	DOCUMENT NO: 98ASA00228D	REV: A
	STANDARD: NON–JEDEC	
	SOT908–4	06 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3100: General Purpose Amplifier and MMIC Biasing

Software

- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2016	• Initial Release of Data Sheet

How to Reach Us:

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Document Number: MML25231HT1
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