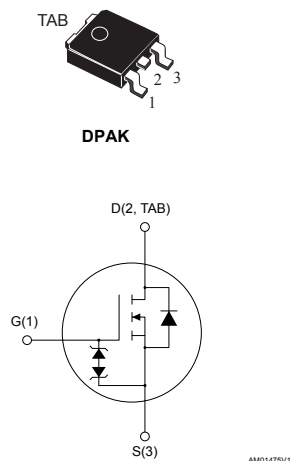


N-channel 620 V, 1.7 Ω typ., 3.8 A MDmesh™ K3 Power MOSFET in DPAK package



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD4N62K3	620 V	2 Ω	3.8 A	70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh™ K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link	
STD4N62K3	
Product summary	
Order code	STD4N62K3
Marking	4N62K3
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	3.8	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	2	A
$I_{DM}^{(1)}$	Drain current (pulsed)	15.2	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive	3.8	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	115	mJ
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	2.5	kV
$dv/dt^{(3)}$	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.
3. $I_{SD} \leq 3.8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.79	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	620			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 620\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 620\text{ V}$ $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.9\text{ A}$		1.7	2	Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	550	-	pF
C_{oss}	Output capacitance			42		
C_{rss}	Reverse transfer capacitance			7		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }496\text{ V}$		27		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	2	5	10	Ω
Q_g	Total gate charge	$V_{DD} = 496\text{ V}$, $I_D = 3.8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	22	-	nC
Q_{gs}	Gate-source charge			4		
Q_{gd}	Gate-drain charge			13		

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 1.9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	10	-	ns
t_r	Rise time			9		
$t_{d(off)}$	Turn-off delay time			29		
t_f	Fall time			19		

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				15.2	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3.8\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	220		ns
Q_{rr}	Reverse recovery charge			1.4		μC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	$I_{SD} = 3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	270		ns
Q_{rr}	Reverse recovery charge			1.9		μC
I_{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_D = 0\text{ A}$, $I_{GS} = \pm 1\text{ mA}$	± 30	-		V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

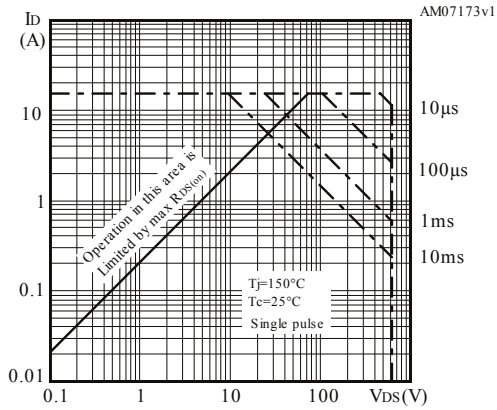
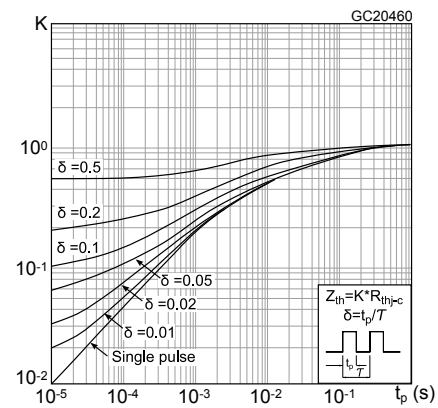
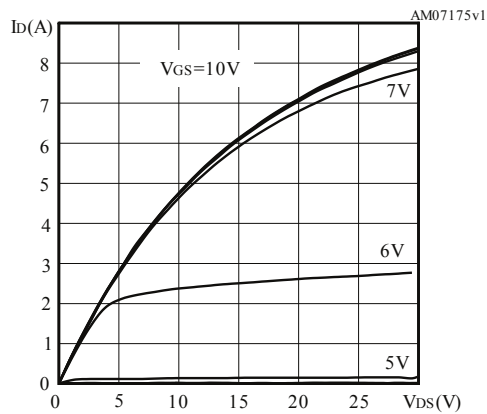
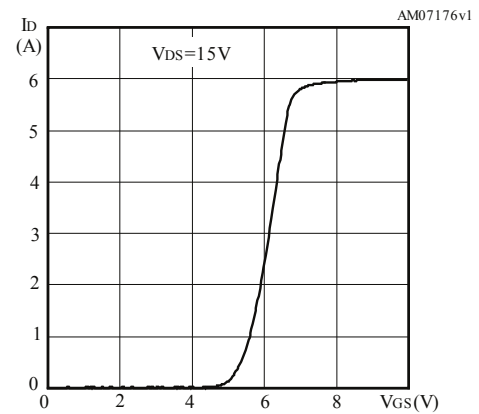
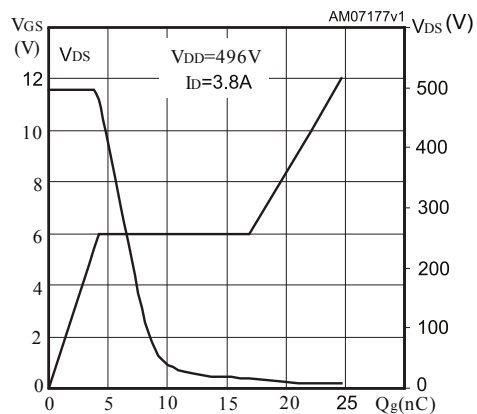
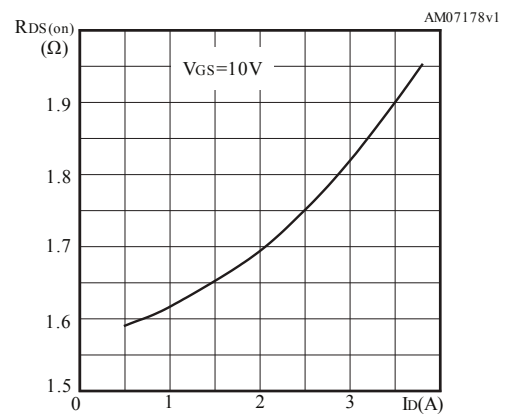
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on resistance


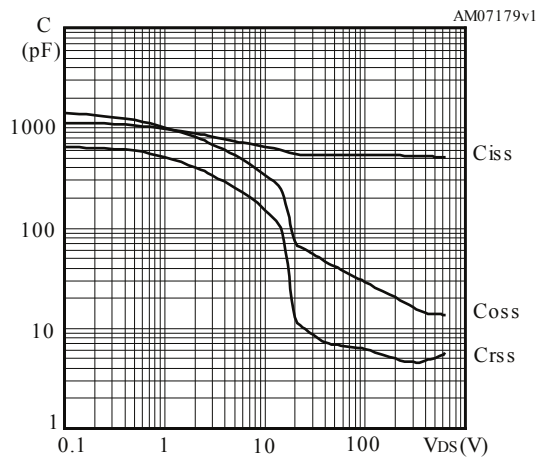
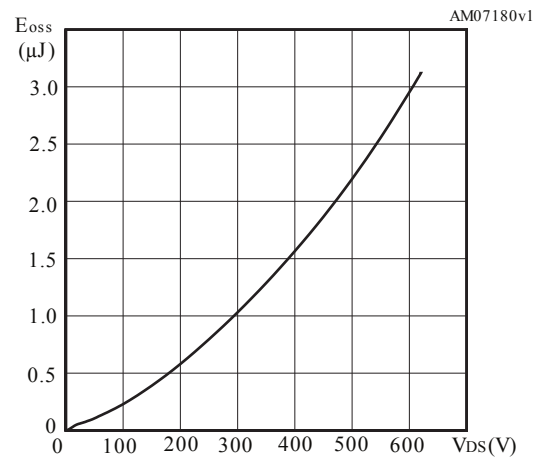
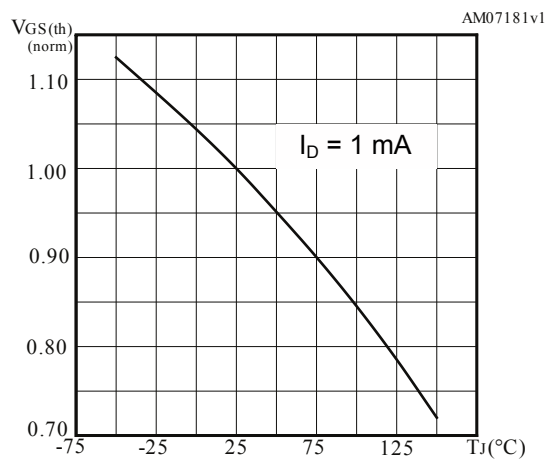
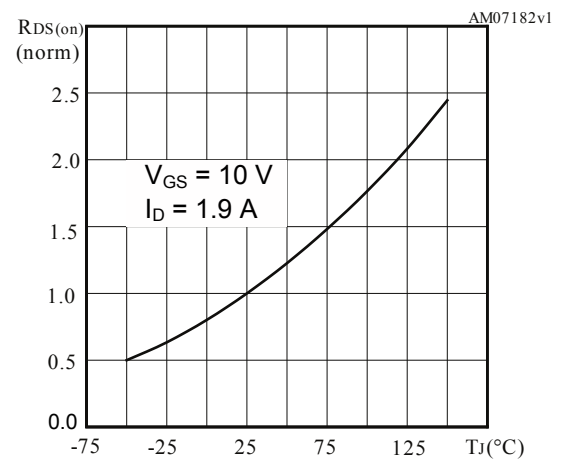
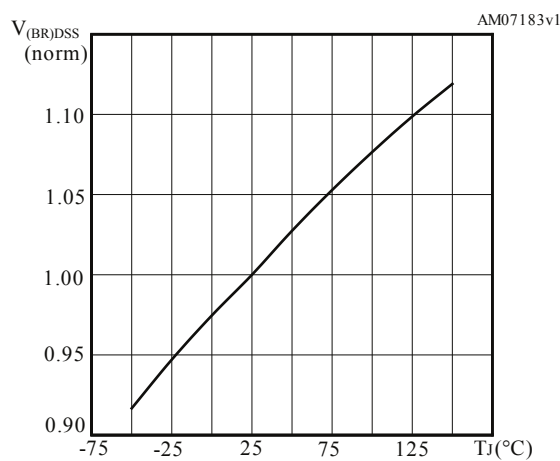
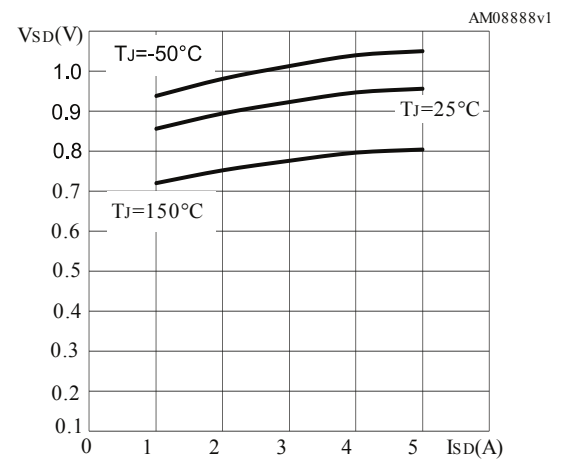
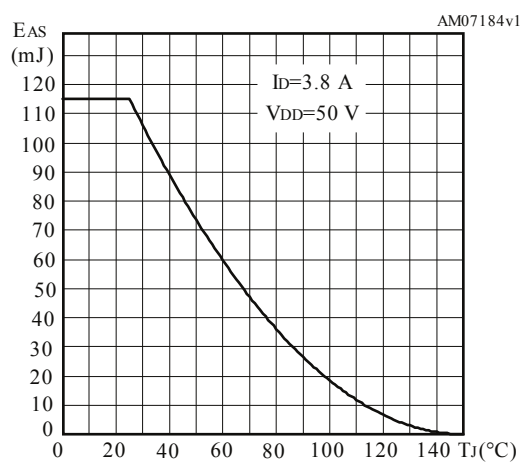
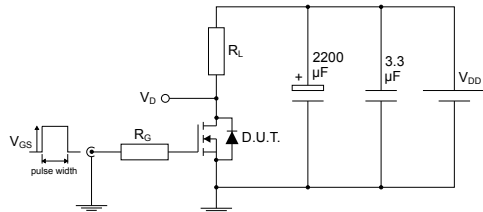
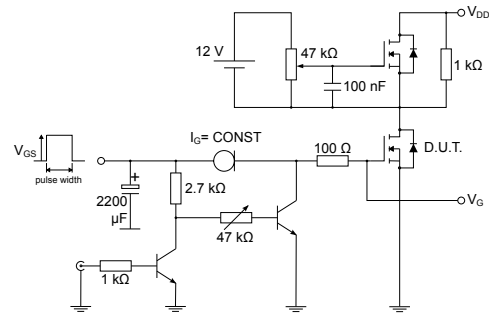
Figure 7. Capacitance variations

Figure 8. Output capacitance stored energy

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on resistance vs temperature

Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

Figure 12. Source-drain diode forward characteristics


Figure 13. Maximum avalanche energy vs temperature


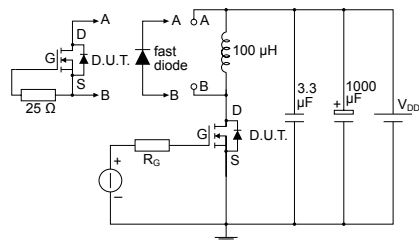
3 Test circuits

Figure 14. Test circuit for resistive load switching times


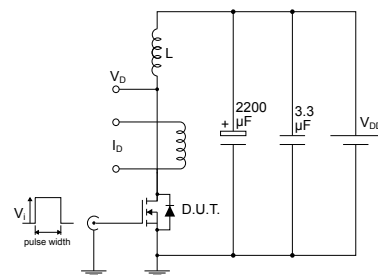
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Figure 15. Test circuit for gate charge behavior


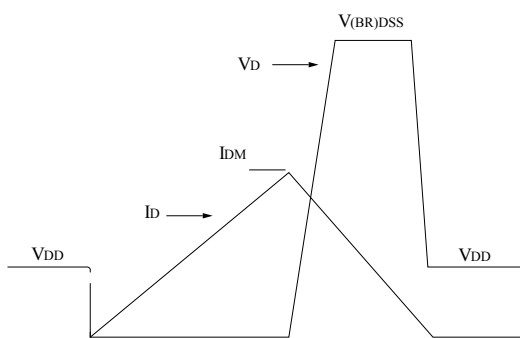
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Figure 16. Test circuit for inductive load switching and diode recovery times


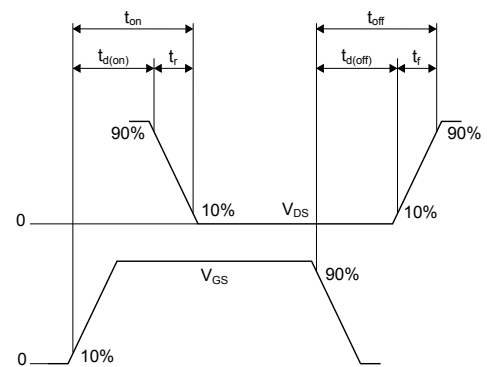
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


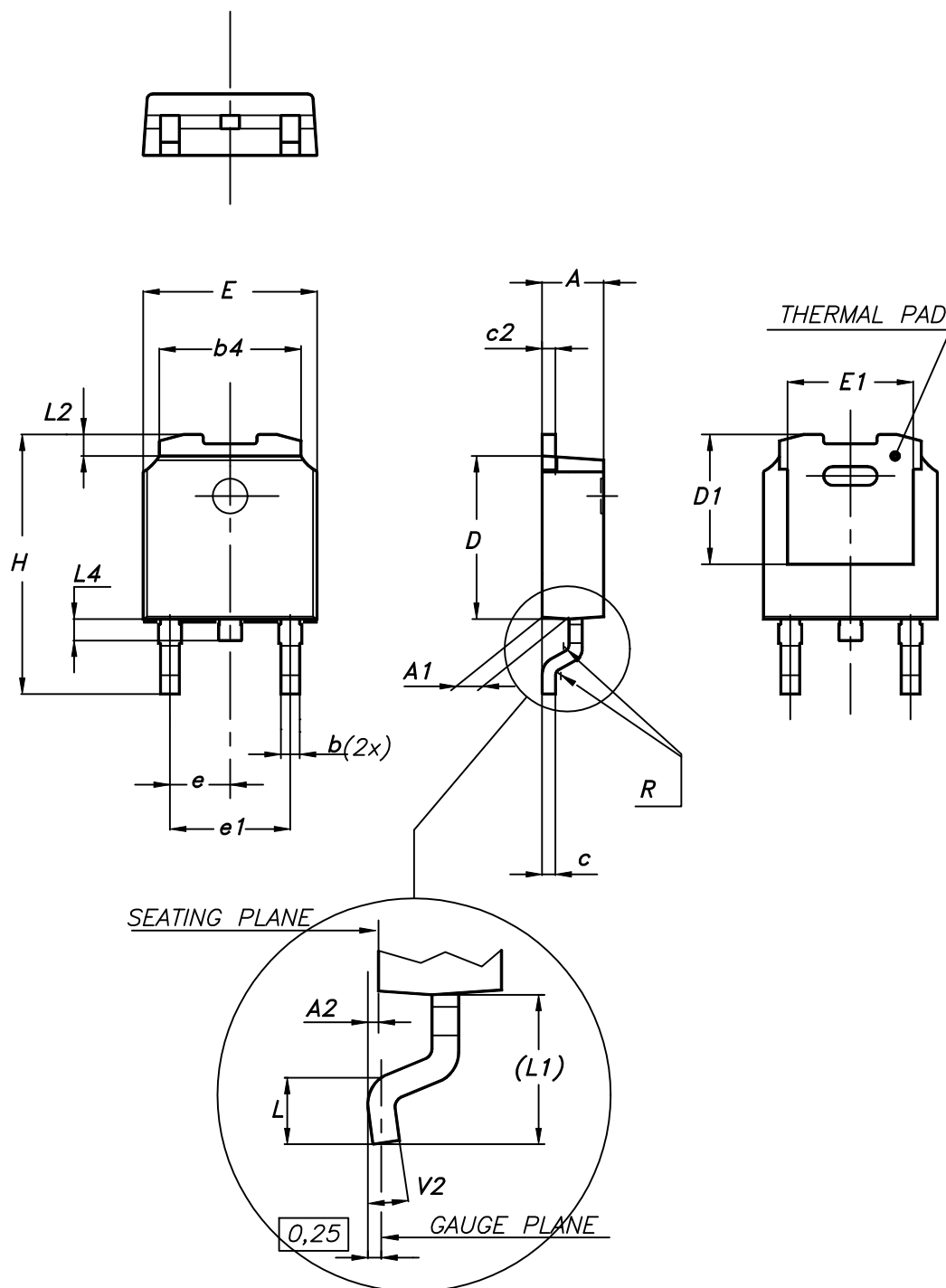
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20. DPAK (TO-252) type A2 package outline



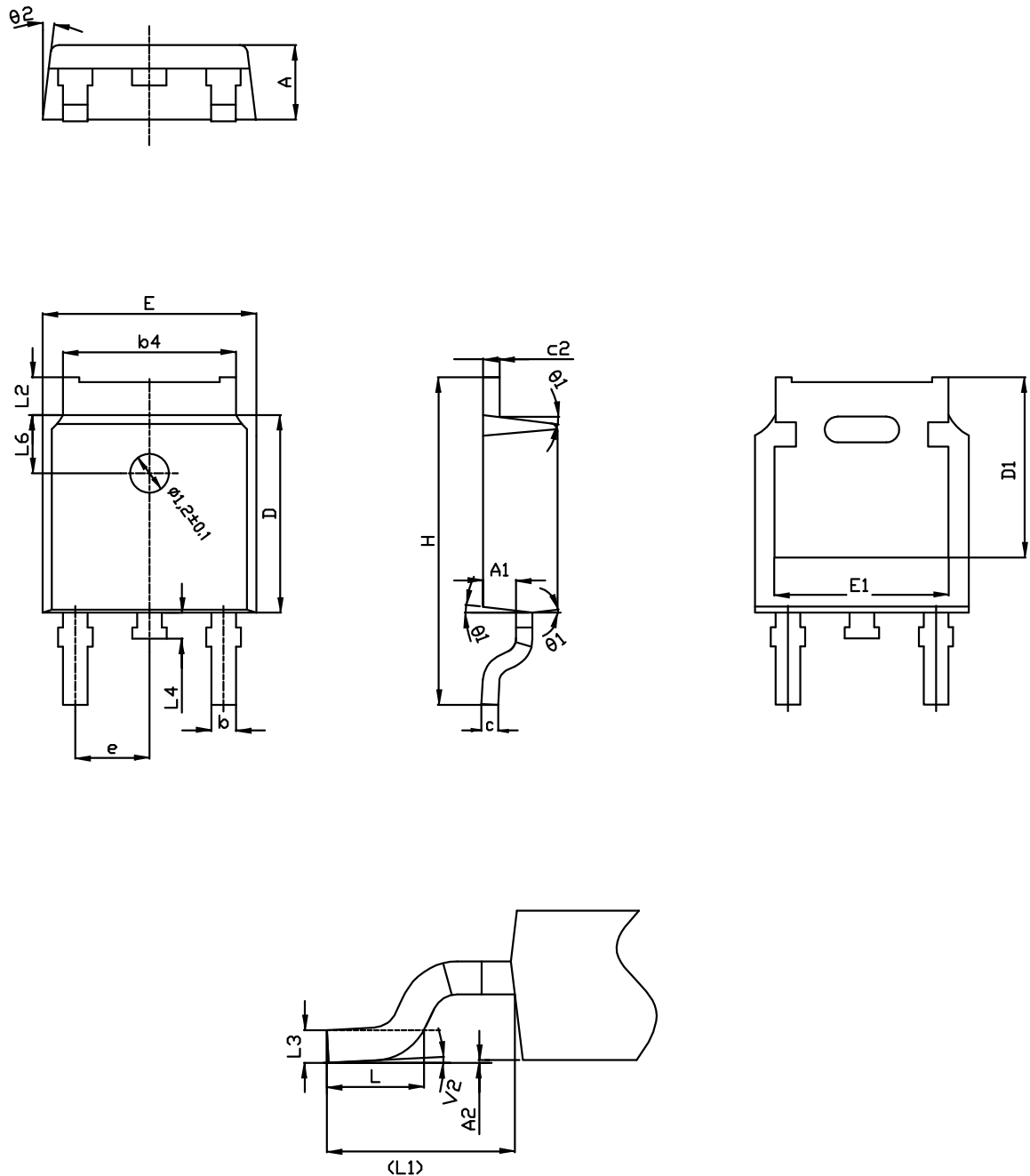
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Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 21. DPAK (TO-252) type C2 package outline



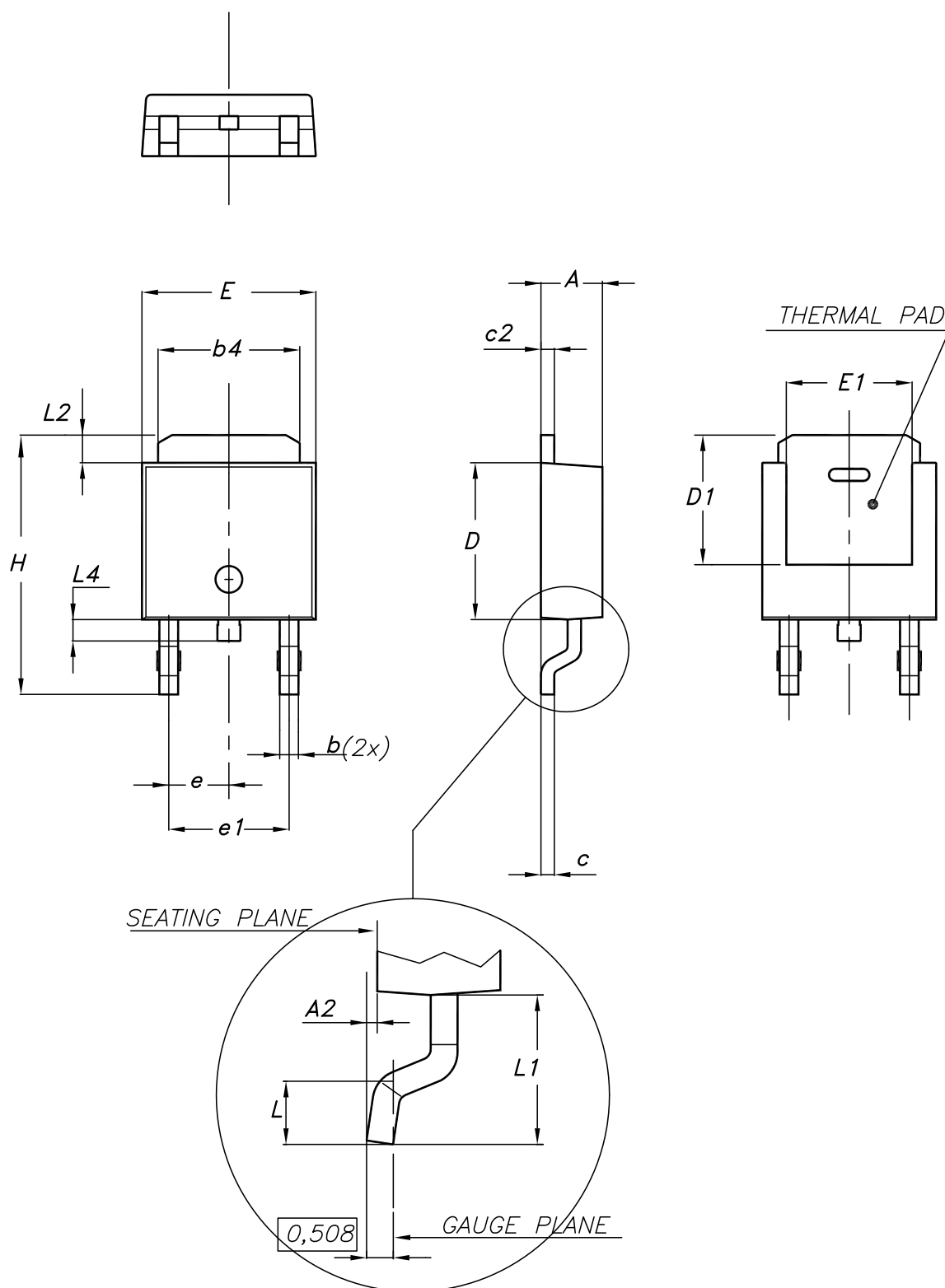
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Table 9. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.3 DPAK (TO-252) type E package information

Figure 22. DPAK (TO-252) type E package outline

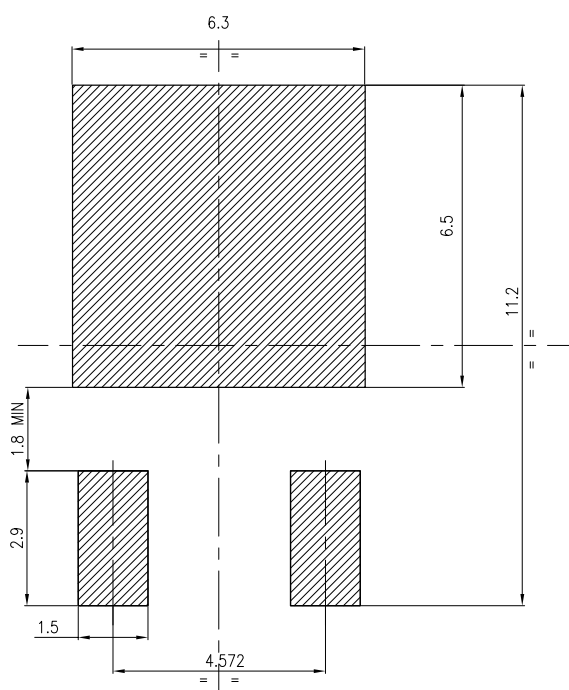


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Table 10. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

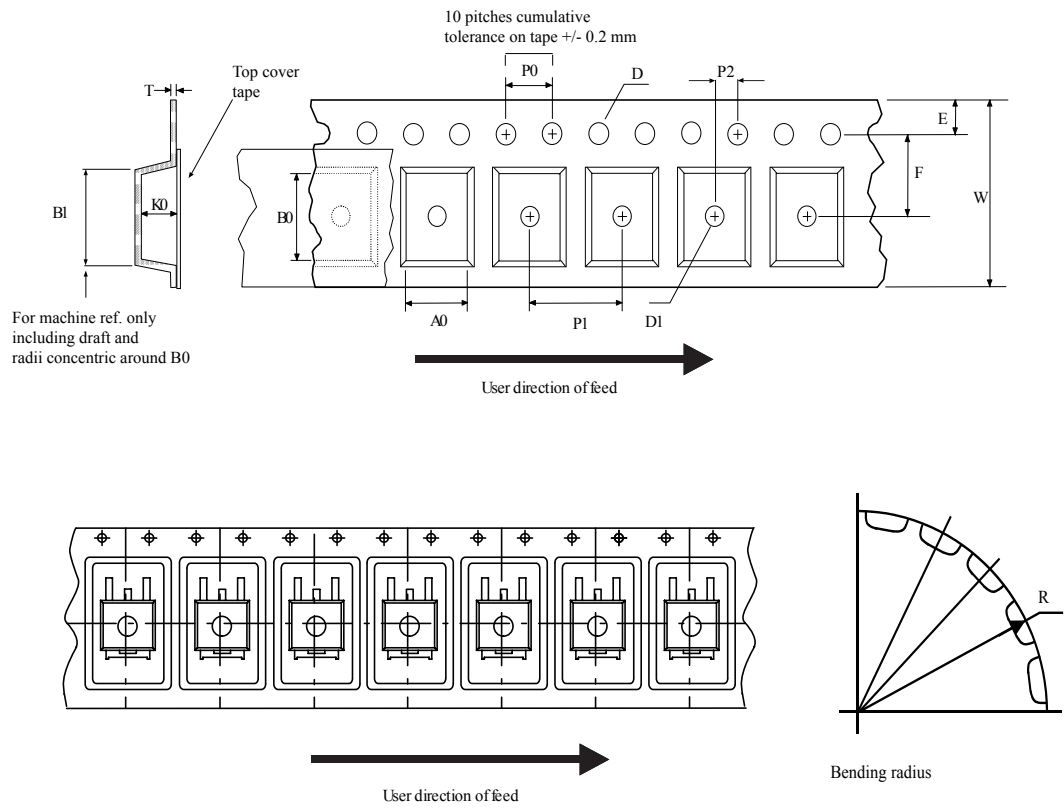
Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)



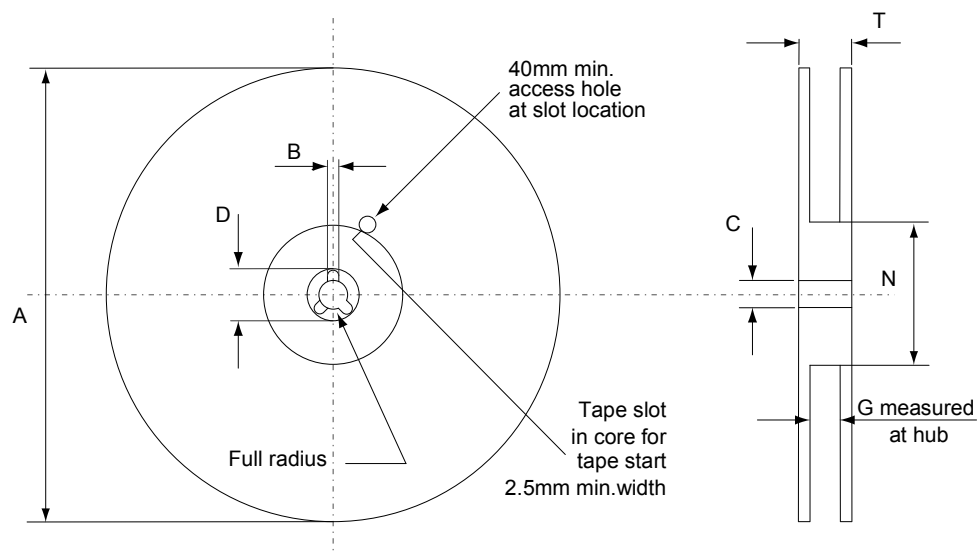
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4.4 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



AM08852v1

Figure 25. DPAK (TO-252) reel outline


AM06038v1

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 12. Document revision history

Date	Revision	Changes
16-Dec-2010	1	First release.
26-Apr-2012	2	Added min and max values for RG in Table 5: Dynamic and Section 5: Packaging mechanical data. Updated Section 4: Package mechanical data. Minor text changes.
09-Sep-2013	3	– Updated: Section 4: Package mechanical data – Minor text changes
03-Aug-2018	4	The part number STB4N62K3 has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated Section 1 Electrical ratings , Section 2 Electrical characteristics and Section 4 Package information . Minor text changes.

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