

# 74LVT244A-Q100; 74LVTH244A-Q100

3.3 V octal buffer/line driver; 3-state

Rev. 1 — 22 April 2013

Product data sheet

## 1. General description

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The 74LVT244A-Q100; 74LVTH244A-Q100 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables (1OE, 2OE), each controlling four of the 3-state outputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

## 2. Features and benefits

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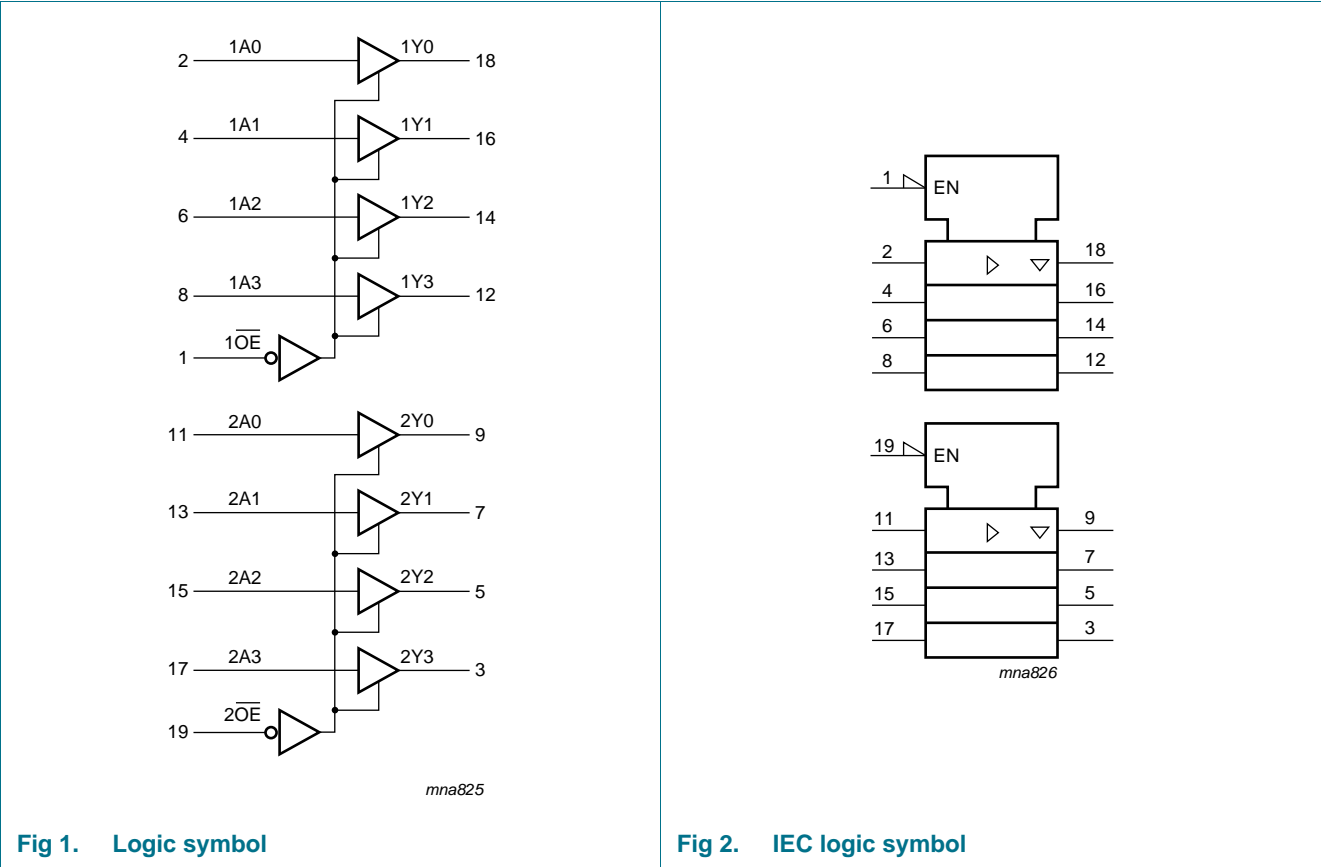
- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and  $-32\text{ mA}$
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
  - ◆ JESD78 Class II exceeds 500 mA
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT244AD-Q100 74LVTH244AD-Q100	−40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT244APW-Q100 74LVTH244APW-Q100	−40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVT244ABQ-Q100 74LVTH244ABQ-Q100	−40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



5. Pinning information

5.1 Pinning

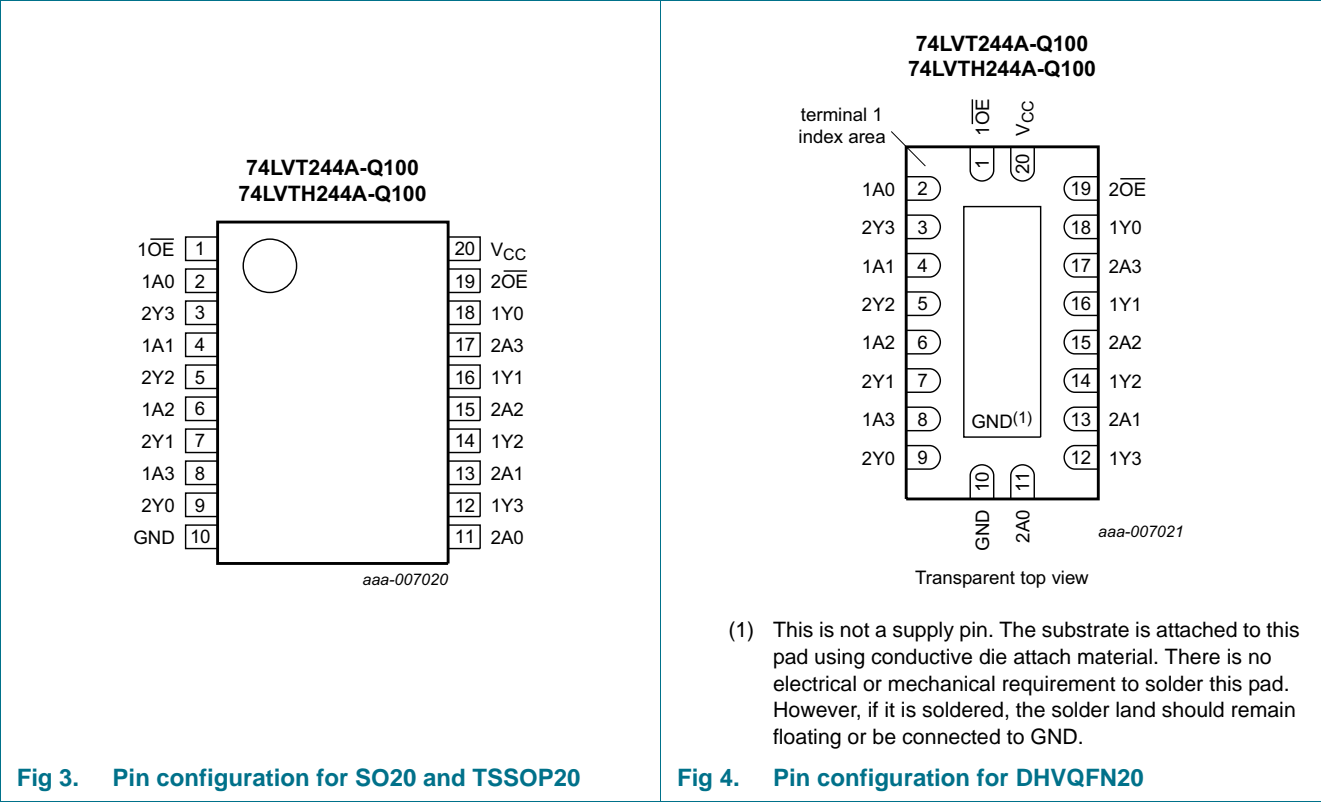


Fig 3. Pin configuration for SO20 and TSSOP20

Fig 4. Pin configuration for DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$ , $\overline{2OE}$	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

### 6.1 Function table

Table 3. Function table [1]

Control	Input	Output
nOE	nAn	nYn
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-	-50	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		[2] -	150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ to $+85$ °C	[3]	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO20 package: above 70 °C derate linearly with 8 mW/K.  
For TSSOP20 package: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 package: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.7	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$I_{OH}$	HIGH-level output current		-	-	-32	mA

Table 5. Operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OL}$	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz	-	-	64	mA
$T_{amb}$	ambient temperature	in free-air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ; $I_{OH} = -8\text{ mA}$	2.4	2.5	-	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$	2.0	2.2	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.1	0.2	V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
$I_I$	input leakage current	all input pins				
		$V_{CC} = 0\text{ V or }3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	$\mu\text{A}$
		control pins				
		$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		data pins [2]				
		$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$	-	0.1	1	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$	-5	-1	-	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V to }4.5\text{ V}$	-	1	$\pm 100$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 3\text{ V}$ ; $V_I = 0.8\text{ V}$ [3]	75	150	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 3\text{ V}$ ; $V_I = 2.0\text{ V}$	-	-150	-75	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	nAn input; $V_{CC} = 0\text{ V to }3.6\text{ V}$ ; $V_I = 3.6\text{ V}$	500	-	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	nAn input; $V_{CC} = 0\text{ V to }3.6\text{ V}$ ; $V_I = 3.6\text{ V}$	-	-	-500	$\mu\text{A}$
$I_{LO}$	output leakage current	nYn output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 3.0\text{ V}$	-	60	125	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V to }V_{CC}$ ; $V_I = \text{GND or }V_{CC}$ ; nOE = don't care [4]	-	$\pm 1$	$\pm 100$	$\mu\text{A}$

**Table 6.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OZ}$	OFF-state output current	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$				
		$V_O = 3.0\text{ V}$	-	1	5	$\mu\text{A}$
		$V_O = 0.5\text{ V}$	-5	-1	-	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0\text{ A}$				
		output HIGH	-	0.13	0.19	mA
		output LOW	-	3	12	mA
		outputs disabled [5]	-	0.13	0.19	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at $V_{CC}$ or GND [6]	-	0.1	0.2	mA
$C_I$	input capacitance	$V_I = 0\text{ V}$ or $3.0\text{ V}$	-	4	-	pF
$C_O$	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or $3.0\text{ V}$	-	8	-	pF

[1] All typical values are at  $T_{amb} = 25\text{ }^\circ\text{C}$ .[2] Unused pins at  $V_{CC}$  or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of 100  $\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25\text{ }^\circ\text{C}$  only.[5]  $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.[6] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

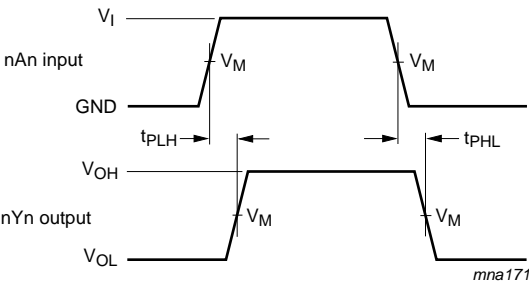
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40\text{ }^\circ\text{C}</math> to <math>+85\text{ }^\circ\text{C}</math> [1]</b>						
$t_{PLH}$	LOW to HIGH propagation delay	nAn to nYn; see <a href="#">Figure 5</a>				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1	2.5	4.1	ns
$t_{PHL}$	HIGH to LOW propagation delay	nAn to nYn; see <a href="#">Figure 5</a>				
		$V_{CC} = 2.7\text{ V}$	-	-	5.1	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1	2.6	4.1	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.7\text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1	3.2	5.2	ns
$t_{PZL}$	OFF-state to LOW propagation delay	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.7\text{ V}$	-	-	6.7	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1.1	3.1	5.2	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.7\text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1.9	3.3	5.6	ns

Table 7. Dynamic characteristics ...continued  
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	see Figure 6				
		V <sub>CC</sub> = 2.7 V	-	-	5.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	3.3	5.1	ns

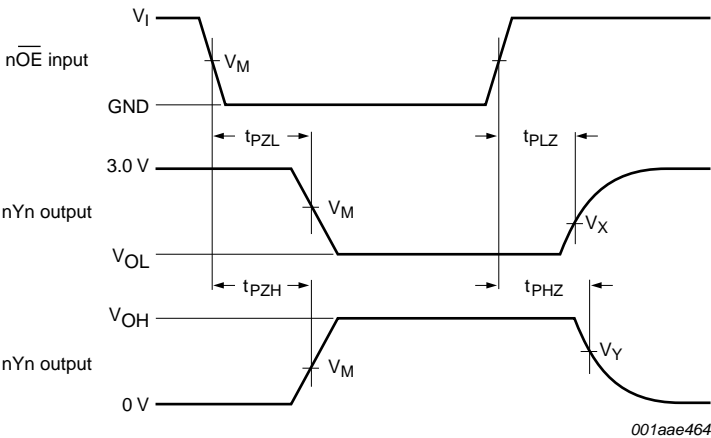
[1] All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

11. Waveforms



Measurement points are given in Table 8.  
V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (nAn) to output (nYn) propagation delays

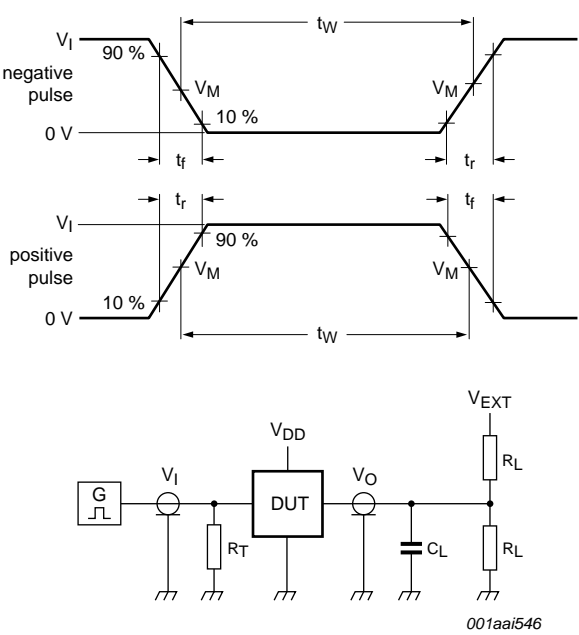


Measurement points are given in Table 8.  
V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig 6. 3-state output enable and disable times

Table 8. Measurement points

Input	Output		
V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



Test data is given in [Table 9](#).  
Definitions test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = Test voltage for switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open



12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

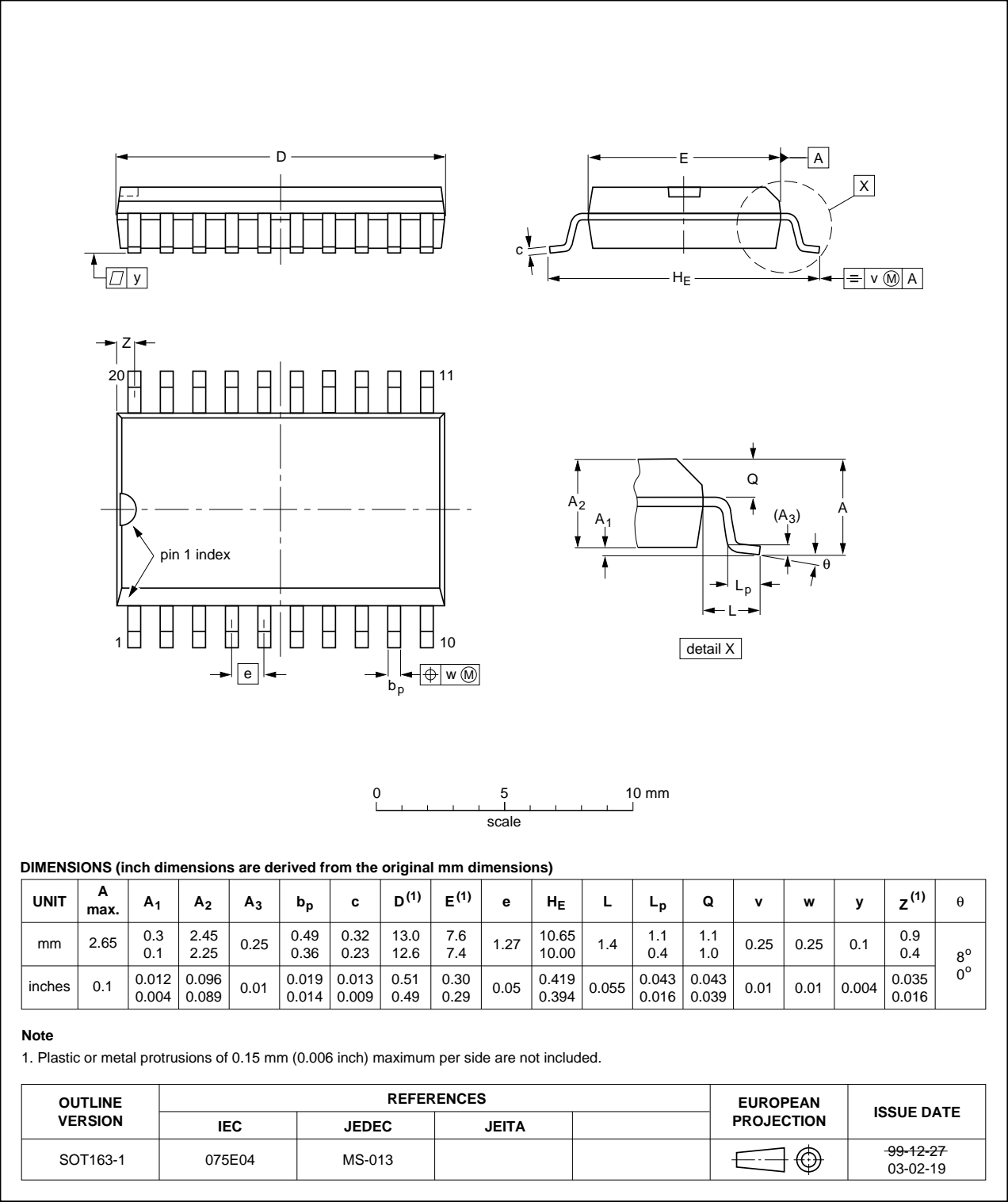


Fig 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

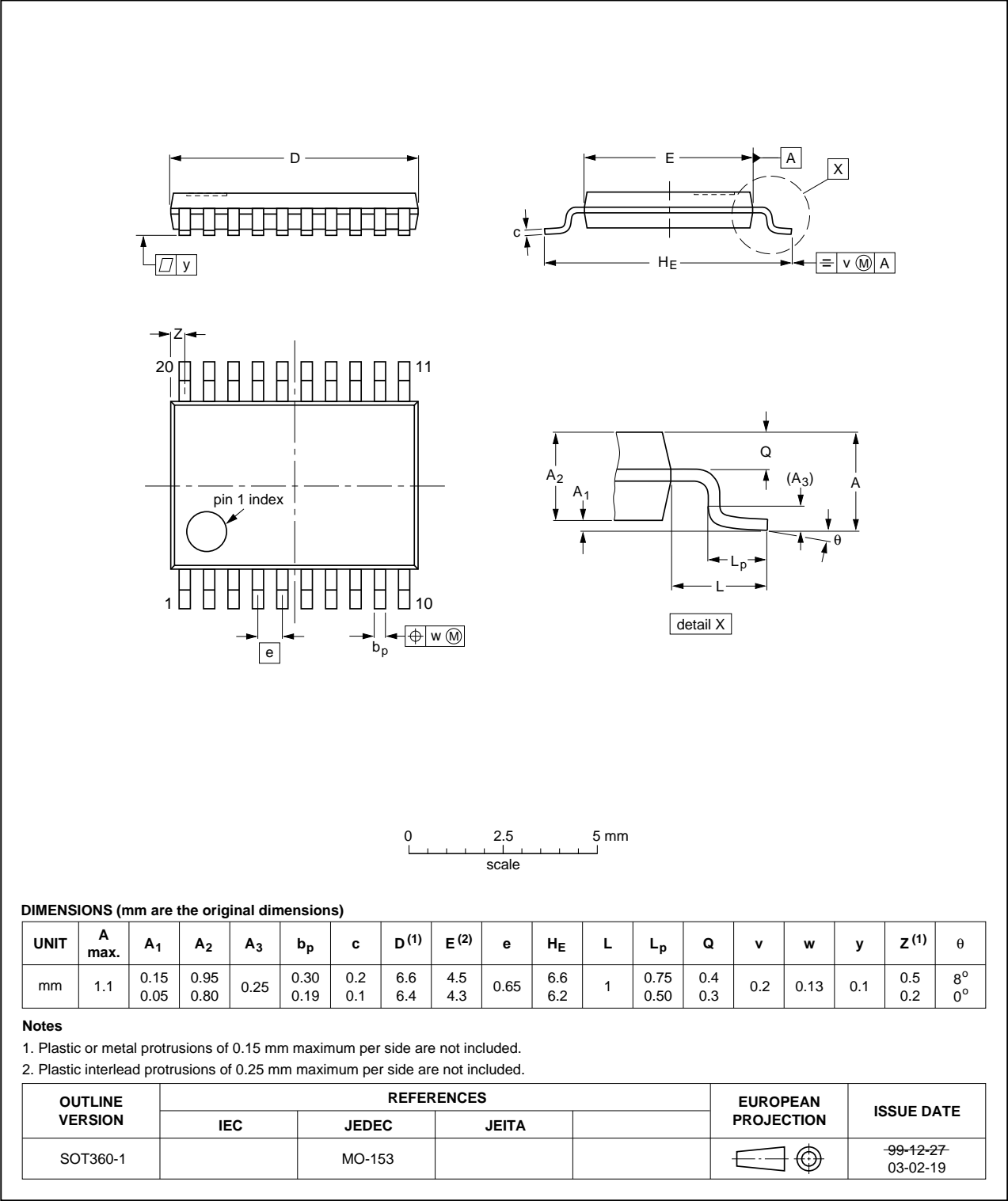


Fig 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

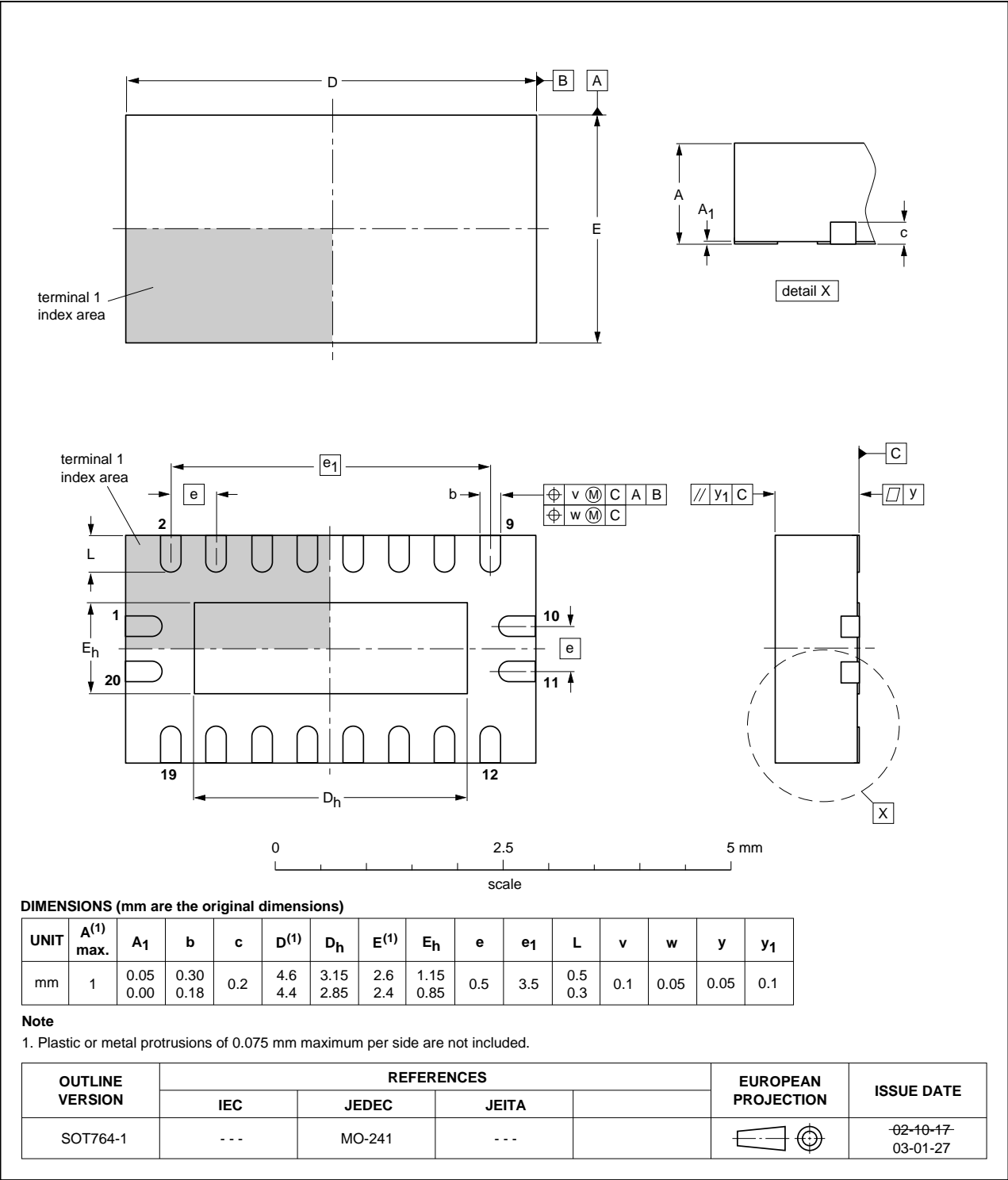


Fig 10. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bi-polar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244A_Q100 v.1	20130422	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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