

Vishay Semiconductors

### Hyperfast Rectifier, 2 x 10 A FRED Pt®



**TO-220AB** 



**TO-220 FULL-PAK** 

Base common cathode 02 Common cathode 3



VS-20CTH03PbF

VS-20CTH03FPPbF

PRODUCT SUMMARY					
Package	TO-220AB, TO-220FP				
I <sub>F(AV)</sub>	2 x 10 A				
$V_{R}$	300 V				
V <sub>F</sub> at I <sub>F</sub>	1.25 V				
t <sub>rr</sub> typ.	See Recovery table				
T <sub>J</sub> max.	175 °C				
Diode variation	Common cathode				

#### **FEATURES**

- Hyperfast recovery time
- · Low forward voltage drop
- 175 °C operating junction temperature
- Low leakage current
- Fully isolated package (V<sub>INS</sub> = 2500 V<sub>RMS</sub>)
- UL E78996 pending
- Compliant to RoHS Directive 2002/95/EC
- AEC-Q101 qualified (TO-220)
- Designed and qualified for industrial level (TO-220FP)

#### **DESCRIPTION/APPLICATIONS**

300 V series are the state of the art hyperfast recovery rectifiers designed with optimized performance of forward voltage drop and hyperfast recovery time.

The planar structure and the platinum doped life time control, guarantee the best overall performance, ruggedness and reliability characteristics.

These devices are intended for use in the output rectification stage of SMPS, UPS, DC/DC converters as well as freewheeling diodes in low voltage inverters and chopper motor drives.

Their extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

ABSOLUTE MAXIMUM RATINGS								
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Peak repetitive reverse voltage		$V_{RRM}$		300	V			
	per diode	4	T <sub>C</sub> = 160 °C	10				
Average rectified forward current	(FULL-PAK) per diode		T <sub>C</sub> = 135 °C					
	per device			20	A			
Non-repetitive peak surge current		I <sub>FSM</sub>	T <sub>J</sub> = 25 °C	120				
Operating junction and storage temperatures		T <sub>J</sub> , T <sub>Stg</sub>		- 65 to 175	°C			

<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Breakdown voltage, blocking voltage	V <sub>BR</sub> , V <sub>R</sub>	Ι <sub>R</sub> = 100 μΑ	300	-	-		
Forward voltage	V <sub>F</sub>	I <sub>F</sub> = 10 A	-	1.05	1.25	V	
		I <sub>F</sub> = 10 A, T <sub>J</sub> = 125 °C	-	0.85	0.95		
Reverse leakage current I <sub>R</sub>		$V_R = V_R$ rated	-	-	20		
		$T_J = 125  ^{\circ}C$ , $V_R = V_R$ rated	-	6	200	μΑ	
Junction capacitance	C <sub>T</sub>	V <sub>R</sub> = 300 V	-	30	-	pF	
Series inductance	L <sub>S</sub>	Measured lead to lead 5 mm from package body	-	8	-	nΗ	

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## VS-20CTH03PbF, VS-20CTH03FPPbF

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<b>DYNAMIC RECOVERY CHARACTERISTICS</b> (T <sub>C</sub> = 25 °C unless otherwise specified)								
PARAMETER	SYMBOL	TEST CO	MIN.	TYP.	MAX.	UNITS		
Reverse recovery time		$I_F = 1 \text{ A}, dI_F/dt = 50 \text{ A}$	/μs, V <sub>R</sub> = 30 V	-	ı	35		
	t <sub>rr</sub>	I <sub>F</sub> = 1 A, dI <sub>F</sub> /dt = 100 A/μs, V <sub>R</sub> = 30 V		-	-	30		
		T <sub>J</sub> = 25 °C	I <sub>F</sub> = 10 A dI <sub>F</sub> /dt = 200 A/μs V <sub>R</sub> = 200 V	-	31	-	ns A nC	
		T <sub>J</sub> = 125 °C		-	42	-		
Dools woods on a commont	I <sub>RRM</sub>	T <sub>J</sub> = 25 °C		-	2.4	-		
Peak recovery current		T <sub>J</sub> = 125 °C		-	5.6	-		
Reverse recovery charge	Q <sub>rr</sub>	T <sub>J</sub> = 25 °C		-	36	-		
		T <sub>J</sub> = 125 °C		-	120	-		

THERMAL - MECHANICAL SPECIFICATIONS									
PARAMETER		SYMBOL	TEST CONDTIONS	MIN.	TYP.	MAX.	UNITS		
Maximum junction and storage temperature range		T <sub>J</sub> , T <sub>Stg</sub>		- 65	-	175	°C		
Thermal resistance,	per diode		Mounting surface, flat, smooth and greased	=	-	1.5	°C/W		
junction to case	(FULL-PAK) per diode	H <sub>th</sub> JC		-	-	3.9	C/VV		
Marking device			Case style TO-220AB 20CTH03		ГН03				
			Case style TO-220 FULL-PAK		20CTI	103FP			

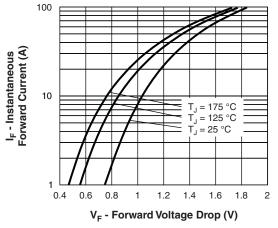


Fig. 1 - Typical Forward Voltage Drop Characteristics

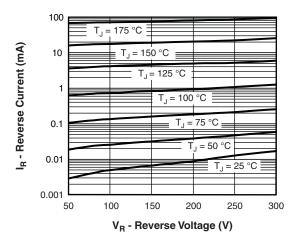


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage



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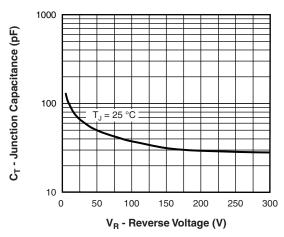


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

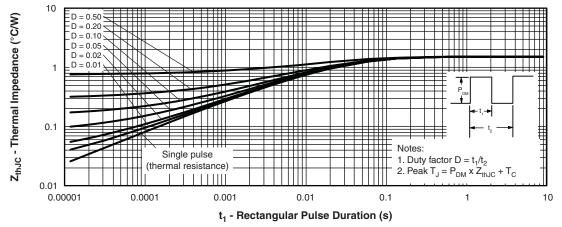


Fig. 4 - Maximum Thermal Impedance Z<sub>thJC</sub> Characteristics

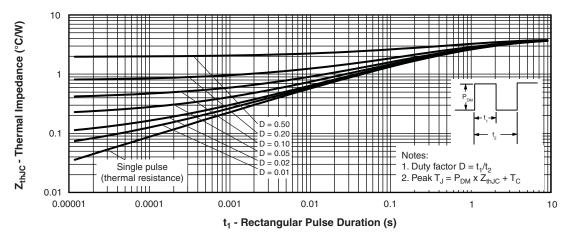
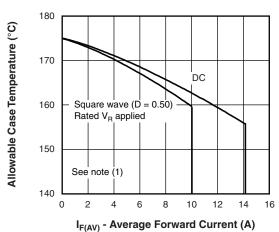


Fig. 5 - Maximum Thermal Impedance ZthJC Characteristics (FULL-PAK)

### VS-20CTH03PbF, VS-20CTH03FPPbF

# Vishay Semiconductors Hyperfast Rectifier, 2 x 10 A FRED Pt®





IF(AV) - Average Forward Current (A)

Fig. 6 - Maximum Allowable Case Temperature vs.
Average Forward Current

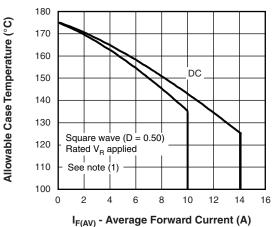


Fig. 7 - Maximum Allowable Case Temperature vs. Average Forward Current (FULL-PAK)

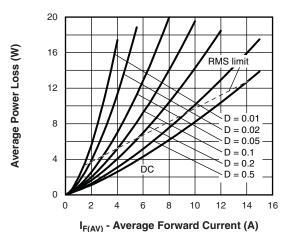


Fig. 8 - Forward Power Loss Characteristics

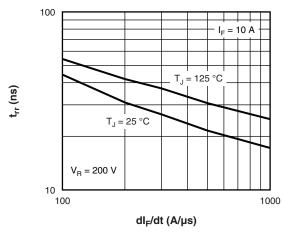


Fig. 9 - Typical Reverse Recovery Time vs.  $dI_F/dt$ 

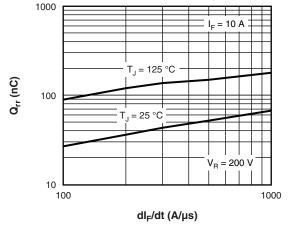


Fig. 10 - Typical Stored Charge vs. dl<sub>F</sub>/dt

#### Note

 $\begin{array}{ll} \text{(1)} & \text{Formula used: } T_C = T_J - (Pd + Pd_{REV}) \times R_{th,JC}; \\ Pd = \text{Forward power loss} = I_{F(AV)} \times V_{FM} \text{ at } (I_{F(AV)}/D) \text{ (see fig. 8);} \\ Pd_{REV} = \text{Inverse power loss} = V_{R1} \times I_R \text{ (1 - D); } I_R \text{ at } V_{R1} = \text{Rated } V_R \\ \end{array}$ 



# Hyperfast Rectifier, 2 x 10 A FRED Pt® Vishay Semiconductors

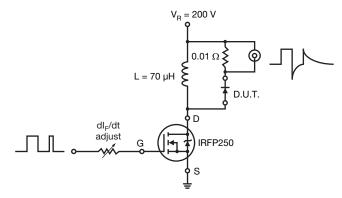
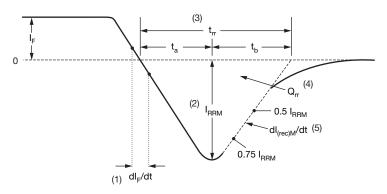


Fig. 11 - Reverse Recovery Parameter Test Circuit



- (1) dl<sub>F</sub>/dt rate of change of current through zero crossing
- (2)  $I_{RRM}$  peak reverse recovery current
- (3) t<sub>rr</sub> reverse recovery time measured from zero crossing point of negative going  $\rm I_F$  to point where a line passing through 0.75  $\rm I_{RRM}$  and 0.50  $\rm I_{RRM}$ extrapolated to zero current.
- (4)  $Q_{rr}$  area under curve defined by  $t_{rr}$ and I<sub>RRM</sub>

$$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$

(5)  $dI_{(rec)M}/dt$  - peak rate of change of current during t<sub>b</sub> portion of t<sub>rr</sub>

Fig. 12 - Reverse Recovery Waveform and Definitions

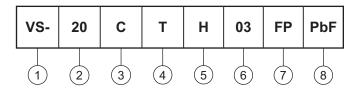
### VS-20CTH03PbF, VS-20CTH03FPPbF

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#### **ORDERING INFORMATION TABLE**

Device code



Vishay Semiconductors product

Current rating (20 = 20 A)

C = Common cathode

T = TO-220,  $D^2PAK$ 

H = Hyperfast recovery

Voltage rating (03 = 300 V)

• None = TO-220AB

• FP = TO-220 FULL-PAK

8 PbF = Lead (Pb)-free

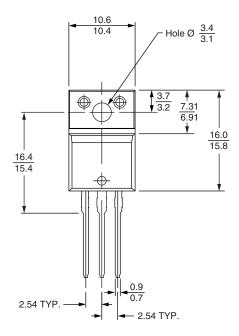
Tube standard pack quantity: 50 pieces

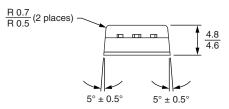
LINKS TO RELATED DOCUMENTS						
Dimensions	TO-220AB	www.vishay.com/doc?95222				
Dimensions	TO-220AB FULL-PAK	www.vishay.com/doc?95072				
Part marking information	TO-220AB	www.vishay.com/doc?95225				
	TO-220AB FULL-PAK	www.vishay.com/doc?95069				

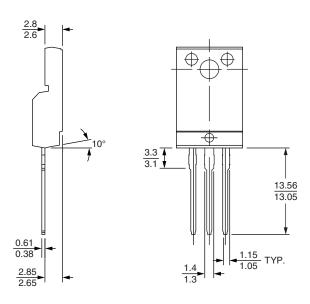


### Vishay Semiconductors

#### **DIMENSIONS** in millimeters







### Lead assignments

#### **Diodes**

- 1. Anode/open
- 2. Cathode
- 3. Anode

Conforms to JEDEC outline TO-220 FULL-PAK



### Vishay Semiconductors

### **TO-220AB**

#### **DIMENSIONS** in millimeters and inches



### Lead assignments

#### **Diodes**

- 1. Anode/open
- 2. Cathode
- 3. Anode

#### Conforms to JEDEC outline TO-220AB

SYMBOL	MILLIN	IETERS	INC	NOTES	
STMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6

SYMBOL	MILLIM	IETERS	INC	NOTES	
STIMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
E	10.11	10.51	0.398	0.414	3, 6
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
е	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
ØΡ	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		
		•	•	•	

#### Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, except A2 (maximum) and D2 (minimum) where dimensions are derived from the actual package outline

Lead tip





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